

1 Report

For the adder implementation (adder.v) tested with the seed 2025 testvector, the design uses an adder width of 384 bits with 3 adders instantiated; it requires 3 cycles to perform one 384-bit addition and 6 cycles for a 381-bit modular addition; timing report shows a WNS (Worst Negative Slack) of 2.796 ns, and resource utilization from the implemented design is 902 Slice LUTs and 1,540 Slice Registers (flip-flops).