Assignment 1

1. The code and peripheral memory maps were found in the MDS in the following figures respectively: Figure 6-2 (MDS pg. 92) and Figure 6-4 (MDS pg. 94).

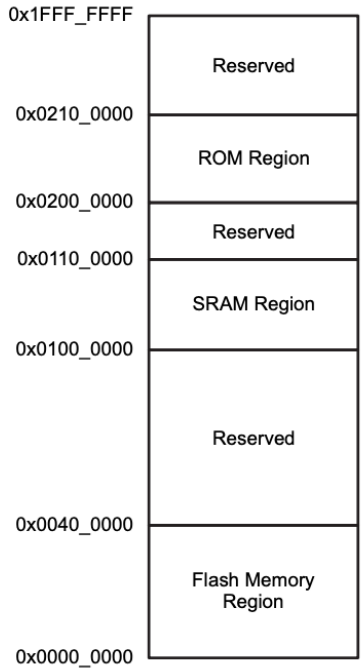

Figure 6-2. Code Zone Memory Map

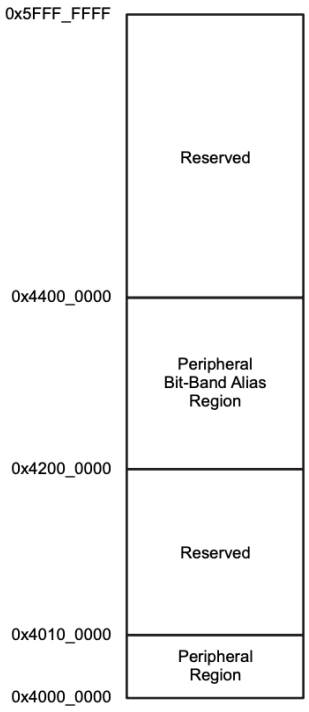

Figure 6-4. Peripheral Zone Memory Map

2. There are 5 internal oscillators, the DCO,VLO, MODOSC, REFO, and SYSOSC.
3. The MSP432P401R has 7 timers. Four of the timers are 16-bit timers each with up to five capture, compare, and PWM capability. Two of the timers are 32-bit timers each with interrupt generation capability. The last timer is a watchdog timer that acts as a 2-bit clock select that does a controlled system restart.
4. The maximum sampling rate of the ADC is 1Msps
5. $$N_{ADC} = 16384\frac{V_{in+} - V_R}{V_{R+} - V_R}, 1LSB = \frac{V_{R+} - V_R}{16384}$$ Equation 7
6. PCMCTL0 is the primary register used to change power modes
7. As temperature increases, the digital output current also increases.
8. The high drive I/Os produce about 5 times as much current as the normal drive I/Os.