Georgia Institute of Technology
School of Computer Science
CS 3220: Fall 2017
Project 2: Single Cycle Processor [100 Points]

Project Description

In this project, you will design a single-cycle processor and synthesize it on your FPGA board. The processor should be able to support a specific ISA. You can find the description for the ISA in the separate file that is uploaded to T-Square (project2-ISA-description.pdf). There is no performance requirement for this project (no logic optimization is required) and the only criterion for this project is the correct functionality of your implementation.

To get you started, we have provided you with a zip file (project2-template.zip) that includes the settings, timing requirements, and some of the Verilog codes for the design. It is highly recommended to begin working on the assembler and on the processor design immediately. There won't be any extension for this project. Once your assembler works, if your design has problems, you can use the assembler to create test programs that you could potentially use to identify and pinpoint errors in your design.

We've also uploaded two assembly files sample.a32 and sorter.a32, and a sample object file sample.mif to T-Square. You should implement your own assembler that reads the assembly code and generates the object files.

Project Milestones

This project has three milestones. In the first two milestones, you have to complete part of your project and submit the deliverables to T-Square. In the last milestone, you have to submit a fully functional single cycle processor and assembler according to the project description.

First Milestone [20 pts] (Due: Sunday, 11:55 PM, November 5^{th}, 2017)

For this milestone, you have to implement the assembler. The assembler should be written in Python 2.7. You can find the specification for assembler in file project2-ISA-description.pdf. You can verify your assembler with the provided assembly files, namely sample.a32 and sorter.a32. As a point of reference, we also include the generated object file (sample.mif) for sample.a32 assembly file

The assembler file has to be named assembler-[Student's Full Name].py (*e.g.* assembler-AmirYazdanbakhsh.py). We will use the following command to test your assembler.

- python assembler-[Student's Full Name].py [input assembly file] [output object file]

You have to put your assembler in a folder, called MS1-[Student's Full Name] (*e.g.* MS1-AmirYazdanbakhsh). Then, zip this folder and name the zip file as MS1-[Student's Full Name].zip (*e.g.* MS1-AmirYazdanbakhsh.zip). Please submit this zip file to T-Square by the deadline. Team members can work together and implement the assembler. However, each of you have to submit your own zip file.

Second Milestone [40 pts] (Due: Sunday, 11:55 PM, November 12^{th}, 2017)

In this milestone, you will implement a single cycle processor with a limited number of instructions. Your implemented single cycle processor has to be functional and includes ALU-R, ALU-I, CMP-R, and CMP-I instruction categories. The list of instructions belong to each category is provided in project2-ISA-description.pdf. Your design has to include a separate module for the controller of the single-cycle processor. You have to name this file SCProc-Controller.v. The project directory name and the zip file name have to comply with the following naming formats. Similar to the first milestone, you have to create a folder, called MS2-[Student's Full Name] (*e.g.* MS2-AmirYazdanbakhsh) and include all of your Quartus project files into this folder. Please zip this folder as MS2-[Student's Full Name].zip (*e.g.* MS2-AmirYazdanbakhsh.zip) and upload it to T-Square by the deadline. Team members can work together and implement the single cycle processor. However, each of you have to submit your own zip file.

Third Milestone [40 pts] (Due: Sunday, 11:55 PM, November 20^{th}, 2017)

You have to implement the single cycle processor in the entirety. That is, the processor has to be fully functional and can execute all the instructions specified in project2-ISA-description.pdf. Similar to the previous milestone, your design has to include a separate module for the controller of the single-cycle processor. You have to name this file SCProc-Controller.v. There are three deliverables that you have to submit:

1. A project report file in PDF. *Each* person has to submit his or her own report. The report should describe the approach taken when implementing the project, which problems were encountered, how the identified problems were fixed, and what the student's own contribution (*i.e.* which member of the group did what) to the project was. Note that it is acceptable if the two members of the group worked together on the implementation (as in, sat together and got something working), and it is OK to say so in the report. If your report is missing, you will lose 50% of the points.
2. Quartus project files of your single cycle processors.
3. Python assembler file from the first milestone.

If you miss to upload any file that your project requires for testing, you will not be allowed to fix your project by pulling files from somewhere other than T-Square. You should adhere with the following format and organization for the third milestone:

- Create a directory and name it MS3-[Student's Full Name] (*e.g.* MS3-AmirYazdanbakhsh)
- Create a subdirectory named report and include your report file. The report file has to be named SCProc-[Student's Full Name].pdf (*e.g.* SCProc-AmirYazdanbakhsh.pdf).
- Create another subdirectory name quartus and include all the Quartus project files and subdirectories.
- Create another subdirectory name assembler and include your assembler (*e.g.* assembler-AmirYazdanbakhsh.py).
- Archive directory MS3-[Student's Full Name] into MS3-[Student's Full Name].zip (*e.g.* MS3-AmirYazdanbakhsh.zip) and submit this zip file to T-Square.

Note 1. You get zero points if you do not follow the naming format.

Note 2. Your Quartus project has to be synthesized on FPGA without any other modifications.

Note 3. Please use **Quartus II Web Edition 13.0sp1** from Altera. Here's a quick installation guide: `https://www.cc.gatech.edu/~hadi/teaching/cs3220/doc/quick-start/quick-start-de0.pdf`.

Note 4. This project is a **team** project. As such, you must work together with your teammate. The zip file you submit should the same as the one submitted by your teammate. However, each person has to write their own report. Identical reports in a team get **zero** points.

Note 5. Double check your submission to T-Square and make sure that all the files are correctly uploaded. We can not accept any missing files after the deadline. The best practice would be to download the zip file from T-Square and test your work again to make sure it is correct.

Note 6. Testbench is not required, but is encouraged to verify your design.

Good Luck!