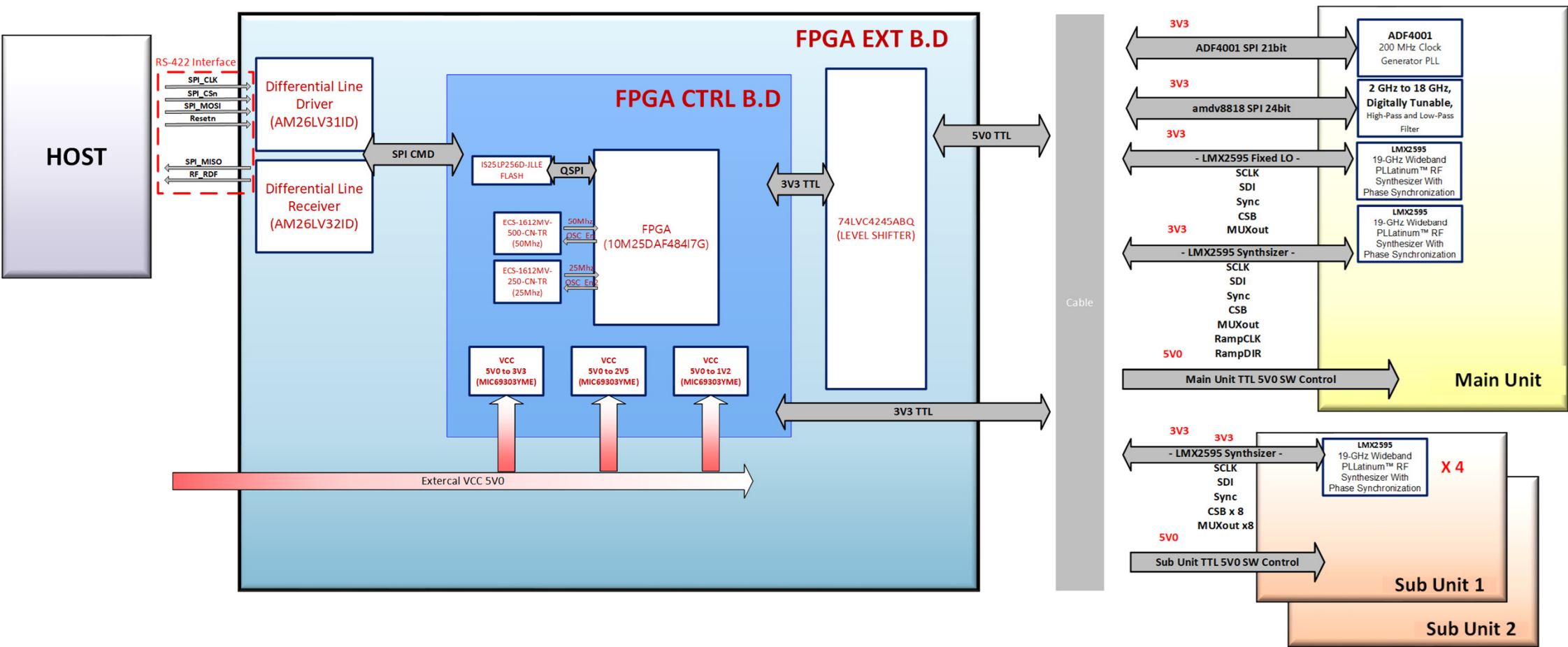
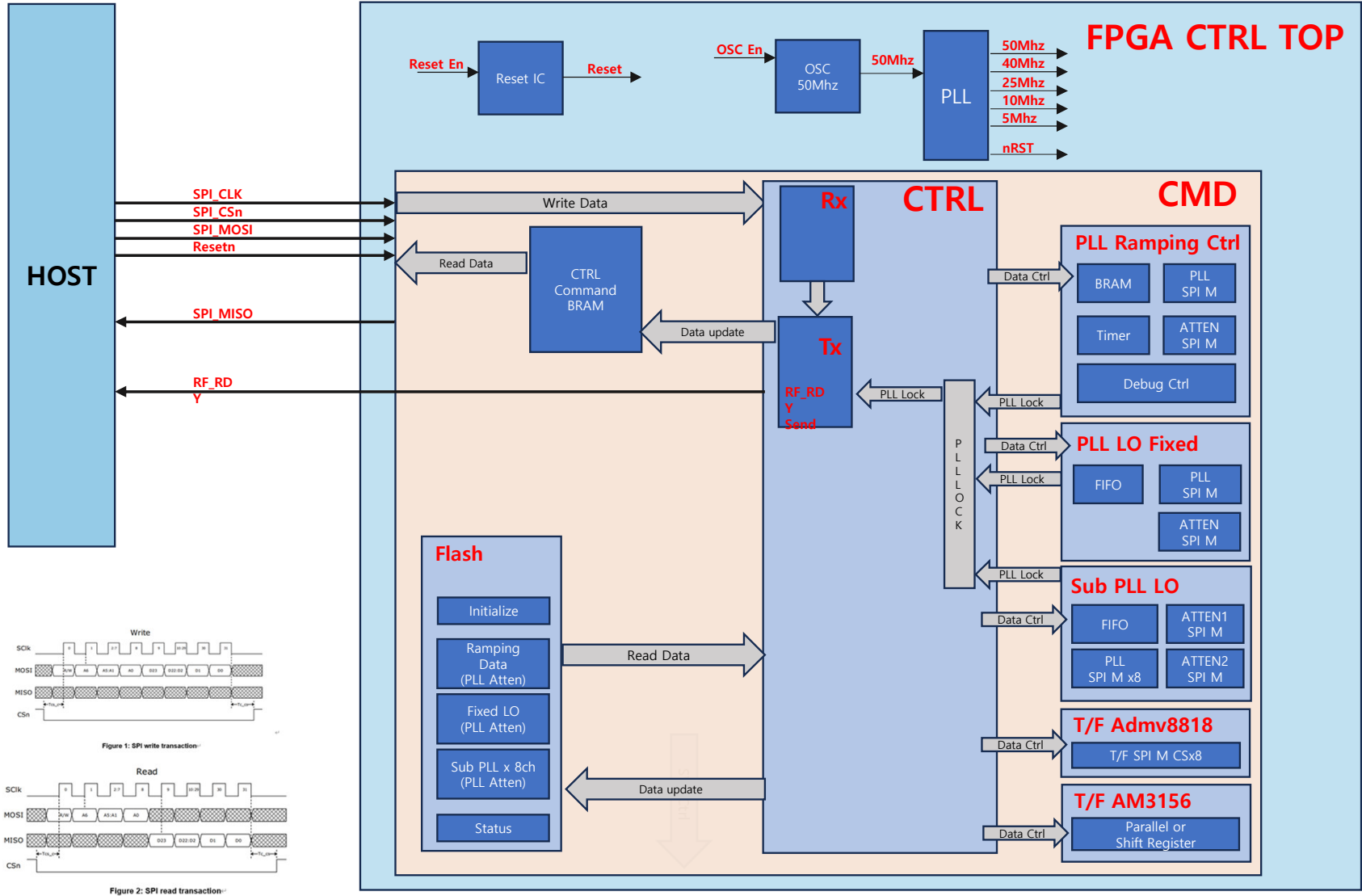


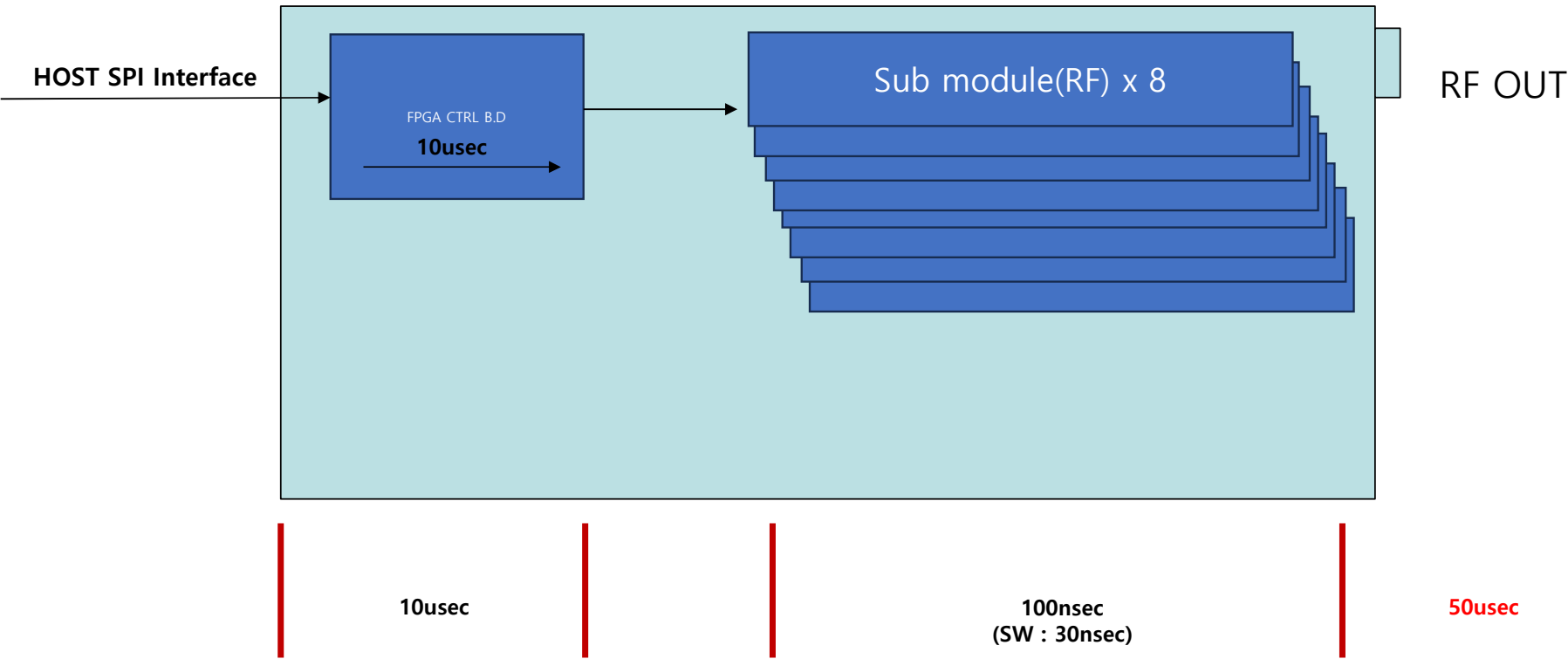
1. HardWare Block Diagram



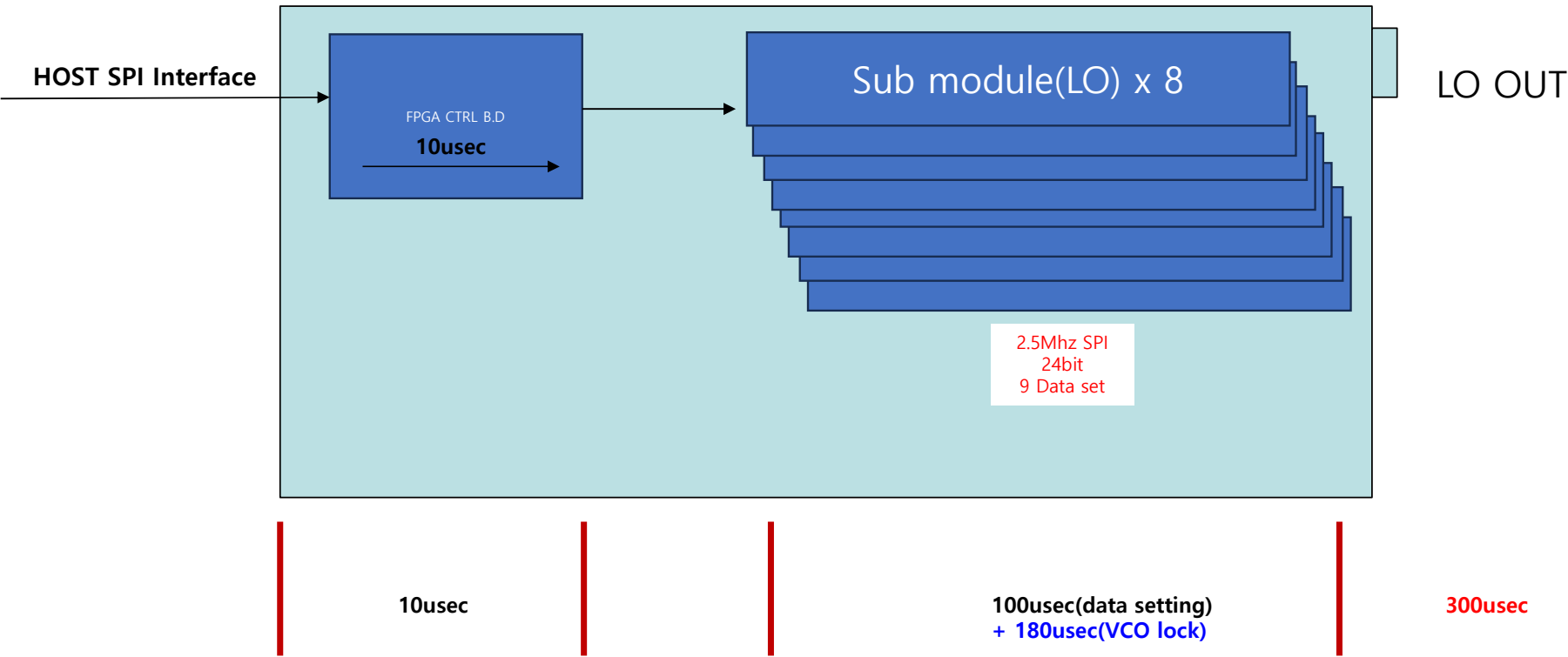
2. SoftWare Block Diagram



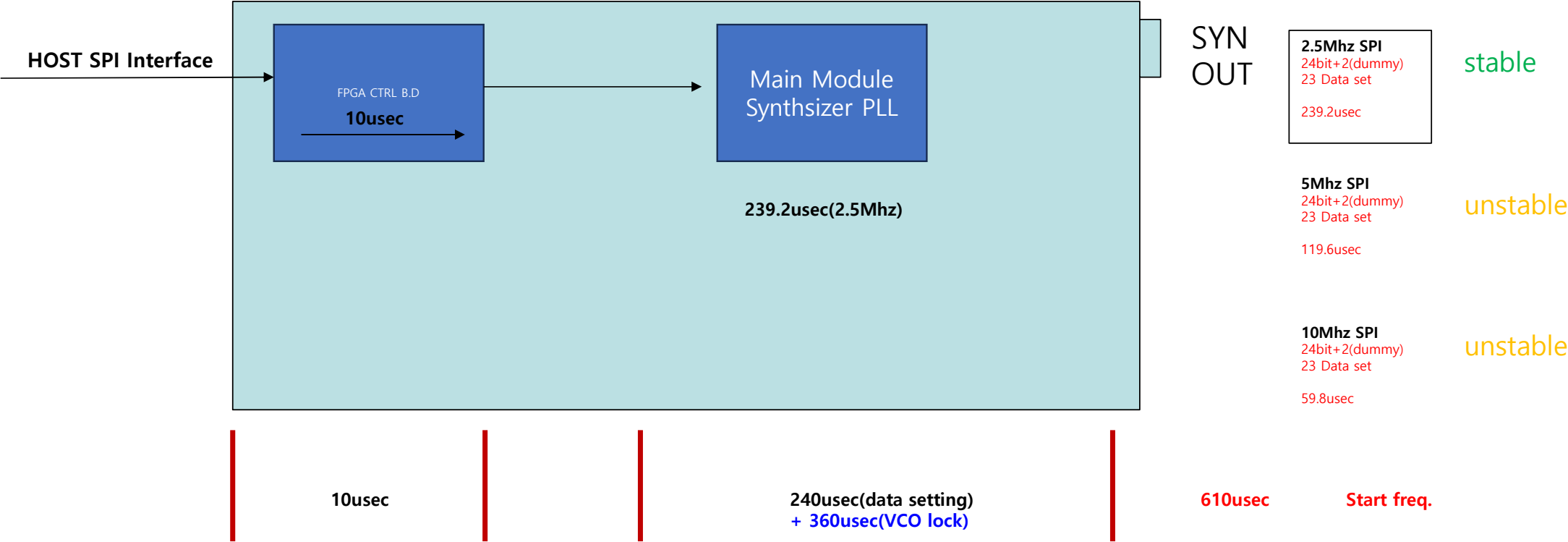
3.1 HOST to LO output Time



3.2 HOST to LO output Time



3.3 HOST to SYN(CAL) Time



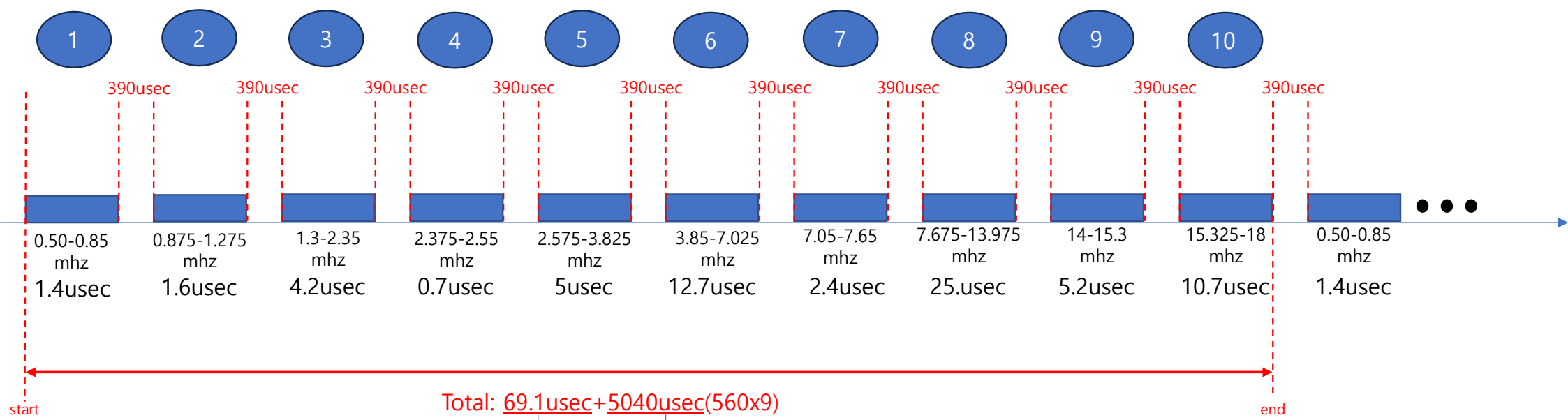
4.1 BIT SYNTHESIZER FREQ PLAN

In order to ramping using by LMX2595, frequency is needed to be changed.
(Freq: 0.5~18GHz, Step size: 25MHz)

BIT LO SYNTHESIZER FREQ PLAN										
No	PLL									RAMP
	START	END	R	Fpd	N Divider	Channel Divider	VCO	Fvco	RFoutA	RAMP0 Step Freq
1	500MHz	850MHz	5	25MHz	320	16	VCO	8000MHz	500MHz	400MHz
2	875MHz	1275MHz	5	25MHz	420	12	VCO	10500MHz	875MHz	300MHz
3	1300MHz	2350MHz	5	25MHz	312	6	VCO	7800MHz	1300MHz	150MHz
4	2375MHz	2550MHz	5	25MHz	570	6	VCO	14250MHz	2375MHz	150MHz
5	2575MHz	3825MHz	5	25MHz	412	4	VCO	10300MHz	2575MHz	100MHz
6	3850MHz	7025MHz	5	25MHz	308	2	VCO	7700MHz	3850MHz	50MHz
7	7050MHz	7650MHz	5	25MHz	564	2	VCO	14100MHz	7050MHz	50MHz
8	7675MHz	14000MHz	5	25MHz	307	2	VCO	7675MHz	7675MHz	25MHz
9	14000MHz	15300MHz	5	25MHz	560	2	VCO	14000MHz	14000MHz	25MHz
10	15300MHz	18000MHz	10	12.5MHz	612	2	VCO Doubler	7650MHz	15300MHz	12.5MHz

4.2 HOST to SYN(CAL) Time

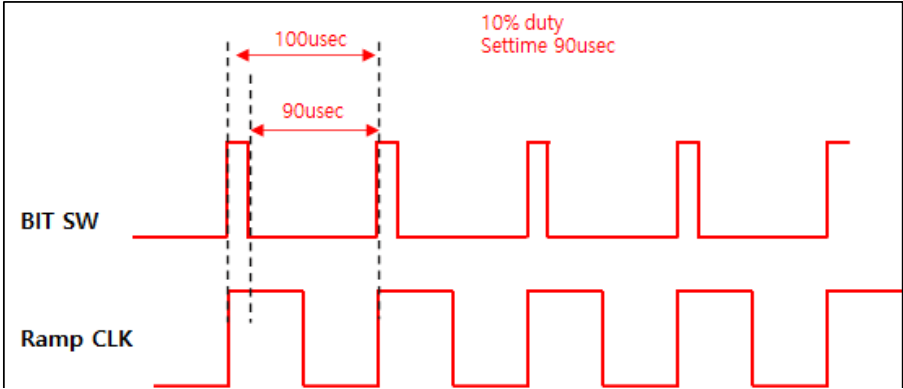
390usec is required for every single switching the frequency.



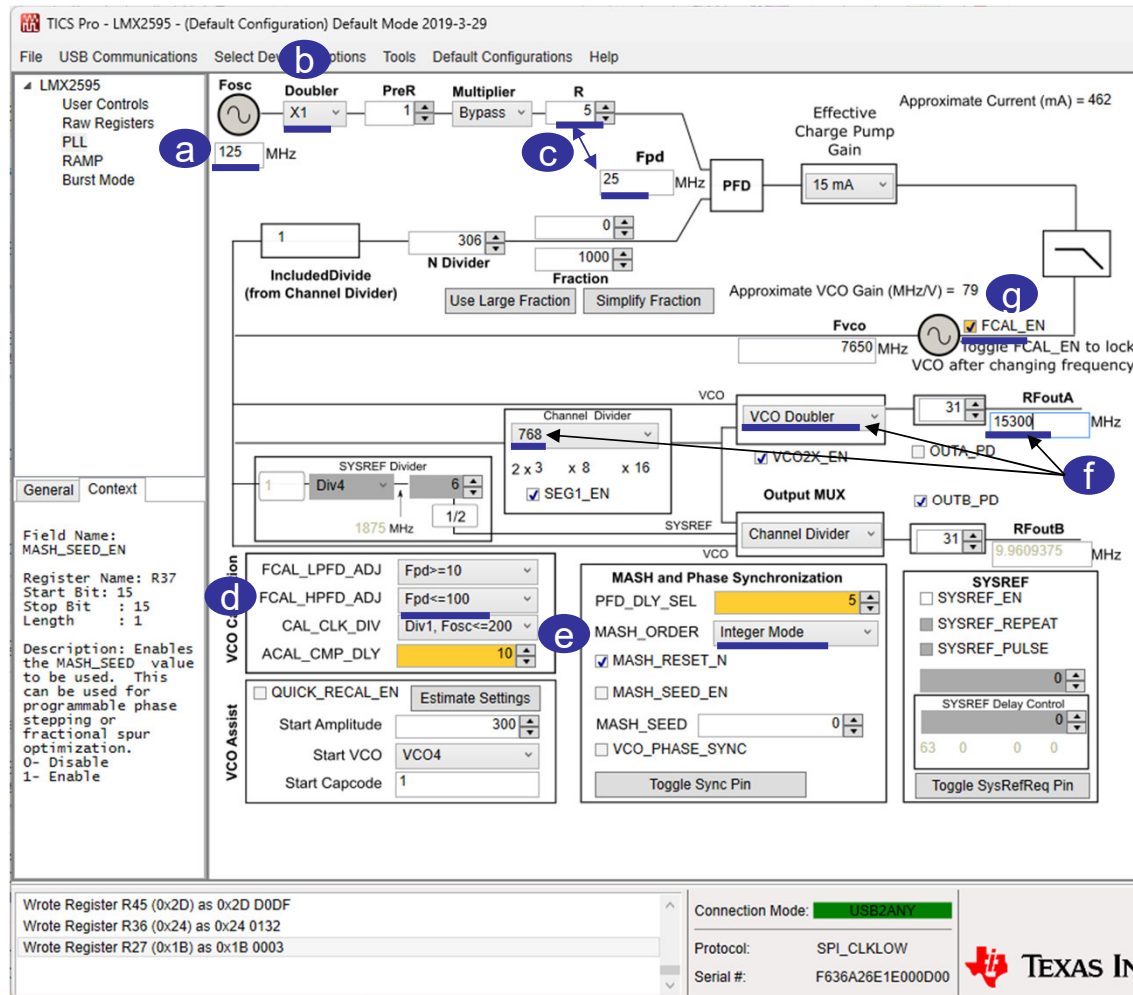
Ramping timing Freq changing timing

ELTA's requirement Ramping timing: 70usec

BRN's requirement Ramping timing: 5109.1usec



5. LMX2595 SYNTHESIZER RAMPING SETTING(1)



1. PLL REG Order

- Fosc: 125MHz
Wrote Register R36 (0x24) as 0x24 0038
- Doubler(OSCin doubler): x1
Wrote Register R9 (0x9) as 0x09 0604
Wrote Register R36 (0x24) as 0x24 0070
- R: 5 ->[Fpd:25MHz]자동변경
Wrote Register R36 (0x24) as 0x24 0230
Wrote Register R11 (0xB) as 0x0B 0058
- FCAL_HPFD_ADJ: Fpd<=100
Wrote Register R0 (0x0) as 0x00 241C
- MASH_ORDER: Integer Mode
Wrote Register R44 (0x2C) as 0x2C 1FA0
- RFoutA: 15300MHz(VCO DOUBLER)
Wrote Register R45 (0x2D) as 0x2D D0DF
Wrote Register R36 (0x24) as 0x24 0132
Wrote Register R27 (0x1B) as 0x1B 0003
- FCAL_EN
Wrote Register R0 (0x0) as 0x00 2414
Wrote Register R0 (0x0) as 0x00 241C

<RAMPING PLL 세팅>

5. LMX2595 SYNTHESIZER RAMPING SETTING(2)

From PLL Tab
VCO Start (MHz) 7650 Phase Detector (MHz) 25 Accumulator Start 51338280
Ensure that the PLL denominator is set to a value of 4294967295 on the PLL tab as it is forced to this in ramping mode

Ramp Limits
VCO Output Limit: High 20000 MHz, Low 5000 MHz
RAMP_LIMIT Register Programming: Decimal Value 4294967295, 2's Complement 4294967295, -1778384896, 6811549695

VCO Calibration
Threshold 30 MHz
RAMP_THRESH 20132659
RAMP_DLY_CNT, RAMP_SCALE_CNT

Manual Ramping Mode
RAMP_MANUAL checked
Clock Ramp, Reverse Direction
Ramp Step Frequency (MHz): RAMP0 12.5, RAMP1 -100
Ramping Setup Procedure:
1. Ensure RAMP_EN=0
2. Define $F_{sm} = F_{osc} / (2 \cdot CAL_CLK_DIV)$ or Use Input Multiplier to adjust
3. If $F_{pd} > F_{sm}$, then increase CAL_CLK_DIV
4. If F_{pd} Exceeds 125 MHz, then reduce it
5. Setup Ramp GUI. Note it can still be setup with RAMP_EN=0
6. Whenever "Update Ramp GUI" button is orange or phase detector frequency is changed, press the button...
- Ensures that PLL Denominator is 4294967295
- Calculates all Values on Ramp Tab
- Validates Calculations on Ramp Tab
7. Set RAMP_EN=1

Automatic Ramping Mode

Ramp	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	RST	Duration (us)	Dly	Next Ramp	Actual End Frequency (MHz)	RAMPx_LEN	Actual Length With VCO Calibration (us)
RAMP0	14000	14000		100		RAMP1	14000	0	0
RAMP1	14000	14000		100		RAMP0	14000	0	0

Burst Ramping Mode

Log:
Wrote Register R79 (0x4F) as 0x4F 0133
Wrote Register R80 (0x50) as 0x50 3333
Wrote Register R0 (0x0) as 0x00 A41C

Connection Mode: USB2ANY
Protocol: SPI_CLKLOW
Serial #: F636A26E1E000D00

2. Manual Ramping Mode

a. RAMP0(Step Freq: 12.5MHz/
VCO Doubler)

Wrote Register R98 (0x62) as 0x62 0200
Wrote Register R102 (0x66) as 0x66 3C00

b. Update Ramp GUI

PLL_DEN must be 4294967295 in Ramping Mode. Forcing this value on the PLL tab.

Wrote Register R38 (0x26) as 0x26 FFFF
Wrote Register R39 (0x27) as 0x27 FFFF
Wrote Register R82 (0x52) as 0x52 FFFF
Wrote Register R83 (0x53) as 0x53 FFFF
Wrote Register R84 (0x54) as 0x54 0001
Wrote Register R85 (0x55) as 0x55 95FF
Wrote Register R86 (0x56) as 0x56 FFFF
Wrote Register R106 (0x6A) as 0x6A 0001
Wrote Register R79 (0x4F) as 0x4F 0133
Wrote Register R80 (0x50) as 0x50 3333

c. RAMP_EN

Wrote Register R0 (0x0) as 0x00 A41C

<RAMPING 세팅>

5. LMX2595 SYNTHESIZER RAMPING SETTING(3)

TICS Pro - LMX2595 - (Default Configuration) Default Mode 2019-3-29

File USB Communications Select Device Options Tools Default Configurations Help

LMX2595
User Controls
Raw Registers
PLL
RAMP
Burst Mode

Fosc 125 MHz
Doubler X1
PreR 1
Multiplier Bypass
R 5
Fpd 25 MHz
PFD
Effective Charge Pump Gain 15 mA
Approximate Current (mA) = 462

IncludedDivide (from Channel Divider) 1
N Divider 306
Fraction 0
1000
Use Large Fraction
Simplify Fraction
Approximate VCO Gain (MHz/V) = 79
Fvco 7650 MHz
FCAL_EN

Channel Divider 768
2 x 3 x 8 x 16
SEG1_EN
VCO Doubler
VCO2X_EN
Output MUX
Channel Divider
RFoutA 15300 MHz
RFoutB 9.9609375 MHz

SYSREF Divider
Div4
1875 MHz
1/2

VCO Calibration
FCAL_LPFADJ Fpd >= 10
FCAL_HPFD_ADJ Fpd <= 100
CAL_CLK_DIV Div1, Fosc <= 200
ACAL_CMP_DLY 10
QUICK_RECEN_EN
Start Amplitude 300
Start VCO VCO4
Start Capcode 1

MASH and Phase Synchronization
PFD_DLY_SEL 5
MASH_ORDER Integer Mode
MASH_RESET_N
MASH_SEED_EN
MASH_SEED 0
VCO_PHASE_SYNC
Toggle Sync Pin

SYSREF
SYSREF_EN
SYSREF_REPEAT
SYSREF_PULSE
SYSREF Delay Control
63 0 0 0
Toggle SysRefReq Pin

Field Name: MASH_SEED_EN
Register Name: R37
Start Bit: 15
Stop Bit: 15
Length: 1
Description: Enables the MASH_SEED value to be used. This can be used for programmable phase stepping or fractional spur optimization.
0- Disable
1- Enable

Write Register R45 (0x2D) as 0x2D D0DF
Write Register R36 (0x24) as 0x24 0132
Write Register R27 (0x1B) as 0x1B 0003

Connection Mode: USB2ANY
Protocol: SPI_CLKLOW
Serial #: F636A26E1E000D00

TEXAS INSTRUMENTS

3. FCAL_EN

a. FCAL_EN(해지 후 다시 체크)

Wrote Register R0 (0x0) as 0x00 A414
Wrote Register R0 (0x0) as 0x00 A41C

FCAL_EN

<RAMPING 세팅 후 FCAL_EN 재 설정>

6. BLOCK DIAGRAM FOR POWER SUPPLY FLOW

