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910-0372
MQFC Software ICD

Ref. specification – xxxxxx

Revision Table

Rev	Description	Date
-_02	Updates per IDD meeting 08/02/21	2021-08-04
-_01	Add hold bit and A2D refresh bits to Status register. Updates to Cal config and Switch register to reflect hardware.	2021-07-01
-_00	Initial Release	2021-06-22

Document State = Pre-Prod Release

1 Connector Definitions

1.1 Connector TBD

Pin	Name	Function	Type	
	SClk	SPI_Clk	LVTTL 3.3V Input	
	CSn	SPI_CSn	LVTTL 3.3V Input	
	MOSI	SPI_MOSI	LVTTL 3.3V Input	
	MISO	SPI_MISO	LVTTL 3.3V Output	
		Reset	LVTTL 3.3V Input	
	GNDD	Digital Ground	Digital Ground	

2 Communication Format

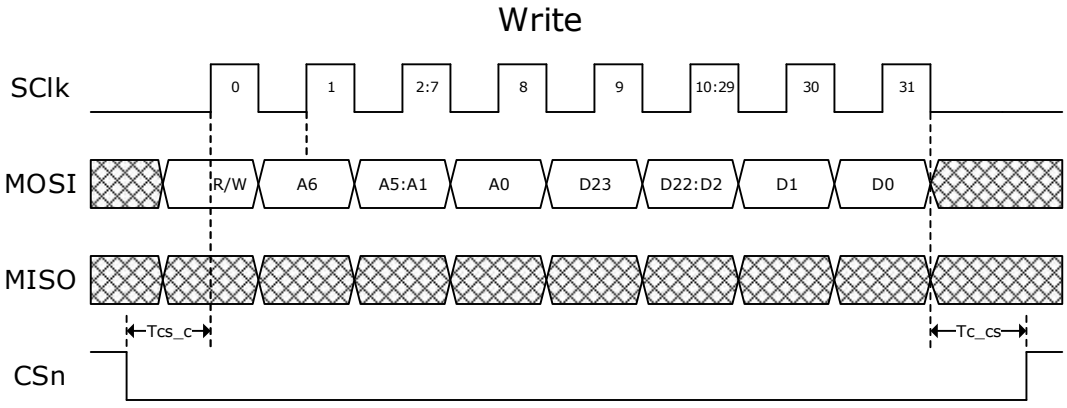
The MQFC controller acts as the "SLAVE" and the main controller acts as the "MASTER". The MQFC controller uses a typical SPI interface. The SPI interface consists of four lines: SClk, CSn, MOSI, and MISO. The SPI interface uses 32-bit commands. All write commands transmitted to MQFC must be 32-bits long. Read commands contain the R/W bit set to 1 and the register address on MOSI while the returning data is clocked out on the MISO line during the data portion of the same 32-bit sequence.

2.1 SPI Interface Specifications

The specified clock frequency for this application is 10MHz. Only the MASTER controller supplies the SPI 10MHz clock. The 10MHz clock is only supplied during SPI transactions.

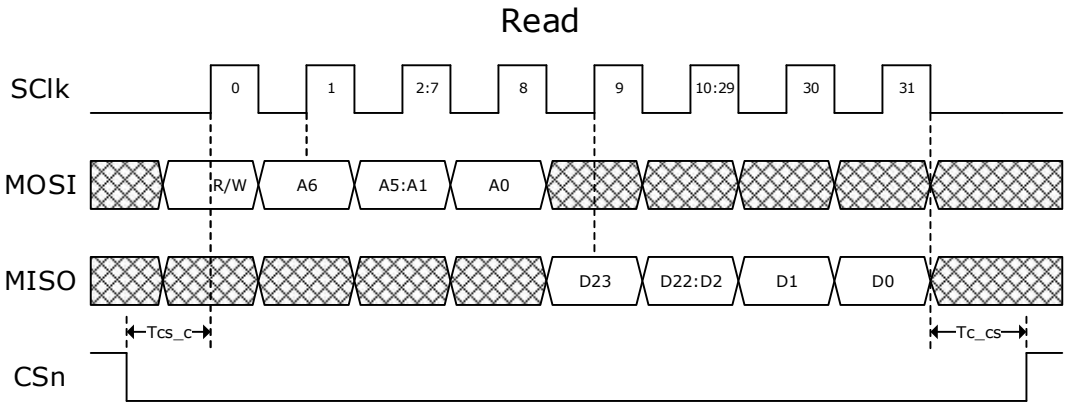
2.1.1 SPI Write Transaction

A typical Write transaction is shown below. The new command goes out on the MOSI line, and the data is registered by the SLAVE on each positive clock edge. The R/W bit is set to 0. The transaction is initiated when the MASTER pulls the CSn line low for a period of Tcs_c before the first positive clock edge and held low for the remainder of the transaction. The MASTER then pulls the CSn line high Tc_cs after the last negative clock edge. See timing constraints in the table below for minimum timing specifications.



2.1.2 SPI Read Transaction

A typical Read transaction is shown below. The Read transaction sequence starts out with the MASTER clocking out the R/W bit set to 1 and clocking out the address bits on each positive clock edge. The SLAVE then starts clocking out the read data on the next clock falling edge. The MASTER registers the 24 bits of data on the remaining 24 positive clock edges.



2.1.3 Timing constraints

Parameter	Description	Min	Max
SPI Clock Frequency	Maximum frequency of SPI Clock		10 MHz
Tcs_c	Time between CSn going low and the first positive clock edge	TBDns	
Tc_cs	Time between last negative clock edge and CSn going high	TBDns	

3 SPI Command Set

Table 3.0 contains a list of SPI commands/registers used to communicate with the MQFC. For details about each command, refer to the section 4, "Command Details".

	b31	b30:b24	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Command	**R/W**	**A6:A0**	**D23:D0**																							
Status	1	0x00	0	0	0	Busy	0	0	Load Rdy	RF Rdy	Temperature								0	0	0	COM	PS	LDC	LDR	LDL
Frequency	1/0	0x01	Hold	0	0	0	0	0	0	0	0	Frequency														
Atten Ctrl	1/0	0x02	Hold	Ch4 Atten					0	Ch3 Atten					0	Ch2 Atten					0	Ch1 Atten				
RF Setup	1/0	0x03	Hold	0	0	Atten					0	Frequency														
Switch Sel	1/0	0x04	Hold	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW4		SW3		SW2		SW1	
Cal Config	1/0	0x05	Hold	0	0	0	0	0	Cal Config		0	Cal Frequency														
Mod Load	1/0	0x06	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1
Spare	1/0	0x07	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
AD Ch 1&2	1	0x08	A2D Channel 2												A2D Channel 1											
AD Ch 3&4	1	0x09	A2D Channel 4												A2D Channel 3											
AD Ch 5&6	1	0x0A	A2D Channel 6												A2D Channel 5											
AD Ch 7&8	1	0x0B	A2D Channel 8												A2D Channel 7											
Spare	1/0	0x0C	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Serial Num	1	0x0D	0	0	0	0	Serial Number																			
S/W Rev	1	0x0E	0	0	0	0	0	0	0	0	0	0	Major Revision							Minor Revision						
Spare	1/0	0x0F	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Registers 0x10-0x7F are factory reserved																										

Table 3.0: SPI Command Set

4 Command Details

4.1 Status

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read only
Address	30:24	Register address bits	0000000
Unused	23:21	Spare bits	0
Busy	20	Indicates whether the CPU is busy. All write commands received while this bit is high will be ignored. Read register commands will be addressed as usual.	0: CPU is not busy 1: CPU is busy
Unused	19:18	Spare bits	0
Load Ready	17	Indicates whether the output preload registers are ready to be loaded to the RF module.	0: Not ready 1: Ready
RF Ready	16	Indicates when the RF module is finished loading.	0: Not ready 1: Ready
Temperature	15:8	Module temperature in 2's compliment format.	C9 = -55°C … 7D = 125°C
Unused	7:5	Spare bits	0
COM Error	4	Sets when register entry is out of range. Clears and sets when CPU hold is cleared.	0: No error 1: Error
PS	3	Power supply status	0: Fail 1: Pass
LDC	2	Indicates whether the Cal/BIT synthesizer is locked	0: Cal/BIT synth is unlocked 1: Cal/BIT synth is locked
LDR	1	Indicates whether the Reference synthesizer is locked	0: Ref synth is unlocked 1: Ref synth is locked
LDL	0	Indicates whether the LO synthesizer is locked	0: LO synth is unlocked 1: LO synth is locked

4.1.1 The Status register can be read at any time. The R/W bit must be set to 1.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	Busy	0	0	Load Rdy	RF Rdy	Temperature								0	0	0	COM	PS	LDC	LDR	LDL

4.2 Frequency

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write to register 1: Read from register
Address	30:24	Register address bits	0000001
CPU hold	23	Setting this bit high, holds the CPU from updating any of the output preload registers. Used to update multiple registers at once.	0: CPU updates output preload registers 1: CPU does not update output preload registers
Unused	22:15	Spare bits	0
Frequency	14:0	Tune frequency for the MQFC. Entry should be in MHz.	000 0111 1101 0000: 2000 000 0111 1111 1000: 2040 ... 100 0110 0101 0000: 18000

4.2.1 The Frequency register controls the tune frequency for the MQFC. The setting should be in MHz and has a range of 2000-18000. All entries outside this range or outside the MQFC specified step size will be ignored and frequency will be returned to current setting.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Frequency in MHz														
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.2.2 The Frequency register can be read at any time. Response will be in MHz.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	Frequency in MHz														

4.3 Attenuation Control

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write to register 1: Read from register
Address	30:24	Register address bits	0000010
CPU hold	23	Setting this bit high, holds the CPU from updating any of the output preload registers. Used to update multiple registers at once.	0: CPU updates output preload registers 1: CPU does not update output preload registers
Ch4 Attenuation	22:18	Attenuation Control for RF channel 4. Entry should be in dB.	00000: 0dB … 11110: 30dB
Unused	17	Spare bit	0
Ch3 Attenuation	16:12	Attenuation Control for RF channel 3. Entry should be in dB.	00000: 0dB … 11110: 30dB
Unused	11	Spare bit	0
Ch2 Attenuation	10:6	Attenuation Control for RF channel 2. Entry should be in dB.	00000: 0dB … 11110: 30dB
Unused	5	Spare bit	0
Ch1 Attenuation	4:0	Attenuation Control for RF channel 1. Entry should be in dB.	00000: 0dB … 11110: 30dB

4.3.1 The Attenuation register controls the RF attenuation for the MQFC. Settings are in dB and have a range of 0-30. All entries outside this range or outside the MQFC specified step size will be ignored and attenuation will be returned to current setting.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	0	1	0	0	Ch4 Atten					0	Ch3 Atten					0	Ch2 Atten					0	Ch1 Atten				
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.3.2 The Attenuation register can be read at any time. Responses will be in dB.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	Ch4 Atten					0	Ch3 Atten					0	Ch2 Atten					0	Ch1 Atten				

4.4 RF Setup

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write to register 1: Read from register
Address	30:24	Register address bits	0000011
CPU hold	23	Setting this bit high, holds the CPU from updating any of the output preload registers. Used to update multiple registers at once.	0: CPU updates output preload registers 1: CPU does not update output preload registers
Unused	22:21	Spare bits	0
Attenuation	20:16	Attenuation Control for all RF channels. Entry should be in dB.	00000: 0dB … 11110: 30dB
Unused	15	Spare bit	0
Frequency	14:0	Tune frequency for the MQFC. Entry should be in MHz.	000 0111 1101 0000: 2000 000 0111 1111 1000: 2040 ... 100 0110 0101 0000: 18000

4.4.1 The RF Setup register command combines the Frequency and Attenuation register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	0	1	1	0	0	0	Attenuation					0	Frequency														
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.4.2 The RF Setup register can be read at any time. The tune frequency portion will be in MHz and the gain control portion will be in dB.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	Attenuation					0	Frequency														

4.5 Switch Select

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write to register 1: Read from register
Address	30:24	Register address bits	0000100
CPU hold	23	Setting this bit high, holds the CPU from updating any of the output preload registers. Used to update multiple registers at once.	0: CPU updates output preload registers 1: CPU does not update output preload registers
Unused	22:8	Spare bit	0
SW4	7:6	Antenna 4 switch position	TBD: Antenna Left TBD: Antenna Right TBD: Terminated TBD: BIT/Cal
SW3	5:4	Antenna 3 switch position	TBD: Antenna Left TBD: Antenna Right TBD: Terminated TBD: BIT/Cal
SW2	3:2	Antenna 2 switch position	TBD: Antenna Left TBD: Antenna Right TBD: Terminated TBD: BIT/Cal
SW1	1:0	Antenna 1 switch position	TBD: Antenna Left TBD: Antenna Right TBD: Terminated TBD: BIT/Cal

4.5.1 The Switch Select register is used to configure the input RF switches.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW4		SW3		SW2		SW1	
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.5.2 The Switch Select register can be read at any time.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW4		SW3		SW2		SW1	

4.6 Cal Configuration

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write to register 1: Read from register
Address	30:24	Register address bits	0000101
CPU hold	23	Setting this bit high, holds the CPU from updating any of the output preload registers. Used to update multiple registers at once.	0: CPU updates output preload registers 1: CPU does not update output preload registers
Unused	22:18	Spare bits	0
Cal/BIT Configuration	17:16	Used to configure the Cal/BIT circuit. Cal Off: The cal synthesizer is powered down. CW mode: Use Switch Select register to set input switch paths. Cal pulsed: The input switches are pulsed between the Cal path and the Switch Select register paths.	00: Cal Off 01: Cal set to CW mode 10: Cal pulsed at 10uS PW, 100uS PRI 11: Cal pulsed at 100uS PW, 1mS PRI
Unused	15	Spare bit	0
Cal Frequency	14:0	Cal/BIT signal tune frequency. Entry should be in MHz.	000 0111 1101 0000: 2000 000 0111 1111 1000: 2040 ... 100 0110 0101 0000: 18000

4.6.1 The Cal Configuration register is used to turn on or off the Cal/BIT function. The Cal Configuration register is also used to control the Cal Frequency. The setting should be in MHz and has a range of 2000-18000. All entries outside this range or outside the MQFC specified step size will be TBD.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	1	0	1	0	0	0	0	0	0	Cal Config		0	Cal Frequency														
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.6.2 The Cal Configuration register can be read at any time. The Cal Frequency response will be in MHz.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	0	0	0	Cal Config		0	Cal Frequency														

4.7 Module Load

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	0: Write only
Address	30:24	Register address bits	00000110
Module Load	23:0	12-bit A2D value from A2D channel 4	0x8000A5

4.7.1 The Module Load register is used to trigger an update to the RF module. There is only one bit configuration that can be used. Once sent, the RF Rdy bit in the Status register is cleared until the update is complete.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1
MISO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

4.8 A2D Channel 1 & 2

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001000
A2D Channel 2	23:12	12-bit A2D value from A2D channel 2	
A2D Channel 1	11:0	12-bit A2D value from A2D channel 1	

4.8.1 The A2D channels 1 & 2 can be read at any time. Note: Data is only current if the A2D bit in the Status register is set to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	A2D Channel 2												A2D Channel 1											

4.9 A2D Channel 3 & 4

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001001
A2D Channel 4	23:12	12-bit A2D value from A2D channel 4	
A2D Channel 3	11:0	12-bit A2D value from A2D channel 3	

4.9.1 The A2D channels 3 & 4 can be read at any time. Note: Data is only current if the A2D bit in the Status register is set to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	A2D Channel 4												A2D Channel 3											

4.10 A2D Channel 5 & 6

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001010
A2D Channel 6	23:12	12-bit A2D value from A2D channel 6	
A2D Channel 5	11:0	12-bit A2D value from A2D channel 5	

4.10.1 The A2D channels 5 & 6 can be read at any time. Note: Data is only current if the A2D bit in the Status register is set to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	A2D Channel 6												A2D Channel 5											

4.11 A2D Channel 7 & 8

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001011
A2D Channel 8	23:12	12-bit A2D value from A2D channel 8	
A2D Channel 7	11:0	12-bit A2D value from A2D channel 7	

4.11.1 The A2D channels 7 & 8 can be read at any time. Note: Data is only current if the A2D bit in the Status register is set to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	A2D Channel 8												A2D Channel 7											

4.12 Serial Number

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001101
Unused	23:20	Spare bits	0
Serial Number	19:0	The unit's Serial Number	Valid range: 0-999999

4.12.1 The Serial Number register is a read only register and can be read at any time. The R/W bit must be set to 1.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	0	Serial Number																			

4.13 Software Revision

Parameter	Bit(s)	Description	Possible Values
R/W	31	Read or Write bit	1: Read Only
Address	30:24	Register address bits	0001110
Unused	23:14	Spare bits	0
Major Rev	13:7	Major Software Revision	Valid range: 0-99
Minor Rev	6:0	Minor Software Revision	Valid range: 0-99

4.13.1 The Software Revision register is a read only register and can be read at any time. The R/W bit must be set to 1.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	0	0	0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	Major Revision							Minor Revision						

5 Updating the RF Module

The following description explains the intended process for configuring the RF module. The intention is to load the CPU with all necessary data with minimal delay time between commands and to allow the CPU to preload output registers for the RF module before being triggered to update. This minimizes RF module update time.

5.1 Start by sending all necessary commands with the hold bit high except for the last command. The last command should be sent with the hold bit low to trigger the CPU to calculate and store the output preload registers.

5.2 Immediately after receiving the command with the hold bit cleared, the CPU will set the busy bit in the Status register high.

5.2.1 At this point, the unit will not except any new commands. Registers can still be read.

5.3 The CPU will confirm the buffered commands are valid and update the associated registers.

5.3.1 If an invalid command is given, all commands are rejected with no register updates, the COM Error bit is set high, the busy bit is cleared, and the unit is ready for commands.

5.4 The CPU makes the necessary calculations and updates the output preload registers.

5.5 Once the CPU is finished, the busy bit is cleared, and the Module Load bit of the status register is set high.

5.6 At this point, the Module Load command can be used at any time to trigger the update of the RF module. When the Module Load command is sent, the

CPU clears the RF Ready bit in the Status register and dumps the output preload registers to update the RF module. Once the update is complete, the RF Ready bit is set high.

5.6.1 The lock detect bits are independent from the RF Ready bit.

6 Spectral Inversion

Freq (GHz)	Spectral Inversion
2.00	Inverted
4.77	Non-inverted
7.13	Inverted
8.73	Non-inverted
12.29	Inverted
16.25	Non-inverted

Table 5.0: Spectral Inversion