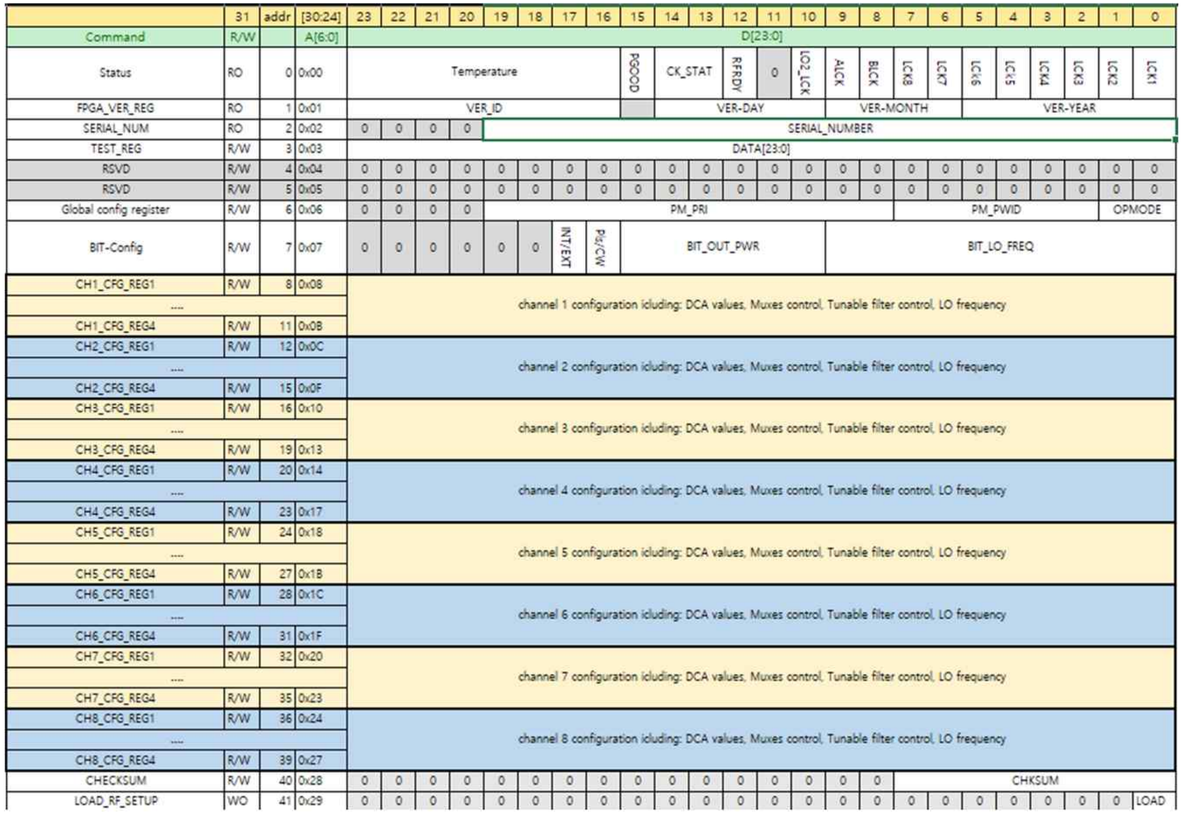
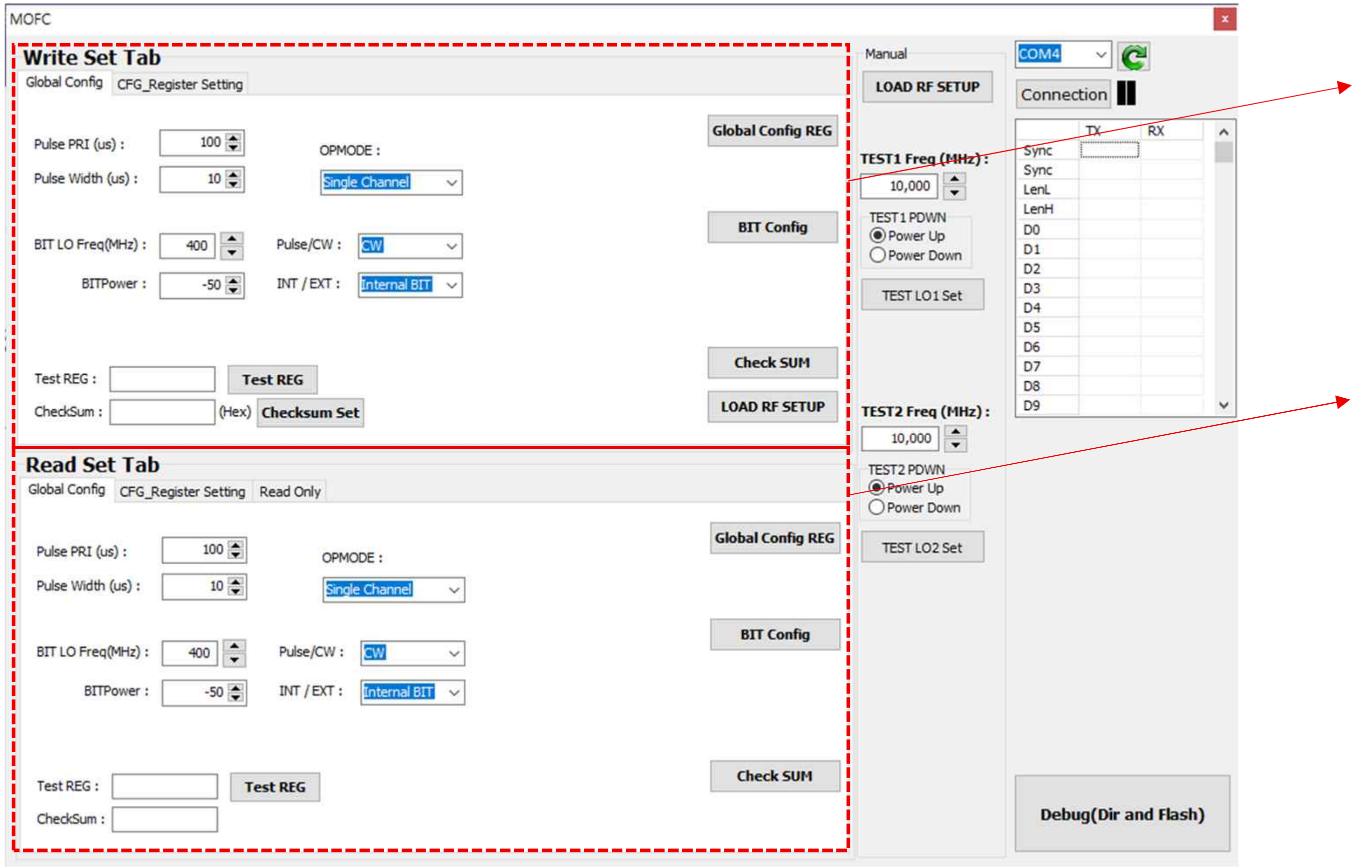


	31	addr	[30:24]	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command	R/W		A[6:0]	D[23:0]																							
Status	RO	0	0x00	Temperature								PGOOD	CK_STAT		RFRDY	0	LO2_LCK	ALCK	BLCK	LCK8	LCK7	LCK6	LCK5	LCK4	LCK3	LCK2	LCK1
FPGA_VER_REG	RO	1	0x01	VER_ID									VER-DAY					VER-MONTH				VER-YEAR					
SERIAL_NUM	RO	2	0x02	0	0	0	0	SERIAL_NUMBER																			
TEST_REG	R/W	3	0x03	DATA[23:0]																							
RSVD	R/W	4	0x04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	R/W	5	0x05	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Global config register	R/W	6	0x06	0	0	0	0	PM_PRI												PM_PWID						OPMODE	
BIT-Config	R/W	7	0x07	0	0	0	0	0	0	INT/EXT	Pls/CW	BIT_OUT_PWR						BIT_LO_FREQ									
CH1_CFG_REG1	R/W	8	0x08	channel 1 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH1_CFG_REG4	R/W	11	0x0B																								
CH2_CFG_REG1	R/W	12	0x0C	channel 2 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH2_CFG_REG4	R/W	15	0x0F																								
CH3_CFG_REG1	R/W	16	0x10	channel 3 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH3_CFG_REG4	R/W	19	0x13																								
CH4_CFG_REG1	R/W	20	0x14	channel 4 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH4_CFG_REG4	R/W	23	0x17																								
CH5_CFG_REG1	R/W	24	0x18	channel 5 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH5_CFG_REG4	R/W	27	0x1B																								
CH6_CFG_REG1	R/W	28	0x1C	channel 6 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH6_CFG_REG4	R/W	31	0x1F																								
CH7_CFG_REG1	R/W	32	0x20	channel 7 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH7_CFG_REG4	R/W	35	0x23																								
CH8_CFG_REG1	R/W	36	0x24	channel 8 configuration icluding: DCA values, Muxes control, Tunable filter control, LO frequency																							
....																											
CH8_CFG_REG4	R/W	39	0x27																								
CHECKSUM	R/W	40	0x28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CHKSUM							
LOAD_RF_SETUP	WO	41	0x29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LOAD

All registers can be read and written using the IDD-based control function configuration.

MOFC BRD GUI Manual



Write Set Tab — Global Config

- Pulse PRI (us) : 100
- Pulse Width (us) : 10
- OPMODE : Single Channel
- BIT LO Freq(MHz) : 400
- Pulse/CW : CW
- BITPower : -50
- INT / EXT : Internal BIT
- Test REG :
- CheckSum : (Hex)

Read Set Tab — Global Config

- Pulse PRI (us) : 100
- Pulse Width (us) : 10
- OPMODE : Single Channel
- BIT LO Freq(MHz) : 400
- Pulse/CW : CW
- BITPower : -50
- INT / EXT : Internal BIT
- Test REG :
- CheckSum :

Manual

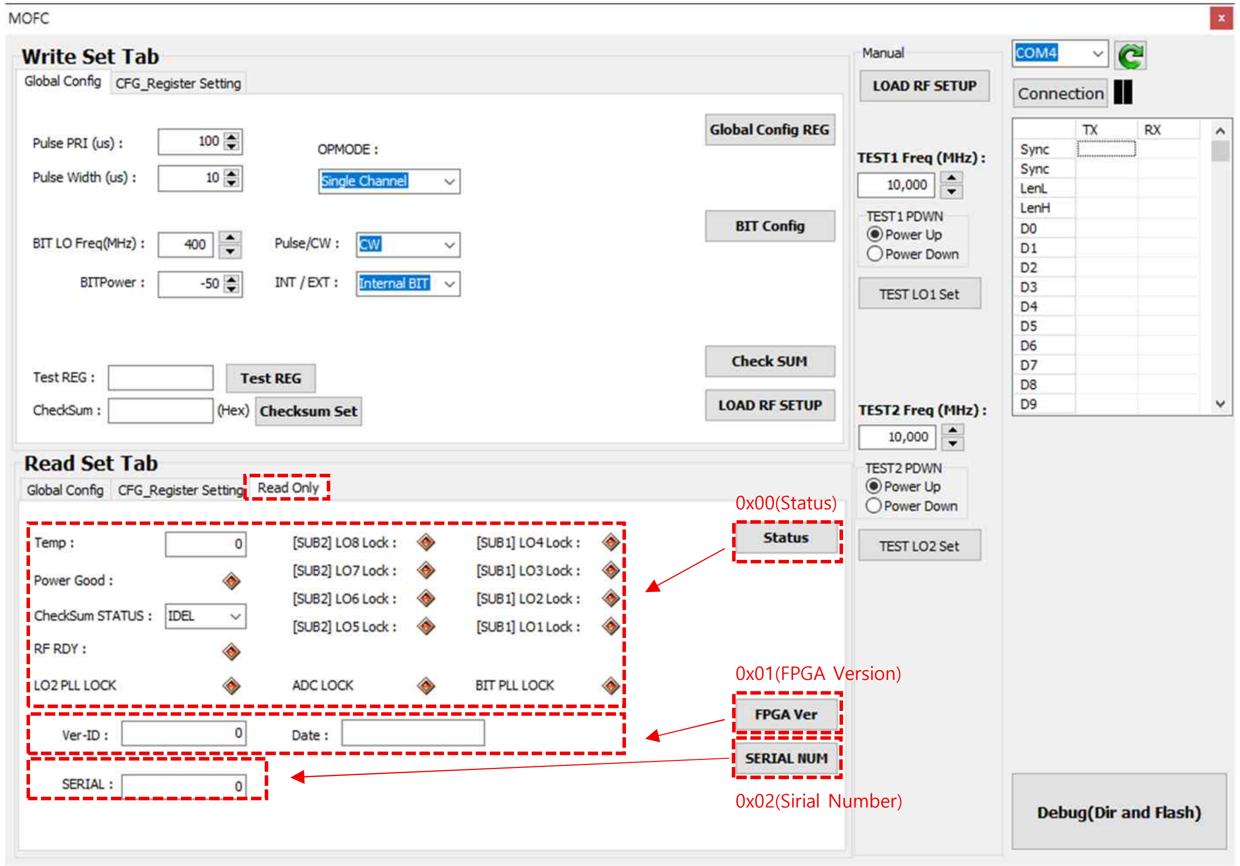
- TEST1 Freq (MHz) : 10,000
- TEST1 PDWN: ● Power Up ○ Power Down
- TEST2 Freq (MHz) : 10,000
- TEST2 PDWN: ● Power Up ○ Power Down
- COM4

All Write Ctrl Tab
ex)
REG 0x06 Send
Adress 0x06 Send

All Read Ctrl Tab
ex)
REG 0x06 Send
Adress 0x86 Send and
Request Data update

The Read and Write functions are separated into upper and lower sections.
The upper section is for Write operations, and the lower section is for Read operations.

MOFC BRD GUI Manual(0x00, 0x01, 0x02)



Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 400

Pulse/CW : CW

BITPower : -50

INT / EXT : Internal BIT

Test REG :

CheckSum : (Hex)

TEST1 Freq (MHz) : 10,000

TEST1 PDWN ● Power Up ○ Power Down

TEST2 Freq (MHz) : 10,000

TEST2 PDWN ● Power Up ○ Power Down

COM4

Temp : 0

CheckSum STATUS : IDEL

Ver-ID : 0

Date :

SERIAL : 0

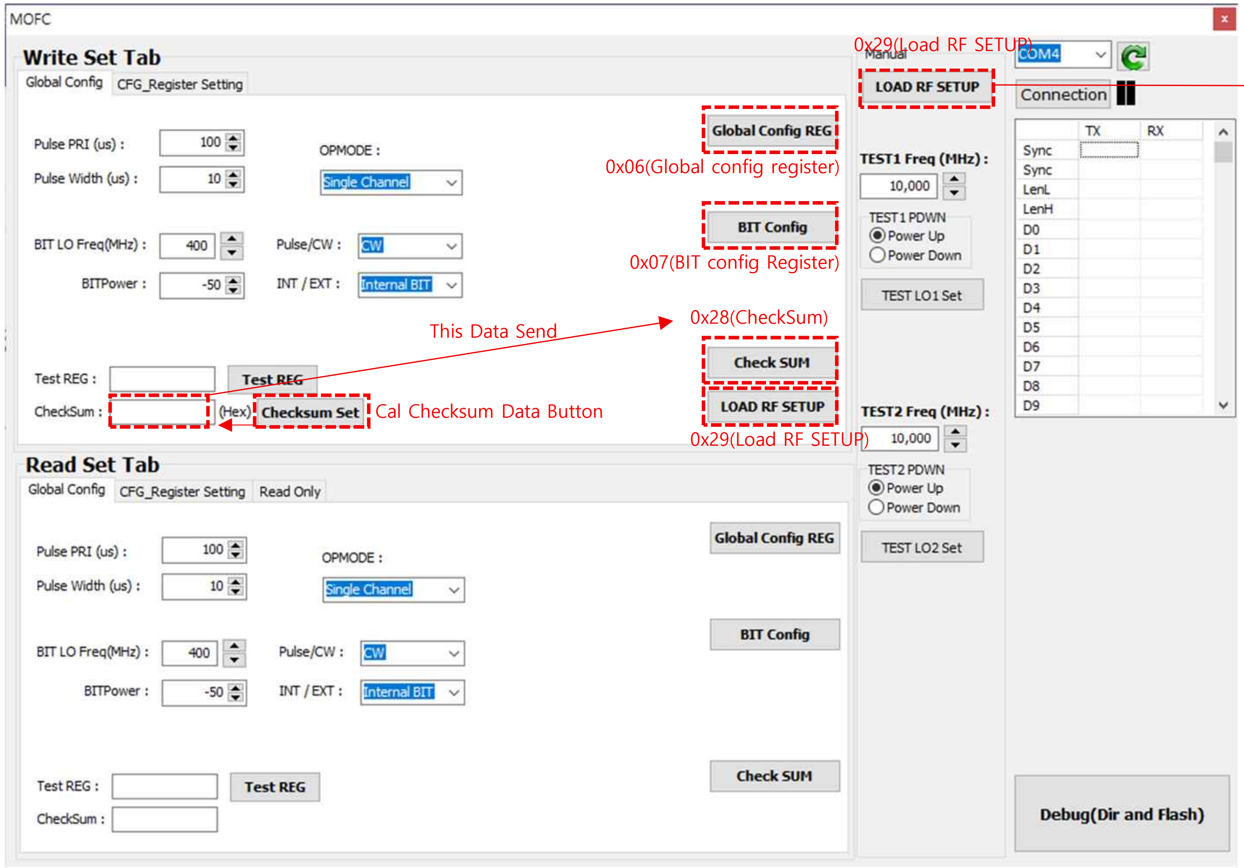
0x00(Status)

0x01(FPGA Version)

0x02(Sirial Number)

The Read Set tab reads status information and current configuration Reg values.

MOFC BRD GUI Manual(0x06, 0x07, 0x28, 0x29)



Write Set Tab – Global Config

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 400

Pulse/CW : CW

BITPower : -50

INT / EXT : Internal BIT

Test REG :

CheckSum : (Hex)

COM4

TEST1 Freq (MHz) : 10,000

TEST1 PDWN

● Power Up

○ Power Down

TEST2 Freq (MHz) : 10,000

TEST2 PDWN

● Power Up

○ Power Down

	TX	RX
Sync		
Sync		
LenL		
LenH		
D0		
D1		
D2		
D3		
D4		
D5		
D6		
D7		
D8		
D9		

Read Set Tab – Global Config

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 400

Pulse/CW : CW

BITPower : -50

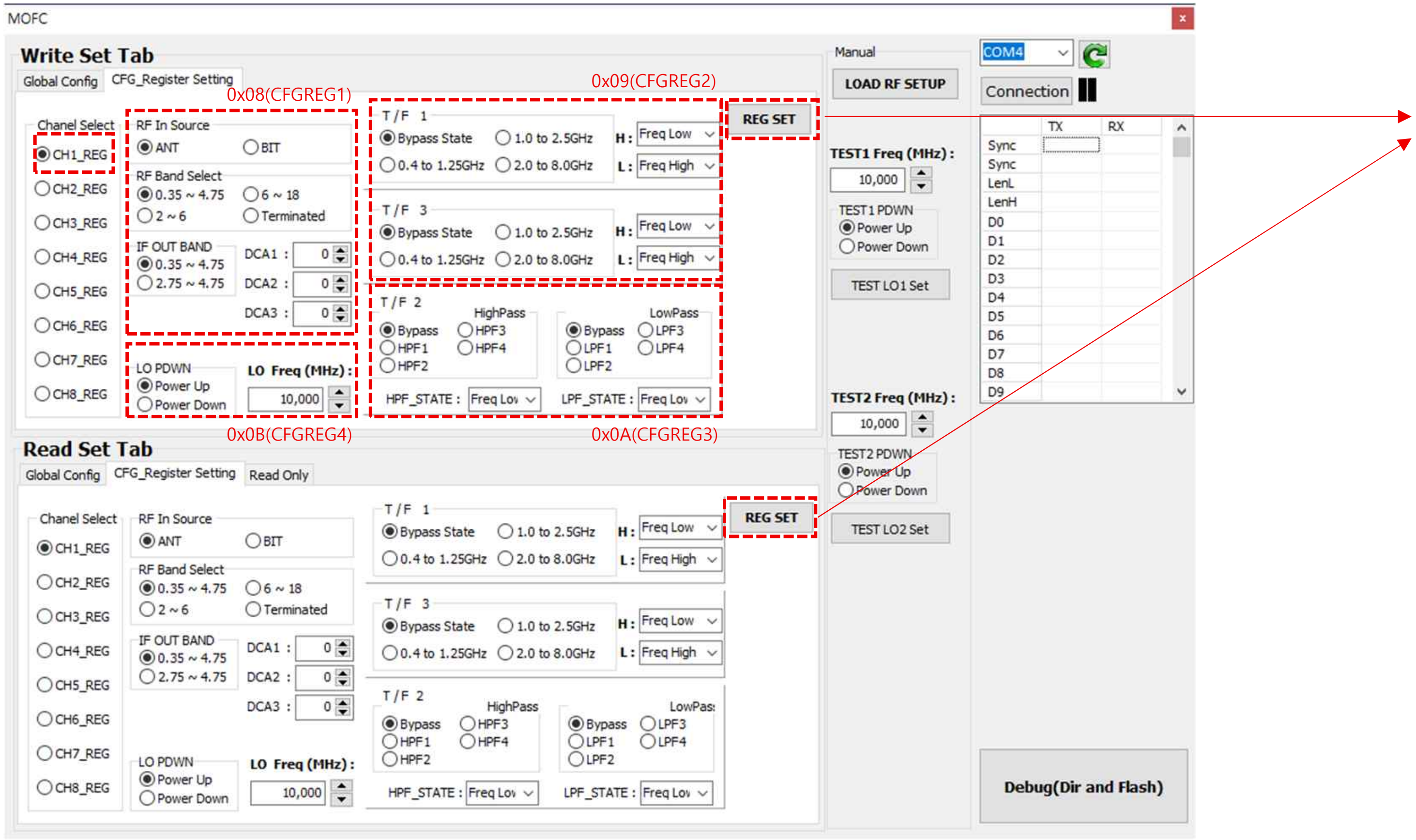
INT / EXT : Internal BIT

Test REG :

CheckSum :

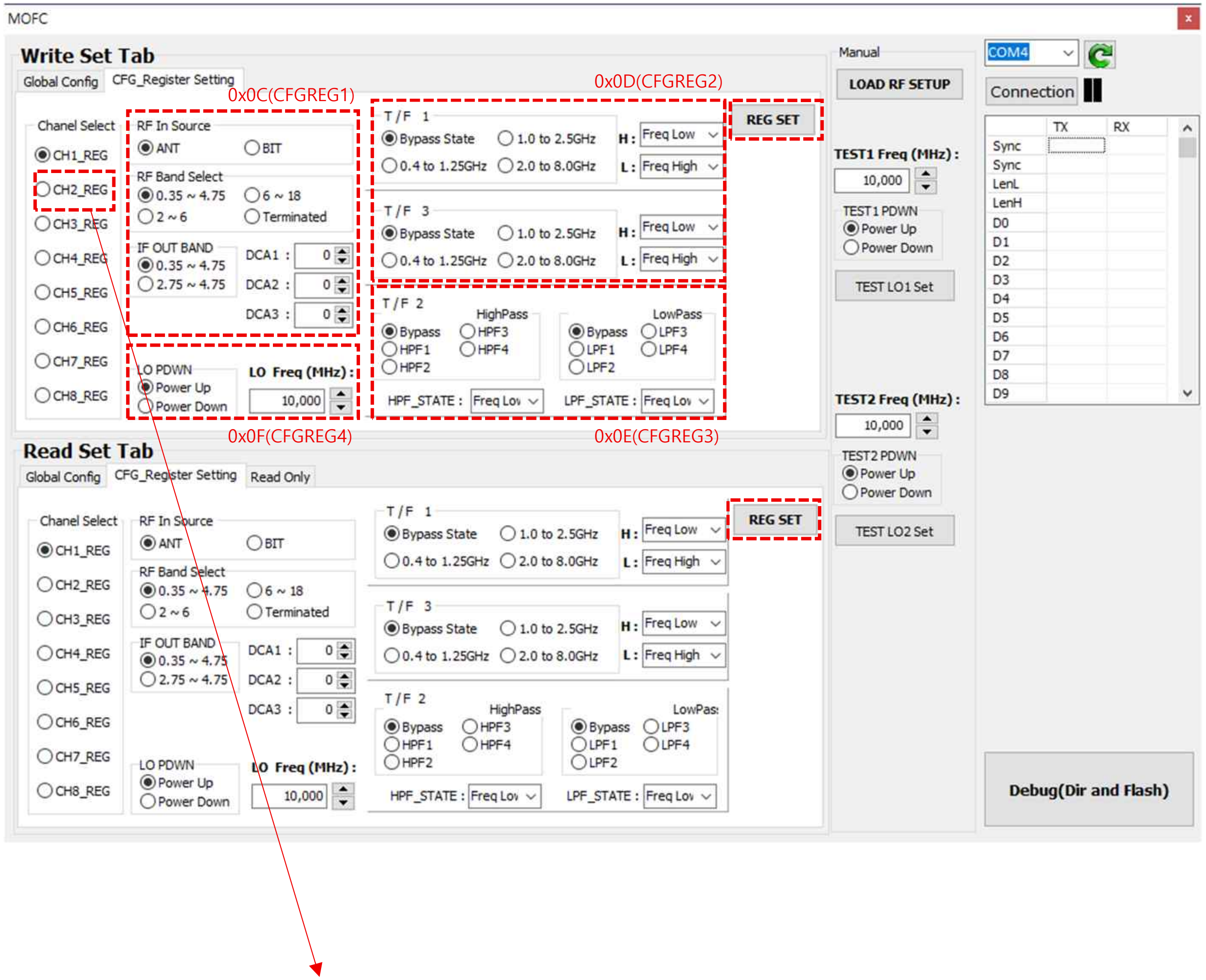
For convenience, I created one more tab outside.

MOFC BRD GUI Manual(Ch1 CFG 0x08, 0x09, 0x0A, 0x0B)



For convenience, pressing the REG SET button will sequentially transmit from CFGREG1 to 4.

MOFC BRD GUI Manual(Ch2 CFG 0x0C, 0x0D, 0x0E, 0x0F)



Write Set Tab — CFG_Register Setting

Chanel Select: ● CH1_REG ○ CH2_REG ○ CH3_REG ○ CH4_REG ○ CH5_REG ○ CH6_REG ○ CH7_REG ○ CH8_REG

RF In Source: ● ANT ○ BIT

RF Band Select: ● 0.35 ~ 4.75 ○ 6 ~ 18 ○ 2 ~ 6 ○ Terminated

IF OUT BAND: ● 0.35 ~ 4.75 ○ 2.75 ~ 4.75

DCA1 : 0
DCA2 : 0
DCA3 : 0

LO PDWN: ● Power Up ○ Power Down

LO Freq (MHz) : 10,000

T/F 1: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz; H : Freq Low; L : Freq High

T/F 3: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz; H : Freq Low; L : Freq High

T/F 2: HighPass: ● Bypass ○ HPF3 ○ HPF1 ○ HPF4 ○ HPF2; LowPass: ● Bypass ○ LPF3 ○ LPF1 ○ LPF4 ○ LPF2

HPF_STATE : Freq Lov
LPF_STATE : Freq Lov

Read Set Tab — CFG_Register Setting

Chanel Select: ● CH1_REG ○ CH2_REG ○ CH3_REG ○ CH4_REG ○ CH5_REG ○ CH6_REG ○ CH7_REG ○ CH8_REG

RF In Source: ● ANT ○ BIT

RF Band Select: ● 0.35 ~ 4.75 ○ 6 ~ 18 ○ 2 ~ 6 ○ Terminated

IF OUT BAND: ● 0.35 ~ 4.75 ○ 2.75 ~ 4.75

DCA1 : 0
DCA2 : 0
DCA3 : 0

LO PDWN: ● Power Up ○ Power Down

LO Freq (MHz) : 10,000

T/F 1: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz; H : Freq Low; L : Freq High

T/F 3: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz; H : Freq Low; L : Freq High

T/F 2: HighPass: ● Bypass ○ HPF3 ○ HPF1 ○ HPF4 ○ HPF2; LowPas: ● Bypass ○ LPF3 ○ LPF1 ○ LPF4 ○ LPF2

HPF_STATE : Freq Lov
LPF_STATE : Freq Lov

TEST1 Freq (MHz) : 10,000

TEST1 PDWN: ● Power Up ○ Power Down

TEST2 Freq (MHz) : 10,000

TEST2 PDWN: ● Power Up ○ Power Down

COM4

	TX	RX
Sync		
Sync		
LenL		
LenH		
D0		
D1		
D2		
D3		
D4		
D5		
D6		
D7		
D8		
D9		

You need to change the channel tab.

MOFC BRD GUI Manual(Ch_CFG_REG)

Ch1 : 0x08(CFGREG1), 0x09(CFGREG2), 0x0A(CFGREG3), 0x0B(CFGREG4)

Ch2 : 0x0C(CFGREG1), 0x0D(CFGREG2), 0x0E(CFGREG3), 0x0F(CFGREG4)

Ch3 : 0x10(CFGREG1), 0x11(CFGREG2), 0x12(CFGREG3), 0x13(CFGREG4)

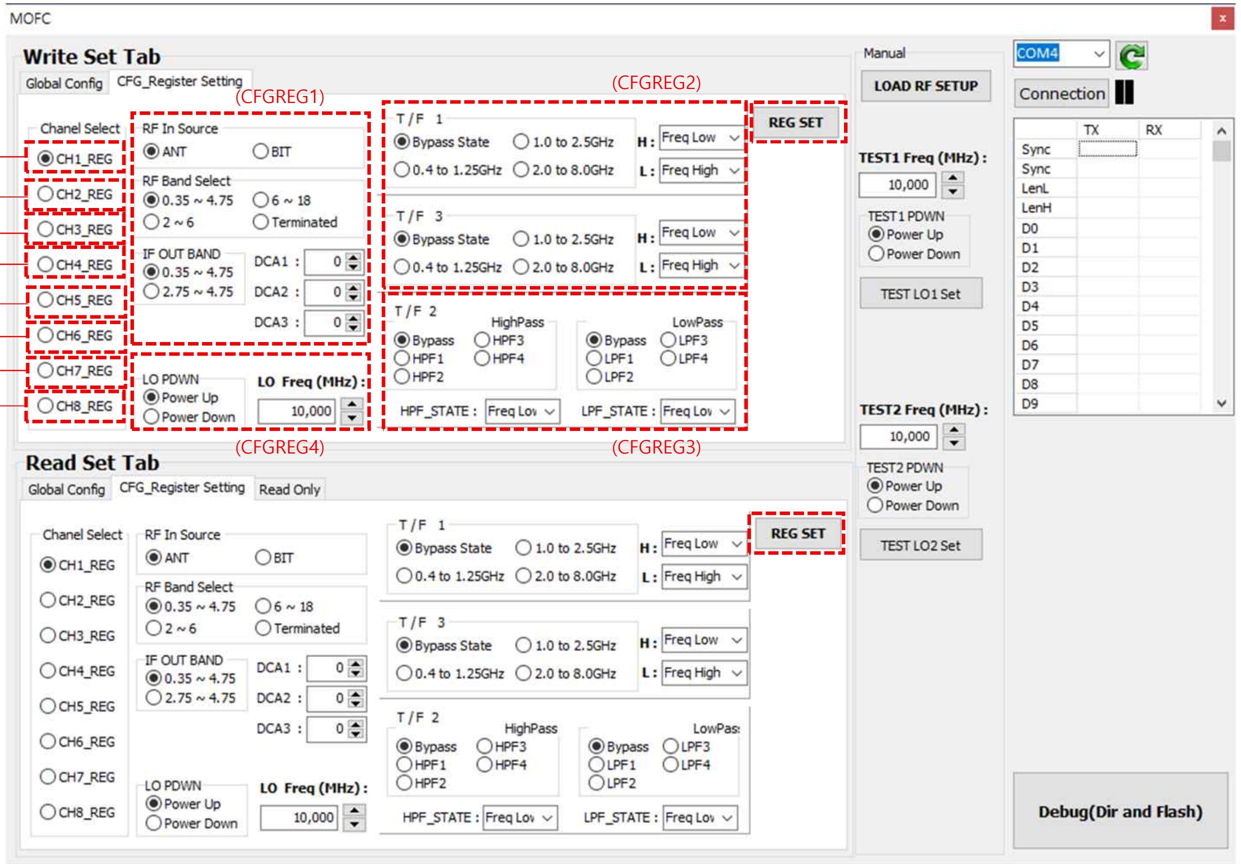
Ch4 : 0x14(CFGREG1), 0x15(CFGREG2), 0x16(CFGREG3), 0x17(CFGREG4)

Ch5 : 0x18(CFGREG1), 0x19(CFGREG2), 0x1A(CFGREG3), 0x1B(CFGREG4)

Ch6 : 0x1C(CFGREG1), 0x1D(CFGREG2), 0x1E(CFGREG3), 0x1F(CFGREG4)

Ch7 : 0x20(CFGREG1), 0x21(CFGREG2), 0x22(CFGREG3), 0x23(CFGREG4)

Ch8 : 0x24(CFGREG1), 0x25(CFGREG2), 0x26(CFGREG3), 0x27(CFGREG4)



MOFC

Write Set Tab

Global Config | CFG_Register Setting

(CFGREG1) (CFGREG2)

Chanel Select: ● CH1_REG ○ CH2_REG ○ CH3_REG ○ CH4_REG ○ CH5_REG ○ CH6_REG ○ CH7_REG ○ CH8_REG

RF In Source: ● ANT ○ BIT

RF Band Select: ● 0.35 ~ 4.75 ○ 6 ~ 18 ○ 2 ~ 6 ○ Terminated

IF OUT BAND: ● 0.35 ~ 4.75 ○ 2.75 ~ 4.75

DCA1 : 0 DCA2 : 0 DCA3 : 0

LO PDWN: ● Power Up ○ Power Down

LO Freq (MHz) : 10,000

T / F 1: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz H : Freq Low L : Freq High

T / F 3: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz H : Freq Low L : Freq High

T / F 2: HighPass ● Bypass ○ HPF3 ○ HPF1 ○ HPF4 ○ HPF2; LowPass ● Bypass ○ LPF3 ○ LPF1 ○ LPF4 ○ LPF2

HPF_STATE : Freq Low LPF_STATE : Freq Low

REG SET

(CFGREG4) (CFGREG3)

Read Set Tab

Global Config | CFG_Register Setting | Read Only

Chanel Select: ● CH1_REG ○ CH2_REG ○ CH3_REG ○ CH4_REG ○ CH5_REG ○ CH6_REG ○ CH7_REG ○ CH8_REG

RF In Source: ● ANT ○ BIT

RF Band Select: ● 0.35 ~ 4.75 ○ 6 ~ 18 ○ 2 ~ 6 ○ Terminated

IF OUT BAND: ● 0.35 ~ 4.75 ○ 2.75 ~ 4.75

DCA1 : 0 DCA2 : 0 DCA3 : 0

LO PDWN: ● Power Up ○ Power Down

LO Freq (MHz) : 10,000

T / F 1: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz H : Freq Low L : Freq High

T / F 3: ● Bypass State ○ 1.0 to 2.5GHz ○ 0.4 to 1.25GHz ○ 2.0 to 8.0GHz H : Freq Low L : Freq High

T / F 2: HighPass ● Bypass ○ HPF3 ○ HPF1 ○ HPF4 ○ HPF2; LowPass ● Bypass ○ LPF3 ○ LPF1 ○ LPF4 ○ LPF2

HPF_STATE : Freq Low LPF_STATE : Freq Low

REG SET

Manual: LOAD RF SETUP

TEST1 Freq (MHz) : 10,000

TEST1 PDWN: ● Power Up ○ Power Down

TEST LO1 Set

TEST2 Freq (MHz) : 10,000

TEST2 PDWN: ● Power Up ○ Power Down

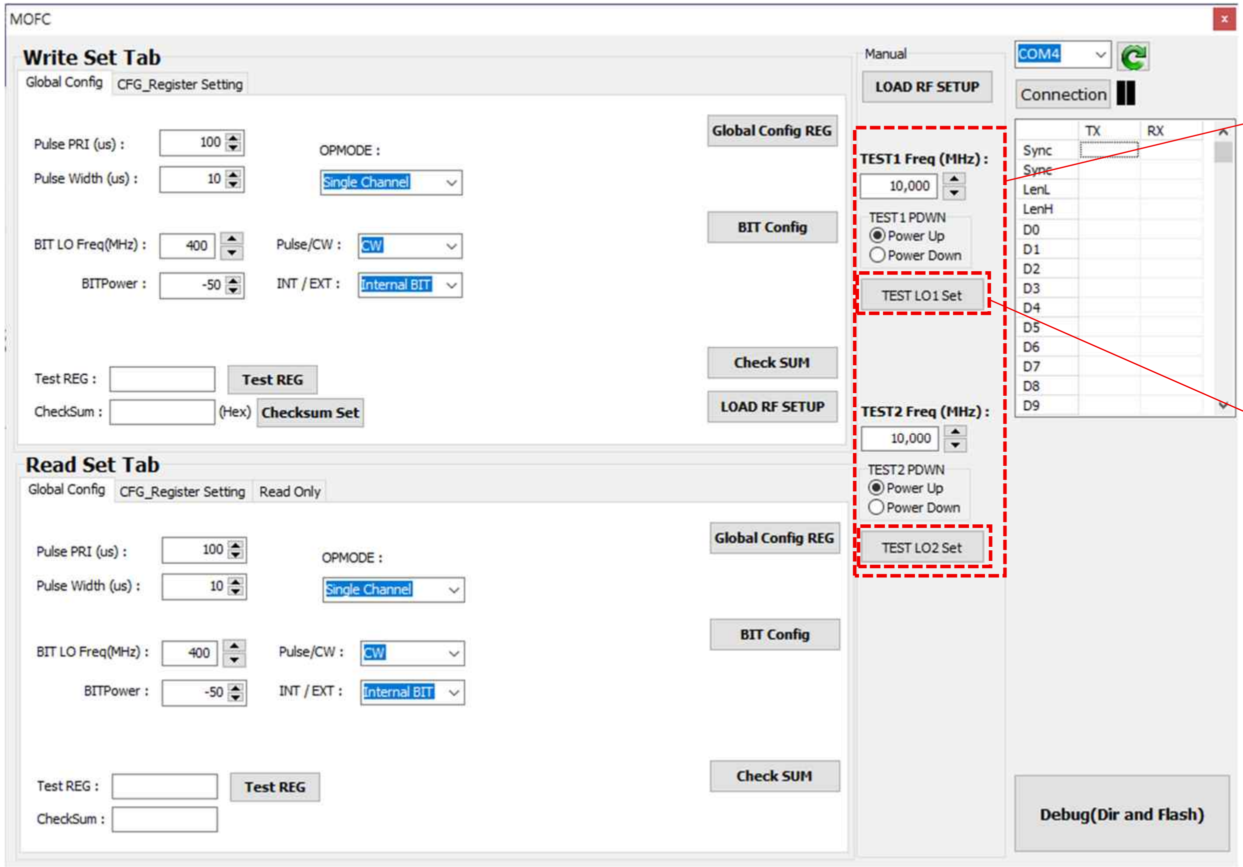
TEST LO2 Set

COM4 Connection

	TX	RX
Sync		
Sync		
LenL		
LenH		
D0		
D1		
D2		
D3		
D4		
D5		
D6		
D7		
D8		
D9		

Debug(Dir and Flash)

MOFC BRD GUI Manual



MOFC

Write Set Tab

Global Config | CFG_Register Setting

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 400

Pulse/CW : CW

BITPower : -50

INT / EXT : Internal BIT

Test REG :

CheckSum : (Hex)

Read Set Tab

Global Config | CFG_Register Setting | Read Only

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 400

Pulse/CW : CW

BITPower : -50

INT / EXT : Internal BIT

Test REG :

CheckSum :

Manual

TEST1 Freq (MHz) : 10,000

TEST1 PDWN
- ● Power Up
- ○ Power Down

TEST2 Freq (MHz) : 10,000

TEST2 PDWN
- ● Power Up
- ○ Power Down

The TEST LO control is not specified in the IDD, so it has been implemented by assigning an address arbitrarily for control purposes.

The settings are applied immediately, regardless of the Load RF SETUP (0x29) command.

	addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command		R/W	A[6:0]							D[23:0]																							
	110	WO	0x6E							0x1 : Test1 LO Direct				Rserved											LO_PDWN	LO_FREQ LSB = 50 MHz per step							
	110	WO	0x6E							0x2 : Test2 LO Direct				Rserved											LO_PDWN	LO_FREQ LSB = 50 MHz per step BIT LO Frequency (MHz) = 10000 + (Register Value x 50)							