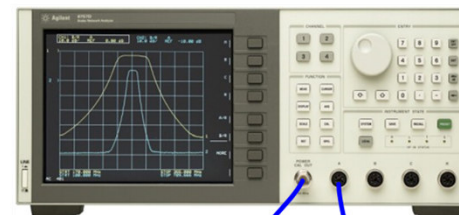


Scalar Network Analyzer



Signal Generator



10MHz (Ref.)

Power Supply



+28VDC

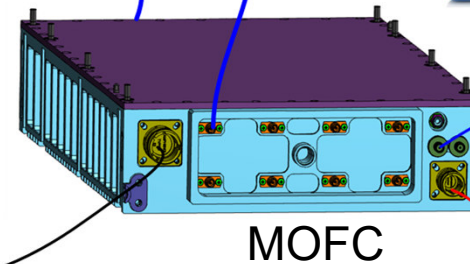
Power Supply



Control

[Test JIG]

MOFC



Write Set Tab

Global Config CFG_Register Setting

Pulse PRI (us): 100

Pulse Width (us): 10

OPMODE: Single Channel

BIT LO Freq(MHz): 500

BITPower: -80

INT / EXT: Internal BIT

Test REG: Test REG

CheckSum: (Hex) Checksum Set

Global Config REG

BIT Config

Check SUM

LOAD RF SETUP

Read Set Tab

Global Config CFG_Register Setting Read Only

Pulse PRI (us): 100

Pulse Width (us): 10

OPMODE: Single Channel

BIT LO Freq(MHz): 500

BITPower: -80

INT / EXT: Internal BIT

Test REG: Test REG

CheckSum: Check SUM

	ADDR	D1	D2	D3
REG_0x0	0	0	40	10
REG_0x1	1	2	41	11
REG_0x2	2	4	42	12
REG_0x3	3	6	43	13
REG_0x4	4	8	44	14
REG_0x5	5	A	45	15
REG_0x6	6	C	46	16
REG_0x7	7	E	47	17
REG_0x8	8	10	48	18
REG_0x9	9	12	49	19
REG_0xA	A	14	4A	1A
REG_0xB	B	16	4B	1B
REG_0xC	C	18	4C	1C
REG_0xD	D	1A	4D	1D
REG_0xE	E	1C	4E	1E
REG_0xF	F	1E	4F	1F
REG_0x10	10	20	50	20
REG_0x11	11	22	51	21
REG_0x12	12	24	52	22
REG_0x13	13	26	53	23
REG_0x14	14	28	54	24
REG_0x15	15	2A	55	25
REG_0x16	16	2C	56	26
REG_0x17	17	2E	57	27
REG_0x18	18	30	58	28
REG_0x19	19	32	59	29
REG_0x1A	1A	34	5A	2A
REG_0x1B	1B	36	5B	2B
REG_0x1C	1C	38	5C	2C
REG_0x1D	1D	3A	5D	2D
REG_0x1E	1E	3C	5E	2E
REG_0x1F	1F	3E	5F	2F
REG_0x20	20	40	60	30
REG_0x21	21	42	61	31
REG_0x22	22	44	62	32
REG_0x23	23	46	63	33
REG_0x24	24	48	64	34
REG_0x25	25	4A	65	35
REG_0x26	26	4C	66	36
REG_0x27	27	4E	67	37
REG_0x28	28	50	68	38

Reg Write

Reg Read

No	Data
D0	
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	
D9	
D10	
D11	
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D36	
D37	
D38	
D39	
D40	

COM8

Connection

TX RX

Sync

Sync

LenL

LenH

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

COM CHECK

Debug(Dir and Flash)

Read

File Write

File Read

Set

RadioGroup1

Read

Write

Write Set Tab

Global Config CFG_Register Setting

Pulse PRI (us): 100

Pulse Width (us): 10

OPMODE: Single Channel

BIT LO Freq(MHz): 500

Pulse/CW: SW

BITPower: -80

INT / EXT: Internal BIT

Test REG: Test REG

Checksum: (Hex) Checksum Set RF Load

Global Config REG

BIT Config

Check SUM

LOAD RF SETUP

Read Set Tab

Global Config CFG_Register Setting Read Only

Pulse PRI (us): 100

Pulse Width (us): 10

OPMODE: Single Channel

BIT LO Freq(MHz): 500

Pulse/CW: SW

BITPower: -80

INT / EXT: Internal BIT

Test REG: Test REG

Checksum:

Global Config REG

BIT Config

Check SUM

	ADDR	D1	D2	D3
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REG_0x6	6	C	46	16
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REG_0x8	8	10	48	18
REG_0x9	9	12	49	19
REG_0xA	A	14	4A	1A
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REG_0xC	C	18	4C	1C
REG_0xD	D	1A	4D	1D
REG_0xE	E	1C	4E	1E
REG_0xF	F	1E	4F	1F
REG_0x10	10	20	50	20
REG_0x11	11	22	51	21
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REG_0x13	13	26	53	23
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REG_0x16	16	2C	56	26
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REG_0x18	18	30	58	28
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REG_0x1C	1C	38	5C	2C
REG_0x1D	1D	3A	5D	2D
REG_0x1E	1E	3C	5E	2E
REG_0x1F	1F	3E	5F	2F
REG_0x20	20	40	60	30
REG_0x21	21	42	61	31
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REG_0x24	24	48	64	34
REG_0x25	25	4A	65	35
REG_0x26	26	4C	66	36
REG_0x27	27	4E	67	37
REG_0x28	28	50	68	38

Reg Write

Reg Read

No	Data
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D4	
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D39	
D40	

COM8

Connection

TX RX

Sync

Sync

LenL

LenH

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

COM CHECK

Debug(Dir and Flash)

Read

File Write

File Read

Set

RadioGroup1

Read

Write

Write Set Tab

Global Config CFG_Register Setting

Pulse PRI (us) : 100
Pulse Width (us) : 10
OPMODE : Single Channel
BIT LO Freq(MHz) : 500
Pulse/CW : SW
BITPower : -80
INT / EXT : Internal BIT

Global Config REG

BIT Config

Check SUM

LOAD RF SETUP

Test REG : Test REG

CheckSum : (Hex) Checksum Set RF Load

Read Set Tab

Global Config CFG_Register Setting Read Only

Pulse PRI (us) : 100
Pulse Width (us) : 10
OPMODE : Single Channel
BIT LO Freq(MHz) : 500
Pulse/CW : SW
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Global Config REG

BIT Config

Check SUM

Test REG : Test REG

CheckSum : Checksum Set

	ADDR	D1	D2	D3
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REG_0x6	6	C	46	16
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REG_0x8	8	10	48	18
REG_0x9	9	12	49	19
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REG_0xC	C	18	4C	1C
REG_0xD	D	1A	4D	1D
REG_0xE	E	1C	4E	1E
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REG_0x10	10	20	50	20
REG_0x11	11	22	51	21
REG_0x12	12	24	52	22
REG_0x13	13	26	53	23
REG_0x14	14	28	54	24
REG_0x15	15	2A	55	25
REG_0x16	16	2C	56	26
REG_0x17	17	2E	57	27
REG_0x18	18	30	58	28
REG_0x19	19	32	59	29
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REG_0x1B	1B	36	5B	2B
REG_0x1C	1C	38	5C	2C
REG_0x1D	1D	3A	5D	2D
REG_0x1E	1E	3C	5E	2E
REG_0x1F	1F	3E	5F	2F
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REG_0x21	21	42	61	31
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REG_0x24	24	48	64	34
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Reg Write

Reg Read

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D33	
D34	
D35	
D36	
D37	
D38	
D39	
D40	

COM8

Connection

TX RX
Sync
Sync
LenL
LenH
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9

COM CHECK

Debug(Dir and Flash)

Read

File Write

File Read

Set

RadioGroup1
☒ Read
☐ Write

Write Set Tab

Global Config CFG_Register Setting

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 500

Pulse/CW : SW

BITPower : -80

INT / EXT : Internal BIT

Test REG :

Test REG

Checksum : (Hex)

Checksum Set

RF Load

Global Config REG

BIT Config

Check SUM

LOAD RF SETUP

Read Set Tab

Global Config CFG_Register Setting Read Only

Pulse PRI (us) : 100

Pulse Width (us) : 10

OPMODE : Single Channel

BIT LO Freq(MHz) : 500

Pulse/CW : SW

BITPower : -80

INT / EXT : Internal BIT

Test REG :

Test REG

Checksum :

Check SUM

Global Config REG

BIT Config

Check SUM

	ADDR	D1	D2	D3
REG_0x0	0	0	40	10
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REG_0xD	D	1A	4D	1D
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REG_0x15	15	2A	55	25
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REG_0x18	18	30	58	28
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REG_0x1B	1B	36	5B	2B
REG_0x1C	1C	38	5C	2C
REG_0x1D	1D	3A	5D	2D
REG_0x1E	1E	3C	5E	2E
REG_0x1F	1F	3E	5F	2F
REG_0x20	20	40	60	30
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REG_0x24	24	48	64	34
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REG_0x28	28	50	68	38

Reg Write

Reg Read

No	Data
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D35	
D36	
D37	
D38	
D39	
D40	

COM8

Connection

TX

RX

Sync

Sync

LenL

LenH

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

COM CHECK

Debug(Dir and Flash)

Read

File Write

File Read

Set

RadioGroup1

Read

Write

Debug

Direct PLLFlash_CtrlFlash_Read

PLL SET

Fixed LO

BIT

Test 1

LO1

LO2

LO3

LO4

Test 2

LO5

LO6

LO7

LO8

☐ R0[0] POWER_DOWN

☐ R0[1] RESET

☐ R0[2] MUXOUT_ID_SEL

R0[8:5] FCAL_L_PFD_ADJ : 0: PFD ≥ 10 MHz

R0[8:7] FCAL_H_PFD_ADJ : 0: PFD ≤ 100 MHz

☐ R0[9] OUT_MUTE

☐ R0[14] VCO_PHASE_SYNC

R0[15] RAMP_EN : 0

R1[2:0] CAL_CLK_DIV : 0: FOSC ≤ 200 MHz

R11[11:4] PLL_R : 5

R14[6:4] CPG : 7: 15 mA

☐ R27[0] VCO2X_EN

☒ R31[1:4] CHDIV_DIV2

R75[10:6] CHDIV : 6: 24

FOSC : 125 (Mhz)

FVCO : 9600 (Mhz)

PPFD : 25 (Mhz)

R34[2:0] PLL_N[18:16] : 0

R36[15:0] PLL_N[15:0] : 384

R37[13:8] PFD_DLY_SEL : 3

R38[15:0] PLL_DEN[31:16] : 0

R39[15:0] PLL_DEN[15:0] : 1000

R42[15:0] PLL_NUM[31:16] : 0

R43[15:0] PLL_NUM[15:0] : 0

R44[2:0] MASH_ORDER : 3: Third order modulator

☐ R44[5] MASH_RESET_N

☐ R44[6] OUTA_PD

☒ R44[7] OUTB_PD

R44[13:8] OUTA_PVIR : 31

R45[12:11] OUTA_MUX : 0: Channel divider

R45[10:0] OUT_ISEL : 0: Maximum output power boost

R45[5:0] OUTB_PVIR : 31(Default)

PLL_N : 384

PLL_DEN : 1000

PLL_NUM : 0

REG_R0

REG_R1

REG_R2

REG_R3

REG_R4

REG_R5

REG_R6

REG_R7

REG_R8

REG_R9

REG_R10

REG_R11

REG_R12

REG_R13

REG_R14

REG_R15

	ADDR	D1	D2	D3
REG_R0	70	00	24	18
REG_R1	70	01	08	08
REG_R2	70	08	00	58
REG_R3	70	0E	1E	70
REG_R4	70	18	00	02
REG_R5	70	1F	43	EC
REG_R6	70	22	00	00
REG_R7	70	24	01	80
REG_R8	70	25	03	04
REG_R9	70	26	00	00
REG_R10	70	27	03	E8
REG_R11	70	2A	00	00
REG_R12	70	2B	00	00
REG_R13	70	2C	1F	83
REG_R14	70	2D	C0	DF
REG_R15	70	4B	08	C0

Reg Write

Direct Register Set: (Hex) Send

RF OUT SET: 400 (Mhz) ☒ R0[3] FCAL_EN