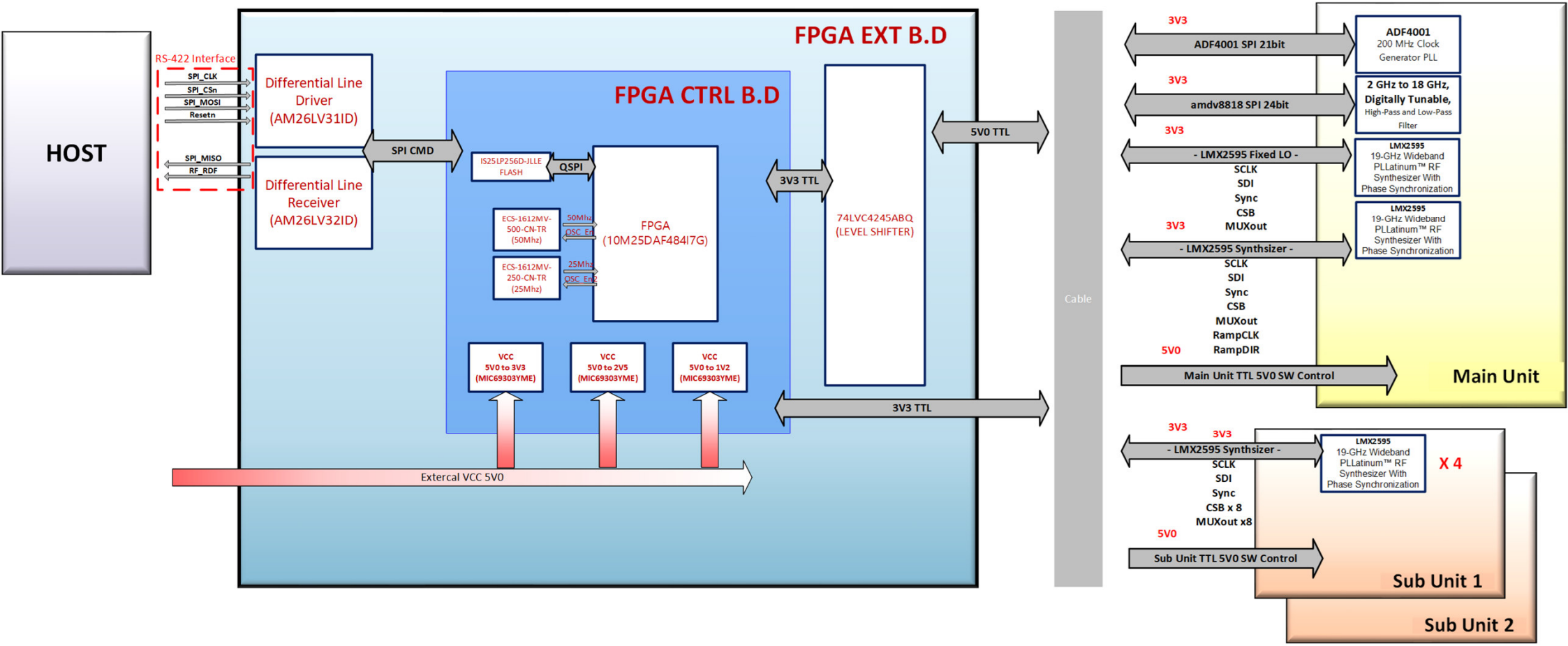
1. HardWare Block Diagram



2. SoftWare Block Diagram

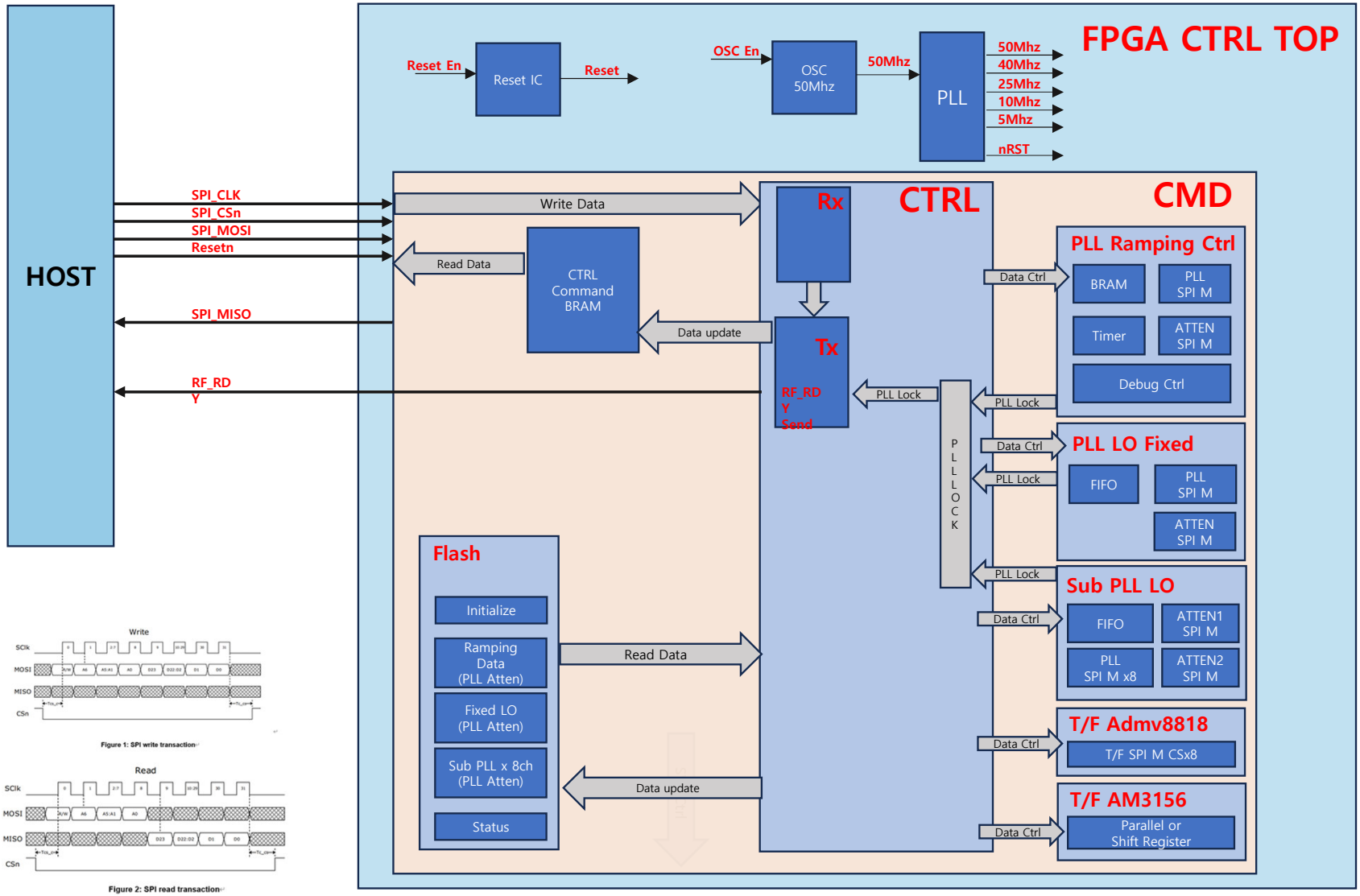
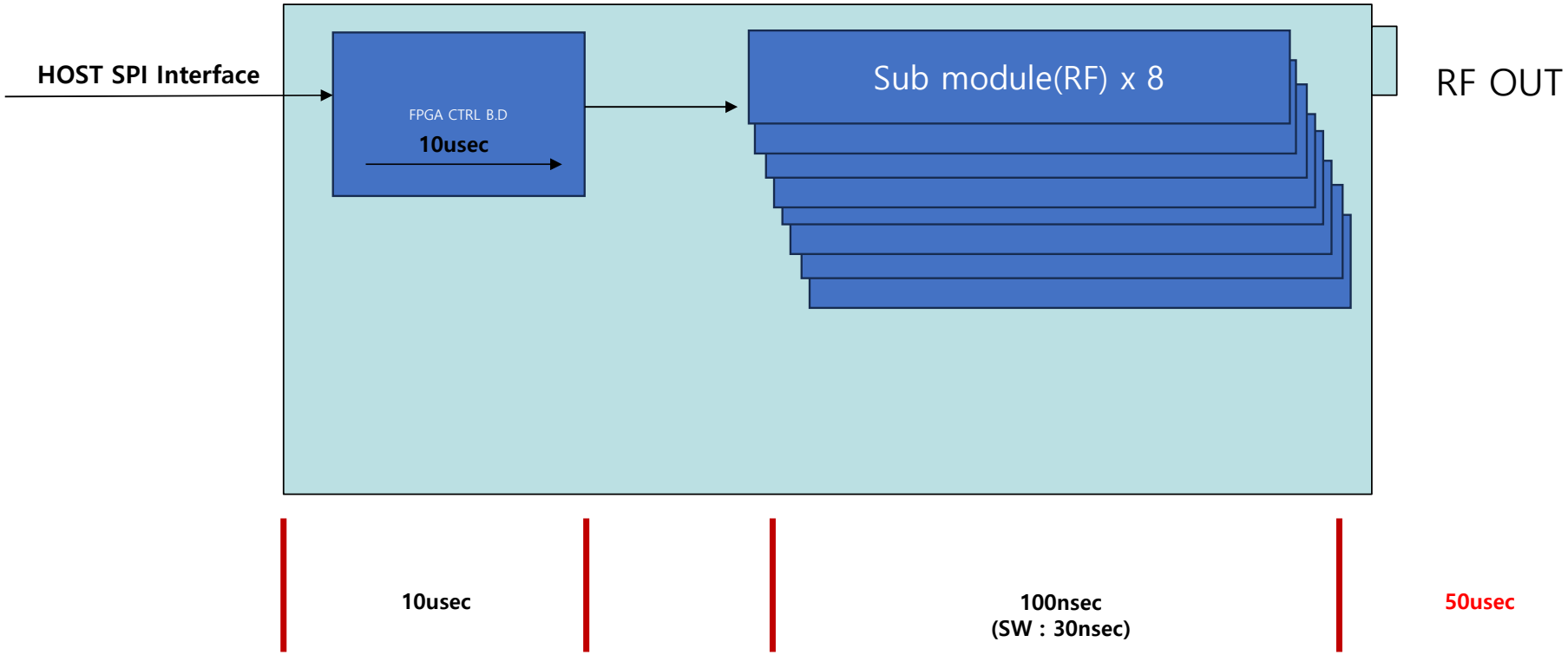


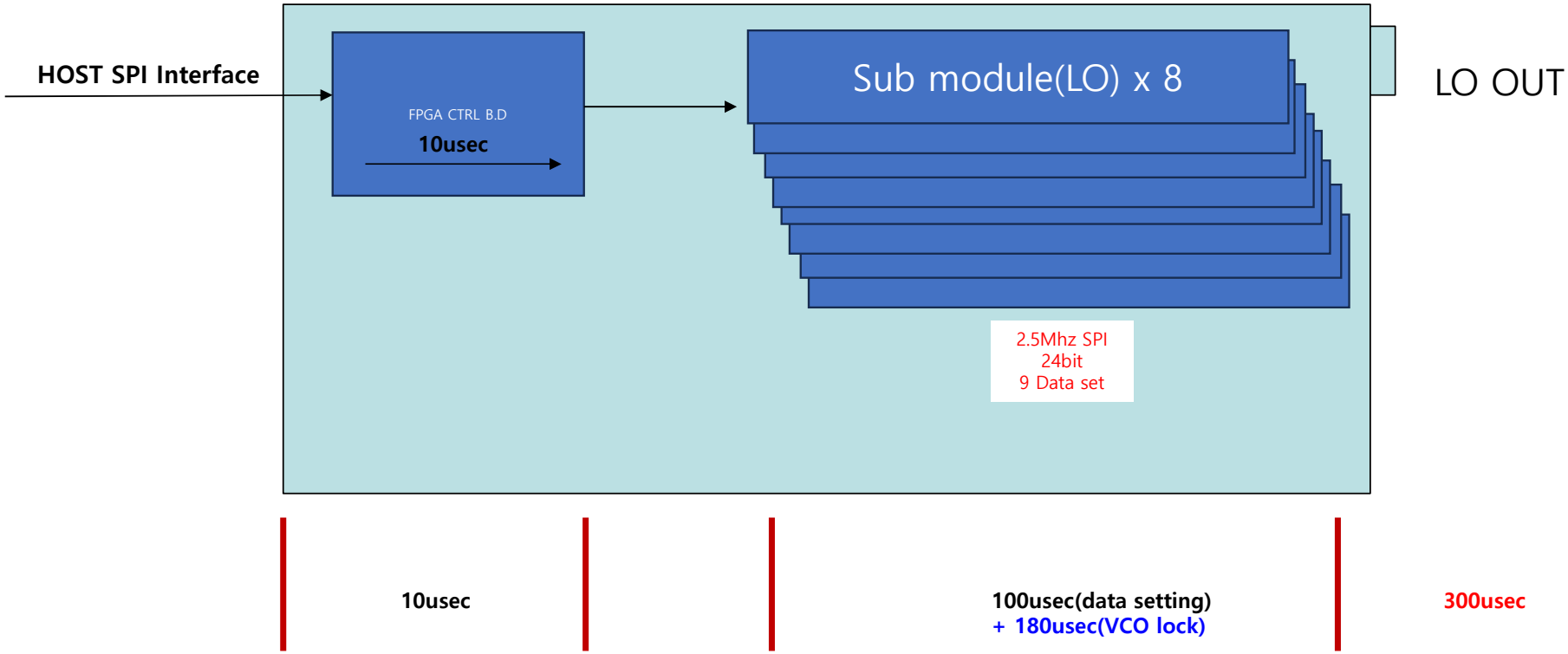
Figure 1: SPI write transaction

Figure 2: SPI read transaction

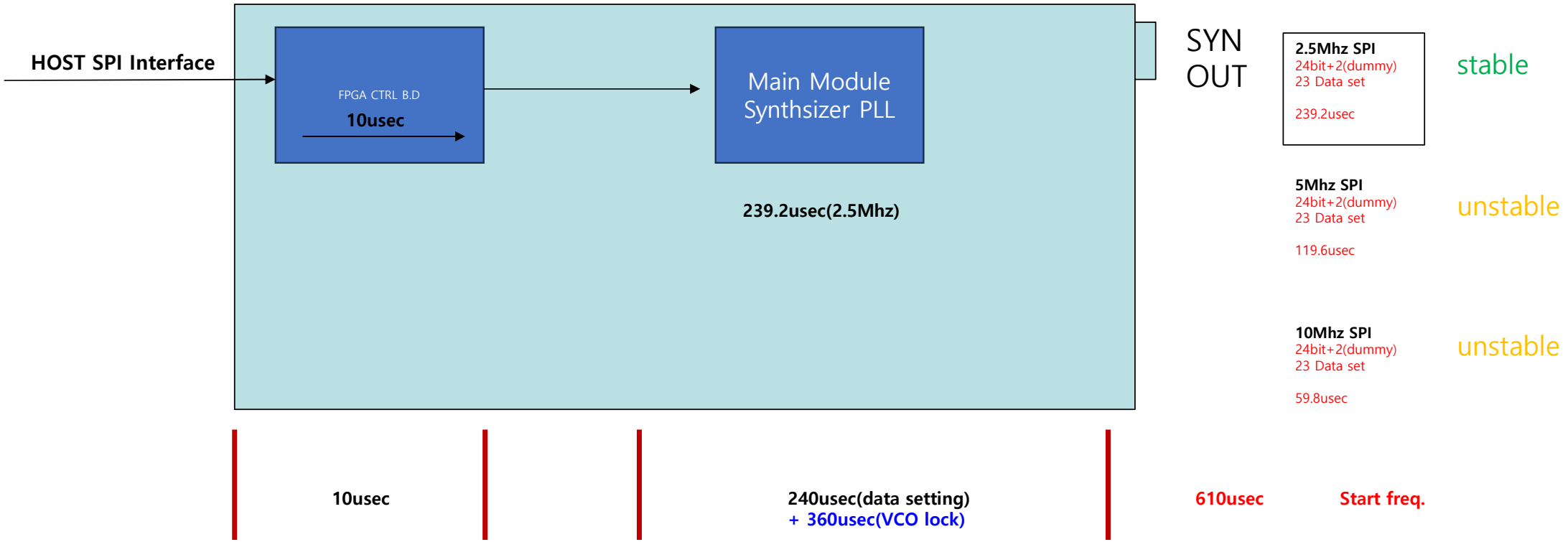
3.1 HOST to LO output Time



3.2 HOST to LO output Time



3.3 HOST to SYN(CAL) Time



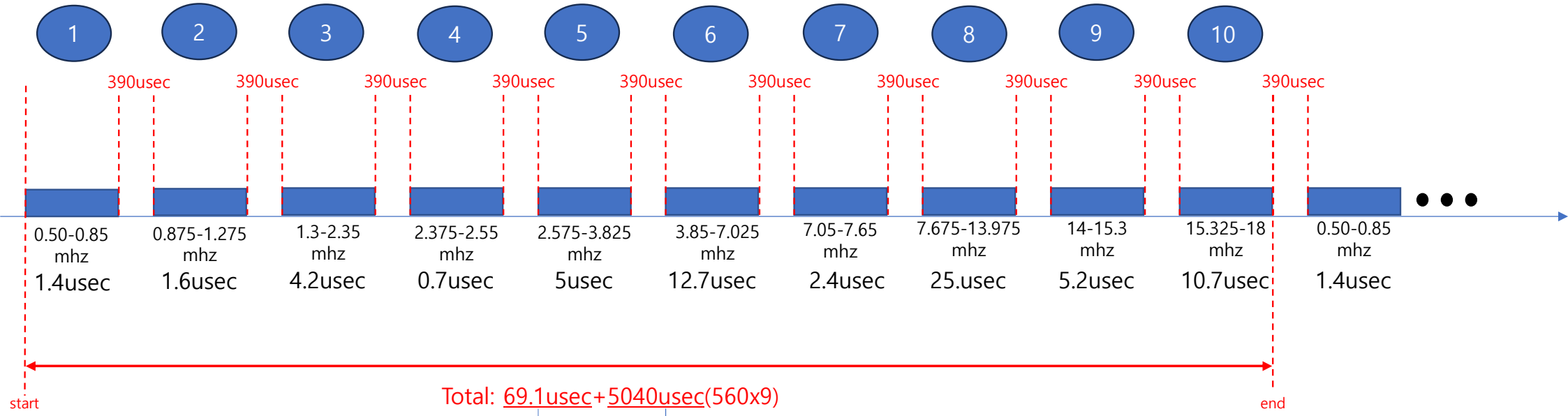
4.1 BIT SYNTHESIZER FREQ PLAN

In order to ramping using by LMX2595, frequency is needed to be changed.
(Freq: 0.5~18GHz, Step size: 25MHz)

BIT LO SYNTHESIZER FREQ PLAN										
No	PLL									RAMP
	START	END	R	Fpd	N Divider	Channel Divider	VCO	Fvco	RFoutA	RAMP0 Step Freq
1	500MHz	850MHz	5	25MHz	320	16	VCO	8000MHz	500MHz	400MHz
2	875MHz	1275MHz	5	25MHz	420	12	VCO	10500MHz	875MHz	300MHz
3	1300MHz	2350MHZ	5	25MHz	312	6	VCO	7800MHz	1300MHz	150MHz
4	2375MHz	2550MHz	5	25MHz	570	6	VCO	14250MHz	2375MHz	150MHz
5	2575MHz	3825MHz	5	25MHz	412	4	VCO	10300MHz	2575MHz	100MHz
6	3850MHz	7025MHz	5	25MHz	308	2	VCO	7700MHz	3850MHz	50MHz
7	7050MHz	7650MHz	5	25MHz	564	2	VCO	14100MHz	7050MHz	50MHz
8	7675MHz	14000MHz	5	25MHz	307	2	VCO	7675MHz	7675MHz	25MHz
9	14000MHz	15300MHz	5	25MHz	560	2	VCO	14000MHz	14000MHz	25MHz
10	15300MHz	18000MHz	10	12.5MHz	612	2	VCO Doubler	7650MHz	15300MHz	12.5MHz

4.2 HOST to SYN(CAL) Time

390usec is required for every single switching the frequency.

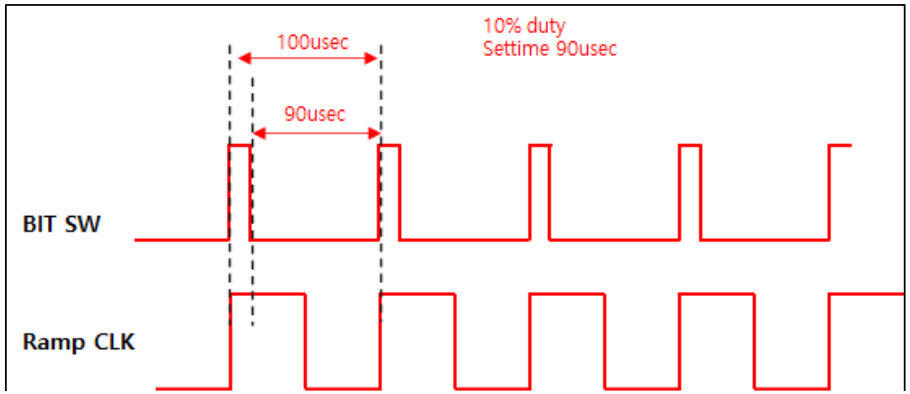


Total: 69.1usec+5040usec(560x9)

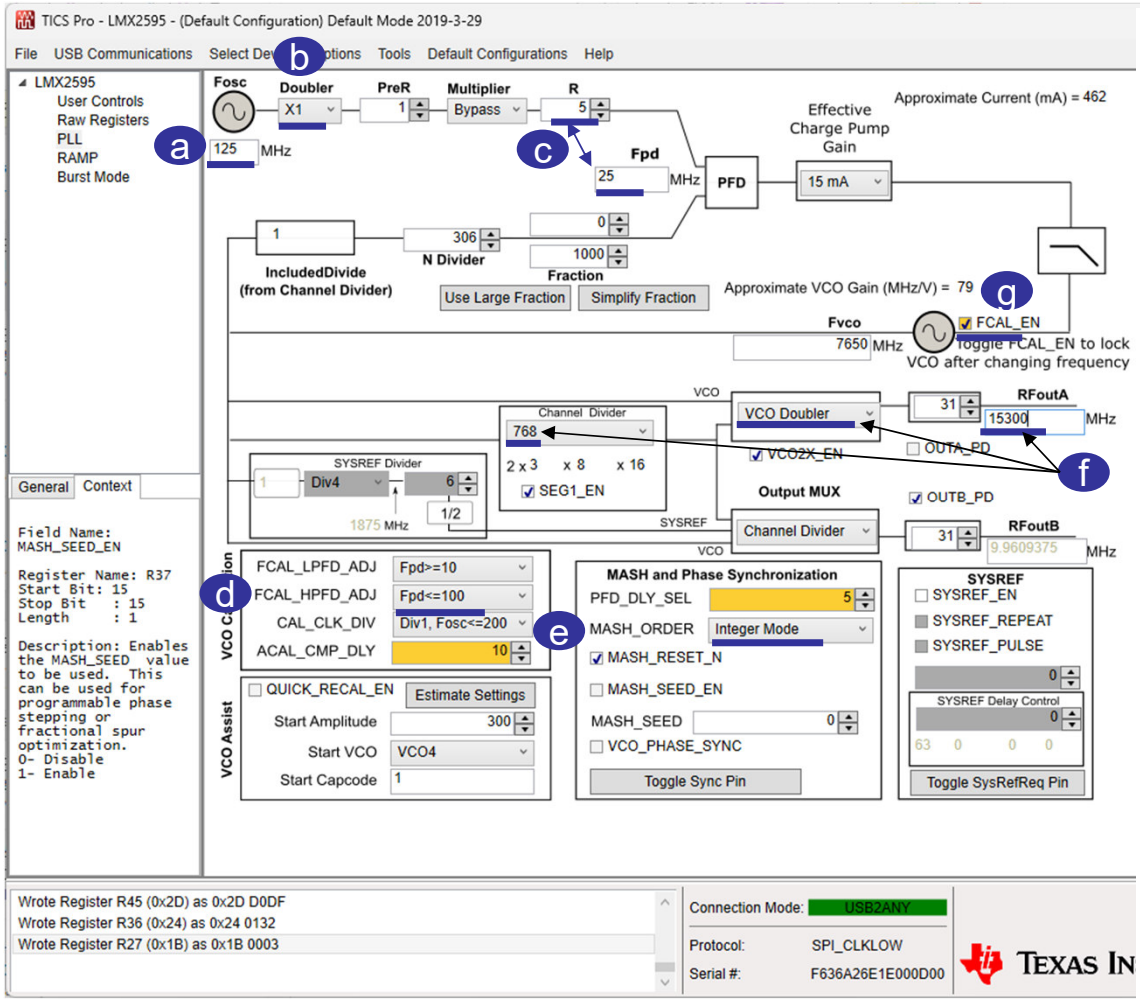
Ramping timing	Freq changing timing

ELTA's requirement Ramping timing: 70usec

BRN's requirement Ramping timing: 5109.1usec



5. LMX2595 SYNTHESIZER RAMPING SETTING(1)



<RAMPING PLL 세팅>

1. PLL REG Order

a. Fosc: 125MHz

```
Wrote Register R36 (0x24) as 0x24 0038
```

b. Doubler(OSCin doubler): x1

```
Wrote Register R9 (0x9) as 0x09 0604
Wrote Register R36 (0x24) as 0x24 0070
```

c. R: 5 ->[Fpd:25MHz]자동변경

```
Wrote Register R36 (0x24) as 0x24 0230
Wrote Register R11 (0xB) as 0x0B 0058
```

d. FCAL_HPFD_ADJ: Fpd<=100

```
Wrote Register R0 (0x0) as 0x00 241C
```

e. MASH_ORDER: Integer Mode

```
Wrote Register R44 (0x2C) as 0x2C 1FA0
```

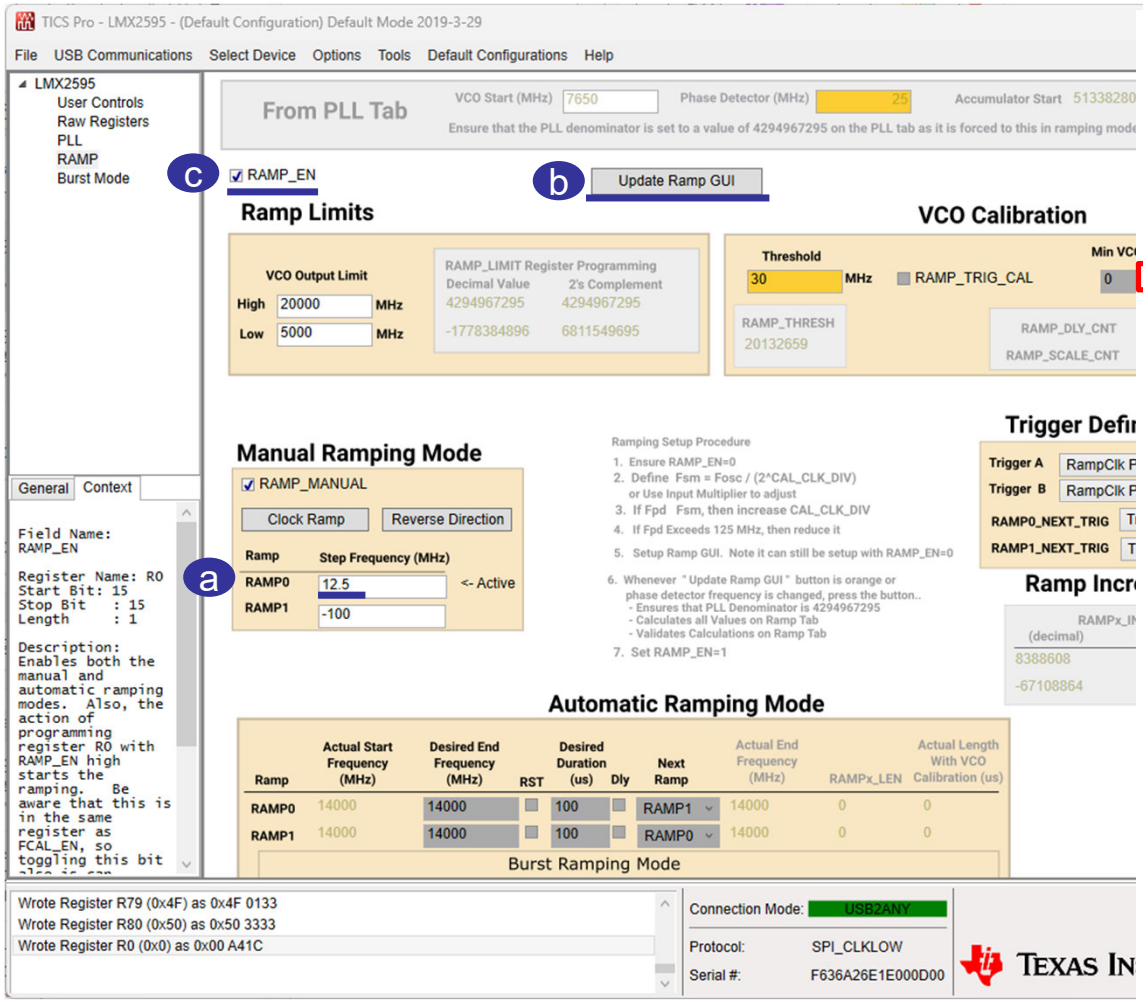
f. RFoutA: 15300MHz(VCO DOUBLER)

```
Wrote Register R45 (0x2D) as 0x2D D0DF
Wrote Register R36 (0x24) as 0x24 0132
Wrote Register R27 (0x1B) as 0x1B 0003
```

g. FCAL_EN

```
Wrote Register R0 (0x0) as 0x00 2414
Wrote Register R0 (0x0) as 0x00 241C
```

5. LMX2595 SYNTHESIZER RAMPING SETTING(2)



2. Manual Ramping Mode

a. RAMP0(Step Freq: 12.5MHz/ VCO Doubler)

```
Wrote Register R98 (0x62) as 0x62 0200
Wrote Register R102 (0x66) as 0x66 3C00
```

b. Update Ramp GUI

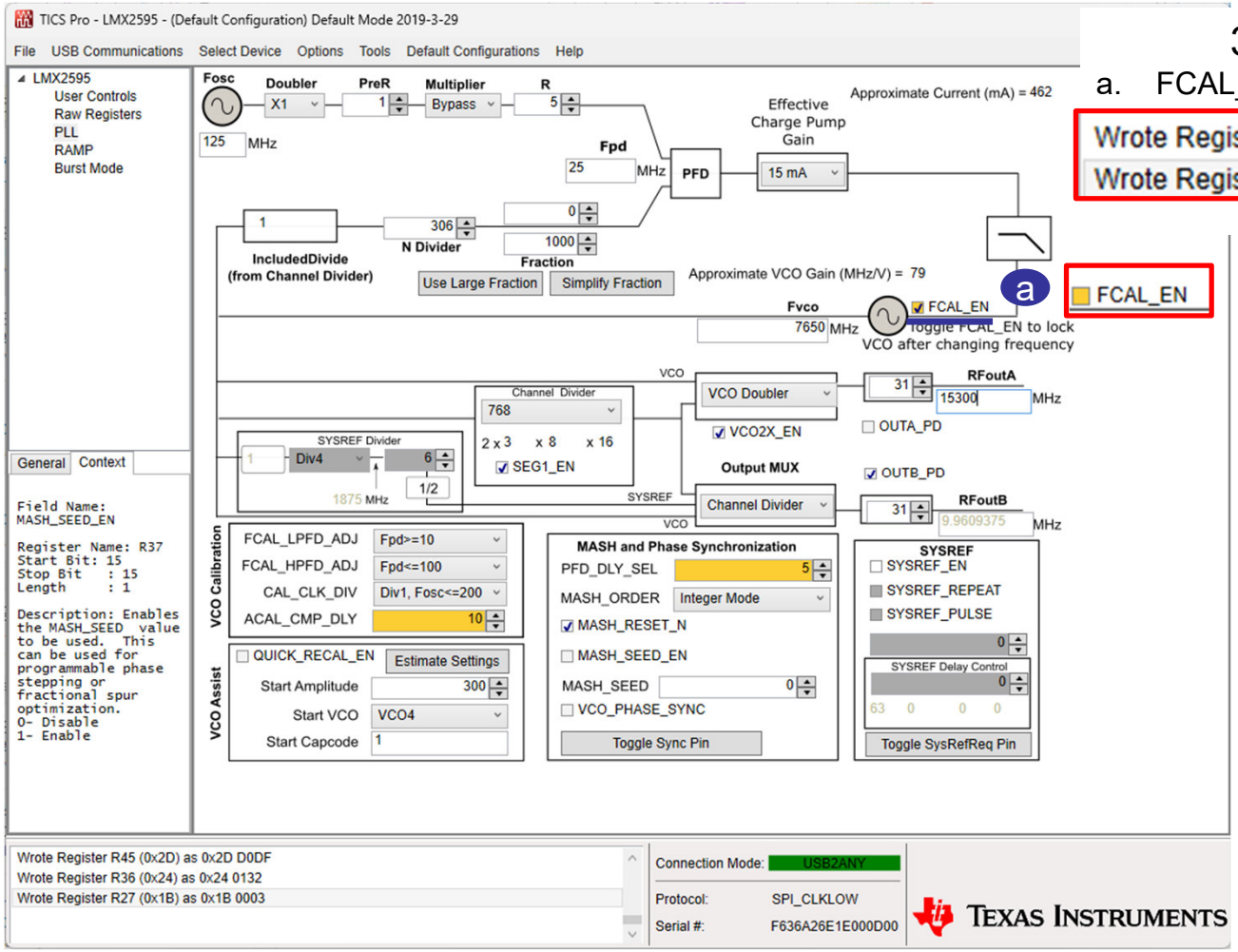
```
PLL_DEN must be 4294967295 in Ramping Mode.  Forcing this value on the PLL tab.
Wrote Register R38 (0x26) as 0x26 FFFF
Wrote Register R39 (0x27) as 0x27 FFFF
Wrote Register R82 (0x52) as 0x52 FFFF
Wrote Register R83 (0x53) as 0x53 FFFF
Wrote Register R84 (0x54) as 0x54 0001
Wrote Register R85 (0x55) as 0x55 95FF
Wrote Register R86 (0x56) as 0x56 FFFF
Wrote Register R106 (0x6A) as 0x6A 0001
Wrote Register R79 (0x4F) as 0x4F 0133
Wrote Register R80 (0x50) as 0x50 3333
```

c. RAMP_EN

```
Wrote Register R0 (0x0) as 0x00 A41C
```

<RAMPING 세팅>

5. LMX2595 SYNTHESIZER RAMPING SETTING(3)



3. FCAL_EN

a. FCAL_EN(해지 후 다시 체크)

Wrote Register R0 (0x0) as 0x00 A414
Wrote Register R0 (0x0) as 0x00 A41C

<RAMPING 세팅 후 FCAL_EN 재 설정>

6. BLOCK DIAGRAM FOR POWER SUPPLY FLOW