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# Scope

This document defines the SPI interface and protocol for configuring and controlling the **MOFC (Miniature Octal Frequency Converter)** device. The purpose of this document is to:

* Establish a clear communication protocol between the **MASTER** and **SLAVE** devices over SPI.
* Define the command structure for reading from and writing to configuration registers.
* Provide guidelines for the implementation of SPI-based control in the FPGA firmware.
* Detail the electrical and timing requirements for SPI communication.
* Outline the process of configuring and updating the RF module of the MOFC device.

This document serves as a reference for both the firmware development team implementing the SPI interface and the hardware design team ensuring compliance with the interface specifications

# Connector Definitions

## Connector TBD

## Digital ICD

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Name | Function | Type |
| SClk | SPI\_Clk | SPI Clock | LVTTL 3.3V Input |
| CSn | SPI\_CSn | Chip Select | LVTTL 3.3V Input |
| MOSI | SPI\_MOSI | Master Out, Slave In | LVTTL 3.3V Input |
| MISO | SPI\_MISO | Master In, Slave Out | LVTTL 3.3V Output |
| Reset | LVTTL 3.3V Input | System Reset | LVTTL 3.3V Input |
| RF\_RDY | RF\_READY | Indicates the tuner Rf is assigned and stable | LVTTL 3.3V output |
| GNDD | Digital Ground | Digital Ground | Digital Ground |

Table 1: Digital ICD

# Communication format

The MOFC controller acts as the “SLAVE” and the main controller acts as the “MASTER”. The MOFC controller uses a typical SPI interface. The SPI interface consists of four lines: SClk, CSn, MOSI, and MISO. The SPI interface uses 32-bit commands. All write commands transmitted to MOFC must be 32-bits long. Read commands contain the R/W bit set to 1 and the register address on MOSI while the returning data is clocked out on the MISO line during the data portion of the same 32-bit sequence.

## SPI Interface Specifications

The specified clock frequency for this application is 10MHz. Only the MASTER controller supplies the SPI 10MHz clock. The 10MHz clock is only supplied during SPI transactions.

### SPI write transaction

A typical Write transaction is shown below. The new command goes out on the MOSI line, and the data is registered by the SLAVE on each positive clock edge. The R/W bit is set to 0. The transaction is initiated when the MASTER pulls the CSn line low for a period of Tcs\_c before the first positive clock edge and held low for the remainder of the transaction. The MASTER then pulls the CSn line high Tc\_cs after the last negative clock edge. See timing constraints in the table below for minimum timing specifications.

A row of squares with numbers

Description automatically generated

Figure 1: SPI write transaction

### SPI Read transaction

A typical Read transaction is shown below. The Read transaction sequence starts out with the MASTER clocking out the R/W bit set to 1 and clocking out the address bits on each positive clock edge. The SLAVE then starts clocking out the read data on the next clock falling edge. The MASTER registers the 24 bits of data on the remaining 24 positive clock edges.

A diagram of a computer

Description automatically generated

Figure 2: SPI read transaction

### Timing constrains

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Description | Min | Max |
| SPI Clock Frequency | Maximum frequency of SPI Clock | 10 MHz |  |
| Tcs\_c | Time between CSn going low and the first positive clock edge | TBDns |  |
| Tc\_cs | Time between last negative clock edge and CSn going high | TBDns |  |

Table 2: Timing consrains

# SPI Command set

Table 3.0 contains a list of SPI commands/registers used to communicate with the MQFC. For details about each command, refer to the section 5, “Command Details”.

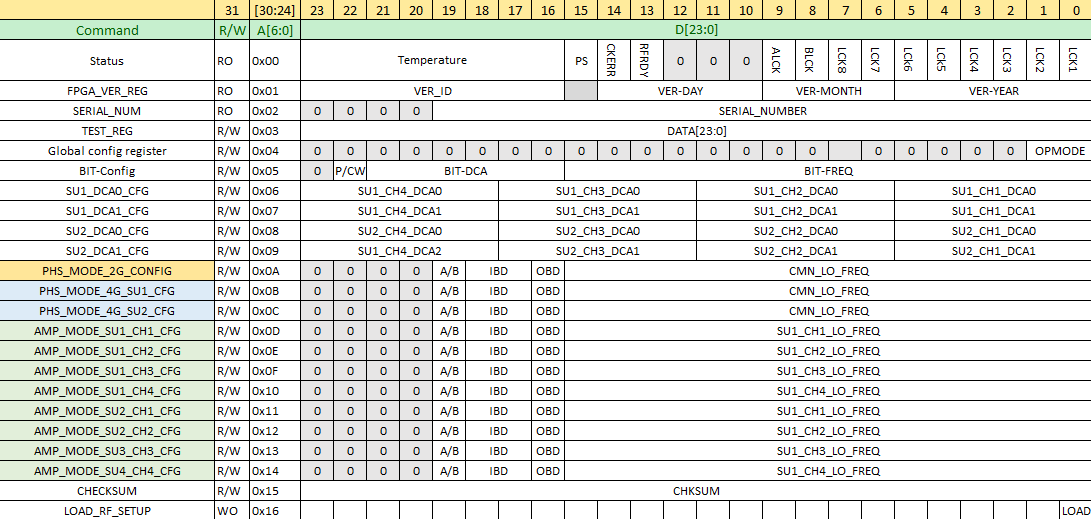


Table 3: SPI commands

Figure below clarify the fields of IBD,OBD,A/B,DCA0,DCA1 within the SPI command table



# Command details

## status

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x0 |
| Temperature | 23:16 | Module temperature is 2’s complement format | C9 = -55°C  …7D = 125°C |
| PS | 15 | Power status | 0-Fail  1-Pass |
| CKERR | 14 | CheckSum error, this bit will be updated when receiving command CHECKSUM, detail regarding how to verify the checksum | 0-CheckSum OK  1- CheckSum error |
| RFRDY | 13 | RF ready, is asserted low after receiving command ‘LOAD\_RF\_SETUP’, and only after complete setup of tuner is asserted High, the RFRDY out is also reflected at the output at PIN READY |  |
| RSVD | 12:11 | Unused bits | 0x0 |
| LO2\_LCK | 10 | LO2 pll lock | 0 – unlocked: 1-Locked |
| ALCK | 9 | Clock toward ADC lock | 0 – unlocked: 1-Locked |
| BLCK | 8 | Bit PLL lock | 0 – unlocked: 1-Locked |
| LCK2\_4 | 7 | Subunit 2 LO4 lock indication | 0 – unlocked: 1-Locked |
| LCK2\_3 | 6 | Subunit 2 LO3 lock indication | 0 – unlocked: 1-Locked |
| LCK2\_2 | 5 | Subunit 2 LO2 lock indication | 0 – unlocked: 1-Locked |
| LCK2\_1 | 4 | Subunit 2 LO1 lock indication | 0 – unlocked: 1-Locked |
| LCK1\_4 | 3 | Subunit 1 LO4 lock indication | 0 – unlocked: 1-Locked |
| LCK1\_3 | 2 | Subunit 1 LO3 lock indication | 0 – unlocked: 1-Locked |
| LCK1\_2 | 1 | Subunit 1 LO2 lock indication | 0 – unlocked: 1-Locked |
| LCK1\_1 | 0 | Subunit 1 LO1 lock indication | 0 – unlocked: 1-Locked |

## FPGA\_VER\_REG

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x1 |
| VER\_ID | 23:16 | Version ID represented by 2 hexa digits | 0x01 – 0xff |
| VER\_DAY | 14:10 | FPGA firmware date - day | 1 to 31 |
| VER\_MONTH | 9:6 | FPGA firmware date - year | 1-12 |
| VER\_YEAR | 5:0 | FPGA firmware date - year | 24-63 |

## SERIAL\_NUMBER

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x2 |
| rsvd | 23:20 | Unused bits | 0X0 |
| SER\_NUM | 19:0 | Module serail number | 0x00 – 0xfffff |

## TEST\_REG

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x3 |
| DATA | 23:0 | Register purpose is just for testing the complete 24 bits can be write/write by master in order to test basic communication | 0x00 – 0xffffff |

## Global config Reg

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x4 |
| RSVD | 19:0 | Unused bits | 23:2 |
| OPMODE | [1:0] | Operation mode | 0x0: 2G\_PHS\_MODE  0x1:4G\_PHS\_MODE 0x2:16G AMP MODE |

## Bit config Reg

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x5 |
| RSVD | 22 | Unused bit | 0x0 |
| P/CW | 22 | Select between Pulse or CW | 0 - BIT  1 - CW |
| BIT\_DCA | 21:16 | BIT Attenuation, each lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| BIT\_FREQ | 15:0 | Select BIT frequency, LSB unit [TBD] range [TBD] | TBD |

## SU1\_DCA0\_CFG

This register configure the first level DCA’s for the 4 channels for Subunit1

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 06 |
| SU1\_CH4\_DCA0 | 23:18 | Subunit1 DCA0 channel4 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH3\_DCA0 | 23:18 | Subunit1 DCA0 channel3 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH2\_DCA0 | 23:18 | Subunit1 DCA0 channel2 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH1\_DCA0 | 23:18 | Subunit1 DCA0 channel1 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |

## SU1\_DCA1\_CFG

This register configure the second level DCA’s for the 4 channels for Subunit1

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x7 |
| SU1\_CH4\_DCA1 | 23:18 | Subunit1 DCA1 channel4 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH3\_DCA1 | 23:18 | Subunit1 DCA1 channel3 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH2\_DCA1 | 23:18 | Subunit1 DCA1 channel2 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU1\_CH1\_DCA1 | 23:18 | Subunit1 DCA1 channel1 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |

## SU2\_DCA0\_CFG

This register configure the first level DCA’s for the 4 channels for Subunit2

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x8 |
| SU2\_CH4\_DCA0 | 23:18 | Subunit2 DCA0 channel4 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH3\_DCA0 | 23:18 | Subunit2 DCA0 channel3 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH2\_DCA0 | 23:18 | Subunit2 DCA0 channel2 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH1\_DCA0 | 23:18 | Subunit2 DCA0 channel1 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |

## SU2\_DCA1\_CFG

This register configure the second level DCA’s for the 4 channels for Subunit1

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x7 |
| SU2\_CH4\_DCA1 | 23:18 | Subunit1 DCA1 channel4 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH3\_DCA1 | 23:18 | Subunit1 DCA1 channel3 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH2\_DCA1 | 23:18 | Subunit1 DCA1 channel2 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |
| SU2\_CH1\_DCA1 | 23:18 | Subunit1 DCA1 channel1 Attenuation, lsb is 0.5[db] range is 0 to 31.5[db] | 0x0-0x3F |

## PHS\_MODE\_2G\_CONFIG

This register will be used to assign all 8 channels in case the ‘OPMODE’ filed in the GlobalConfigCommand = 0x0 (2G\_PHS\_MODE)

|  |  |  |  |
| --- | --- | --- | --- |
| Param | Bits | Description | Possible Values |
| R/W | 31 | Read / Write bit | Read only |
| Address | 30:24 | Register address bits | 0x8 |
| RSDV | 23:20 | Unused bits | 0x0 |
| A/B | 23:18 | Indicates channels input are from Ant of BIT | 0x0-0x3F |
| IBD | 17 | RF IN BANDS options are  2-6/6-18/0.5-4.75/0.5-2.4 | 0x0: 2-6  0x1: 6-18  0x10: Direct 0.5-4.75  0x11: Direct 0.5-2.4 |
| OBD | 16:15 | IF Out Band select options are  0.5-2.4 / 2.75-4.75 | 0-0.5-2.4  1: 2.75-4.75 |
| LO\_FREQ | 15:0 | LO1 frequency lsb is [TBD] range is [TBD} | [TBD} |

## PHS\_MODE\_4G\_SU<1/2>\_CFG

The registers PHS\_MODE\_4G\_SU1\_CONFIG and PHS\_MODE\_4G\_SU2\_CONFIG are used to configure all four channels of the Subunit (SU) when the OPMODE field in the GlobalConfigCommand register is set to 0x1 (indicating **4G\_PHS\_MODE**).

These registers inherit the same structure and fields as described for the configuration in section **5.11**.

## AMP\_MODE\_SU<1/2>\_CH<1/2/3/4>\_CFG

The eight registers, AMP\_MODE\_SU<1/2>\_CH<1/2/3/4>\_CFG, are used when the OPMODE field in the GlobalConfigCommand register is set to 0x2, indicating **16G\_AMP\_MODE**. These registers are used to configure the four channels of Subunit 1 (SU1) and the four channels of Subunit 2 (SU2) independently.

Each register corresponds to one channel within a specific subunit, allowing for independent configuration of all eight channels when operating in **16G\_AMP\_MODE**.

# Other Design requirements/specificatiosn

## SPI back to back transaction

## Maximum Slave processing time from receiving LOAD command to RF RDY