**Connector Definitions**

1.1 Connector TBD

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Name | Function | Type |
| SClk | SPI\_Clk | LVTTL 3.3V Input |  |
| CSn | SPI\_CSn | LVTTL 3.3V Input |  |
| MOSI | SPI\_MOSI | LVTTL 3.3V Input |  |
| MISO | SPI\_MISO | LVTTL 3.3V Output |  |
| Reset | LVTTL 3.3V Input |  |  |
| GNDD | Digital Ground | Digital Ground |  |

**2 Communication Format**

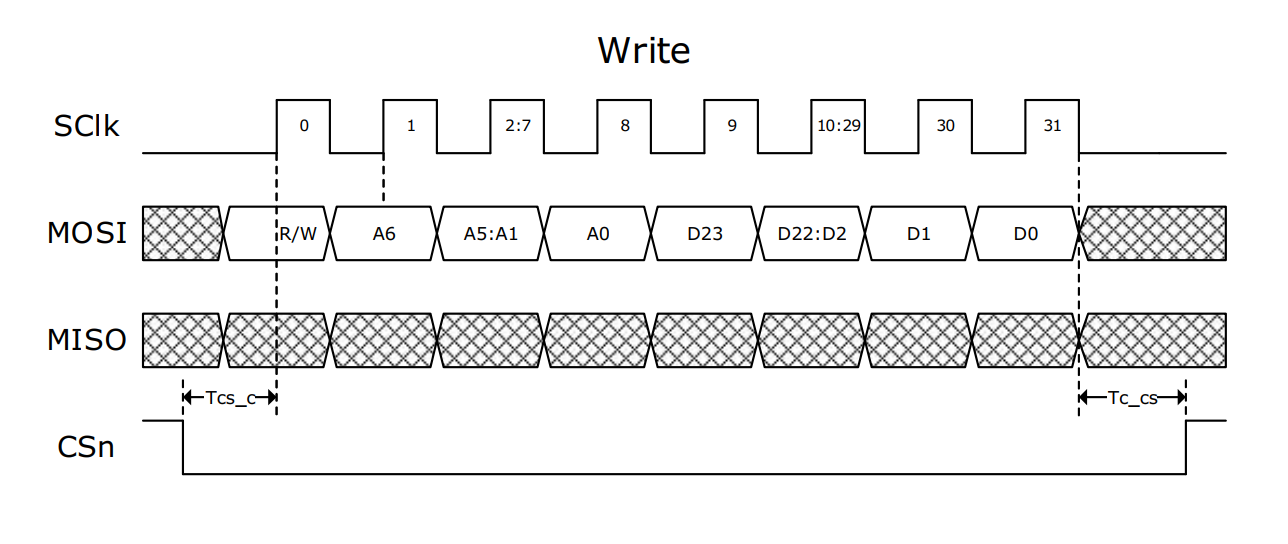
The MOFC controller acts as the “SLAVE” and the main controller acts as the “MASTER”. The MOFC controller uses a typical SPI interface. The SPI interface consists of four lines: SClk, CSn, MOSI, and MISO. The SPI interface uses 32-bit commands. All write commands transmitted to MOFC must be 32-bits long. Read commands contain the R/W bit set to 1 and the register address on MOSI while the returning data is clocked out on the MISO line during the data portion of the same 32-bit sequence.

2.1 SPI Interface Specifications

The specified clock frequency for this application is 10MHz. Only the MASTER controller supplies the SPI 10MHz clock. The 10MHz clock is only supplied during SPI transactions.

2.1.1 SPI Write Transaction

A typical Write transaction is shown below. The new command goes out on the MOSI line, and the data is registered by the SLAVE on each positive clock edge. The R/W bit is set to 0. The transaction is initiated when the MASTER pulls the CSn line low for a period of Tcs\_c before the first positive clock edge and held low for the remainder of the transaction. The MASTER then pulls the CSn line high Tc\_cs after the last negative clock edge. See timing constraints in the table below for minimum timing specifications.

SPI Read Transaction

A typical Read transaction is shown below. The Read transaction sequence starts out with the MASTER clocking out the R/W bit set to 1 and clocking out the address bits on each positive clock edge. The SLAVE then starts clocking out the read data on the next clock falling edge. The MASTER registers the 24 bits of data on the remaining 24 positive clock edges.

A diagram of a computer

Description automatically generated

Timing constraints

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Description** | **Min** | **Max** |
| SPI Clock Frequency | Maximum frequency of SPI Clock | 10 MHz |  |
| Tcs\_c | Time between CSn going low and the first positive clock edge | TBDns |  |
| Tc\_cs | Time between last negative clock edge and CSn going high | TBDns |  |