

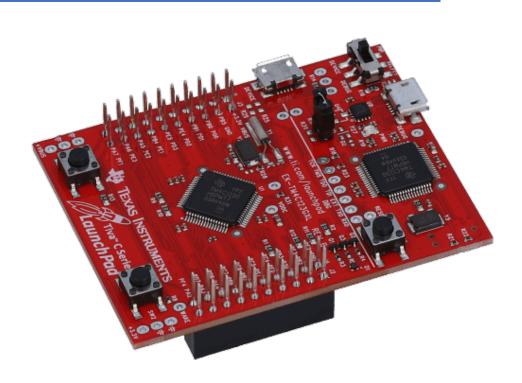
EE447- Introduction to Microprocessors Laboratory With Assembly Programming

(Preliminary Work 2)

EXPERIMENTAL WORK NO: 2

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Question 1) DELAY150 subroutine

In this part of the preliminary work, it is asked to write a subroutine that add 150msec delay when called. Below you can find the time pass of every different line

$$BL = 0.250 \, \mu sec$$
 $PUSH \{LR, RO\} = 0.250 \, \mu sec$
 $LDR \, R1 = \frac{0.250 \times 2}{3} \, \mu sec$
 $SUBS = \frac{0.250}{3} \, \mu sec$
 $BNE = 0.250 \, \mu sec$
 $BX \, LR = 0.250 \, \mu sec$
 $POP \{LR, RO\} = 0.250 \, \mu sec$

When we call the DELAY function from main part BL takes $0.250~\mu sec$ so ignore it. Then $PUSH~\{LR,RO\},LDR~R1,BX~LR,POP~\{LR,RO\}$ these four lines will be executed ones so we will subtract them from 150msec

$$150000\mu \sec{-\frac{0.250 \times 2}{3}\mu sec} - 0.750 \mu sec$$

In every loop we used 8 NOP and one SUBS these take $0.750~\mu sec$ and one BNE takes $0.250~\mu sec$ so in every loop we consume $1~\mu sec$ if we divide the remaining part with 1qsec then we require 149.999 times loop. One can see the consumed time in figure 1. Note that main part takes $250~\mu sec$ so ignore it from the result.

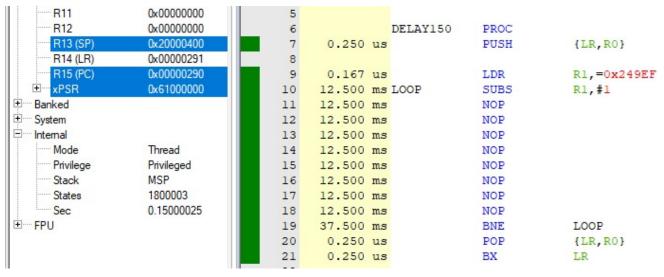


Figure 1: DELAY150 function result

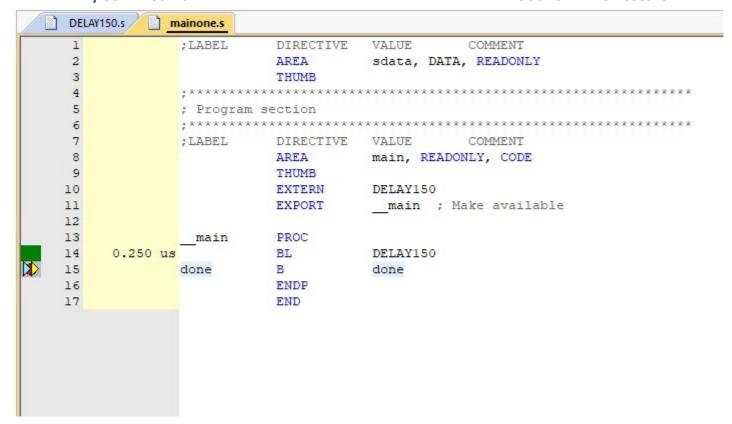


Figure 2: Main part of the question 1

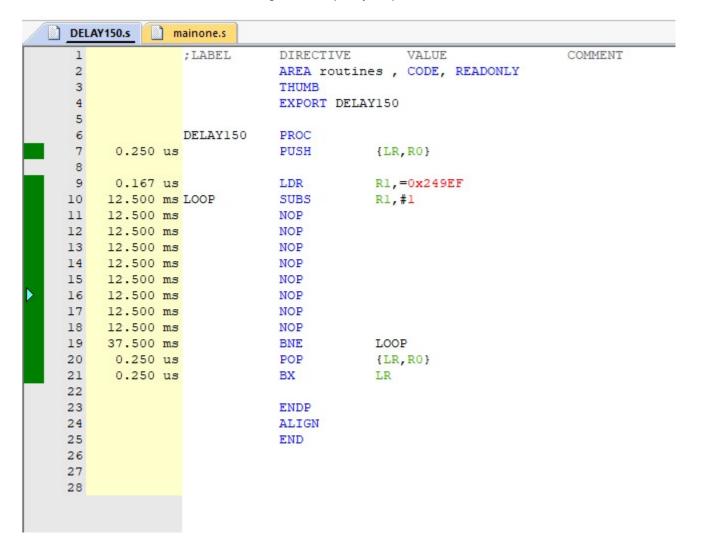


Figure 3: DELAY150 function codes

Question 2) Simple Input LED system

```
init portB.s
                       DELAY150.s
maintwo.s
4 ; EQU Directives
5; These directives do not allocate memory
6 : ************************
                 DIRECTIVE
                           VALUE
                                       COMMENT
8 PB INP
                 EQU
                           0x4000503C
                                        ; data register for inputs
9 PB OUT
                 EQU
                           0x400053C0
                                        ; data register for outputs
10 number
                 EQU
12; Program section
14 ; LABEL
           DIRECTIVE
                    VALUE
                                 COMMENT
15
                    main, READONLY, CODE
           AREA
16
           THUMB
17
           EXTERN
                    DELAY150
18
           EXTERN
                    init portB
19
           EXPORT
                     main
20
  main
           PROC
21
           BL
                    init portB
                                 ; initialize PORTB
22 loop
                    R9, #number
23
           MOV
                    RO, #PB OUT
24
           MOV32
25
                    R1, [R0]
           LDR
                    R1, R1
26
           MVN
                    R2, R1, #0xF0
27
           AND
                    R2, R2, #4
28
           LSR
29
           MVN
                    R3, R2
30
31
           MOV32
                    RO, #PB INP
32
                    R3, [R0]
           STR
33
           В
                    delay
34 delay
           CMP
                    R9,#0
35
           BEQ
                     loop
36
           SUB
                    R9, R9, #1
37
           BL
                    DELAY150
38
           BL
                    delay
39
40
           ENDP
```

Figure 4: Part two main

```
maintwo.s init_portB.s DELAY150.s
  2; EQU Directives
  3; These directives do not allocate memory
  5 : SYMBOL
                DIRECTIVE VALUE
                                      COMMENT
  6 SYSCTL_RCGC2 EQU
7 GPIO_PORTB_DIR EQU
                          0x400FE108
                           0x40005400
  8 GPIO_PORTB_AFSEL
                  EQU
                          0x40005420
  8 GPIO_PORTB_PUR EQU
                          0x40005510
                         0x4000551C
 10 GPIO PORTB DEN
 11
 13; Program section
 15; LABEL DIRECTIVE VALUE COMMI
16 AREA main, READONLY, CODE
                               COMMENT
 17
            THUMB
            EXPORT
                   init_portB
 19 init_portB PROC
 20
           PUSH
                    {R0, R1, LR}
 21
 22 ; Enable the clock signal
           LDR
                     RO, =SYSCTL RCGC2
 24
            LDR
                     R1, [R0]
 25
            ORR
                     R1,#0x12
 26
            STR
                    R1, [R0]
 27
            NOP
 28
            NOP
 29
            NOP
 30
 31:
                     RO,=GPIO_PORTB_DIR
            LDR
 32
 33
            LDR
                     R1, [R0]
 34
            BIC
                     R1, #0xF0
                                ; clear bit 7-4 for inputs
 35
            ORR
                     R1, #0x0F
                                ; clear bit 3-0 for outputs
 36
            STR
                     R1, [R0]
 37
```

Figure 5:Part two port initialization 1

```
maintwo.s init_portB.s DELAY150.s
 30
 31;
 32
              LDR
                        RO, =GPIO_PORTB_DIR
 33
              LDR
                        R1, [R0]
                        R1, #0xF0
R1, #0x0F
              BIC
                                     ; clear bit 7-4 for inputs
 34
 35
              ORR
                                     ; clear bit 3-0 for outputs
 36
              STR
                        R1, [R0]
 37
 38
             LDR
                        RO,=GPIO_PORTB_AFSEL
 39
              LDR
 40
                        R1, [R0]
              BIC
                        R1,#0xFF
 42
             STR
                        R1, [R0]
 43
 44; pull up resistors for the switches
                      R0,=GPIO_PORTB_PUR
R1,#0xF0
 45
             LDR
             MOV
 46
             STR
                       R1, [R0]
 48
 49
            LDR
                        RO,=GPIO_PORTB_DEN ; Enable digital
                        R1, [R0]
R1, #0xFF
 51
             LDR
 52
             ORR
             STR
                        R1,[R0]
 54
             POP
                        {RO, R1, LR}
 55
 57
            BX
 58
              ENDP
 60 ;******************
 DIRECTIVE VALUE
 63 ; LABEL
                                      COMMENT
              ALIGN
 64
 65
 66
```

Figure 6:Part two port initialization 2

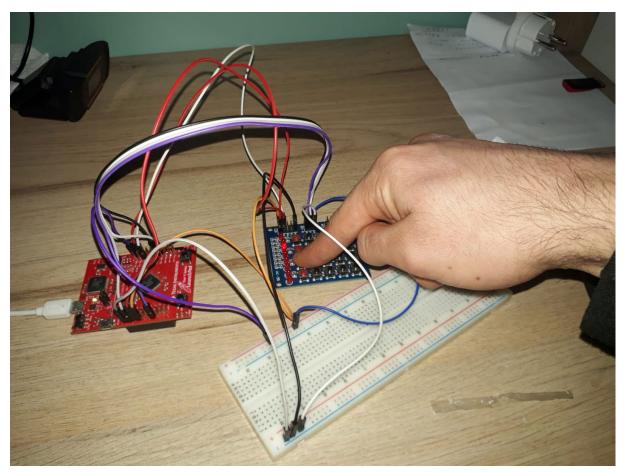


Figure 7: A sample photo that show system configuration

Question 3) 4*4 Keypad system

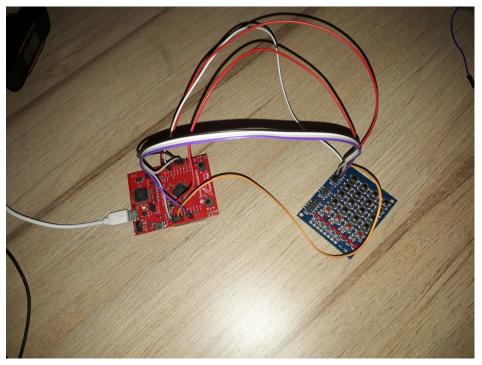


Figure 8: PART3-Circuit Connection Diagram

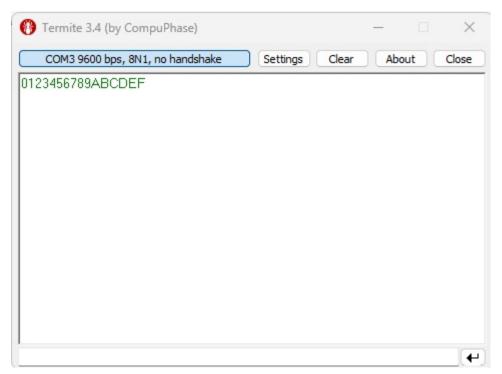


Figure 9: Termite Screen to show the results

```
mainthree.s init_portB.s DELAY150.s
    ;*******************
  2 ; mainthree.s
  4 ; EQU Directives
  5
    ; These directives do not allocate memory
     COMMENT
     ;SYMBOL
                   DIRECTIVE VALUE
                         0x4000503C ; data register for inputs
0x400053C0 ; data register for outputs
  8
     PB INP
                    EQU
                   EQU
    PB OUT
                         20
0xF0
                                          ; DELAY150 loop time
  10 number
                    EQU
  11 FO
                    EQU
                                          ; 1111_0000
                                          ; 0000_1111
  12 OF
                    EQU
                             OXOF
 13
    ;************************
 14
  15
    ; Program section
  ;LABEL DIRECTIVE VALUE COMM
AREA main, READONLY, CODE
 17
 18
  19
              THUMB
                      init_portB
DELAY150
 20
              EXTERN
             EXTERN
EXPORT
 21
 22
                        main
                       OutChar
 23
             EXTERN
 24
              PROC
                                 ;Initialize port B
 25
             BL
                       init portB
                       R5,#2
 26
              MOV
                                    ;2 for shift operations
                                   ;2 for shilt operation;
;short time delay for debouncing
 27
                       R10,#3
              MOV
                                   ; ARM input
                       R1, =PB_OUT
R2, =PB_INP
 28 start
              LDR
 29 press_check LDR
                                    ; KEYPAD input
              MOV
                       R6, #0
 30
                                    ;Initialization
  31
              STR
                        R6, [R2]
                                    ;R2=R6
                                   ;R0 = ARM input
  32
              LDR
                        RO, [R1]
  33
              AND
                        RO, #FO
 34
              CMP
                        RO, #FO
                                   ;Comparison
                        R3, R0
  35
              MOV
                                    ;R3:Temporary data
              BEQ
                       press check
 36
                        DELAY150
  37
              BL
              LDR
                        RO. [R1]
  38
```

Figure 10:Main_Part_Three_1

```
init_portB.s DELAY150.s
mainthree.s
                               DELAY150
  37
                  BL
                  LDR
  38
                               RO, [R1]
  39
                  AND
                               R0, #F0
  40
                  CMP
                               R0, #F0
  41
                  MOV
                                               ;R9:Temporary data
                               R9, R0
  42
                  BEQ
                               press_check
  43
                  CMP
                               R3, R9
                                               ; DEBOUNCING
  44
                  BEO
                               row_det
                                               ; DEBOUNCING
  45
                  BNE
                               press check
                                               : DEBOUNCING
                  MOV
  46
                               R4, #0xEF
     row_det
                                               ; Determinin the row
  47
  48
      shift
                  UDIV
                               R4, R5
                                               ;Divide R4 value with 2
                               R4, [R2]
  49
                  STR
  50
      Shortdelay
                  CMP
                               R10.#0
  51
                  NOP
  52
                   SUBS
                               R10,#1
  53
                  BNE
                               exit
                               Shortdelay
  54
  55
                  MOV
                               R10,#3
      exit
  56
                   LDR
                               RO, [R1]
  57
                  AND
                               R0, #F0
  58
                  CMP
                               R0, #F0
  59
                  MOV
                               R3, R0
  60
                  BEQ
                               shift
                                               ;According to button pressed or not
  61
                  В
                               go_to
  62
                  LSR
                               RO, #4
  63
      go_to
                                               ;Divide by sixteen
                               R0, R0
  64
                  MVN
                                               ;Take coloumn number
  65
                  AND
                               RO, #OF
  66
                  MVN
                               R4, R4
                                               ;Take row number
  67
                  AND
                               R4, #OF
                                               ;By using and reset 7-4 bits
  68
  69
      ; Check Corresponding Row Number
  70
                  MOV
                               R7, #0
                                               ;Row counter
  71
      row_n
                  UDIV
                               R0, R5
                                               ;Divide RO value with 2
  72
                  CMP
                               RO, #0x0
  73
                  BEQ
                               mov_column
  74
                                               :Number of the corresponding row
```

Figure 11:Main_Part_Three_2

```
init_portB.s DELAY150.s
mainthree.s
  73
74
75
                                     mov_column
R7, #1
                       BEQ
                       ADD
                                                         ; Number of the corresponding row
                                     row_n
R8, #0
                       BNE
                                                         ;Column counter
  77
78
        column_n
                       UDIV
                                      R4. R5
                                                         ;Divide R4 value with 2
                       CMP
  79
                                     Conc
R8, #1
                       BEO
                                                         ; Number of the corresponding column
                                     column n
  81
                       BNE
  82
                                     R9, #4
R7, R7, R9
R9, R8, R7
R9, #0x9
                       MOV
                                                         ; TO MULTIPLY ROW BY 4 --> BUTTON ID = ROW*4 + COLUMN
  83
        Conc
                      MUL
ADD
  85
                                                         ; Store value of the pressed button at R8
  86
                       CMP
                                     R0, R9, #0x30
R0, R9, #0x37
OutChar
                       ADDLS
  88
                       ADDHI
                       BL
  89
  90
91
                       LDR
                                     R2, =PB INP
                                                         ;Check if the pressed buton is released or not
        check r
                       MOV
                                     R6, #0x00
R6, [R2]
  93
                       STR
  94
                       BL
                                     DELAY150
  95
       checkerl
                       LDR
                                     R1, =PB_OUT
                                     R0, [R1]
R0, #F0
R0, #F0
  98
                       LDR
                       AND
  99
 100
                       CMP
 101
                       BNE
                                      check r
 102
                       BL
                                     DELAY150
 103
                       BEQ
                                     checker2
 104
                                      R1, =PB_OUT
 105
        checker2
                       LDR
                                     RO, [R1]
RO, #FO
RO, #FO
checker1
 106
                       LDR
 107
                       AND
 108
                       CMP
 109
                       BNE
 110
                       BT.
                                     DELAY150
 111
                                                         ;Turn to beginning
                                      start
 112
113
                       ENDP
 114
                       END
```

Figure 12:Main_Part_Three_3

Part - a)

Since just one row of switches provides data when it is pressed in the case of one-by-one enabling, it is possible to identify the pressed switch's row by examining the change in the input data register.

b)

> By checking energy level of the all input pins. If they are all have high voltage level then we can say that the pressed button is relased. However if there is one pin with low level voltage which means that the pressed button is not released.

c)

> By checking all rows and inputs we can understand which key is pressed. Just check their voltage level and search for low level one.

d)

➤ Debouncing can be avoided by apply some delay time after pressing or double checking the input pin

e)

f)