Design Guide: TIDA-010956

48V, 3.5kW Small Form-Factor Three-Phase Inverter Reference Design for Integrated Motor Drives

Description

This reference design demonstrates a three-phase inverter with nominal 48V DC input and 85A_{rms} output current rating. The 100V intelligent half-bridge gate driver DRV8162L enables a small size, robust and high efficiency power stage. Multichannel shutdown paths using the split power supply architecture of RV8162L are proposed for the Safe Torque Off (STO) function. With the internal V_{DS} monitor and protection feature of the DRV8162L, the power stage is protected against overcurrent failures of shoot-through or outputs short-circuit. Precision phase current sensing is achieved using the INA241A. The design offers a 3.3V I/O interface to connect a host controller like a C2000™ MCU for quick and easy evaluation.

Resources

TIDA-010956	Design Folder
DRV8162, INA241A	Product Folder
TMP6131, LMR38010	Product Folder
LAUNCHXL-F280039C	Tool Folder

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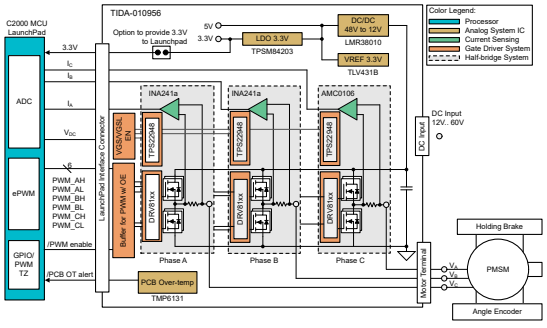
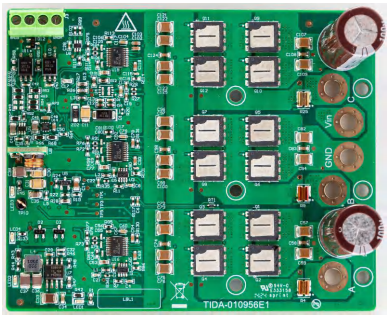
Features

- Three-phase inverter with 24V DC to 60V DC input and 85A_{RMS} continuous output current
- Smart half-bridge gate driver DRV8162L with on-chip hardware protection
- Fully-protected power stage: shoot-through, overcurrent, short circuit, undervoltage, overtemperature protections
- Programmable gate driver source and sink currents from 16mA, 32mA to 1A, 2A eases optimization of efficiency and EMI performance
- Configurable dead-time insertion to avoid shoot-through
- In-phase shunt (0.2mΩ) based current sensing with INA241A high-common mode rejection, zero-drift current-sense amplifier
- Multichannel shutdown paths to enable flexible system design of STO function

Applications

- Single and multiaxis servo drives
- Robotics
- AC inverter and VF drives
- Industrial and collaborative robot
- Mobile robot





1 System Description

Many low-voltage, three-phase inverters for DC-fed motor drives are powered by a 24V DC to 60V DC rail. When looking at robotics systems, the motors often have different power ratings, typically at 200W, 400W, 750W, 1.5kW, and 2.5kW, or even higher occasionally, depending on the functions to implement. These motors have different requirements on the current rating of the motor drives.

This design supports motors from 1.5kW to 4kW. For a 48V DC input motor drive system, the rated output current can be about $32A_{rms}$ to $85A_{rms}$; and in some occasions even reach up to around $100A_{rms}$.

In designing these power stages, high efficiency is a key point of the targets. With high efficiency, a small PCB size can be achieved, and the driver is able to fit into the shell of an integrated motor drive system, where the power stage can only use the motor shell as the heat sink for thermal dissipation.

To achieve a small PCB size in this design, the smart gate driver DRV8162L helps a lot with the integrated protection functions against the power stage shoot-through, overcurrent and short circuit. These important features were realized in the past using external circuity which adds to the PCB size.

To optimize system efficiency and EMI performance, without adding any external circuitry, the smart DRV8162L gate driver adds the ability to program the output source and sink current. A V_{GS} handshake with dead time insertion can be enabled to prevent shoot-through from happening.

To enable the drive to control the motor at the highest efficiency, an in-phase shunt-based current sensing is adopted using the INA241A, a high common-mode rejection, zero-drift featured current sense amplifier. Due to the high gain of the amplifier, a 0.2mΩ shunt is used; and the low resistance shunt selection also contributes to the high efficiency of the system.

Designing the system to be able to stop the motor safely and prevent any unexpected start-ups are critical requirements for robotics and factory automation applications. To assist these system level requirements and achieve the so-called Safe Torque Off (STO) function, this reference design proposes various combinations of shutdown paths for the gate drivers to prevent the motor from unexpected power up.

1.1 Reference Design Overview

This reference design implements a 48V three-phase inverter with smart half-bridge gate drivers for low-voltage servo motors. The design is fully tested at 48V.

The major building blocks of this reference design can be split into six different subsystems:

1. Three-phase power stage including gate drivers and FETs
2. Voltage and in-phase current sensing
3. Host processor interface
4. Diagnostic measurements
5. System power supply
6. Multilevel shutdown options of the gate driver

Figure 2-1 shows the TIDA-010956 block diagram. The host processor to control the motor is not part of this design.

The focus of this design is to test the three-phase power stage, focusing on the gate drivers and the FETs. Functional tests of the in-phase current sensing is also being done. The diagnostic measurements and the shutdown options are not yet fully tested in this design.

1.2 Key System Specifications

Table 1-1. TIDA-010956 Specifications

PARAMETER	VALUE (TYPICAL)	COMMENT
DC input voltage	24V to 60V	Absolute maximum 80VDC
Output phase current	±85A_{rms}	Continuous. A heat sink is possibly needed and airflow for the FETs is important
In-phase current sense range	±165A	Scaled to 0V to 3.3V range, inverted, with a 1.65V bias
In-phase current sense shunt	0.2mΩ	Differential, non-isolated amplifier INA241A3, with enhanced pulse-width modulation (PWM) rejection
PWM switching frequency	16kHz	Up to 40kHz
PWM dead time	User defined	Default 370ns with the hardware R_{DT} setting
Temperature range	–40°C to 85°C	Possibly need the proper heat sink and airflow for thermal dissipation of the FET
Protections	Short-circuit protection	With the default R_{VDSLVL} setting. See also Table 2-1
	Shoot-through protection	Automatic dead-time insertion handshake
	Temperature protection	Temperature sensor mounted on PCB to indicate overtemperature.
	UVLO	Integrated at 4.8V
PCB temperature sense range and accuracy	–40°C to 150°C	Using a TMP6131, ±1%, 10kΩ linear thermistor
Controller interface signals	3.3V I/O for PWM, I-V sensing, PWM buffer and gate driver enables, fault	TI BoosterPack™ compatible; supporting 3.3V signal levels. See pin assignments in Section 3.1.2.
Indicator LEDs	Power rails and user-defined	3.3V, 12V, V_{IN} input and one for user software control
PCB layer stack	Eight-layer, 70µm copper	2oz copper
Form Factor	80mm × 98mm	3150mil × 3860mil

2 System Overview

2.1 Block Diagram

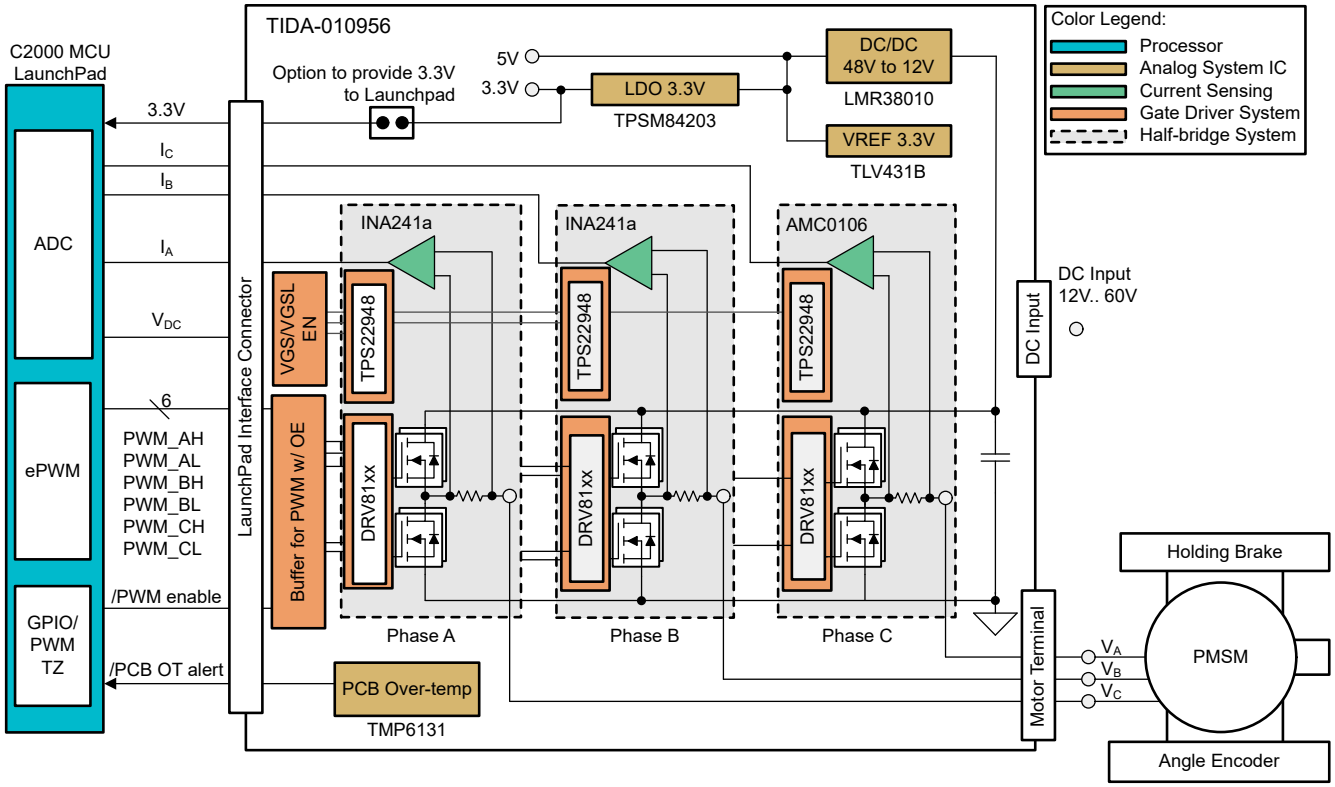


Figure 2-1. System Block Diagram of TIDA-010956

2.2 Design Considerations

2.2.1 Hardware Design

2.2.1.1 Power Stage Gate Driver

2.2.1.1.1 Gate Driver

The DRV8162L is used to drive two N-CH power MOSFETs in half-bridge configuration. The device supports 16-level gate drive peak currents up to 1A source and 2A sink. This reference design optimized the gate drive current for the best switching performance of the power stage

2.2.1.1.2 Protection Features

The overcurrent event of the power stage is detected with the DRV8162L by measuring the drain-source voltage drop V_{DS} of the FET. The overcurrent trip threshold of the DRV8162L can be set using strap resistors with 13-level threshold options. These values are found in *protection circuits* in the *electrical characteristics* section of the *DRV8162L* data sheet using the variable V_{DS_LVL}. The minimum is 100mV and the maximum is 2.0V.

With this feature, a blanking time is also adopted to make sure no overshoots are being detected during switching of the FETs.

For more information on the protection features, see *gate driver protective circuits* in the *DRV8162L* data sheet.

2.2.1.1.3 V_{GVDD} Definition

The DRV8162L has two power-supply pins (GVDD and GVDD_LS) for the high-side and low-side operations, respectively. The high-side power supply voltage V_{GVDD} can be between 5V to 20V, and the low-side power supply voltage V_{GVDD_LS} can be even lower, to a minimum of 3.5V. These values are found in the *electrical characteristics* section of the *DRV8162L* data sheet using the V_{GVDD} variable.

Typically, in this design, the V_{GVDD} and the V_{GVDD_LS} are set to 12V for the best performance of the FETs selected.

When picking the FETs, knowing the values of the V_{GS} and $R_{DS(ON)}$ is important. These parameters of the FETs have significant impacts on the efficiency of the overall system.

2.2.1.1.4 Strap Functions

When designing application circuits with the DRV8162L, the following parameters can be adjusted using strap resistors:

- Drive strength
- Dead time
- Control mode
- V_{DS} over-current threshold

2.2.1.2 Power Stage FETs

With the targeted power rating of this system, it is important to choose a FET which can meet the system needs. In this design, a choice of paralleling two FETs was made to meet the high current requirements.

2.2.1.2.1 V_{GS} versus $R_{DS(ON)}$

The selection of specific V_{GVDD} and V_{GVDD_SL} voltages can define the ON state V_{GS}, or the actual gate voltage high level of the FETs in an application.

This value can be used to find the $R_{DS(ON)}$ of the FET at the given voltage. The $R_{DS(ON)}$ is needed in defining the overcurrent trip level of the DRV8162L.

With these considerations, the calculation of the FET chosen is shown in Table 2-1. This design implements two parallel FETs to achieve low $R_{DS(ON)}$ and enable high-current output. The calculation was done using Ohms law.

Table 2-1. Overcurrent Trip Level of DRV8162 With Regards to FET NTMTSC1D6N10 V_{DS}

PARAMETER	NTMTSC1D6N10		2 × NTMTSC1D6N10	
I_D	267A		534A	
I_{DM}	900A		1800A	
Q_G	106nC		212nC	
Junction Temperature	25°C	125°C	25°C	125°C
$R_{DS(ON)}$ @ V_{GS} = 10V	1.42mΩ	2.50mΩ	0.71mΩ	0.88mΩ
TRIP LEVEL1-0: 0.15V	106A	60A	211A	120A
TRIP LEVEL1-1: 0.2V	141A	80A	282A	160A

In the case of fast switching FETs, an RC snubber network was chosen on each half bridge for a test and debug option to suppress ringing of the circuit, if needed. This step was not needed for our test cases.

2.2.1.3 Phase Current and Voltage Sensing

The ADC converter of the controller MCU selected for testing the system accepts a maximum input voltage of 3.3V. Therefore, it is imperative to scale the measured voltages into the 0V to 3.3V range.

2.2.1.3.1 Phase Current

The amplifier with a shunt for in-phase current sense needs to scale the full current-sense range into the 0V to 3.3V voltage range for the input of the ADC converter. In this design, the in-phase currents measured are bidirectional, so the voltage range calculated is further scaled by 2.

This design is specified to support a rated motor current of $85A_{rms}$ or $120A_{rms}$ at the peak. Allowing for some margin, the maximum current-sense range is set to 165A. With this specification, a 0.2mΩ, 8W shunt resistor and an amplifier with a gain of 50 was chosen for the design.

Using Equation 1, the voltage range of the output of the amplifier is shown.

$$V_{scale} = I_{ph} \times R_{shunt} \times G_{amp} \times 2 = 165A \times 0.2m\Omega \times 50 \times 2 = 3.3V \quad (1)$$

The voltage scale of 3.3V is chosen to fit the LaunchPad™ Development Kit used to test the design. When using other hardware, a voltage scale of 3.0V can be used.

With the scale set to 3.3V, set the voltage reference of the amplifier to make sure that 0A is the center point of the voltage scale.

Also important is to make sure that the power loss of the sense resistor can sustain the current of the system.

$$P_{loss} = I_{rms}^2 \times R_{shunt} = 165A^2 \times 0.2m\Omega = 5.445W \quad (2)$$

The 165A is only in case of a fault condition. Nominal current can be $85A_{rms}$, which can give a power loss of merely 1.445W. The 8W shunt resistor has enough margin.

2.2.1.3.2 Phase Current – Bias Voltage Reference

Since the design is built to scale at 3.3V, a LAUNCHXL-F280039C control board was used in testing the system, the following considerations were also accounted for:

- A voltage reference is chosen which can support both 3.0V and 3.3V reference voltages. This is done using the TLV431. Figure 2-2 shows the schematic.

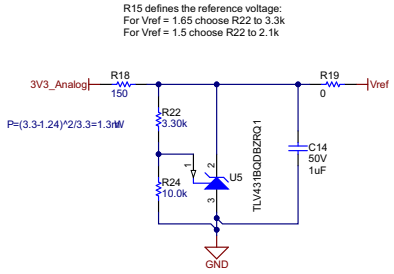


Figure 2-2. TLV431 Schematic From TIDA-010956

- Using this reference voltage circuit, the resistor R18 controls how much current is flowing into the circuit. This can affect the stable of the output voltage. Here, a 150Ω resistor is chosen.
- The next step is to pick the correct voltage divider; and this is done by choosing R15 and R18. R18 is fixed to 10.0kΩ here. Then, R15 can be chosen as 2.1kΩ for 1.5V, or 3.3kΩ for 1.65V for the bias reference of the INA241A.

2.2.1.3.3 Voltage

The DC input voltage (V_{IN}) and the three phase voltages of the motor are measured in this design. These voltages can be up to 80V maximum, limited by the buck converter LMR38101 which is used to generate the 12V voltage rail for the gate drivers.

In this design, the voltage sense dividers are set to support a maximum sense voltage of 75V, which is enough for the rated V_{IN} of 48V for the system.

Figure 2-3 shows a schematic view of a 75V phase-voltage measurement.

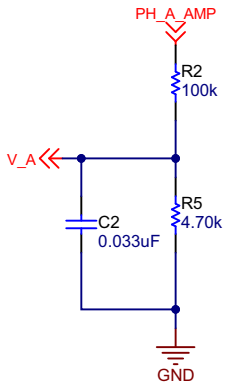


Figure 2-3. TIDA-010956 Phase-Voltage Sense Circuit

Equation 3 was used for the calculation.

$$R_5 = \frac{R_2 \times V_{out}}{V_{in} - V_{out}} = \frac{100k\Omega \times 3.3V}{75V - 3.3V} = 4,603\Omega \quad (3)$$

where

- R2 is chosen as 100kΩ

For the specific voltage divider, a low-pass filter is added and is done with C2.

For the motor phase voltages and the V_{IN} voltage measurements, the following values were entered into Equation 3: V_{IN} = 75V, V_{out} = 3.3V, R_2 = 100kΩ. This means R_5 = 4603Ω. Due to this, a 4700, 1% resistor was chosen.

2.2.1.4 Host Processor Interface

The processor interface was designed to work with a LAUNCHXL-F280039C through two headers of J1 and J2.

2.2.1.5 Gate Drive Shutdown Path

Due to the V_{GVDD} and V_{GVDD_LS} split-supply feature of the half-bridge gate driver DRV8162L, there is an option to shut down the high-side outputs and the low-side outputs of the gate drivers of the three phases with independent paths. An example circuit is implemented in this design.

There are two load switches (U12 and U14, TPS22810DRVR) built into the system for the V_{GVDD} and the V_{GVDD_LS} supplies, respectively. Inside the DRV8162L, the V_{GVDD_LS} is used to supply the low-side driver circuits and the V_{GVDD} is used to supply the high-side bootstrap circuit.

There is a third shutdown path built into the system with a specific load switch (U9, TPS22948DCKT) for the 3.3V power supply of the two PWM buffers and level translator chips (U13 and U15, TXU0304BQA). The output-enable (OE) pins of both devices can be configured to be fed with either an GPIO output of the system control MCU (J2-Pin18 of the host processor interface) or an external input signal through an opto-emulator isolator (U10 or U11, ISOM8710DFF).

2.2.1.6 System Diagnostic Measurements

2.2.1.6.1 Temperature Measurement

A temperature sensor (RT1, TMP6131DYAR) is used in this design to provide an option for the host controller to either simply turn off the three phases outputs or perform some comprehensive output control in case of the temperature of the PCB, sensed at a point just beside the C-phase low-side FET of Q3, is too high.

2.2.1.7 System Power Supply

As mentioned in previous chapters, the DRV8162L smart gate driver has two split power supplies for the high-side (V_{GVDD}) and the low-side (V_{GVDD_LS}), respectively. Both are fed with an intermediate supply rail of

12V, through the U12 or U14 load switches. So, the actual V_{GS} voltage applied to the power MOSFETs can be affected by the 12V supply rail.

2.2.1.7.1 12V Rail

To generate the 12V intermediate supply rail for the DRV8162L gate drivers of the three phases, a 4.2V to 80V input synchronous buck converter LMR38010 (U7) is used, and configured to run at 1MHz which is set by using R47 = 25.5kΩ.

The buck converter (U7) can provide a maximum output current of 1A. To make sure the system consumption is below this 1A power budget, a calculation is made for the loads.

Table 2-2. Current Budget of the Buck Converter at 12V

PART #	VOLTAGE RAIL	CURRENT CONSUMPTION BY DATA SHEET	WATT	CURRENT ON 12V WITH 80% EFFICIENCY
DRV8162L (Need 3 ×)	12V	18mA (V_{GVDD})	0.648W	67.5mA
F280039C	3.3V	108mA	0.356W	37mA
Total				**104.5mA**

This indicates that there is still an output current capacity of 895.5mA in the 12V rail left for additional circuitry to use.

2.2.1.7.2 3.3V Rail

In this design, the 3.3V rail needs to supply a load current of around 0.5A maximum for both the C2000 host control LaunchPad and the onboard components of system control circuits, including the sensing, diagnostic, and shut down control sections.

As for the input voltage range of the 3.3V rail power supply circuit, since the GVDD pin can accept a supply voltage of between 5V and 20V according to the *DRV8162L* data sheet, it is reasonable to make a design that can cover this full range, so that the 3.3V rail supply circuit can directly use the V_{GVDD} as the input.

The TPSM84203 has an input voltage range of 4.5V to 28V, and can provide up to 1.5A output current. This device comes with some fixed output voltage options to minimize external components and PCB size. A 3.3V output version is selected in this design.

The schematic example shown in the *typical application* section of the *TPSM84203* data sheet, shows how to build a 3.3V voltage rail. One input capacitor and two output capacitors are needed as external components. For these capacitors, X5R or X7R ceramic capacitors are recommend. The *input capacitors* section of the *TPSM84203* data sheet shows example choices.

2.2.2 Software Design

The software used to test this reference design was modified from the `servo_drive_with_can` example project in C2000Ware_MotorControl_SDK. The example project was tuned to work with the TIDA-010956 hardware following instructions in the related documentation which is found in the installation folder.

First, modify the analog and digital I/O port settings. Make sure the PWM signals from the C2000™ MCU are configured correctly for the high-side and low-side FETs. Make sure the control outputs, the fault feedback inputs and the ADC channels are all configured correctly for the LaunchPad I/O ports used.

Secondly, tune the related parameters and codes for the reference design hardware and system control. The reference design was tested using build level 2, which means the system is run in an open loop configuration.

Download the `servo_drive_with_can` example code from *C2000Ware_MotorControl_SDK*.
Install the SDK using the default settings, then locate the example code at:
`c:\ti\c2000\C2000Ware_MotorControl_SDK_5_01_00_00\solutions\servo_drive_with_can`.
The documentation is also found in the `doc` folder in this path.

For questions on the software or C2000Ware_MotorControl_SDK, see also the C2000 microcontrollers forum E2E design support forum.

2.3 Highlighted Products

2.3.1 DRV8162L

The DRV816x devices are integrated half-bridge gate drivers capable of driving high-side and low-side N-channel power FETs. The device generates the gate drive voltages from the GVDD supply pin and uses a bootstrap circuit to drive the high-side FET. A trickle charge pump supports 100% duty cycle operation. The gate drive architecture supports peak gate drive currents up to 1A source and 2A sink. These devices can be used to drive various types of loads including brushless or brushed DC motors, PMSM, stepper motors, switched reluctance motors (SRM), and solenoids.

The 1-pin PWM, 2-pin PWM, and independent FET PWM modes allow for simple interfacing to controller circuits and flexible FET power stage configurations. The hardware pins help configure device settings including current sense amplifier gain, gate drive current, and VDS overcurrent protection. The DRV8161 device integrates a low-side current sense amplifier to provide current measurement information back to the controller. The DRV8162L variant offers separate GVDD and GVDD_LS pins to help system design of safe torque off (STO) function.

Internal protection functions are provided for under-voltage lockout, FET over-current, and over-temperature. The nFAULT pin indicates fault events detected by the protection features.

2.3.2 INA241A

The INA241x is an ultra-precise, bidirectional current sense amplifier than can measure voltage drops across shunt resistors over a wide common-mode range from –5V to 110V, independent of the supply voltage. The high-precision current measurement is achieved through a combination of low offset voltage (±10µV, maximum), small gain error (±0.01%, maximum) and a high DC CMRR (typical 166dB). The INA241x is designed for high-voltage, bidirectional measurements in switching systems that see large common-mode voltage transients at the device inputs. The enhanced PWM rejection circuitry inside the INA241x maintains minimal signal disturbance at the output due to the common-mode voltage transitions at the input.

The INA241x operates from a single 2.7V to 20V supply, drawing 2.5mA of supply current. The INA241x is available in five gain options: 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V. Multiple gain options allow for optimization between available shunt resistor values and wide output dynamic range requirements.

The INA241x is specified over operating temperature range of −40°C to +125°C.

2.3.3 LMR38010

The LMR38010 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. The LMR38010 operates during input voltage dips as low as 4.2V, at nearly 100% duty cycle if needed, making the device an excellent choice for wide input industrial applications and MHEV or EV systems.

The LMR38010 uses precision enable to provide flexibility by enabling a direct connection to the wide input voltage or precise control over device start-up and shutdown. The power-good flag, with built-in filtering and delay, offers a true indication of system status, eliminating the need for an external supervisor. The device incorporates pseudo random spread spectrum for minimal EMI and switching frequency and can be configured between 200kHz and 2.2MHz to avoid noise sensitive frequency bands. In addition, the frequency can be selected for improved efficiency at low operating frequency or smaller design size at high operating frequency.

The device has built-in protection features such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LMR38010 is available in an 8-pin HSOIC PowerPAD integrated circuit package.

2.3.4 TMP6131

The TMP61 linear thermistor offers linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. The low power consumption and a small thermal mass of the device minimize self-heating.

With built-in fail-safe behaviors at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times.

Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory.

The TMP61 is currently available in a 0402 X1SON package, a 0603 SOT-5X3 package, and a 2-pin through-hole TO-92S package.

3 Hardware, Software Test Requirements and Test Results

3.1 Hardware Requirements

3.1.1 PCB Overview

Figure 3-1 shows a photo of the top side of the TIDA-010956 PCB with the LAUNCHXL-F280039C.

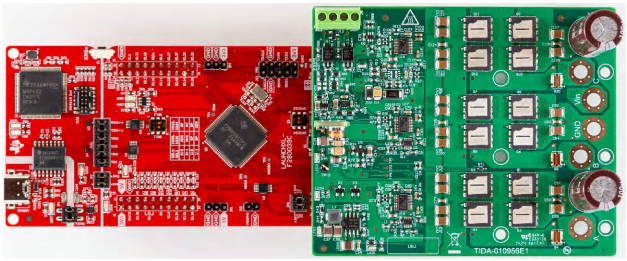


Figure 3-1. Board Picture (Top View)

3.1.2 Hardware Configuration

3.1.2.1 Prerequisites

The following hardware equipment and software are required for the evaluation tests of the TIDA-010956 design guide.

Table 3-1. Prerequisites

EQUIPMENT	COMMENT
TIDA-010956	Available from the *Design Folder*
TMS320F280039C LaunchPad™ development kit for C2000™ real-time MCU	Available from *LAUNCHXL-F280039C*
Code Composer Studio™ integrated development environment (IDE) version 12	Download from *CCSTUDIO*
C2000Ware_MotorControl_SDK	Download from *C2000WARE-MOTORCONTROL-SDK*.
Motor	Needs to support voltage and current level of the design
Power supply	Needs to support voltage and current level of the design

3.1.2.2 Default Resistor and Jumper Configuration

Prior to working with the TIDA-010956 board, make sure that the correct resistor settings are applied. Table 3-2 shows the default resistor settings. As for the jumpers on the LAUNCHXL-F280039C, remove the JP1 to disconnect the 5V power supply from the PC USB port; since this reference has supplied the MCU controller board with a 3.3V power rail directly by the default setting of R29..

Table 3-2. Default Resistor and Jumper Settings

HEADER and RESISTOR	JUMPER SETTING
R51 and R58	Resistor to disable the isolator for the external shutdown input signal
R54 and R56	Resistor defining which shutdown path drives the load switch for PWM disable function
R61 and R63	Resistor defining which shutdown path can drive the load switch for high-side gate driver disable function
R67 and R69	Resistor defining which shutdown path can drive the load switch for low-side gate driver disable function
R29	0Ω resistor to supply the LAUNCHXL-F280039C with the 3.3V onboard. Remove JP1 on the LaunchPad before use.
R83, R86; R98, R101; R111, R114	Resistors to configure the gate drive current of the DRV8162L in the three phases. *The default setting is LEVEL0 for both IDRIVE1 and IDRIVE2.*
R84, R99, R112	Resistors to configure the V_{DS} monitor threshold level of DRV8162L. *The default setting is LEVEL1.*
R85, R100, R113	Resistor outside the DT/MODE pin to set the dead time. *The default setting is LEVEL3.*

3.1.2.3 Connector

3.1.2.3.1 Host Processor Interface

Table 3-3 shows the signals the TIDA-010956 reference design uses to communicate with the C2000 LaunchPad.

Table 3-3. Pinout of J1 and J2 Host Processor Interface

LAUNCHXL-F280039C				TIDA-010956			
J5	**J7**	**J8**	**J6**	**J1**		**J2**	
3.3V	5V(2)	PWM7A	GND	3.3V	NC(2)	PWM_CH	GND
ADCINC1(2)	GND	PWM7B	GPIO27(2)	NC(2)	GND	PWM_CL	NC(2)
GPIO15	ADCINB11	PWM4A	GPIO47	LED4	*Vbus* (1)	PWM_BH	FAULT
GPIO56(2)	ADCINA10, ADCINB1, ADCINC10	PWM4B	GPIO57(2)	NC(2)	*V_C* (1)	PWM_BL	NC(2)
GPIO56(2)	ADCINA5	PWM5A	XRSn(2)	NC(2)	*V_B* (1)	PWM_AH	NC(2)
ADCINA9(2)	ADCINA4, ADCINB8	PWM5B	SD2_D3(2)	NC(2)	*V_A* (1)	PWM_AL	*DAT_PhC* (1)
GPIO58(2)	ADCINB4, ADCINC8(2)	GPIO21(2)	SD2_C3(2)	NC(2)	NC(2)	NC(2)	*SD_CLK* (1)
GPIO4	ADCINB5	EPWM1B(2)	GPIO20	VDSLVLCC	*I_B* (1)	*SD_CLK* (1)	EN_DRV
GPIO18	ADCINA12, ADCINC5	EPWM2A(2)	GPIO26	VDSLVLCB	*I_A* (1)	*CLK_PhC* (1)	PWM_EN
GPIO19	ADCINA0, ADCINB15, ADCINC15	GPIO40(2)	GPIO25(2)	VDSLVLCA	*Temperature* (1)	NC(2)	NC(2)

(1) The signals shown in italic font are not tested in this design yet.
(2) The gray color code shows the pins which are *Not Connected* or are reserved in the TIDA-010956 design.

3.2 Test Setup

The equipment listed in Table 3-4 was used for the TIDA-010956 testing session.

Table 3-4. DRV8162L Settings

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix DPO3054
Probes	Tektronix TPP0200
Current probe	CYBERTEK CP8500A
PMSM Motor	GLOBE6440
Power supply	Agilent 6030A, ITECH IT6724H

For the different tests some of the equipment was used as described in Table 3-4. A test setup used for the system is shown in Figure 3-2.

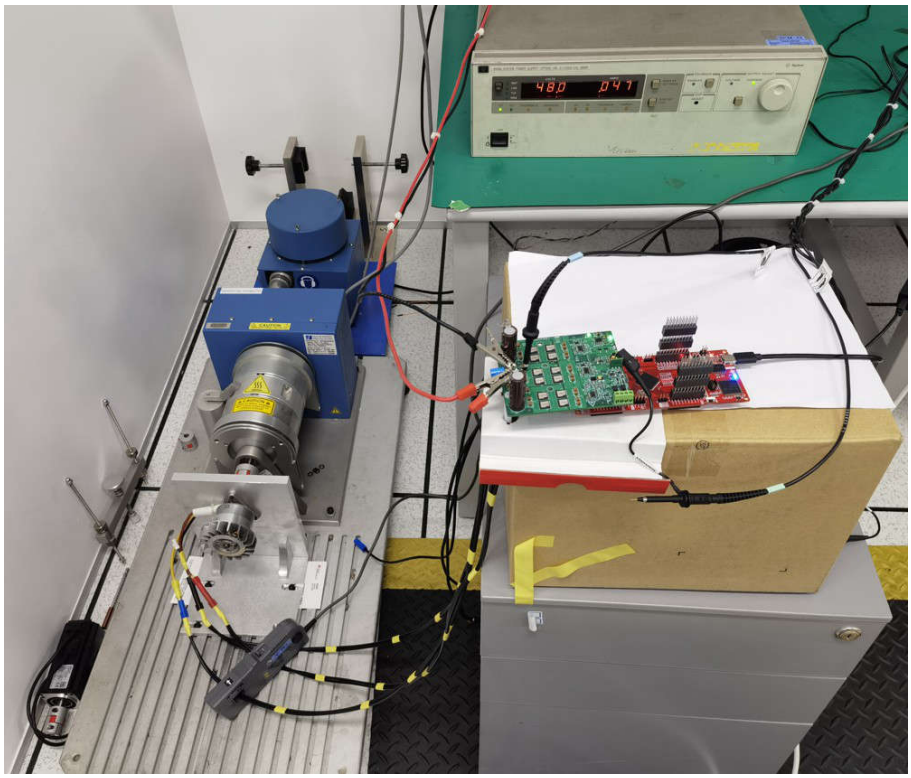


Figure 3-2. TIDA-010956 System Test Setup

The DRV8162L chips were setup in a way shown in Table 3-5 during the tests, if not otherwise specified.

Table 3-5. DRV8162L Settings

IDRIVEP	1024mA	IDRIVE1 = LEVEL0 ($V_{IDRIVE1}$ = 0kΩ) and IDRIVE2 = LEVEL0 ($V_{IDRIVE2}$ = 0kΩ)
IDRIVEN	2048mA	
VDSLVL	LEVEL1-0: 0.15V or LEVEL1-1: 0.2V	LEVEL1 (R_{VDSLVL} = 2kΩ)
DEAD_TIME	370ns dead time	LEVEL3 (R_{DT} = 3.3kΩ)

In the tests, a C2000™ LaunchPad of LAUNCHXL-F280039C was used to control the system. The related MCU software settings are shown in Table 3-6.

Table 3-6. C2000 MCU Settings

PWM	16kHz	Dead time	200ns

Different setups were used in the tests and are described in the related test section.

3.3 Test Results

Tests were done to characterize each individual functional block, as well as the entire board. In particular, the following tests were conducted:

- Power management
- Three-phase power stage tests
- Voltage and Current Sensing Tests
- System thermal performance

Tests were done at room temperature around 28 degrees Celsius.

3.3.1 Power Management

This section shows the power up and power down sequence of the TIDA-010956. The measurements were done in the process shown in Figure 3-3.

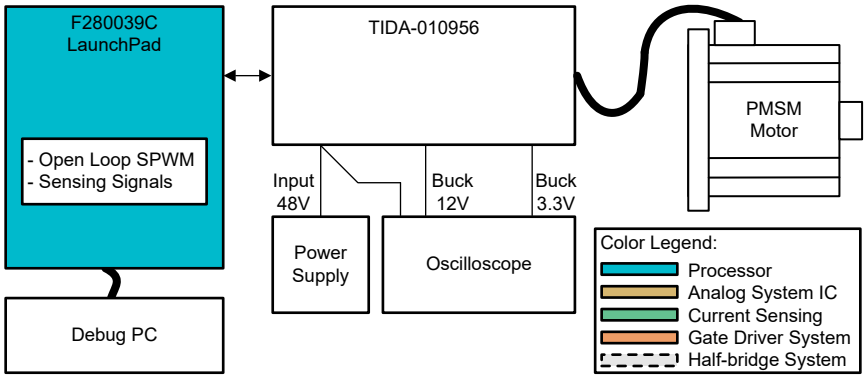


Figure 3-3. TIDA-010956 Diagram of Test Setup for the Voltage Rails

3.3.1.1 Power Up

Figure 3-4 illustrates the TIDA-010956 power-up sequence.

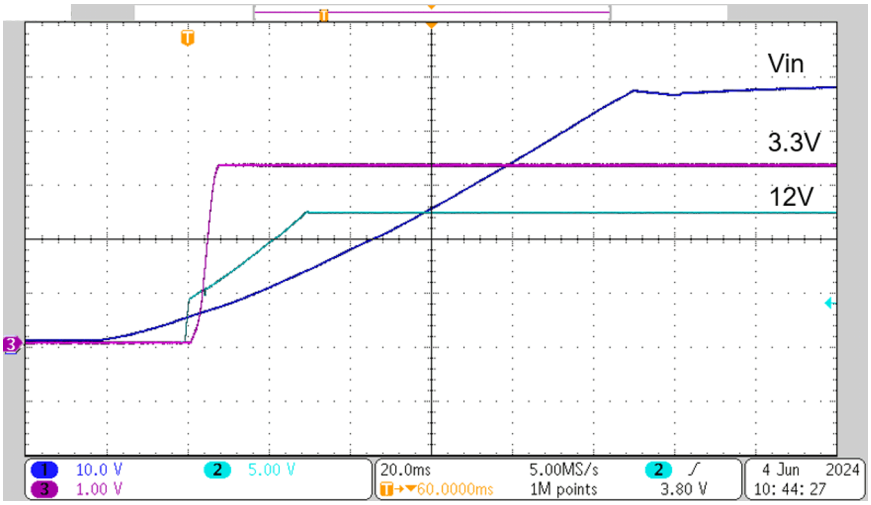


Figure 3-4. TIDA-010956 Power-Up Sequence

The power up sequence of the system is as follows: 48V V_{IN} (CH1 in dark blue) goes above approximately 5V first, then LMR38010FDDAR starts providing the 12V rail (CH2 in light blue). When this 12V rail is approximately 5V, the 3.3V rail (CH3 in purple) is enabled.

The V_{IN} has a slow ramp up while charging the VDC bus capacitors which are mainly of 330µF × 2 + 2.2µF × 20 and sum up to over 700µF. Another 180µF × 20 = 3.6mF needs to be added if a capacitor board is adopted.

3.3.1.2 Power Down

During the power-down process, the V_{IN} ramp down is also slow because the V_{IN} has to discharge the > 700µF capacitance (see Figure 3-5).

As the V_{IN} drops to approximately 7V, the 12V rail starts to power down. When this 12V rail gets to approximately 4V, the V_{IN} shuts down the 3.3V rail. Then the remaining charge of the capacitors dissipates slowly.

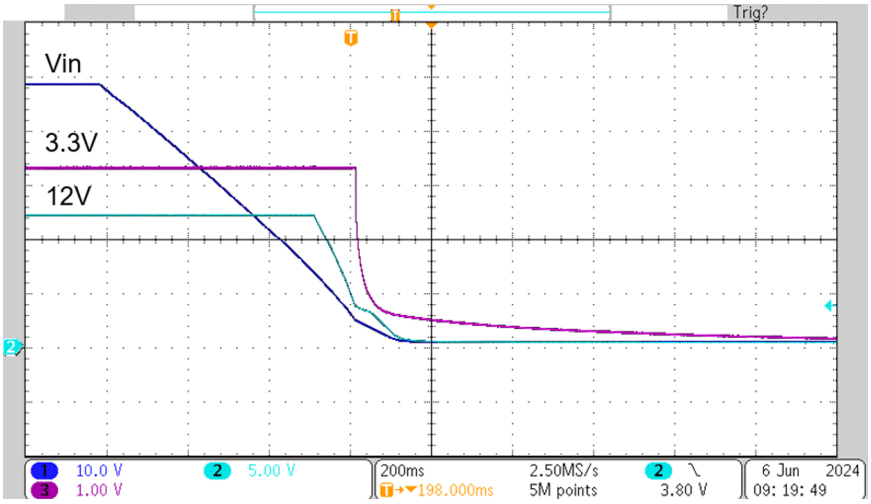


Figure 3-5. TIDA-010956 Power-Down Sequence

Table 3-7 shows the system status when the current is a 12V rail.

Table 3-7. 12V Rail Current in Various System Status

MEASUREMENT	SYSTEM STATUS	12V RAIL CURRENT
Current (mA)	Idle (Gate driver disabled)	73.5
Current (mA)	16kHz PWM	125.4

Note

By default, in this design the C2000 LaunchPad is supposed to be powered up by the TIDA-010956 with the 3.3V supply through a 0Ω resistor (R29). Remove the JP1 (5V power supply from the PC USB) on the LAUNCHXL-F280039C before applying V_{IN}.

3.3.2 Gate Voltage and Phase Voltage

To measure the gate voltage and the phase voltage on the switch node, the following measurements were performed. Figure 3-6 shows the test setup.

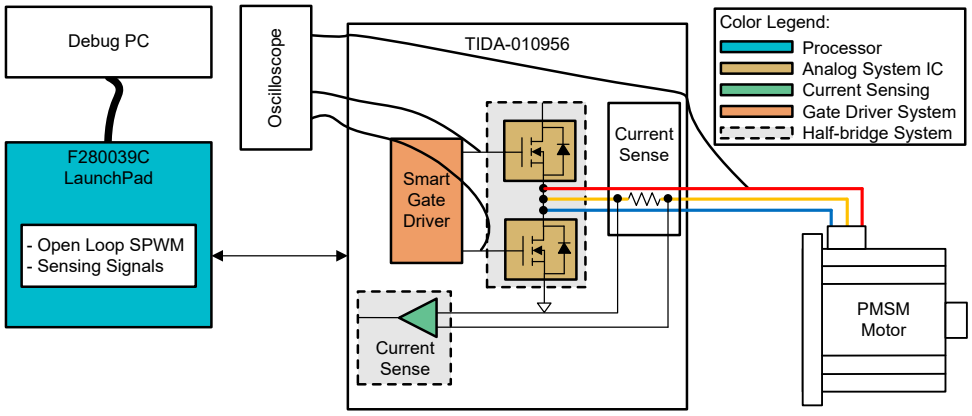


Figure 3-6. Test Setup for the Gate Voltage and Switch Node Voltage Measurements

In these tests the VDC applied was 48V and the motor was set to a fixed angle with open loop vector control. The signals were measured in phase-B, including the gate voltage (CH1, in dark blue) of the low-side MOSFET, the switch node voltage (CH2, in light blue) of the phase, and the output current (CH4, in green). Both voltages are referenced to GND and the positive direction of the phase current is from the drive to the motor.

The measurements in Section 3.3.2.1, Section 3.3.2.2, and Section 3.3.2.3 show the shifts of the phase in the conditions when the current was set to both positive and negative values. All four configurations of soft switching and hard switching of the low-side MOSFET were measured.

3.3.2.1 20 VDC

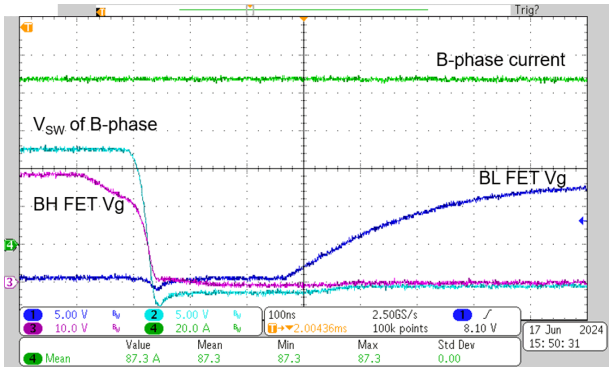


Figure 3-7. Hard Switching, Phase Current at 20V, 87.3A

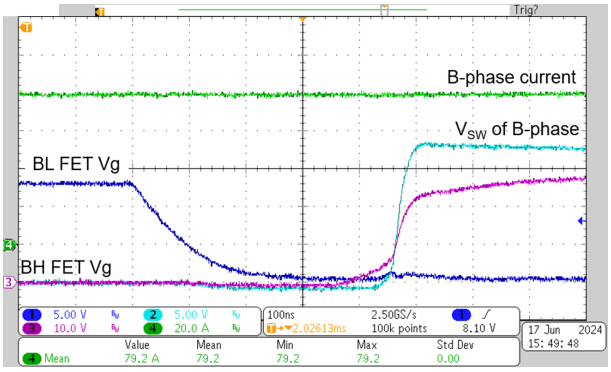


Figure 3-8. Soft Switching, Phase Current at 20V, 79.2A

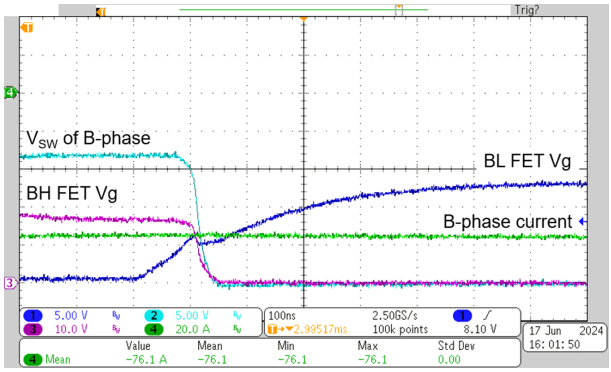


Figure 3-9. Soft Switching, Phase Current at 20V, –76.1A

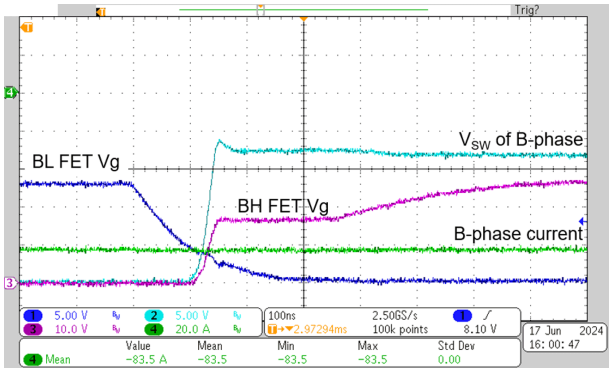


Figure 3-10. Hard Switching, Phase Current at 48V, –83.5A

3.3.2.2 48 VDC

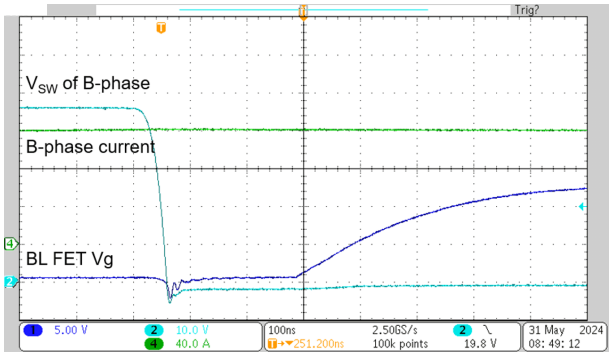


Figure 3-11. Hard Switching, Phase Current at 48V, 120A

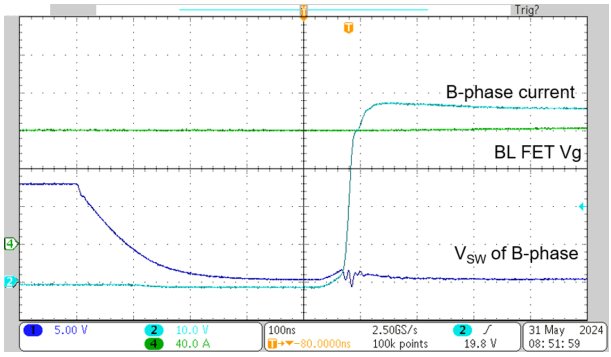


Figure 3-12. Soft Switching, Phase Current at 48V, 120A

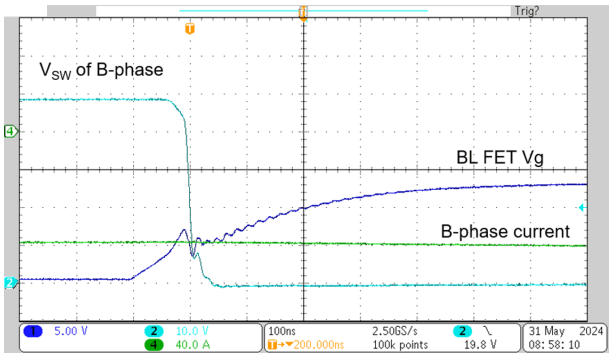


Figure 3-13. Soft Switching, Phase Current at 48V, –120A

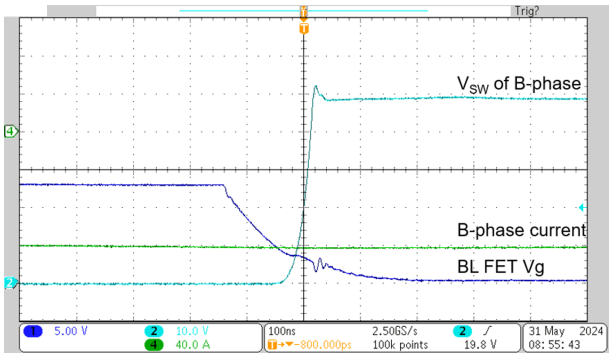


Figure 3-14. Hard Switching, Phase Current at 48V, –120A

3.3.2.3 60 VDC

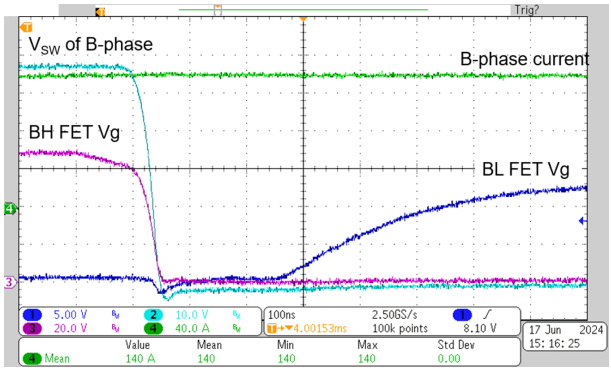


Figure 3-15. Hard Switching, Phase Current at 60V, 140A

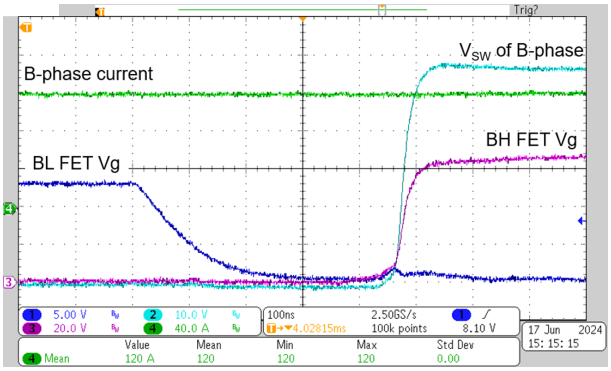


Figure 3-16. Soft Switching, Phase Current at 60V, 120A

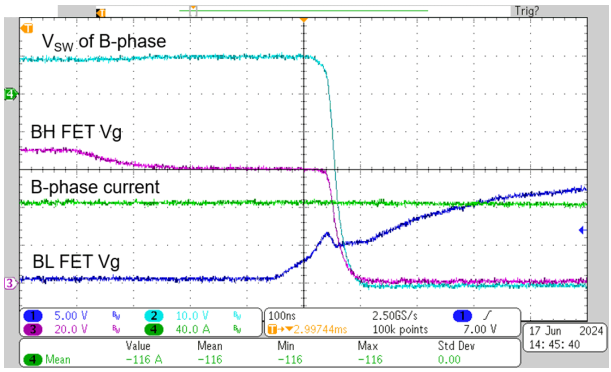


Figure 3-17. Soft Switching, Phase Current at 60V, –116A

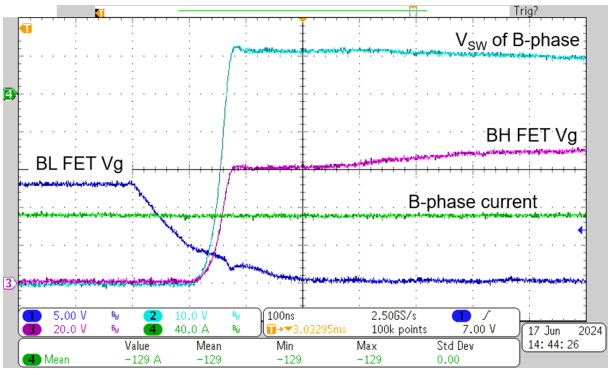


Figure 3-18. Hard Switching, Phase Current at 60V, –129A

3.3.3 Digital PWM and Gate Voltage

In these tests, the propagation delay between the PWM signal and the MOSFET gate voltage was measured in a low-side channel first; and then the dead time between the high-side and low-side digital PWMs as well as the gate voltages of the MOSFETs were measured. Figure 3-19 shows the test setup.

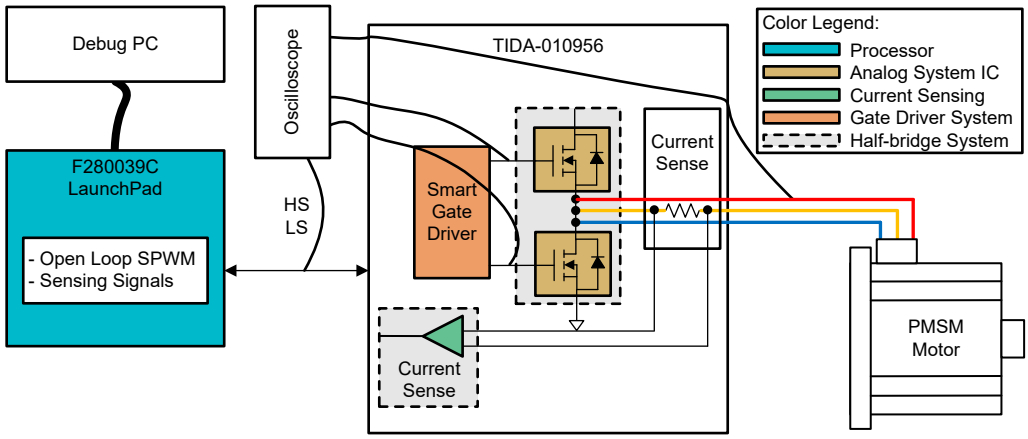


Figure 3-19. Test Setup for the Digital PWM and Gate Voltage Measurements

The system was using a 48V V_{IN} in these tests and the motor was set to a fixed angle with open loop control. The signals were measured in Phase C and all signals were referenced to GND.

The propagation delay in turn-on and turn-off appear in Figure 3-20 and Figure 3-21.

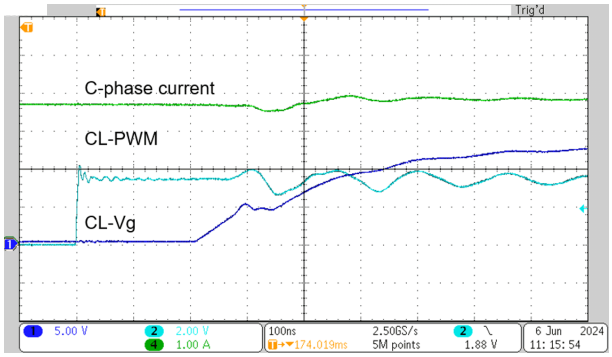


Figure 3-20. Propagation Delay in Turn-On

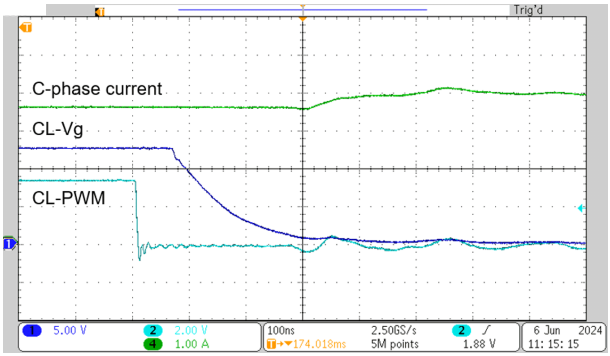


Figure 3-21. Propagation Delay in Turn-off

The turn-on delay was measured at about 200ns and the turn-off delay was measured at about 70ns. The turn-on was postponed by about 130ns due to an extra dead time that was introduced with the DRV8162L, following the DT pin setting of a 3.3kΩ R_{DT} connecting to GND.

Figure 3-22 and Figure 3-23 show the 200ns dead time of the PWM signals and the corresponding gate voltages when the half bridge is switching from low to high (CH2 for CL and CH3 for CH).

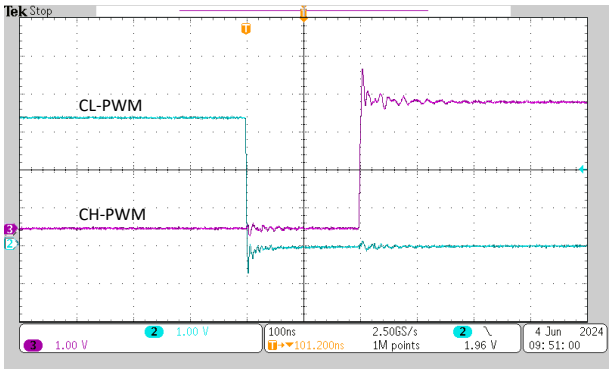


Figure 3-22. PWM Inputs in Positive Shift, DT = 200ns

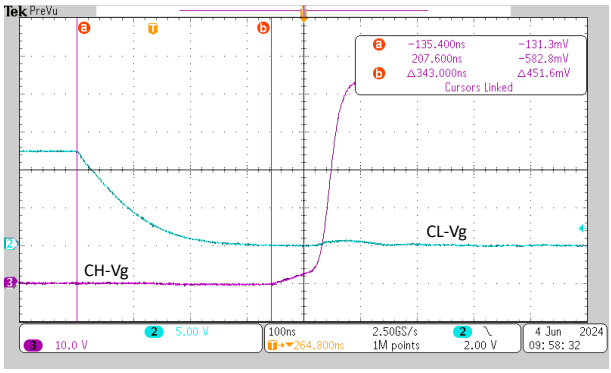


Figure 3-23. Gate Voltages in Positive Shift, DT = 343ns

The dead time between the high-side and the low-side gate voltages was expanded to about 340ns with the DRV8162L.

Figure 3-24 and Figure 3-25 show the half bridge is switching from high to low. The dead time was also expanded to about 340ns with the R_{DT} setting.

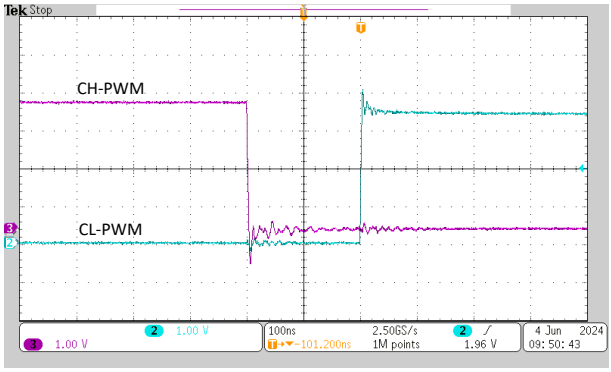


Figure 3-24. PWM Inputs in Negative Shift, DT = 200ns

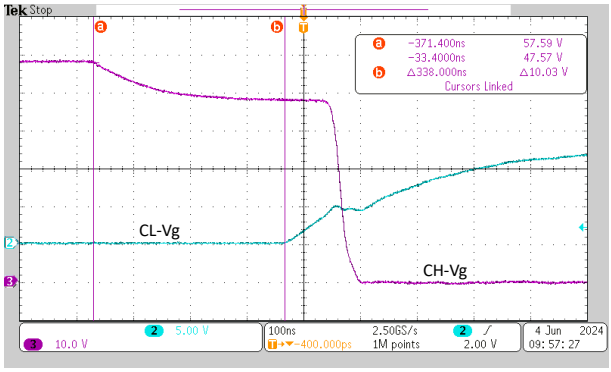


Figure 3-25. Gate Voltages in Negative Shift, DT = 338ns

This DRV8162L automatically inserts dead time and can vary between 20ns to 370ns, depending on the R_{DT} value. See the data sheet for the details.

3.3.4 Phase-Current Measurements

This section shows the phase-current measurement performance generating an open loop rotating field for the motor control.

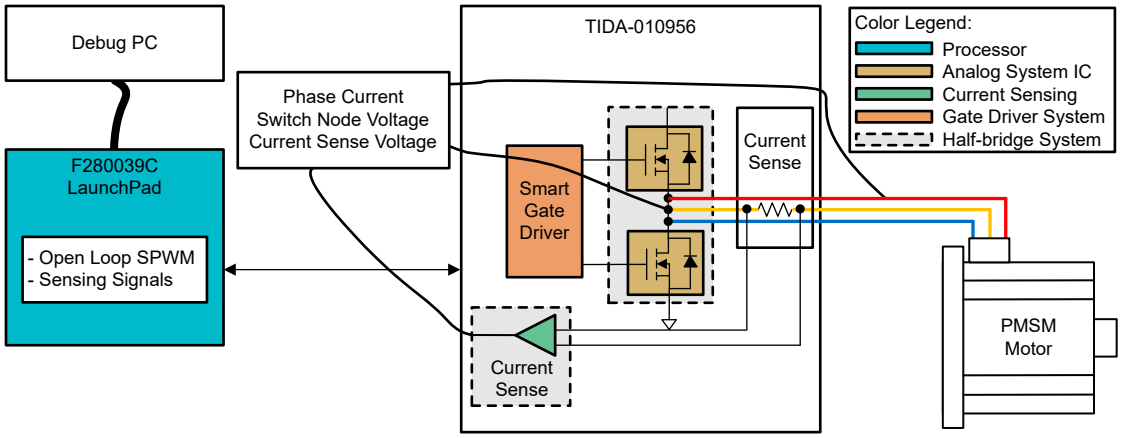


Figure 3-26. TIDA-010956 Diagram of the Test Setup for the Current Measurements

Figure 3-27 shows the motor current (CH4 in green) and the current-sense amplifier output voltage (CH1 in deep blue) of the INA241 measurements in B-phase. The switching node voltage is also shown (CH2 in light blue).

Figure 3-28 shows the sinusoidal-like waveform output of the INA241. Obvious distortions of the sine wave are displayed as the system is running in open loop. Figure 3-28 shows the common-mode performance of the INA241.

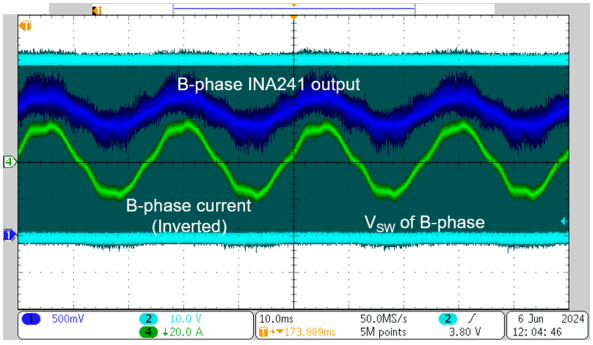


Figure 3-27. Rotating Current Measured on the INA241 Output

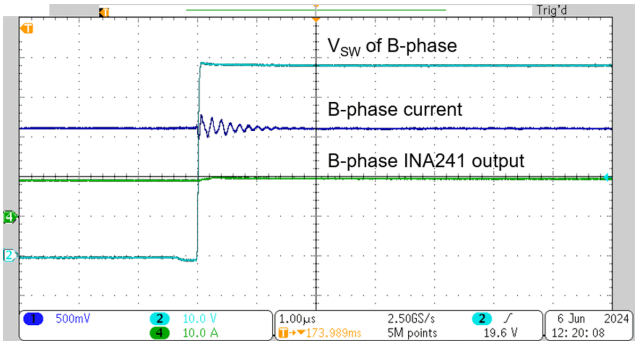


Figure 3-28. INA241 Output Measured During Switch Point

This measurement captures the worst-case scenario of the settling time of the amplifier. Observe that a maximum settling time of around 1.0µs can be expected.

3.3.5 System Test Results

3.3.5.1 Thermal Analysis

Thermal analysis of the design was performed at a 28°C lab temperature with a 48V V_{IN} and 16kHz PWM. A low-voltage PMSM motor was driven with sinusoidal phase currents at a load current of 26.2A_{rms}, (37.0A peak). This test did not use a heat sink or fan. Figure 3-29 shows the thermal picture of the board.

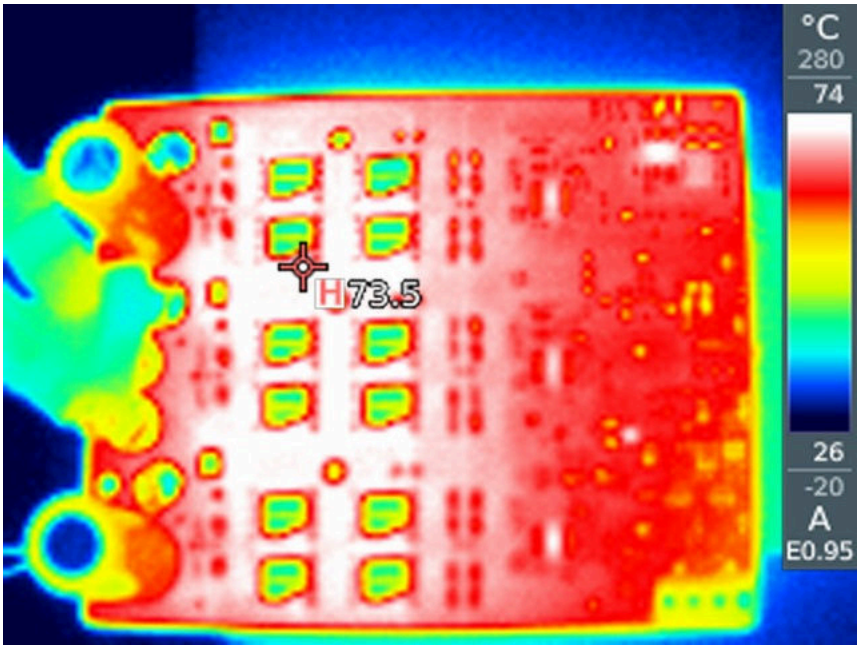


Figure 3-29. TIDA-010956 Thermal Picture at 26.2A_{rms} Output

This measurement shows that at 26.2A_{rms}, the MOSFETs have a temperature rise of 45.5°C. Consider keeping the junction temperature of the MOSFET at less than 125ºC, the current design can work up to 79.5ºC ambient at 26.2A_{rms} without a heat sink. It is possible that a heat sink and cooling fan are needed for higher current or higher ambient temperature conditions.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010956.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010956.

4.2 Tools and Software

Tools

LAUNCHXL-F280039C	C2000™ real-time MCU F280039C LaunchPad™ development kit

Software

C2000WARE-MOTORCONTROL-SDK	MotorControl software development kit (SDK) for C2000™ MCUs

4.3 Documentation Support

1. Texas Instruments, *DRV816x 100V Half-Bridge Smart Gate Driver with Integrated Protection and Current Sense Amplifier Data Sheet*
2. Texas Instruments, *INA241x–5 V to 110 V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection Data Sheet*
3. Texas Instruments, *TMP61 ±1% 10-kΩ Linear Thermistor With 0402 and 0603 Package Options Data Sheet*
4. Texas Instruments, *LMR38010 4.2-V to 80-V, 1-A, Synchronous SIMPLE SWITCHER Power Converter With 40-µA I_Q Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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5 About the Authors

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