Industry Article

Understanding and Mitigating Motor Driver Board Parasitics through Simulation

February 04, 2021 by Matt Hein, Texas Instruments

This article explores using PSpice for TI to simulate potential causes for parasitic effects in a motor-drive design and offers design tips to mitigate the negative effects common with high-power motor-drive systems.

One of the most frustrating parts of high-power system design is the often-elusive results of parasitic effects. This especially applies to high-power motor-drive systems where large board designs, large components, and high output currents can result in output ringing, excessive component ratings, or radiated electromagnetic interference (EMI). In this article, I'll use PSpice® for TI to simulate potential causes for parasitic effects in a motor-drive design and offer design tips to mitigate the negative effects.

What is a High-Power Motor Drive Design?

As someone who gets to be completely immersed in motor-drive systems, I often take for granted the basics of how to architect a motor-drive system depending on a specific challenge. There are two very good reasons why parasitic analysis becomes critical in high-power systems.

First, with high power comes high current: switching 1 A in a motor won't have the same effect as switching 100 A in a motor. With high current, all of those parasitic inductances and capacitances that are inherent on the printed circuit board (PCB) jump out and start causing trouble. The lower you can keep your current, the less these parasitic components matter. For a system with defined high-output power, however, the target output current is fixed – setting the design on a collision course with any stray inductance and capacitance.

Second, high-power motor-drive systems require a gate-driver architecture. Motor drivers come in two flavors: integrated FET (field-effect transistors) and gate drivers with external FETs – see Figure 1. Integrated FET motor drivers are very effective for lower-power systems because they integrate the gate driver, power stage, and any other sensing and protection into a single package. These devices are also incredibly small – for example, DRV8837C is only 2x2 mm, so they significantly reduce board parasitics.

Unfortunately, you cannot drive a 100-A motor with even the highest-current integrated FET solutions (for example DRV8873-Q1 is capable of driving up to 10 A), so the gate-driver architecture is required. When using a gate-driver along with external discrete MOSFETs for a motor driver system, there will always be some PCB trace between components on the board, which contributes to parasitic effects.

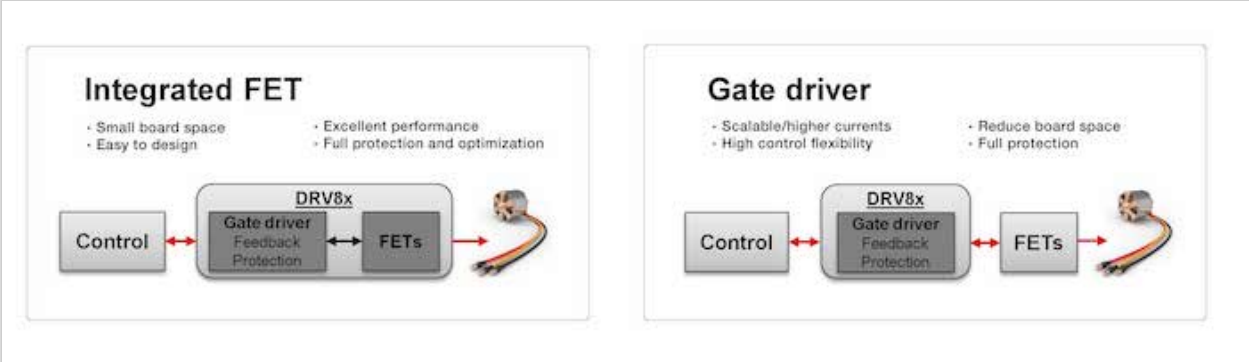

Figure 1. Integrated FET versus gate-driver architectures

The Gate Driver Circuit and Applied Pulse

To build a circuit to analyze, let's start with a simplified half-bridge motor driver (Figure 2). The motor driver I used in this circuit is the Texas Instruments (TI) DRV8343-Q1, a three-phase smart gate motor driver with current shunt amplifiers. The MOSFETs are TI's CSD18540Q5B and the gate-drive strength (IDRIVE) that I selected is 15-mA source and 30-mA sink. I only used one phase and created a model load (240 mΩ and 50 µH) for simplicity. The power supply used in this case is 24 V.

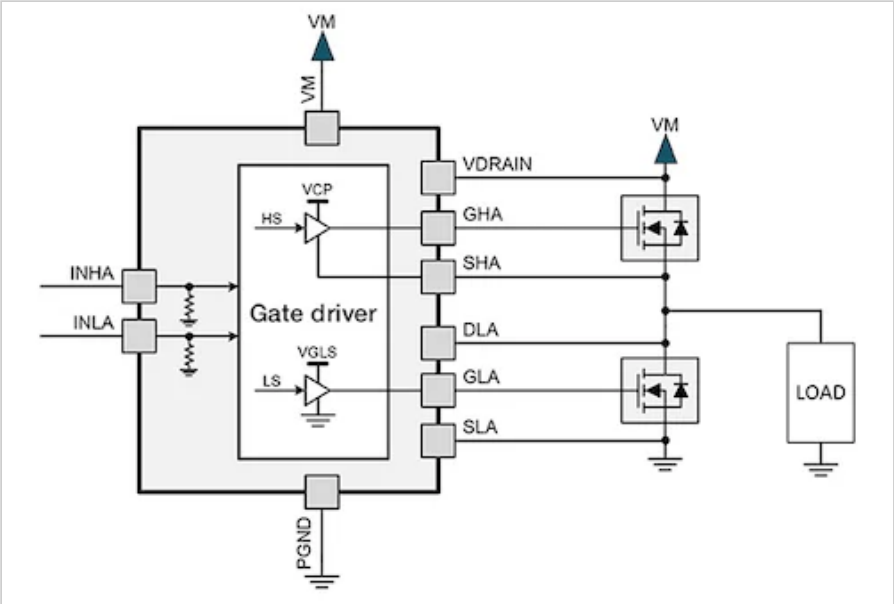

Figure 2. Simplified driver circuit (without parasitic elements)

Next, I simulated a "pulse test," which involves turning on the high-side MOSFET for a certain time, and then quickly pulsing it off and on while significant current flows through the circuit. Simulating a pulse test will enable you to observe any effects created by the falling and rising edges of the output as the high-side MOSFET turns off and back on.

In Figure 3, you can see the applied control signals, the expected ideal waveform for the high-side gate and the output voltage. In this simulation, the high-side MOSFET was turned on for 400 µs, pulsed low for 30 µs, and brought high for the remaining 70 µs. The low-side MOSFET remained off, so any current flowing conducted through the low-side MOSFET body diode.

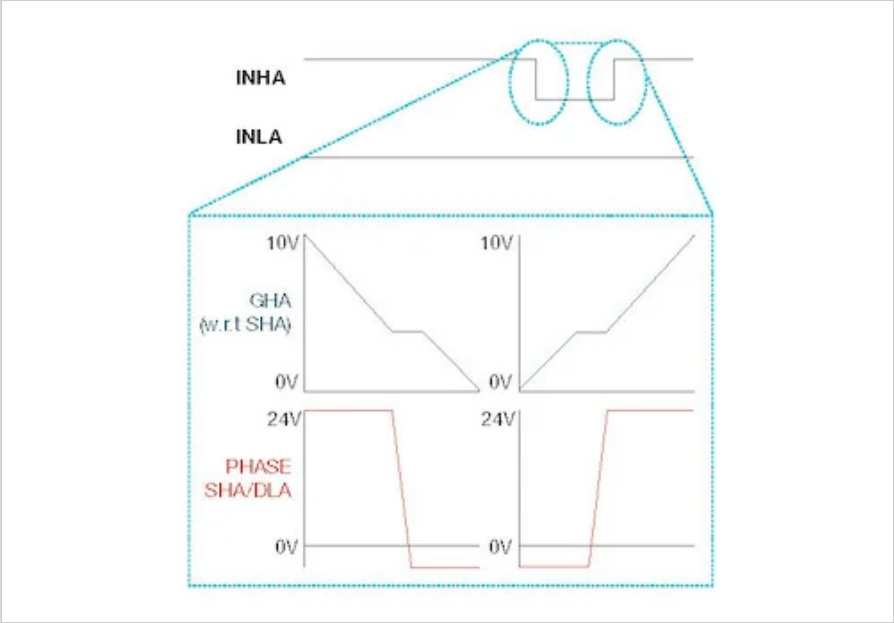

Figure 3. Pulse test waveform (without parasitic elements)

Adding Parasitic Components and Simulating

If you add in the expected parasitic components in this circuit, the complexity increases rather quickly; the circuit schematic ceases to look “nice.” To do this you need to add important parasitic components in three places:

1. Between the supply and the high-side MOSFET (HS).
2. Between the ground and the low-side MOSFET (LS).
3. Between the high-side and low-side MOSFETs (PHASE).

These three locations are where you will typically see a significantly large trace on the PCB, corresponding to a high-current-carrying net. Take a look at Figure 4.

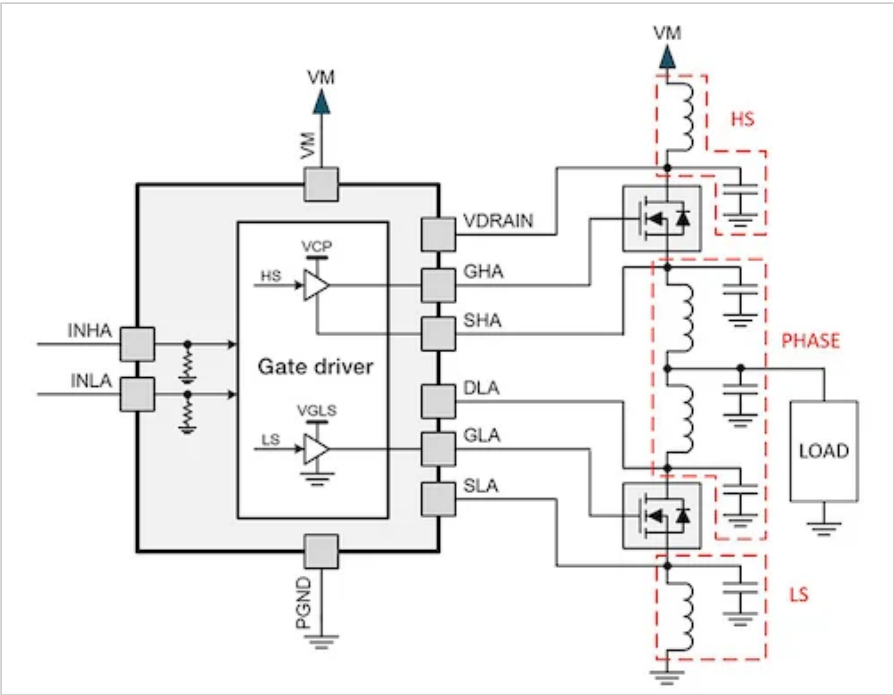

Figure 4. Driver circuit with parasitic elements

For parasitic values, I used the following:

- High side (HS): 10 nF, 5 nH/10 mΩ.
- Phase (PHASE): 2 nF, 2 nH/2 mΩ (per path, with an additional 10 nF on the output to the load).
- Low side (LS): 10 nF, 5 nH/10 mΩ.

Since this is only a simulation, I used (potentially) exaggerated parasitic inductances and capacitances. It is possible to design a board that minimizes these parasitic components, thereby making mitigation easier (albeit following the same process). On the contrary, a poorly designed PCB may have significantly more parasitic inductance and capacitance, which can make mitigating parasitic effects much more difficult. For a review of layout techniques for motor drivers, I recommend the Best Practices for Board Layout of Motor Drivers application note.

When I simulated the circuit before (Figure 2) and after (Figure 4) adding these parasitic components, I got the overwhelming feeling that I had broken the circuit. Take a look at Figure 5 to see significant oscillation on the phase when switching high or low. It's important to mitigate these effects to protect the circuit from damage (such as a –20-V negative voltage spike) or to prevent any unwanted electromagnetic radiation (the oscillating nets will act as antennas).

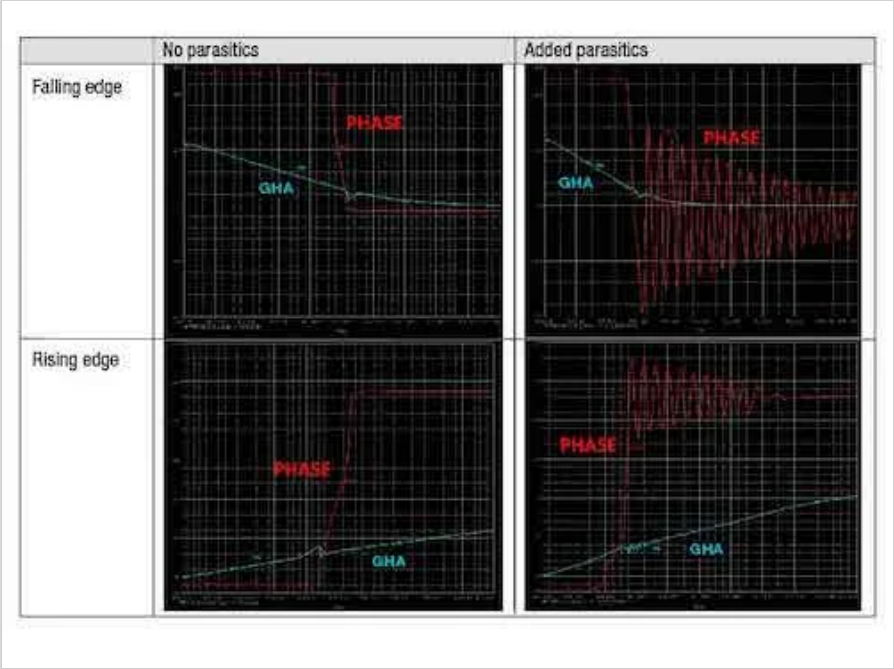

Figure 5. Results of PSpice for TI simulation before and after adding parasitic components

In order to figure out the best mitigation actions, let's break down the different parasitic components one-by-one and simulate the effects of each.

Parasitic Components Between the Supply and the High-Side MOSFET (HS)

When I added the parasitic components between the supply and the high-side MOSFET (Figure 6), the simulation showed very obvious oscillation on the output of the rising edge (Figure 7). Digging into more detail, you can see that the oscillation is coming from the drain of the high-side MOSFET (VDRAIN). In the falling edge, when the high-side MOSFET is turned off, you'll see this same effect even though the output is not affected.

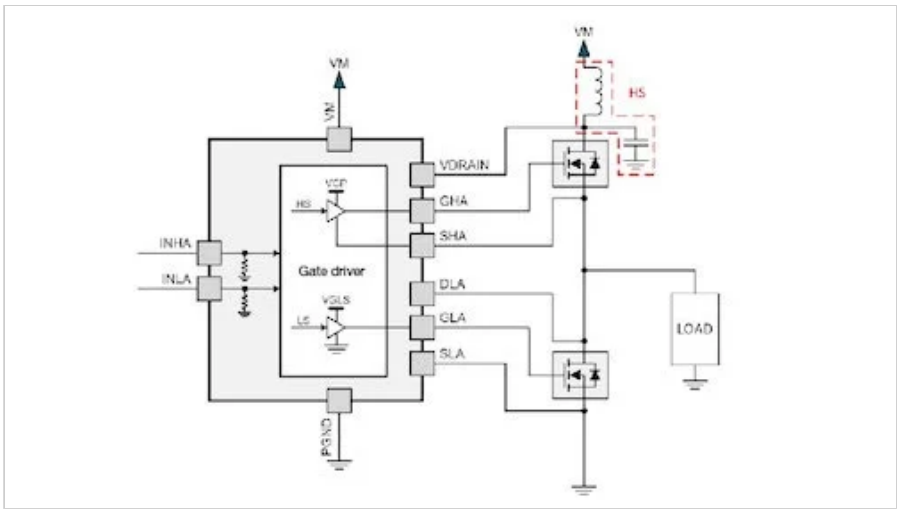

Figure 6. Driver circuit with parasitics in the high-side path (HS)

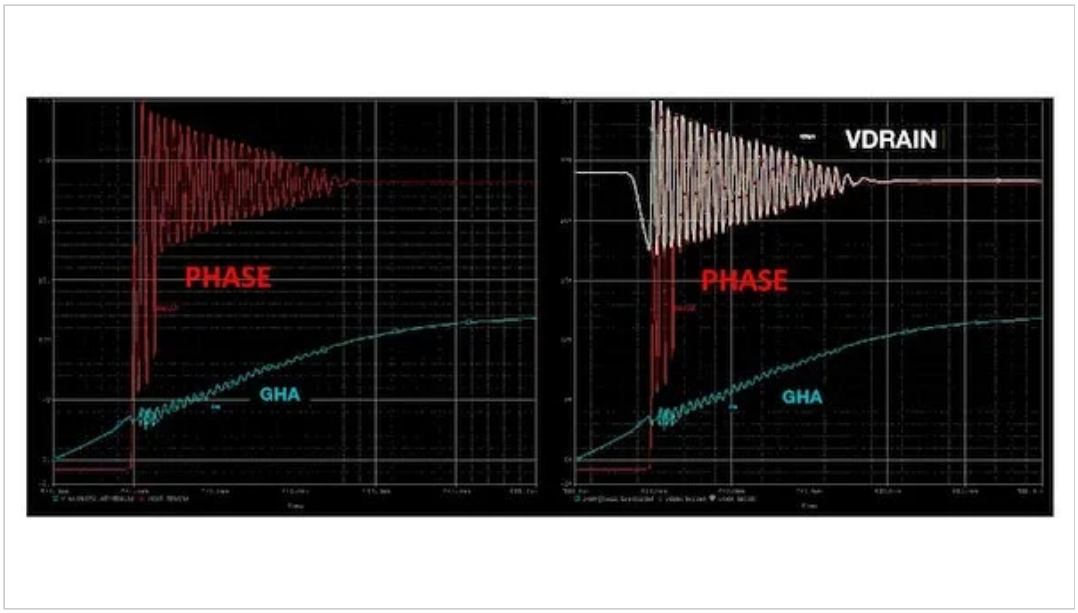

Figure 7. Simulation of rising edge with parasitics added to the high-side path (HS)

At this stage, you might think that you need to add snubbers, or that the slew rate is too high and needs to be reduced. Consider this: snubbers will be most effective at reducing phase oscillations, not VDRAIN oscillations. For the investigation, I implemented a snubber of 1.2 Ω and 33 nF on both the high-side and low-side MOSFETs. You can see the effect in Figure 8, where the VDRAIN still drops out before the switching event, so this is not the best method to mitigate the ringing.

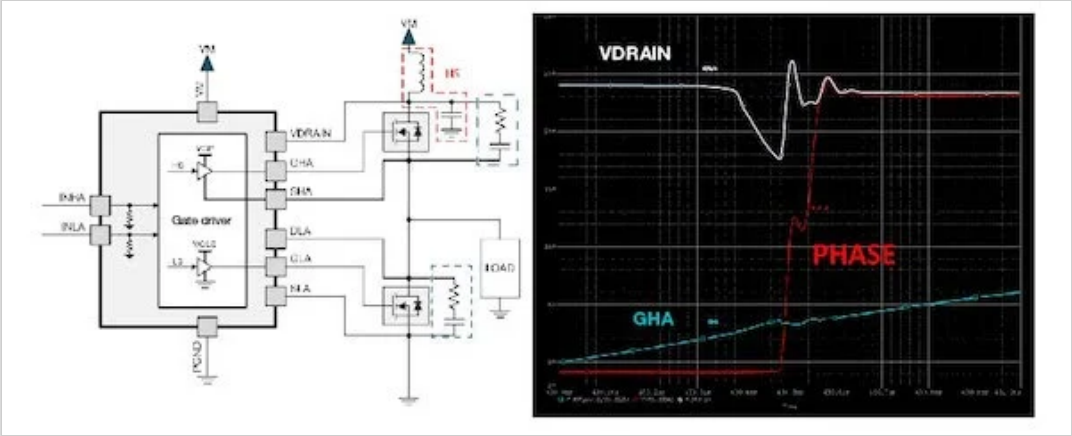

Figure 8. Despite snubbers, mitigation is not effective because of oscillations on VDRAIN

To learn more about snubber design, check out the technical article Power Tips: Calculate an R-C snubber in Seven Steps.

Another possible solution to reduce the oscillation is to reduce the slew rate, which in simulation will significantly reduce but not eliminate the ringing (Figure 9). A reduced slew rate results in more power losses (hotter components) because of higher switching losses, and should be avoided if possible. In this example, I reduced the gate-drive current from a 15-mA source to a 1.5-mA source – a 10x longer rise time.

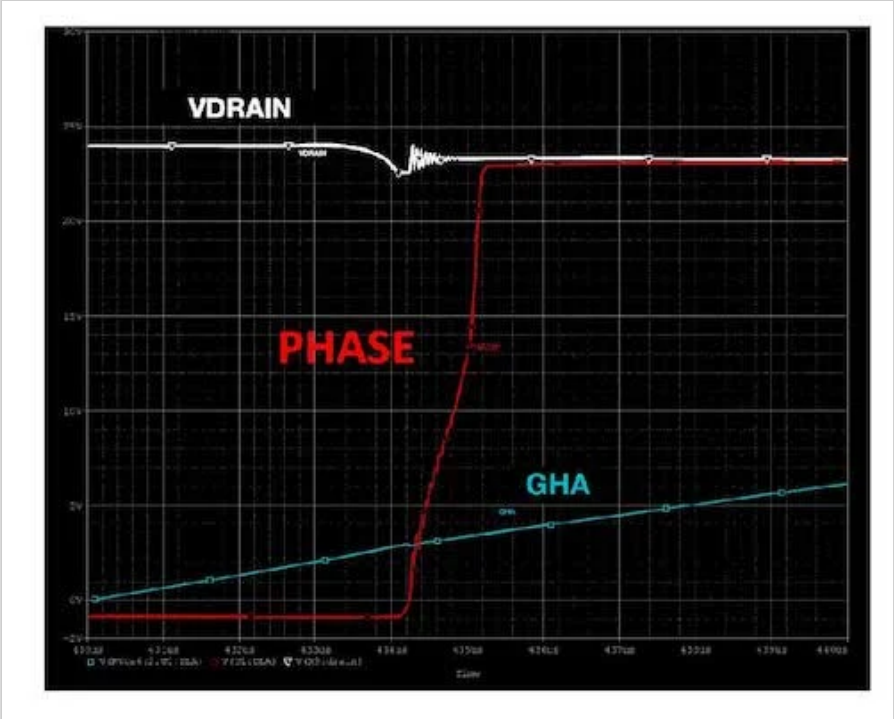

Figure 9. Despite a reduced gate-drive current and a longer rise time, mitigation is not effective because of higher power dissipation and continued oscillation

To better mitigate these effects, let's add a large bulk capacitance on the VDRAIN node (Figure 10); this will make the oscillation significantly slower with less amplitude. I simply made this inductor-capacitor time constant much, much longer. Figure 11 shows the results of such an addition.

In simulation, the addition of the bulk capacitor brought the peak oscillation down from 37 V (13 V above the supply) to a much more manageable 25 V (1 V above the supply). This capacitor must be placed as close to the high-side MOSFET as possible to mitigate any extra parasitic inductance between the capacitor and the MOSFET. Ceramic capacitors are preferable given their lower lead inductance and better high-frequency response.

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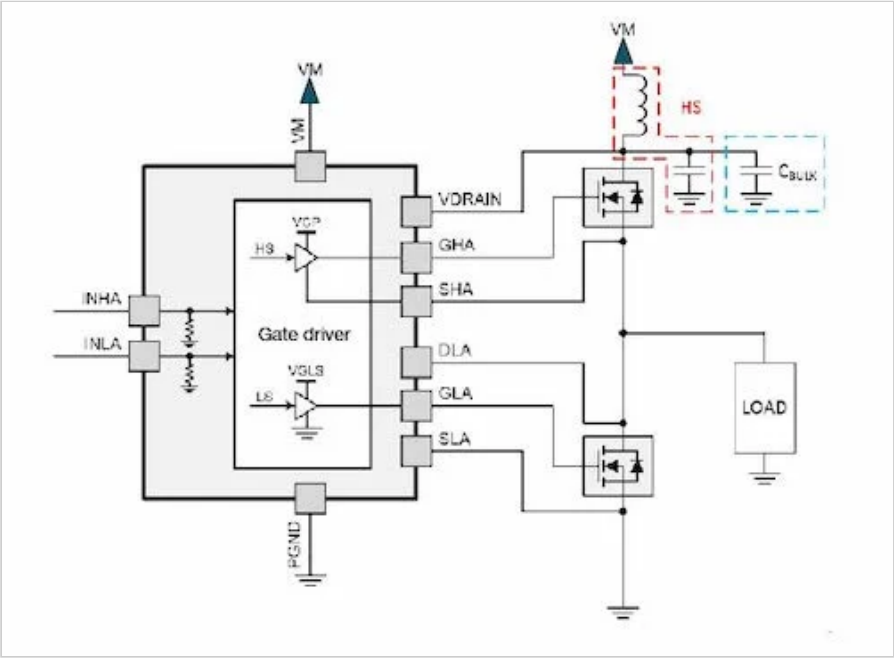


Figure 10. Adding a bulk capacitor on VDRAIN

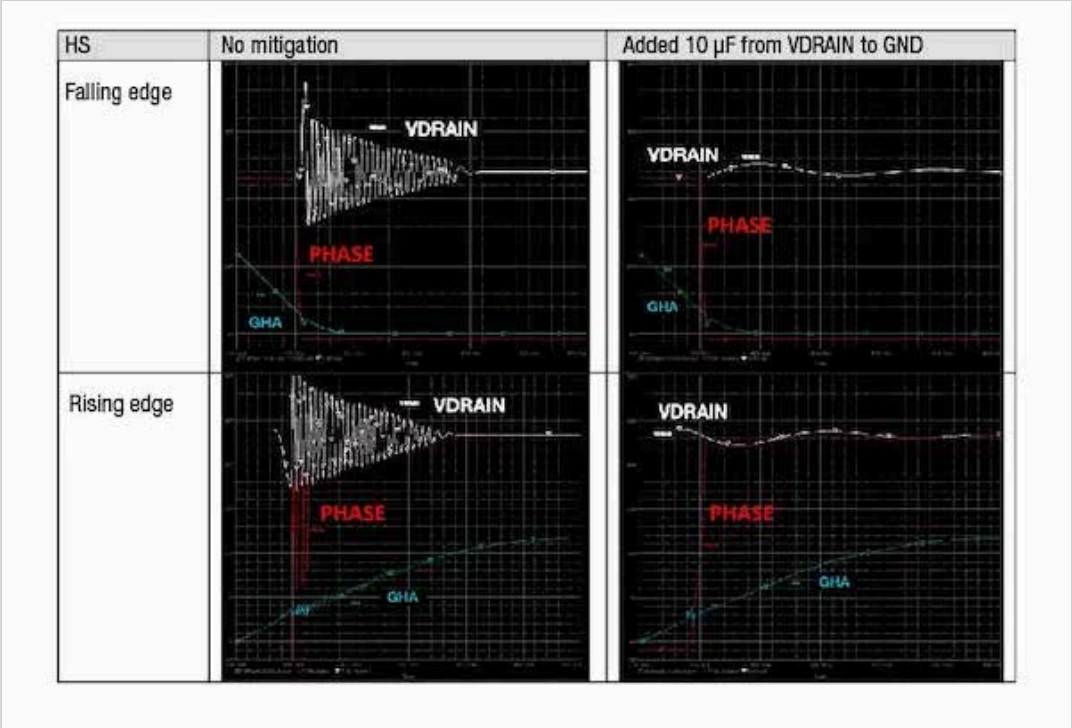


Figure 11. Mitigating high-side parasitic components with a bulk capacitor (VDRAIN to GND)

Parasitic Components Between Ground and the Low-Side MOSFET (LS)

The low-side path is almost the opposite compared to the high-side path. The falling edges resulted in significant oscillations, while the rising edges appeared clean. On closer inspection, you can see that the low-side MOSFET source node (SLA) was ringing in both the rising and falling edges (Figure 12).

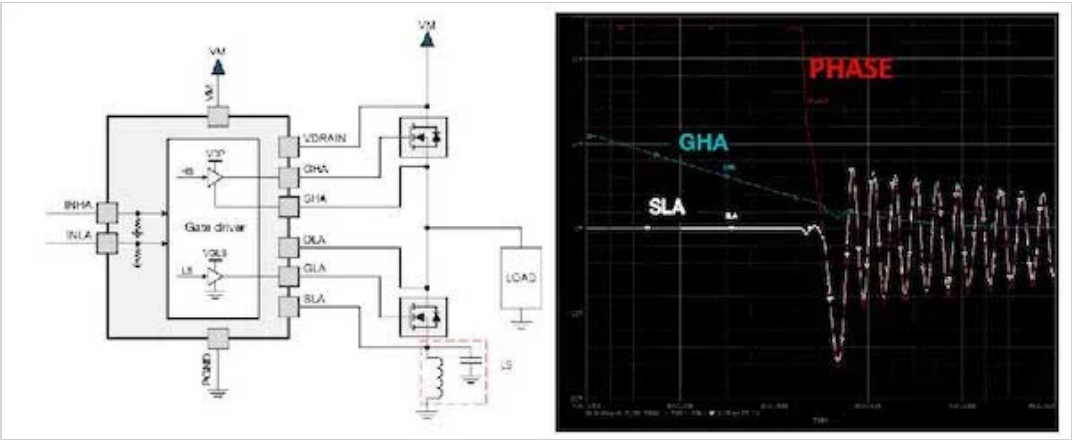


Figure 12. Schematic and simulation with parasitics added to the low-side path (LS)

When faced with this situation, some of you will want to add snubbers or lengthen the rise time to counter the ringing, but, you should also avoid that approach in this case. As I did earlier, I implemented a snubber of 1.2 Ω and 33 nF on both the high-side and low-side MOSFET. The result is a drastic improvement in oscillations on the phase, but the initial negative voltage pulse remains (Figure 13).

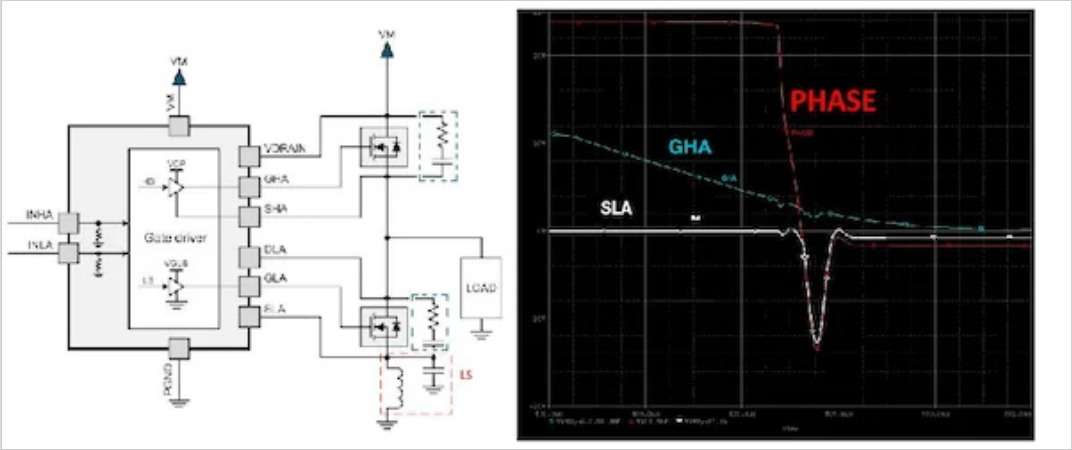


Figure 13. Despite snubbers, mitigation is not effective because of a negative voltage spike

If you reduce the slew rate, the ringing reduces significantly (Figure 14). In this example, the gate-drive current dropped from a 30-mA sink to a 7-mA sink; a >4x longer fall time.

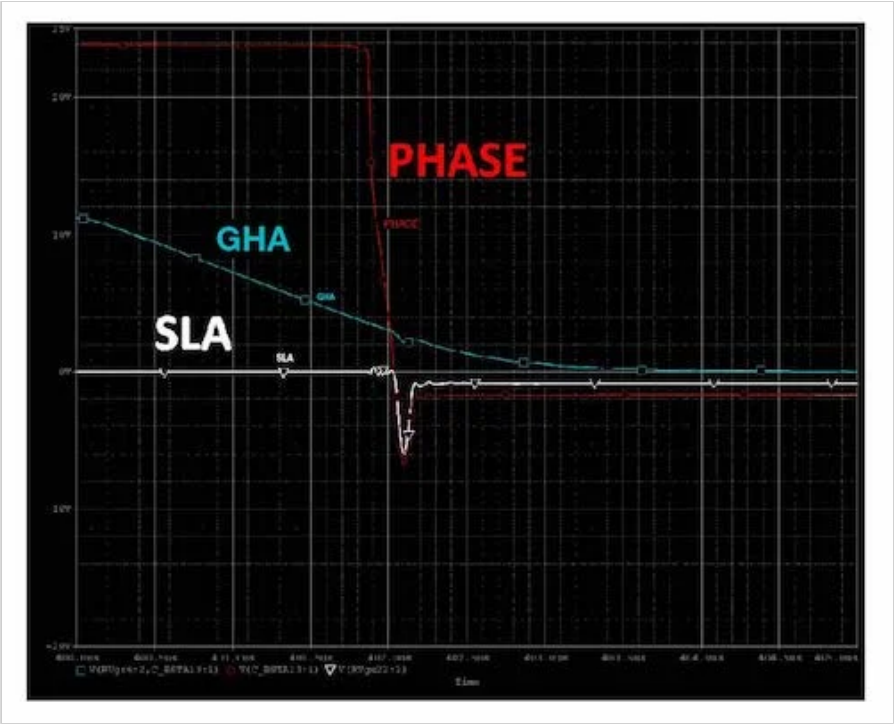


Figure 14. Despite a reduced gate drive current and a longer rise time, mitigation is not effective because of higher power dissipation

You could take a similar approach to the high-side case and add additional bulk capacitance to the board to counter this ringing. In this case, however, you do not want to add a large capacitor from SLA to ground. Most motor-drive systems implement current sensing on the low side using a current-sense resistor and a current-sense amplifier. A typical 2512 package sense resistor will have 1- to 5-nH parasitic inductance, lending some amount of credence to our assumed parasitic values.

A very large capacitor in parallel with a sense resistor will inhibit the ability of the system to sense current properly (Figure 15). The correct place to add this bulk capacitor is from VDRAIN to the low-side source (SLA). Keep in mind that when you add this decoupling capacitor, there will still be some effect on the peak current through the sense resistor. A very large value of this capacitor will impact any peak overcurrent limit derived through low-side current sensing.

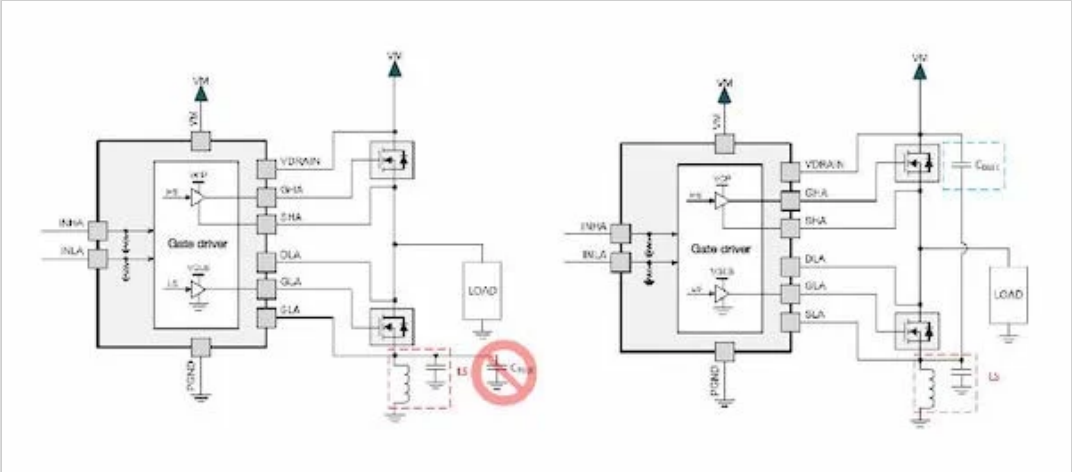


Figure 15. Incorrect (left) and correct placement (right) of a bulk capacitor to mitigate low-side parasitics

Figure 16 illustrates the results of such an addition. In simulation, the addition of the bulk capacitor significantly reduced the peak oscillation from –16 V to –3 V. Similar to the previous case, this capacitor must be placed as close to the high-side MOSFET drain and low-side MOSFET source as possible in order to mitigate any extra parasitic inductance between the capacitor and the MOSFETs. Ceramic capacitors are again preferable given their lower lead inductance and better high-frequency response.

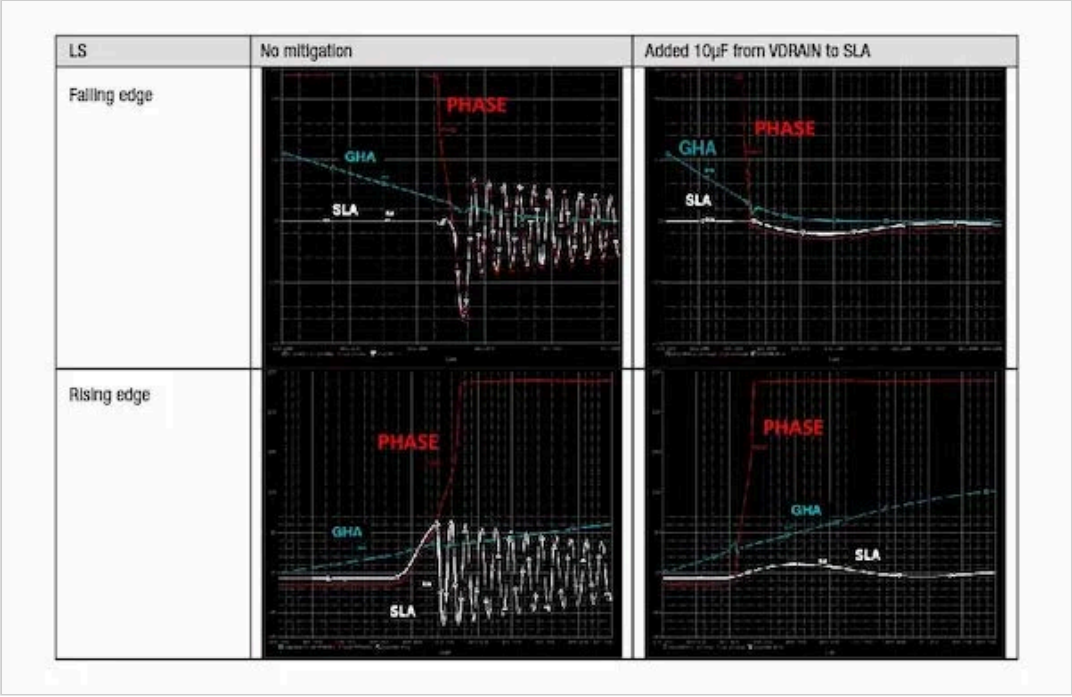


Figure 16. Mitigating low-side parasitic components with a bulk capacitor (VDRAIN to SLA)

Parasitic Components Between the MOSFETs (PHASE)

You may have learned that you should always keep your high-side and low-side MOSFETs as close together as possible in order to minimize parasitic effects when switching. This is very good advice, but you can never completely eliminate these negative effects.

Even the most effective multiple-die MOSFET solutions (see CSD88599Q5DC for example) will still have some parasitic inductance and capacitance between the high-side and low-side MOSFETs. The MOSFET output capacitance (COSS) and

motor cable capacitance (at longer cable lengths) can be significant contributors to the capacitance seen on the phase node outside of the PCB.

In this case, it is not possible to add additional bulk capacitance to the circuit to bypass the parasitic inductance. The output to the motor will be switching high and low, and additional large capacitors on this net will charge and discharge repeatedly – a very inefficient system solution. When this happens, it's best to go to the snubbers as a first strategy (Figure 17).

If you're a snubber proponent, you can breathe a sigh of relief – let's use them now! You can see the effects of adding snubbers to the circuit in Figure 18.

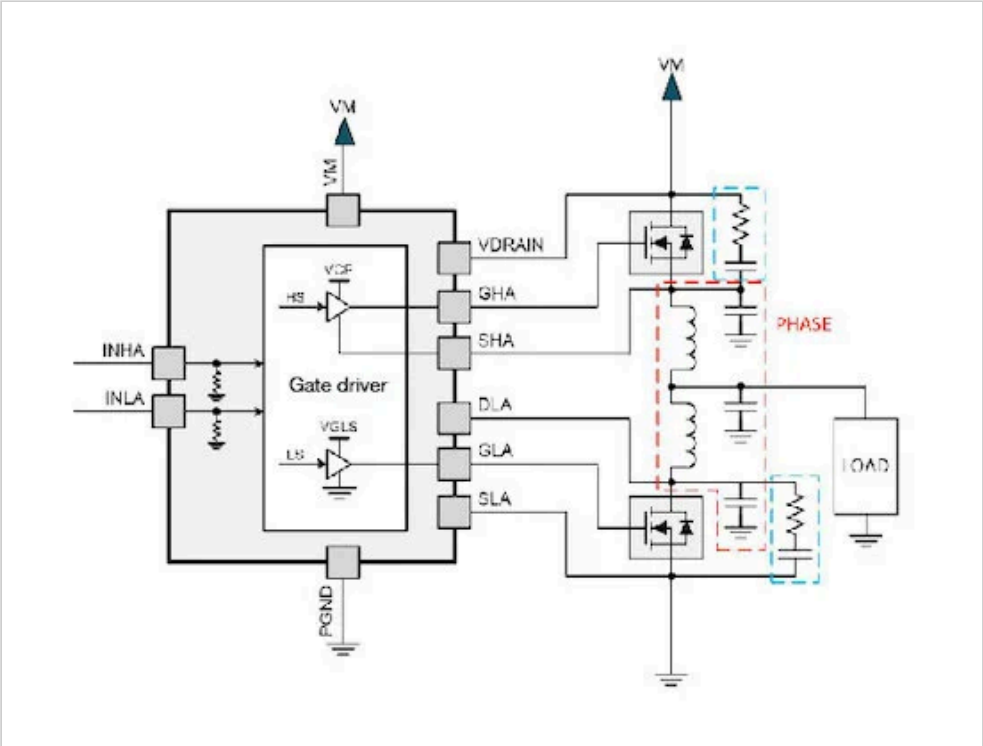


Figure 17. Schematic with parasitics added to the phase path (PHASE) and additional snubbers

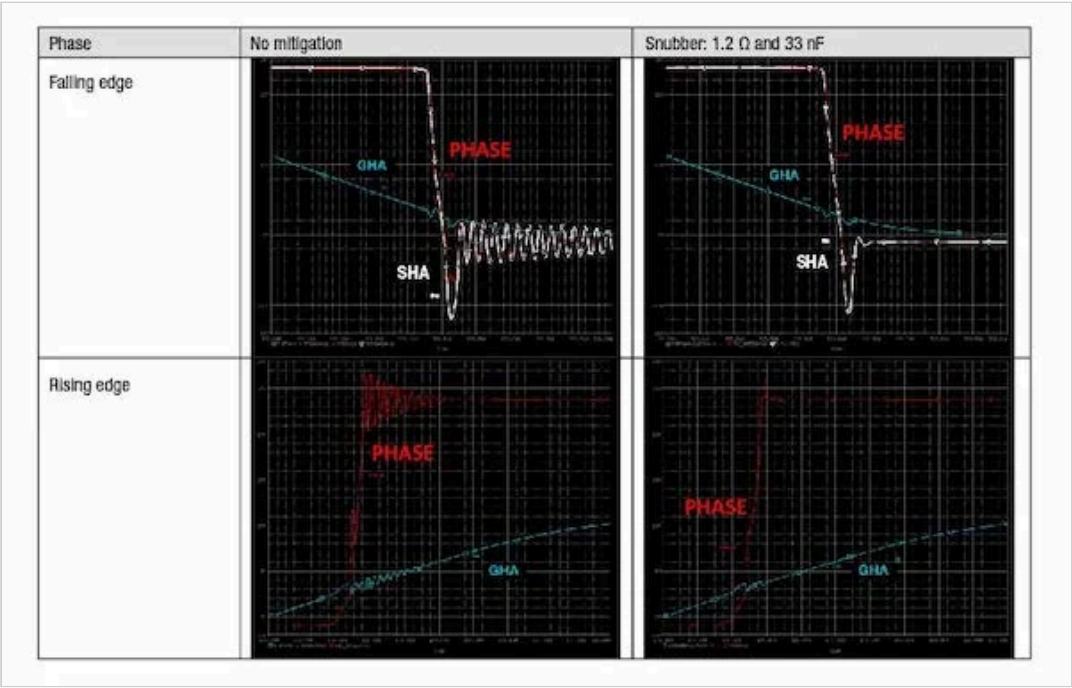


Figure 18. Mitigating phase parasitic components with snubbers

The snubber almost completely solves the oscillation on the rising edge and significantly improves the situation on the falling edge. Like in the previous experiments, I implemented a snubber of 1.2 Ω and 33 nF on both the high-side and low-side MOSFET. However, much like the low-side MOSFET parasitic case (Figure 14), the first negative pulse remains.

At this stage, you can conclude that the fall time needs to be increased in order to completely overcome these parasitic effects. You must improve the –11-V negative voltage spike on the falling edge in Figure 18 so that you remain within the absolute maximum ratings of the DRV8343-Q1 (–7 V for 200 ns). When you reduce the gate-drive current sink from 30 mA to 10 mA, you'll get this negative spike within the maximum rating (Figure 19).

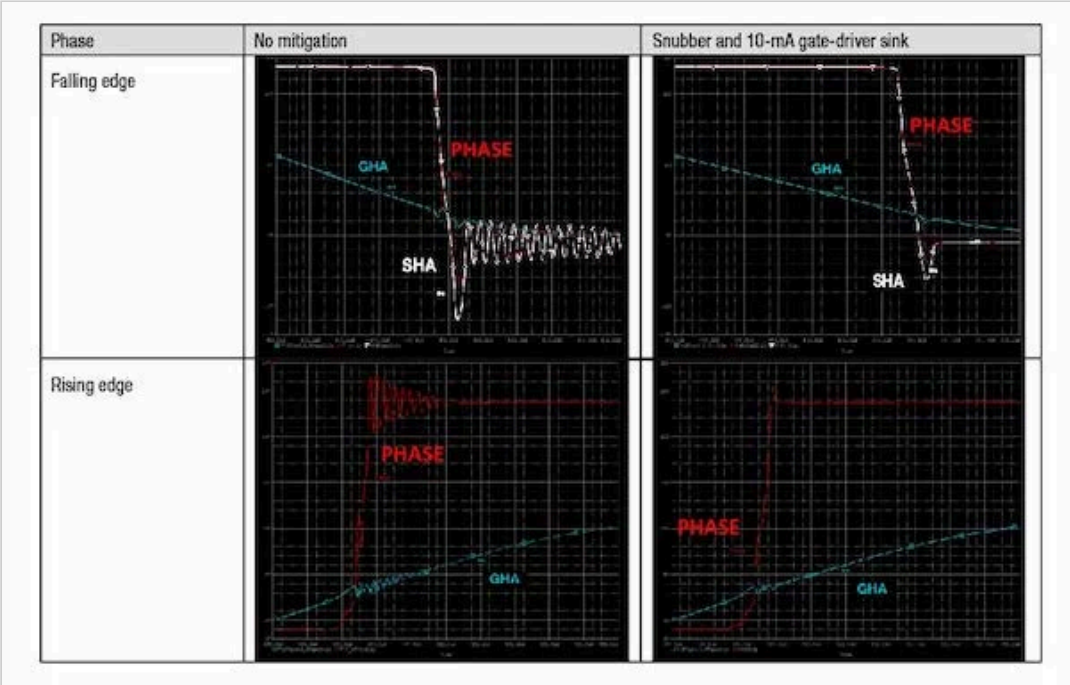
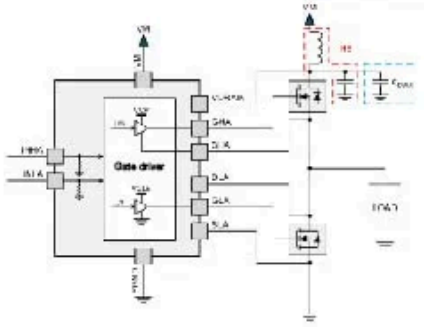
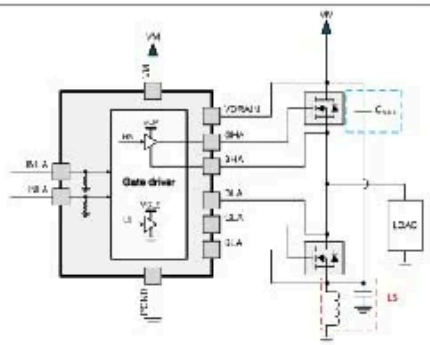
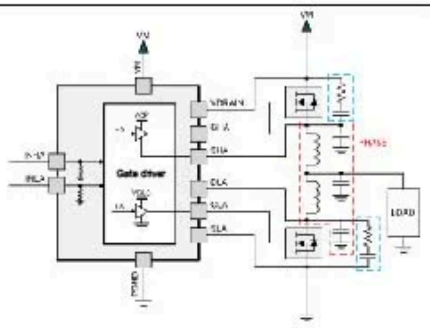


Figure 19. Mitigating phase parasitic components with snubbers and a reduced gate-drive current sink

Putting it All Together

So what have we learned through this simulation exercise? For these three common parasitic effects (high side, low side and phase), there are three different mitigation techniques. If you apply all of the mitigation techniques described in this article to your circuit with all parasitic components included (Table 1), you can significantly reduce overshoot, undershoot and ringing (Figure 20).

Table 1. Summary of Parasitic Component Mitigation Techniques

Schematic of parasitic component and mitigation	Mitigation technique description
	Bulk capacitor bypassing VDRAIN to GND (with the ceramic capacitor as close to the MOSFET as possible)
	Bulk capacitor bypassing VDRAIN to SLA (with the ceramic capacitor as close to the MOSFET as possible)
	Snubbers added across high-side and low-side MOSFETs; if additional mitigation is needed, reduce the gate-driver current (increasing the rise or fall time)

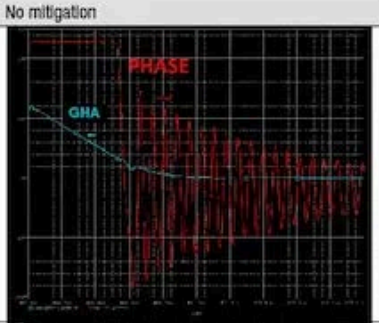
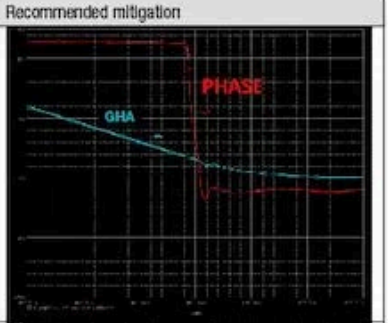
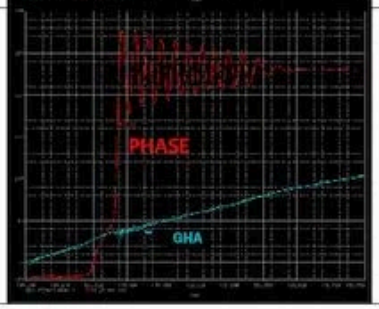
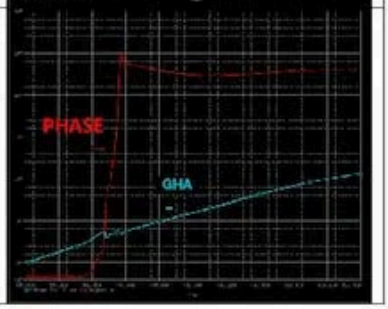
Phase	No mitigation	Recommended mitigation
Falling edge		
Rising edge		

Figure 20. Mitigating all parasitic components using the outlined methods

This was a particularly fun exercise for me, because it gave me a great opportunity to try out the schematic and simulation capabilities of the PSpice for TI simulation tool. These simulations are much easier and quicker to do than physical board experiments and can provide great insights into what to do when you encounter real-world problems with board parasitics.

If you want to learn more about PSpice for TI you can read the technical article How to Simulate Complex Analog Power and Signal-Chain Circuits with PSpice for TI or watch the video training series PSpice for TI: Introduction. For further information on TI motor drivers, training, and resources please visit the motor drivers product page.

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