**1.Direct mapped caches**

How many bytes of data can our cache hold? How many words?



***8bytes and 2words.***

2. Fill in the “Tag bits, Index bits, Offset bits” with the correct T:I:O breakdown according to the diagram.

***Index bits = log2(2) = 1***

***Offset bits = log2(4) = 2***

***Tag bits = 32 – 1 – 2 = 29***

3. Let’s say we have a 8192KiB cache with an 128B block size, what is the tag, index, and offset of 0xFEEDF00D?



***Number of blocks in cache = 8192KiB / 128B = 65536***

***Tag = (0xFEEDF00D / 128) / 65536 = 509 = 0x1FD***

***Index = (0xFEEDF00D / 128) % 65536 = 56288 = 0xDBE0***

***Offset = 0xFEEDf00D % 128 = 13 = 0xD***

4. Fill in the table below. Assume we have a write-through cache, so the number of bits per row includes only the cache data, the tag, and the valid bit.



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Address size(bits) | Cache size | Block size | Tag bits | Index bits | Offset bits | Bits per row |
| 16 | 4KiB | 4B | ***Log2((2^16/4)/(4KiB/4B))=4*** | ***Log2(4KiB/4B)=10*** | ***Log2(4)=2*** | ***4\*8+4+1=37*** |
| 32 | 32KiB | 16B | ***Log2((2^32/16)/(32KiB/16B))=17*** | ***Log2(32KiB/16B)=11*** | ***Log2(16)=4*** | ***16\*8+17+1=146*** |
| 32 | ***2^32B/2^16=64KiB*** | ***64KiB/2^12=16B*** | 16 | 12 | ***Log2(16)=4*** | ***16\*8+16+1=145*** |
| 64 | 2048KiB | ***2048KiB/2^14=128B*** | ***Log2(2^64B/2048KiB)=43*** | 14 | ***Log2(128)=7*** | 1068 |

5.Let’s say you have a byte-addressed computer with a total memory of 1MiB. It features a 16KiB CPU cache with 1KiB blocks.

1）. How many bits make up a memory address on this computer?

2）. What is the T:I:O breakdown? tag bits: 6 index bits: 4 offset bits:

***1)log2(1MiB/1B)=20***

***2)O=log2(1KiB/1B)=10***

6. Given CPU base CPI = 1, clock rate = 4GHz Miss rate/instruction = 2%

Main memory access time = 100ns，With just primary cache，what is Average memory access time (AMAT)？

***AMAT = 1 / 4GHz + 2% \* 100ns = 2.25ns***

7. CPU with 1ns clock, hit time = 1 cycle, miss penalty = 20 cycles, I-cache miss rate = 5%，what is Average memory access time (AMAT)？

***AMAT = (1 + 5% \* 20) \* 1ns = 2ns***

8. Given，I-cache miss rate = 2%，D-cache miss rate = 4%，Miss penalty = 100 cycles

Base CPI (ideal cache) = 2，Load & stores are 36% of instructions，what is Actual CPI

***Actual CPI = 2 + (2% + 36% \* 4%) \* 100 = 5.44***