5.2.1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| word address | binary address = word address \* 4 | tag = word address / 4 | index = word address % 4 | hit or miss |
| 3 | 0x0000000C | 0x0 | 0x3 | miss |
| 180 | 0x000002D0 | 0xB | 0x4 | miss |
| 43 | 0x000000AC | 0x2 | 0xB | miss |
| 2 | 0x00000008 | 0x0 | 0x2 | miss |
| 191 | 0x000002FC | 0xB | 0xF | miss |
| 88 | 0x00000160 | 0x5 | 0x8 | miss |
| 190 | 0x000002F8 | 0xB | 0xE | miss |
| 14 | 0x00000038 | 0x0 | 0xE | miss |
| 181 | 0x000002D0 | 0xB | 0x4 | miss |
| 44 | 0x000000B0 | 0x2 | 0xC | miss |
| 186 | 0x000002E8 | 0xB | 0xA | miss |
| 253 | 0x000003F4 | 0xF | 0xD | miss |

5.2.5

My solution is to increase the block size. The disadvantage of it is that it increases penalty and it may be not able to decrease the miss rate.

5.5.1

miss rate = 2B / 32B = 1 / 16

It’s not sensitive to the size of the cache or the working set; It’s sensitive to block size and access pattern based on the 3C model.

5.7.1

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| word address | binary address = word address \* 4 | tag = word address / 4 | index = word address % 4 / 2 | hit or miss | way 0 | way 1 | way 2 |
| 3 | 0x0000000C | 0x0 | 0x1 | miss | T(0x1)=0x0 |  |  |
| 180 | 0x000002D0 | 0xB | 0x2 | miss | T(0x1)=0x0  T(0x2)=0xB |  |  |
| 43 | 0x000000AC | 0x2 | 0x5 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2 |  |  |
| 2 | 0x00000008 | 0x0 | 0x1 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2 | T(0x1)=0x0 |  |
| 191 | 0x000002FC | 0xB | 0x7 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB | T(0x1)=0x0 |  |
| 88 | 0x00000160 | 0x5 | 0x4 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5 | T(0x1)=0x0 |  |
| 190 | 0x000002F8 | 0xB | 0x7 | hit | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5 | T(0x1)=0x0 |  |
| 14 | 0x00000038 | 0x0 | 0x7 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5 | T(0x1)=0x0  T(0x7)=0x0 |  |
| 181 | 0x000002D0 | 0xB | 0x2 | hit | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5 | T(0x1)=0x0  T(0x7)=0x0 |  |
| 44 | 0x000000B0 | 0x2 | 0x6 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5  T(0x6)=0x2 | T(0x1)=0x0  T(0x7)=0x0 |  |
| 186 | 0x000002E8 | 0xB | 0x5 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5  T(0x6)=0x2 | T(0x1)=0x0  T(0x7)=0x0  T(0x5)=0xB |  |
| 253 | 0x000003F4 | 0xF | 0x6 | miss | T(0x1)=0x0  T(0x2)=0xB  T(0x5)=0x2  T(0x7)=0xB  T(0x4)=0x5  T(0x6)=0x2 | T(0x1)=0x0  T(0x7)=0x0  T(0x5)=0xB  T(0x6)=0xF |  |