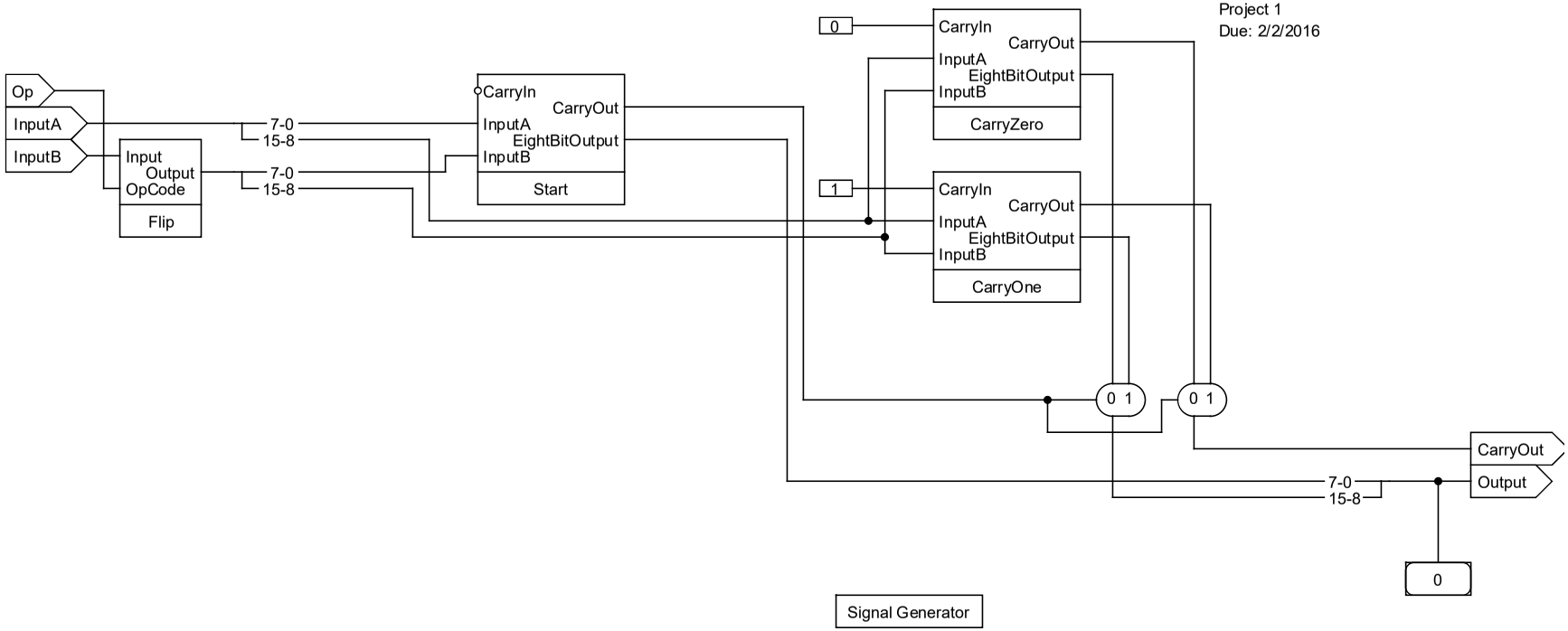
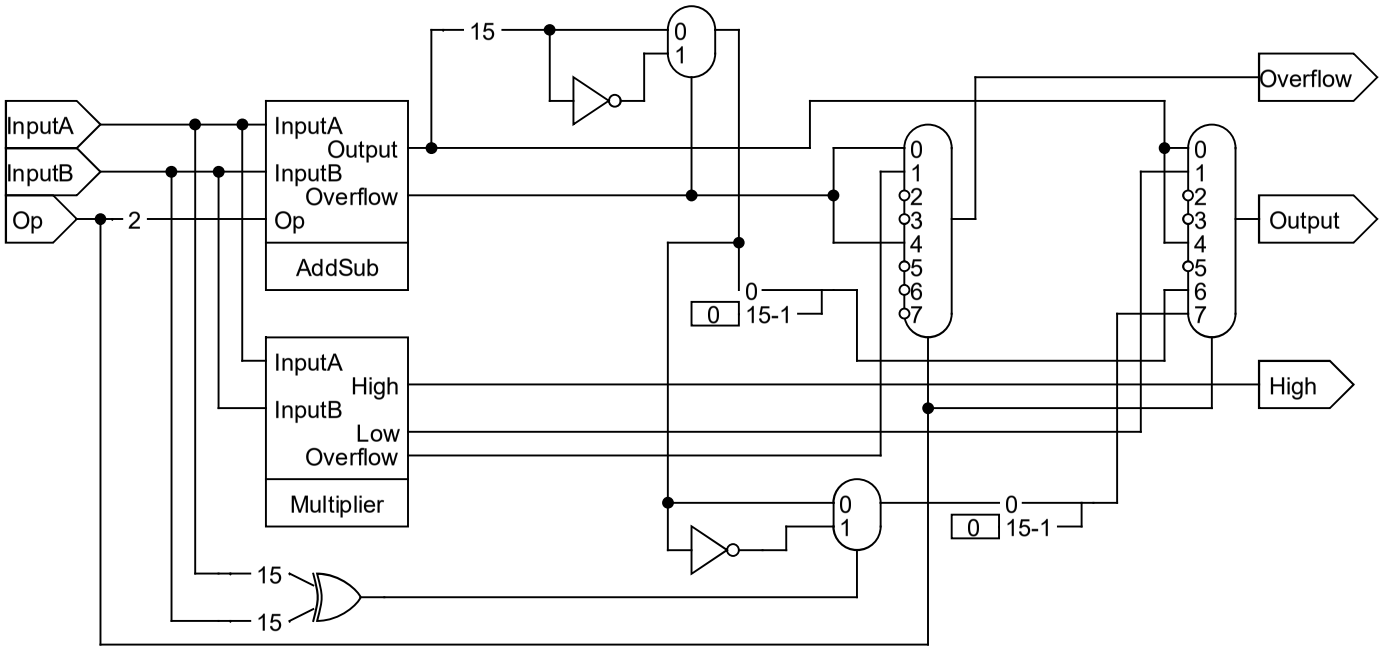
AdderSubtractor

Gage Vander Clay, Bob Heine
AdderSubtractor.jls
Project 1
Due: 2/2/2016



ALU



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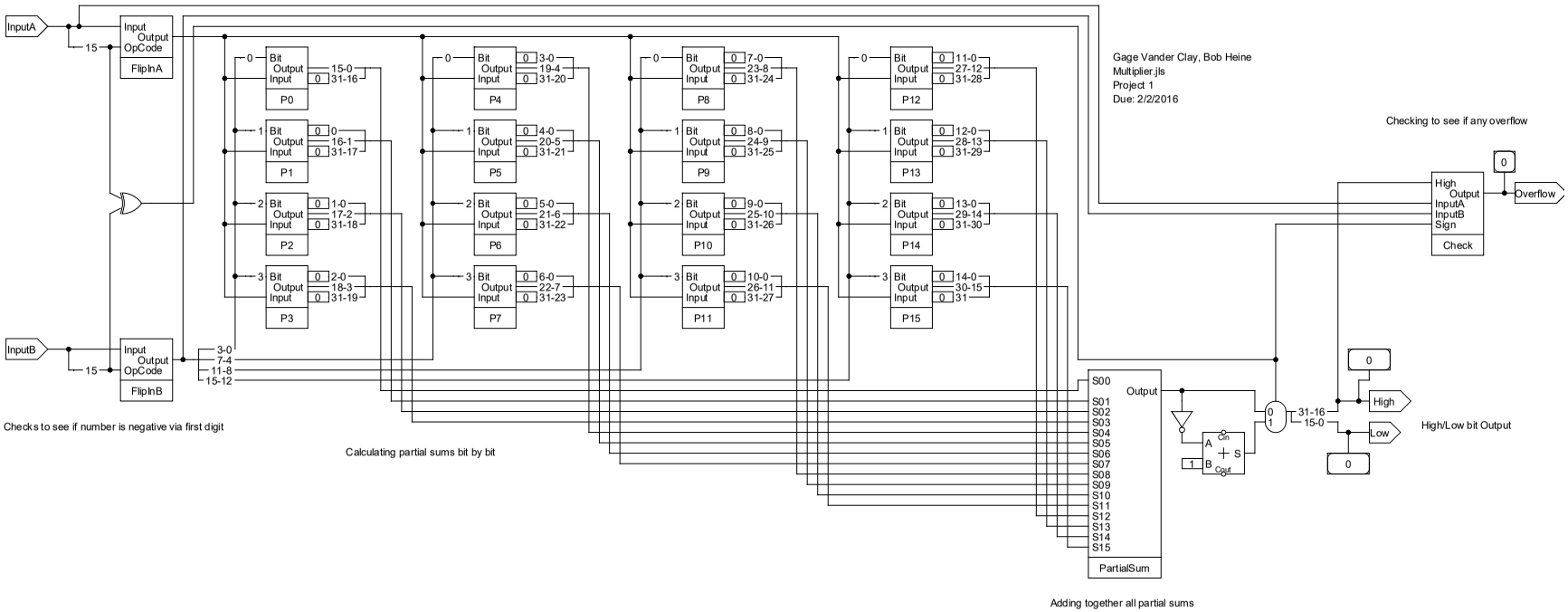
Signal Generator

Multiplier


InputA
InputB
Input
Output
OpCode
FlipInA
FlipInB
15
Bit
Output
Input
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
15-0
31-16
16-1
17-2
18-3
19-4
20-5
21-6
22-7
23-8
24-9
25-10
26-11
27-12
28-13
29-14
30-15
3-0
7-4
11-8
15-12
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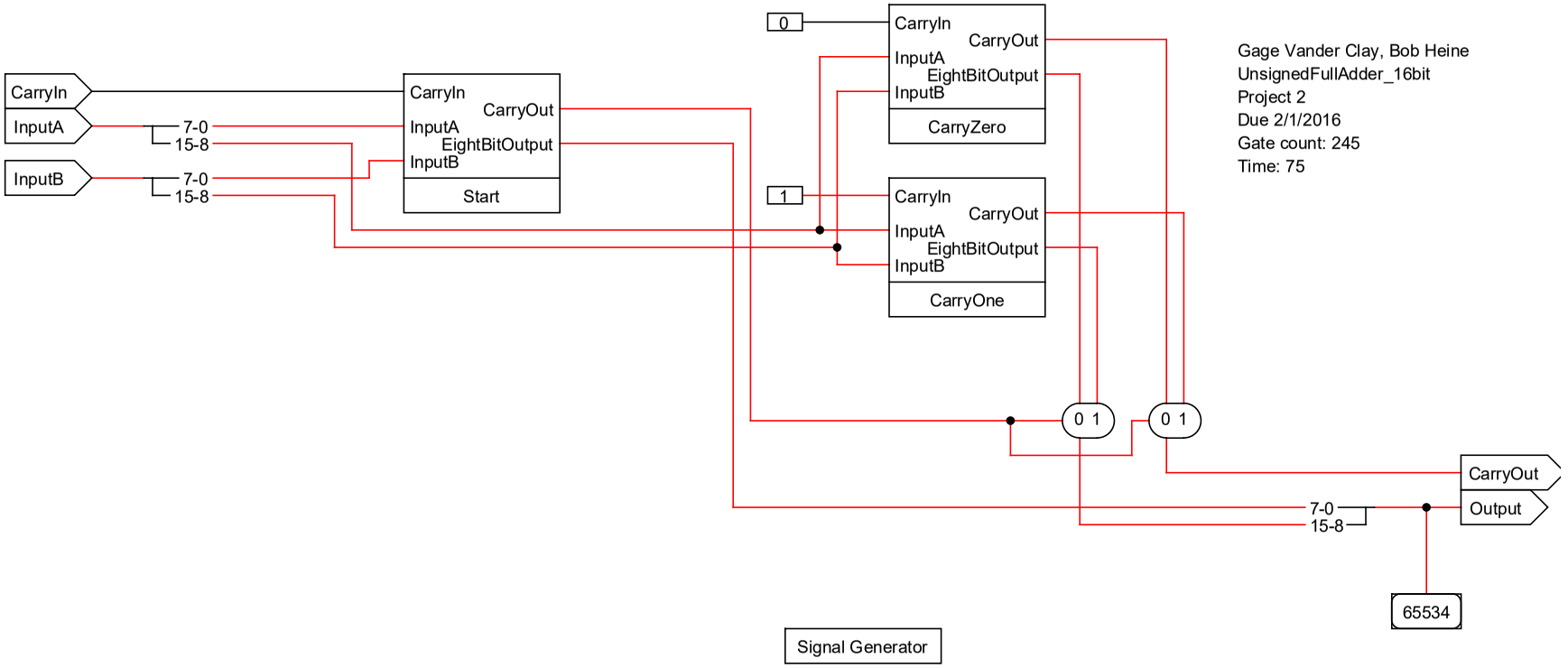
Multiplier.jls
Project 1
Due: 2/2/2016
Checking to see if any overflow
High
InputA
InputB
Sign
Check
Overflow
Checks to see if number is negative via first digit
Calculating partial sums bit by bit
S00
S01
S02
S03
S04
S05
S06
S07
S08
S09
S10
S11
S12
S13
S14
S15
PartialSum
Adding together all partial sums
Cin
Cout
31-16
15-0
Low
High/Low bit Output

UnsignedFullAdder_16bit