Georgios Vavouliotis

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Research Interests

Computer Architecture, High Performance Computing, Machine Learning for Computer Architecture, **Data Centers;** identifying and exploiting the predictability of programs to design μ architectural prefetching and prediction mechanisms for the cache and the TLB hierarchy, improving cache/TLB management for emerging applications with large data and code footprints, leveraging machine learning algorithms to design intelligent μ architectural components, and re-thinking μ architectural designs for server and data center applications.

Education

Universitat Politècnica de Catalunya (UPC)

Barcelona

Doctor of Philosophy (Ph.D.), Advisors: Dr. Marc Casas, Dr. Lluc Alvarez Advanced Hardware Prefetching in Virtual Memory Systems (Cum Laude Award) Sept 2018-Dec 2022

National Technical University of Athens (NTUA)

Athens

Diploma (M.Eng.) on Electrical & Computer Engineering (M.Sc. equivalent), GPA: 8.9/10 2012-March 2018

Academic Directions.....

- Computer Systems & Software
- Computer Networks and Networks Security
- Signal Processing, Automatic Control and Robotics

Employment

Huawei Zurich Research Center	Zurich
	E / 2222

Feb 2023-now Postdoctoral Researcher

Huawei Zurich Research Center Zurich Research Internship Nov 2021-April 2022

Impact of Concurrent Java Garbage Collectors on Cache Locality

Barcelona Supercomputing Center (BSC-CNS) Barcelona Researcher at Computer Architecture & Operating Systems Group Sept 2018-Dec 2022

National Technical University of Athens (NTUA) **Athens** Research Student at Computer Systems Laboratory (CSLab) Feb 2018-July 2018

Honors and Awards

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0	Cum Laude Ph.D. Award For my Ph.D. dissertation entitled Advanced Hardware Prefetching in Virtual Memory Systems	Spain 2023
0	Hisilicon Core Star Award (awarded by Huawei) For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper	Shenzhen 2023
0	Best Paper Award - ISMM 2023 For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper	Orlando 2023
0	HiPEAC 2022 Paper Award For the Page Size Aware Cache Prefetching paper	Chicago 2022
0	Travel Grant for MICRO'22 MICRO 2022 Conference	Chicago 2022
0	Travel Grant for ISCA'22	New York

ISCA 2022 Conference 2022

HiPEAC 2021 Paper Award Virtual

For the Morrigan: A Composite Instruction TLB Prefetcher paper 2021

HiPEAC 2021 Paper Award Virtual For the Exploiting Page Table Locality for Agile TLB Prefetching paper 2021

Best Poster Award

2021 ACM School on HPC Computer Architectures for AI and Dedicated Applications

2021

2019 FPI Doctoral Fellowship

Barcelona

Funded by Spanish Government (MINECO)

2019-2022

Travel Grant for ASPLOS'20

Lausanne/Virtual

ASPLOS 2020 Conference

2020

Mathematics Award - National Technical University of Athens (NTUA)

Excellent marks in all mathematical courses during the first two (2) years.

Athens 2014

"The Great Moment of Education" Eurobank EFG Scholarship

Chalkida

Highest rank in National Qualifications Exams in my school

Chalkida 2012

Peer-Reviewed Conference Publications

- [1] Alexandre Valentin Jamet, **Georgios Vavouliotis**, Lluc Alvarez, Daniel A. Jiménez, Marc Casas, A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering (to appear). Proceedings of the 30th International Symposium on High-Performance Computer Architecture (HPCA), Edinburgh, March 2024.
- [2] Maria Carpen-Amarie, **Georgios Vavouliotis**, Konstantinos Tovletoglou, Boris Grot, Rene Mueller, Concurrent GCs and Modern Java Workloads: A Cache Perspective. Proceedings of the 2023 ACM SIGPLAN International Symposium on Memory Management (ISMM), Orlando, June 2023. [Best Paper Award]
- [3] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, Page Size Aware Cache Prefetching. Proceedings of the 55th IEEE/ACM International Symposium on Microarchitecture (MICRO), Chicago, Oct 2022.
- [4] **Georgios Vavouliotis**, Lluc Alvarez, Boris Grot, Daniel A. Jiménez, Marc Casas, *Morrigan: A Composite Instruction TLB Prefetcher*. Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Virtual, Oct 2021.
- [5] **Georgios Vavouliotis**, Lluc Alvarez, Vasileios Karakostas, Konstantinos Nikas, Nectarios Koziris, Daniel A. Jiménez, Marc Casas, *Exploiting Page Table Locality for Agile TLB Prefetching*. Proceedings of the 48th International Symposium on Computer Architecture (ISCA), Virtual, June 2021. Also presented as a *Poster* at the 49th International Symposium on Computer Architecture (ISCA), New York, June 2022.

Peer-Reviewed Journal/Workshop Publications and Posters

- [1] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, *Leveraging Page Size Information to Enhance Data Cache Prefetching*. Poster at the 2021 ACM Summer School on HPC Computer Architectures for Al and Dedicated Applications, Virtual, Aug 2021. [Best Poster Award]
- [2] **Georgios Vavouliotis**, Lluc Alvarez, Marc Casas, *Pushing the envelope on free TLB prefetching*. Proceedings of the 8th BSC Doctoral Symposium, Virtual, May 2021.
- [3] **Georgios Vavouliotis**, *Cost-Effective Instruction TLB Prefetching*. Second Young Architect Workshop (YArch 2020). In conjunction with The 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Virtual, March 2020.

Dissertations

[1] **Georgios Vavouliotis** "Advanced Hardware Prefetching in Virtual Memory Systems". Book of my Doctoral dissertation.

Thesis Statement: Hardware TLB prefetching can reduce the address translation overheads posed with applications with large data and code footprints while exploiting address translation metadata available at the microarchitecture and runtime levels can improve the performance of cache prefetchers.

[2] **Georgios Vavouliotis**, Goumas Georgios, "Performance Analysis of TLB Prefetching Mechanisms". Book of my Diploma thesis (in Greek).

Invited Talks

Page Size Aware Cache Prefetching 55th IEEE/ACM International Symposium on Microarchitecture (MICRO)	Chicago Oct 2022
Morrigan: A Composite Instruction TLB Prefetcher Huawei Zurich Research Center	Zurich Dec 2021
Morrigan: A Composite Instruction TLB Prefetcher 54th IEEE/ACM International Symposium on Microarchitecture (MICRO)	Virtual Oct 2021
Leveraging Page Size Information to Enhance Data Cache Prefetching ACM School on HPC Computer Architectures for AI and Dedicated Applications	Virtual Aug 2021
Exploiting Page Table Locality for Agile TLB Prefetching 48th International Symposium on Computer Architecture (ISCA)	Virtual June 2021
Pushing the Envelope on Free TLB Prefetching 8th BSC Doctoral Symposium	Virtual <i>May 2021</i>
Professional Activities - Leadership & Service	
European Conference on Parallel and Distributed Computing (Euro-Par'24) Program Committee (PC) member	Madrid 2023-2024
International Symposium on High-Performance Computer Architecture (HPCA'24) Artifact Evaluation Committee member	Edinburgh 2023-2024
International Symposium on Computer Architecture (ISCA'24) Website Co-Chair	Buenos Aires 2023-2024
Technical Reviewer for Conferences and Journals	
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 European Conference on Parallel and Distributed Computing (Euro-Par'24) International Symposium on High-Performance Computer Architecture (HPCA'24)-Artif Journal of Parallel and Distributed Computing (JPDC'23) IEEE Access 2023 ACM Transactions on Architecture and Code Optimization (TACO'23) IEEE Supercomputing Conference (SC'21) IEEE Transactions on Computers (2021) ACM International Conference on Computing Frontiers (CF'21) 	act Evaluation
 European Conference on Parallel and Distributed Computing (Euro-Par'24) International Symposium on High-Performance Computer Architecture (HPCA'24)-Artif Journal of Parallel and Distributed Computing (JPDC'23) IEEE Access 2023 ACM Transactions on Architecture and Code Optimization (TACO'23) IEEE Supercomputing Conference (SC'21) IEEE Transactions on Computers (2021) ACM International Conference on Computing Frontiers (CF'21) 	act Evaluation
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