Georgios Vavouliotis

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Research Interests

Computer Architecture, High Performance Computing, Machine Learning and Artificial Intelligence for Computer Architecture, Data Centers; identify and exploit the predictability of programs to co-design μarchitectural prefetching and prediction mechanisms for the memory hierarchy, re-think cache management for emerging application domains, leverage ML/AI algorithms to design intelligent microarchitectural components, and develop novel microarchitectural designs tailored to the needs of server and datacenter applications.

Education

Doctor of Philosophy (Ph.D.) — **Barcelona**
Universitat Politècnica de Catalunya (UPC) — *Sept 2018-Dec 2022*
Dissertation: "Advanced Hardware Prefetching in Virtual Memory Systems" (Cum Laude Award)
Advisors: Dr. Marc Casas, Dr. Lluc Alvarez

Diploma on Electrical & Computer Engineering (M.Sc. equivalent) — **Athens**
National Technical University of Athens (NTUA), GPA: 8.9/10 — *Sept 2012-March 2018*
Diploma Thesis: *"Performance Analysis of TLB Prefetching Mechanisms"*
Advisors: Dr. Vasileios Karakostas, Dr. Georgios Goumas

Employment

Senior Researcher (CPU Microarchitecture) — **Zurich**
Huawei Technologies Switzerland AG, Zurich Research Center — *April 2024–now*

- Performance modeling of microarchitectural features using in-house cycle-accurate simulation infrastructure to guide optimizations for next-generation Huawei cores.
  - Led the development and contributed to the integration of one (1) performance feature and one (1) power feature in Huawei cores.
- Collaborating with research and product teams in the UK, Israel, and China.
- Chartering research projects and ensure alignment with product teams.
- Leading the collaboration with Barcelona Supercomputing Center on synergistic cache management and cache prefetching strategies for emerging applications.
- Authored papers published at HPCA 2025 and ASPLOS 2025, and filed patents on hardware prefetching and cache management as lead inventor.

Postdoctoral Researcher (CPU Microarchitecture) — **Zurich**
Huawei Technologies Switzerland AG, Zurich Research Center — *Feb 2023–Feb 2024*

- Led in-depth research on hardware prefetching and its interaction with the virtual-memory subsystem, using both internal cycle-accurate simulators and open-source frameworks.
- Analyzed prefetching models and coordination schemes across Huawei products, driving proposals for next-generation prefetcher designs in Huawei cores.
- Led collaboration with Barcelona Supercomputing Center on ML-based hardware prediction and memory management for graph-processing applications.
- Co-authored two papers published at HPCA 2024 and IPDPS 2024 and filed a patent on off-chip prediction.

Research Intern (Memory Management) — **Zurich**
Huawei Technologies Switzerland AG, Zurich Research Center — *Nov 2021–April 2022*

- Researched the impact of Concurrent Java Garbage Collectors (e.g., ZGC) on cache locality of modern microarchitectures
- Authored a paper published at ISMM 2023 [Best Paper Award 🏆]

Researcher (Computer Architecture & Operating Systems) — **Barcelona**
Barcelona Supercomputing Center (BSC-CNS) — *Sept 2018–Dec 2022*

- Carried out research on address translation, speculation mechanisms for microarchitecture, and interaction between computer architecture and artificial intelligence
- Contributed to the writing of research proposals for international grants
- Contributed to collaborative projects on cache management and off-chip prediction

Honors and Awards

- **Innovation Award (by Huawei)** — **Zurich**
  For contributing to the development of a performance feature landed in Huawei cores — *2025*
- **Skyline Award (by Huawei)** — **Zurich**
  For the Instruction-Aware Cooperative TLB and Cache Replacement Policies paper — *2025*
- **Skyline Award (by Huawei)** — **Zurich**
  For the To Cross, or Not to Cross Pages for Prefetching? paper — *2025*
- **Future Star Award** — **Zurich**
  For my research contributions to microarchitectural designs of Huawei CPU cores — *2025*
- **Skyline Award (by Huawei)** — **Zurich**
  For the A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering paper — *2024*
- **HiPEAC 2024 Paper Award** — **Edinburgh**
  For the A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering paper — *2024*
- **Core Star Award (by Huawei)** — **Zurich**
  For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper — *2023*
- **Cum Laude Ph.D. Award** — **Spain**
  For my Ph.D. dissertation entitled Advanced Hardware Prefetching in Virtual Memory Systems — *2023*
- **Best Paper Award - ISMM 2023** — **Orlando**
  For the Concurrent GCs and Modern Java Workloads: A Cache Perspective paper — *2023*
- **HiPEAC 2022 Paper Award** — **Chicago**
  For the Page Size Aware Cache Prefetching paper — *2022*
- **Travel Grant for ISCA'22** — **New York**
  ISCA 2022 Conference — *2022*
- **HiPEAC 2021 Paper Award** — **Virtual**
  For the Morrigan: A Composite Instruction TLB Prefetcher paper — *2021*
- **HiPEAC 2021 Paper Award** — **Virtual**
  For the Exploiting Page Table Locality for Agile TLB Prefetching paper — *2021*
- **Best Poster Award** — **Virtual**
  2021 ACM School on HPC Computer Architectures for AI and Dedicated Applications — *2021*
- **2019 FPI Doctoral Fellowship** — **Barcelona**
  Funded by Spanish Government (MINECO) — *2019-2022*
- **Travel Grant for ASPLOS'20** — **Lausanne/Virtual**
  ASPLOS 2020 Conference — *2020*
- **Mathematics Award - National Technical University of Athens** — **Athens**
  Excellent marks in all mathematical courses during the first two years. — *2014*
- **"The Great Moment of Education" Eurobank EFG Scholarship** — **Chalkida**
  Highest rank in National Qualifications Exams in my school — *2012*

Peer-Reviewed Conference Publications

[1] **Georgios Vavouliotis***, Dimitrios Chasapis*, Daniel A. Jiménez, Marc Casas, Instruction-Aware Cooperative TLB and Cache Replacement Policies. Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Rotterdam, April 2025.

[2] **Georgios Vavouliotis**, Marti Torrents, Boris Grot, Kleovoulos Kalaitzidis, Leeor Peled, Marc Casas, To Cross, or Not to Cross Pages for Prefetching?. Proceedings of the 31st International Symposium on High-Performance Computer Architecture (HPCA), Las Vegas, March 2025.

[3] Alexandre Valentin Jamet, **Georgios Vavouliotis**, Lluc Alvarez, Daniel A. Jiménez, Marc Casas, Practically Tackling Memory Bottlenecks of Graph-Processing Workloads. Proceedings of the 38th IEEE International Parallel & Distributed Processing Symposium (IPDPS), San Francisco, May 2024.

[4] Alexandre Valentin Jamet, **Georgios Vavouliotis**, Lluc Alvarez, Daniel A. Jiménez, Marc Casas, A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering. Proceedings of the 30th International Symposium on High-Performance Computer Architecture (HPCA), Edinburgh, March 2024.

[5] Maria Carpen-Amarie, **Georgios Vavouliotis**, Konstantinos Tovletoglou, Boris Grot, Rene Mueller, Concurrent GCs and Modern Java Workloads: A Cache Perspective. Proceedings of the 2023 ACM SIGPLAN International Symposium on Memory Management (ISMM), Orlando, June 2023. [Best Paper Award 🏆]

[6] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, Page Size Aware Cache Prefetching. Proceedings of the 55th IEEE/ACM International Symposium on Microarchitecture (MICRO), Chicago, Oct 2022.

[7] **Georgios Vavouliotis**, Lluc Alvarez, Boris Grot, Daniel A. Jiménez, Marc Casas, *Morrigan: A Composite Instruction TLB Prefetcher*. Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Virtual, Oct 2021.

[8] **Georgios Vavouliotis**, Lluc Alvarez, Vasileios Karakostas, Konstantinos Nikas, Nectarios Koziris, Daniel A. Jiménez, Marc Casas, *Exploiting Page Table Locality for Agile TLB Prefetching*. Proceedings of the 48th International Symposium on Computer Architecture (ISCA), Virtual, June 2021. Also presented as a *Poster* at the 49th International Symposium on Computer Architecture (ISCA), New York, June 2022.

Peer-Reviewed Journal/Workshop Publications and Posters

[1] **Georgios Vavouliotis**, Gino Chancon, Lluc Alvarez, Paul V. Gratz, Daniel A. Jiménez, Marc Casas, *Leveraging Page Size Information to Enhance Data Cache Prefetching*. Poster at the 2021 ACM Summer School on HPC Computer Architectures for AI and Dedicated Applications, Virtual, Aug 2021. [Best Poster Award 🏆]

[2] **Georgios Vavouliotis**, Lluc Alvarez, Marc Casas, *Pushing the envelope on free TLB prefetching*. Proceedings of the 8th BSC Doctoral Symposium, Virtual, May 2021.

[3] **Georgios Vavouliotis**, *Cost-Effective Instruction TLB Prefetching*. Second Young Architect Workshop (YArch 2020). In conjunction with The 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Virtual, March 2020.

Patents

[1] "PATENT ON SYNERGISTIC CACHE MANAGEMENT" [pending]
[2] "PATENT ON HARDWARE PREFETCH FILTERING" [pending]
[3] "PERCEPTRON-BASED OFF-CHIP PREDICTOR", Alexandre Valentin Jamet, **Georgios Vavouliotis**, Marc Casas, Filed: 21/12/2023

Dissertations

[1] **Georgios Vavouliotis** *"Advanced Hardware Prefetching in Virtual Memory Systems"*. Book of my Doctoral dissertation. [Cum Laude Award 🎗]

> **Thesis Statement:** *Hardware TLB prefetching can reduce the address translation overheads posed with applications with large data and code footprints while exploiting address translation metadata available at the microarchitecture and runtime levels can improve the performance of cache prefetchers.*

[2] **Georgios Vavouliotis**, Goumas Georgios, *"Performance Analysis of TLB Prefetching Mechanisms"*. Book of my Diploma thesis (in Greek).

Invited Talks

- **Importance of Single-Thread Performance in the Many-Core Era** — **Buenos Aires**
  SPARKS Workshop (ISCA 2024) — *July 2024*
- **Microarchitectural Prediction and Prefetching in Virtual Memory Systems** — **Online**
  AMD Research — *May 2024*
- **Advanced Hardware Prefetching in Virtual Memory Systems** — **Athens**
  6th Computing Systems Research Day @ CSLab — *Jan 2023*
- **Page Size Aware Cache Prefetching** — **Chicago**
  55th IEEE/ACM International Symposium on Microarchitecture (MICRO) — *Oct 2022*
- **Morrigan: A Composite Instruction TLB Prefetcher** — **Zurich**
  Huawei Zurich Research Center — *Dec 2021*

- **Morrigan: A Composite Instruction TLB Prefetcher** — **Virtual**
  54th IEEE/ACM International Symposium on Microarchitecture (MICRO) — *Oct 2021*
- **Leveraging Page Size Information to Enhance Data Cache Prefetching** — **Virtual**
  ACM School on HPC Computer Architectures for AI and Dedicated Applications — *Aug 2021*
- **Exploiting Page Table Locality for Agile TLB Prefetching** — **Virtual**
  48th International Symposium on Computer Architecture (ISCA) — *June 2021*
- **Pushing the Envelope on Free TLB Prefetching** — **Virtual**
  8th BSC Doctoral Symposium — *May 2021*

Technical Reviewer for Conferences and Journals

- **International Symposium on High-Performance Computer Architecture (HPCA'26)**
- **IEEE Micro**
- **ACM Transactions on Architecture and Code Optimization (TACO'25)**
- **International Symposium on Microarchitecture (MICRO'25)**
- **International Symposium on Computer Architecture (ISCA'25)**
- **International Symposium on High-Performance Computer Architecture (HPCA'25)**
- **IEEE Micro**
- **International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'25)**
- **International Symposium on Microarchitecture (MICRO'24)**
- **International Symposium on Computer Architecture (ISCA'24)**
- **ACM Transactions on Architecture and Code Optimization (TACO'24)**
- **European Conference on Parallel and Distributed Computing (Euro-Par'24)**
- **International Symposium on High-Performance Computer Architecture (HPCA'24, Artifact Evaluation)**
- **Journal of Parallel and Distributed Computing (JPDC'23)**
- **IEEE Access 2023**
- **ACM Transactions on Architecture and Code Optimization (TACO'23)**
- **IEEE Supercomputing Conference (SC'21)**
- **IEEE Transactions on Computers (2021)**
- **ACM International Conference on Computing Frontiers (CF'21)**

Professional Activities - Leadership & Service

- **ISCA'24** — **Buenos Aires**
  Website Chair — *2024*

Teaching Experience

- **Private Tutor** — **Athens**
  C programming, Computer Architecture, Automatic Control for undergraduate students — *2013–2018*
- **Lab Assistant at National Technical University of Athens (NTUA)** — **Athens**
  C programming — *2013-2017*

Selected Press

- **TCuArch Interview** — **youtube**
  What attracted you to research computer architecture and systems? — *Dec 2022*
- **Page Size Aware Cache Prefetching** — **easyperf.net**
  Oct Newsletter of easyperf.net – Among the Most Interesting MICRO '22 Papers — *Oct 2022*

Languages

- Greek (Native)
- English
- Italian (Beginner)
- Spanish (Beginner)