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E344 Assignment 1

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Report submitted in partial fulfilment of the requirements of the module Design (E) 344 for the degree Baccalaureus in Engineering in the Department of Electrical and Electronic Engineering at Stellenbosch University.

July 25, 2022

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G. Allen Voorletters en van / *Initials and surname*	July 25, 2022 Datum / *Date*

Contents

List of Figures

List of Tables

Nomenclature

Variables and functions

V_{ss}	Voltage positive.
V_{dd}	Voltage negative.

Acronyms and abbreviations

CMRR	Common Mode Rejection Ratio
RC	Resistor Capacitor

Chapter 1

Literature review

The following study presents an overview of the current configurations and design techniques for both operational amplifier and current-sensing circuits. Operational amplifiers limitations are considered, as well as the system requirements. These findings are then discussed to ensure there is enough information to aid the design process, which is followed by simulations.

1.1. Operational amplifiers

Limitations

Often, it is applicable to design an amplifier using the ideal operational amplifier model, however this may be inadequate in low voltage, high current or high frequency environments. The following are common limitations of non-ideal op-amps [1]:

- Voltage supply saturation. For given k, output cannot go above $V_{ss} - k$ or below $V_{dd} + k$.
- Finite bandwidth. The signal starts to cut-off at high frequencies, which can be calculated using t he gain-bandwidth product equation.
- Offset voltage/bias current. Even with no input, there exists a small "offset voltage" and "bias current" into the amplifier. This results in unwanted voltage at the output.
- Finite slew rate. The output cannot change quicker than a specific rate. This is different to the high-cutoff, but has a similar limiting effect.
- Finite common-mode rejection ratio (CMRR). An op-amp should only amplify $V_+ - V_-$, but also amplifies the unwanted common signal (e.g. noise) on both inputs.

Considerations

System requirements should first be considered in order to attain an overview of the specifications:

- The output range of the circuit should be from 0.1 to 3 V. Since a low-side current-sense resistor will be used, this means initial measurements will be at a lower voltage initially.
- The step response of the circuit should reach 90% of its output in less than 100 ms. The op-amps slew rate should be analyzed to ensure this condition is met.

- Noise above 1 kHz should be filtered out such that a 10 mV, 1 kHz signal at the input is less than 250 mV at the output. Filter options should therefore be researched.

It is clear that voltage supply saturation, slew rate and CMRR are the main parameters to be considered. A filter circuit should also be designed for noise specifications.

MCP6242

The op-amp used in this project is the MCP6242. Listed below are its notable parameters [2]:

- Typical CMMR of 75 dB (DC) to 65 dB (1 kHz).
- Ability to output between 0.035 and 5.465 V if $V_{ss} = 6$ V and $V_{dd} = 0$ V
- Slew rate of 0.3 V/uS.

Configurations

A number of well-known op-amp configurations exist that all achieve slightly different amplification goals. The following list compares common configurations [3] which may achieve this project's goal of amplifying a small-signal voltage across a resistor. The figures below also include a modified non-inverting amplifier to allow for input signal filtering:

Type	Advantages	Disadvantages
Non-inverting	- Simple to design and build - High input impedance	- Large input bias currents - Amplifies noise from input
Differential	- Good noise rejection - Flexible	- Complex design - Low input impedance
Instrumentation	- Same as differential - Very high input impedance	- Complex and expensive design

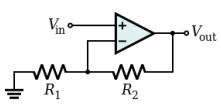

Figure 1.1: Non-inverting amplifier [3]

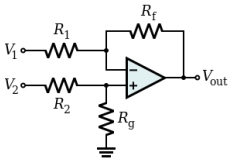

Figure 1.2: Differential amplifier [3]

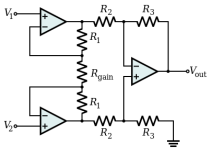

Figure 1.3: Instrumentation amplifier [3]

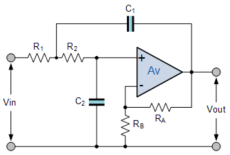

Figure 1.4: Modified non-inverting amplifier [4]

1.2. Current sensing

Chapter 2

Detail design

This process details the design process and calculations for the current sensor/amplifier circuit. It provides insight into what decisions were made and the justification behind these decisions.

2.1. Current sensor

Configuration

The differential amplifier configuration was will be used for this project for the following reasons:

- The configuration is specifically designed to reject common-mode noise, which the non-inverting amp suffers from.
- Only 1 op-amp is needed.
- The design is relatively simple compared to the instrumentation amplifier.

However, a modified version with two extra capacitors will be used. A capacitor will be added in parallel with R_f called C_f, and with R_g called C_g. It is important that these capacitors have the same value in order to preserve CMRR [3]. It is likely, however, that one of these will be dominant due to differing resistor values, and therefore the filter will only be considered as first-order. This is, however, acceptable due to the amps noise-rejecting capabilities.

Gain and Cutoff

Before calculating component values, both the cutoff frequency of the RC filter, and the DC gain of the amplifier, need to be determined. The gain of the amplifier should be determined such that, when the maximum current flows through the sense resistor, the maximum voltage is output.

First, the maximum current of the motor should be measured. This can be done by connecting the motor to a power supply (through an ammeter), stalling the motor, and reading the output current. With a supply voltage of 6.4 V connected, the motor for this project read 740 mA, however different motors may read between 1 and 1.5 A. The average running current, however, is between 200 mA and 300 mA. A value of $I_{max} = 1A$ will therefore be chosen to allow for more headroom and a slightly lower gain. Since a sense resistor of

10 mΩ is to be used, the maximum voltage through this resistor will therefore be 8 mV. A gain of $\frac{3V}{10mV} = 300$ is therefore chosen. Although this voltage level is small, it is expected seeing as the resistance value is so small, and is also desirable as it prevents the circuit "stealing" power from the motor itself.

The cutoff frequency f_H should be selected such that the slew rate requirements are not affected, while still adequately filtering a 1 kHz noise signal. In order for the noise requirement to be satisfied, the input signal must be attenuated by $20 \log \frac{300*10mV}{250mV} \approx 22dB$. This means the cutoff should be around 100 Hz (a decade below 1 kHz). Since the specification requires a change from 0.1 to $3 \times 0.9 = 2.7V$ in less than 100 ms, the output should be capable of oscillating at $\frac{1}{50ms} = 20Hz$, which is below the designed cutoff.

Since input current of the circuit needs to be limited below 150 uA, high resistor values should be chosen:

- Assuming $i_n = 0$, choose $\frac{V_{out(max)}}{R_1+R_f} << 150uA \therefore R_1 + R_f >> 20\,\text{k}\Omega$. Choose $R_f = 100\,\text{k}\Omega$.
- $G = \frac{R_f}{R_1} = 300 \therefore R_1 = 330\,\Omega$
- Choose $R_2 = R_1 = 330\,\Omega$ and $R_g = R_f = 100\,\text{k}\Omega$ for differential symmetry.
- Since R_{eq} of C_f is R_f and of C_g is $R_g||R_2$, it is clear that C_f is dominant, $\therefore C_f = \frac{1}{2\pi \cdot R_f \cdot 100Hz} \approx 15nF$. Also set $C_g = 15nF$ for symmetry. It should be noted, however, that this technique (using time constants) is not always valid - especially in complex circuits such as these - and so these results should be checked using simulations.

Circuit diagram

The following figure details the final circuit design for the sensor and amplifier system.

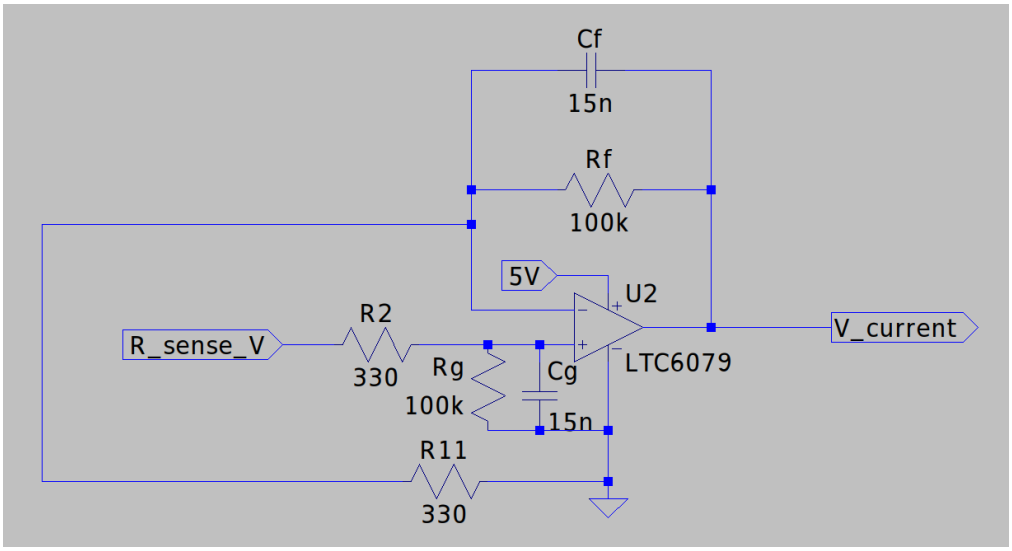

Figure 2.1: Circuit diagram of final configuration

As visible, a single +5 V and 0 V supply will be used. Although there are benefits to a dual rail supply, that would prove impractical in the context of the larger system.

Chapter 3

Results

After running initial simulations, it was clear that the constant assumed in the design stage for the dominant capacitor C_f was too high. The capacitor value was then experimentally increased until a satisfactory response which was reasonably below 250 mV (10-20%) was obtained. This section details the rest of the results of these simulations.

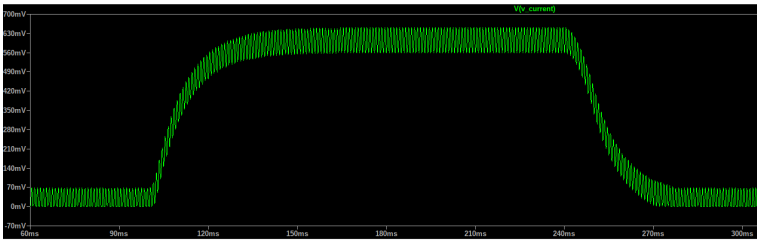

Figure 3.1: Amplifier output in response to step input

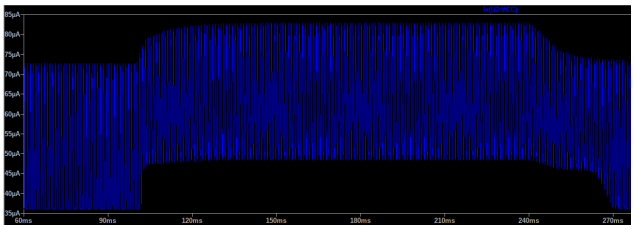

Figure 3.2: Current draw of op-amp

As can be seen, all specifications were adhered to:

- The noise level at idle is well below the 250 mV requirement.
- The step response input changes 20-25 ms, which is below the 100 ms requirement.
- The power draw of the circuit (as measure at the positive terminal of the op-amp) is less than 85 uA, which is much less than the specified 150 uA.

Lastly, the input simulation parameters were modified during testing to analyze the various output voltages for different input currents. For input currents of 400mA, 500mA, 800mA and 1A, the output voltages were 1.22V, 1.52, 2.43 and 3.024 V respectively. This matches perfectly with the initial design.

Bibliography

Appendix A

Social contract

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E-design 344 Social Contract

2022

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and a few paid helpers (Rita van der Walt, Keegan Hull, and Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth, that you are enabled to learn from the module, and demonstrate and be assessed on your skills. We commit to prepare the assignments, to set the assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

I, Gary Allen have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication online of supplementary videos on specific topics, I acknowledge that I am expected to attend the scheduled lectures to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Prof. MJ (Thinus) Booysen	Student number: 23905093
Signature: MJ Booysen Digitally signed by MJ Booysen Date: 2022.07.02 13:22:09 +02'00'	Signature:
Date: 1 July 2022	Date: 25 / 07 / 2022

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Appendix B

GitHub Activity Heatmap