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E344 Assignment 1

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Nomenclature

Variables and functions

V_{ss} Voltage positive.

V_{dd} Voltage negative.

Acronyms and abbreviations

CMRR	Common Mode Rejection Ratio
GBWP	Gain-Bandwidth Product
RC	Resistor-Capacitor
PWM	Pulse Width Modulation
LPF	Low Pass Filter
HPF	High Pass Filter
TTL	Transistor-Transistor Logic
MCU	Microcontroller Unit
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
AFE	Analog Front End
DSP	Digital Signal Processor

Chapter 1

Literature Review

1.1. Operational Amplifiers

1.1.1. Basic Principles

An operational amplifier or "op-amp" is a type of differential amplifier. Fundamentally, these amplifiers multiply the difference between the voltages at their positive (V^+) and negative (V^-) terminals by a specified gain factor. This gain, A_d , is also known as the *differential-mode gain*. Although differential amplifiers are often designed for a specific A_d , op-amps usually aim to have as high a differential gain as possible (for an ideal op-amp, $A_d \rightarrow \infty$).

A_d is also known as the *open-loop gain*. Due to a large-valued open-loop gain, op-amps are often used in *closed-loop* configurations, which are more flexible and take advantage of this large A_d . These configurations arise when there is a negative feedback loop from the output which is connected to the negative input terminal.

1.1.2. Limitations

Often, it is applicable to design an amplifier circuit using the ideal operational amplifier model. This model assumes no current into the input terminals, an infinite, linear, differential-mode gain, and that terminal voltage $V^+ = V^-$ when negative feedback is present. This model, however, may be inadequate in low voltage, high current or high frequency environments. The following are common limitations of non-ideal op-amps [1]:

- Voltage supply saturation. For given k , output cannot go above $V_{ss} - k$ or below $V_{dd} + k$.
- Finite bandwidth. Output signal magnitude reduces at high frequencies. This effect can be analysed using the gain-bandwidth product (GBWP) equation.
- Offset voltage/bias current. Even with no input, there exists a small "offset voltage" and "bias current" into the amplifier. This results in unwanted voltage at the output.
- Finite slew rate. The output cannot change quicker than a specified rate. This is different to the finite bandwidth limitation, but has a similar limiting effect.
- Finite common-mode rejection ratio (CMRR). An op-amp should ideally only amplify $V_+ - V_-$, but also amplifies the unwanted common signal (e.g. noise) on both inputs.

1.1.3. Key Specifications

Based around the above limitations, op-amp datasheets provide a number of key specifications that may be important for design. The op-amp used in this project is the MCP6242. Listed below are its notable specifications [2]:

- Typical CMMR of 75 dB (DC) to 65 dB (1 kHz).
- Ability to output between 0.035 and 5.465 V if $V_{ss} = 5.5$ V and $V_{dd} = 0$ V.
- Slew rate of 0.3 V/uS.
- Common mode input range from $V_{dd} - 0.3$ V to $V_{ss} + 0.3$ V.
- Maximum current output of 23 mA.
- Gain-bandwidth product of 550 kHz.

1.1.4. Configurations

A number of well-known op-amp configurations exist that all achieve slightly different amplification goals. The following list compares some common configurations [3]. Although certain circuits have two inputs, one of the inputs can be set to a specific voltage level for to add an offset to the output. These configurations can also be expanded to allow for signal "summing" by simply adding more inputs in parallel.

Type	Advantages	Disadvantages
Non-inverting	- Simple to design and build - High input impedance	- Large input bias currents - Amplifies noise from input
Differential	- Good noise rejection - Flexible	- Complex design - Low input impedance
Instrumentation	- Same as differential - Very high input impedance	- Complex and expensive design

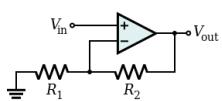


Figure 1.1:
Non-Inverting
Amplifier [5]

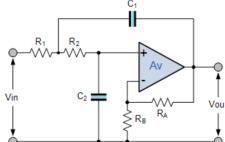


Figure 1.2:
Modified
Non-Inverting
Amplifier [6]

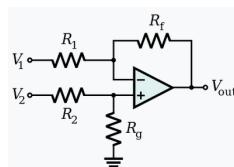


Figure 1.3: Dif-
ferential Ampli-
fier [5]

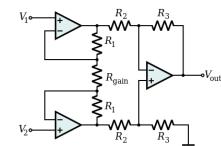


Figure 1.4: In-
strumentation
Amplifier [5]

1.2. Current Sensors

1.2.1. Techniques

Measurement techniques are usually either "invasive" or "non-invasive". Invasive techniques need to be built into the circuit directly and can have a significant affect on its operation, whereas non-invasive techniques may be added after the initial circuit design e.g. by measurement of a conductor's magnetic field. A list of a few of these techniques [7] include:

- A current-sensing resistor in series, which uses Ohm's law with a voltage measurement to calculate current.
- Hall element sensors, which measure the potential difference created as a result of the main current's magnetic field bending another current left/right.
- Direct coil techniques, which make use of Faraday's law.

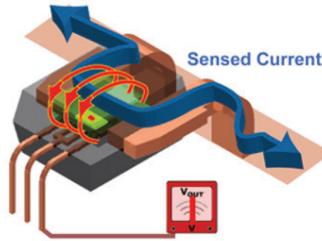


Figure 1.5: Hall Effect Sensor Working Principle [9]

1.2.2. High-Side vs Low-Side

This distinction refers to the placement of a current-sense element (e.g. resistor) relative to the load. For circuits which draw higher currents, high-side sensing can be used (placing the resistor closer to the positive side of the voltage source) and is often more convenient. Low-side sensing, on the other hand, can potentially cause ground loop issues [8], but has the ability to detect faults (e.g. short-circuits) earlier.

1.2.3. AC, DC and Power Requirements

As mentioned, there are various non-invasive and even wireless techniques used to measure current. Coil techniques make use of induction and therefore require AC to operate. The Hall effect and sense resistors, on the other hand, may be used in the DC case. Wireless techniques have benefits over resistors in that they can be configured to draw much less power, whereas sense resistors usually require high power handling capabilities as they pass all current drawn by the actual load through them.

1.3. Ultrasonic Sensors

1.3.1. Interface

The HC-SR04 ultrasonic ranging module's interface will be discussed. It has 4 pins, namely V_{cc} , GND , $Trig$ (*Trigger*) and $Echo$. It should be powered with 5 V_{dc} and requires at least 15 mA to function, meaning it will dissipate 75 mW of power. First, $Trig$ should be pulled high to indicate that the device should send a burst of ultrasonic sound out. Then, if the sound wave is received back, the device will output a distance-proportional pulse on the $Echo$ pin.

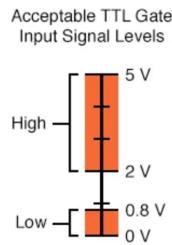


Figure 1.6: TTL Input/Output Levels [10]

The following detailed procedure should be followed to make a distance measurement [3]:

1. A pulse of at least 10 μs should be output onto $Trig$. This pulse must be TTL compliant as indicated in Figure 1.6 i.e. between 2 and 5 V.
2. If the sound wave is received back by the sensor, $Echo$ (also TTL) will go high for t_{high} seconds, where t_{high} is the time it took the wave to return to the sensor. This signal should therefore be conditioned if a circuit which requires 3.3 V is used.
3. The distance can then be calculated. One of the following methods may be used:
 - (a) The length of time of the $Echo$ output signal can be digitally measured and the distance then calculated using $Distance = \frac{t_{high} * v_{sound}}{2}$ (1.1) [3].
 - (b) The output pulse can be converted to an analog signal using filtering. The resultant filtered voltage will also be proportional to t_{high} .
4. A minimum of 60 ms should be present in between each pulse. This allows for a theoretical range of $\frac{60\text{ms} * 340\text{m s}^{-1}}{2} = 10.2\text{ m}$. In practice, the device has a range of $\approx 4\text{m}$.

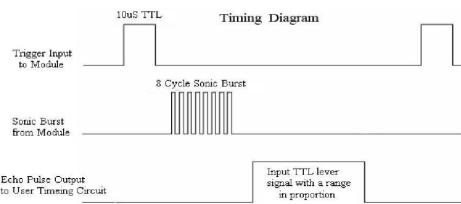


Figure 1.7: Sensor Timing Diagram [3]

1.3.2. Fundamental Operation

Sound Transducers

Ultrasonic sensors work by emitting and receiving sound waves of a high frequency. Electrical "transducers" are used to convert between electrical/sound energy. These are either excited by an electrical signal and caused to vibrate, or vibrate due to an incoming sound-wave and then generate an electrical signal. The two main transducer types used in ultrasound include [19]:

- *Piezoelectric* transducers. These use a vibrating crystal quartz which deforms in response to a changing potential difference.
- *Capacitive* transducers. These make use of a flexible dielectric membrane attached to an electrode. This electrode is attracted and repelled by electrical charges.

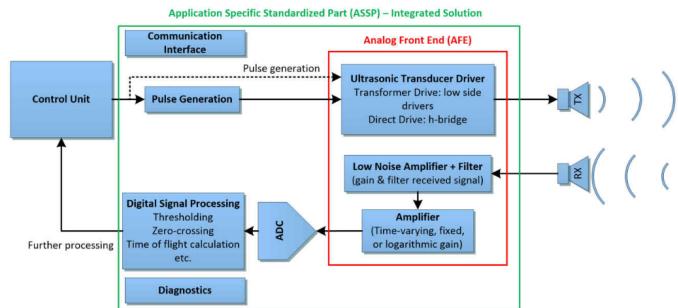


Figure 1.8: Simple Ultrasonic Sensing System [20]

Pulse Generation

Ultrasonic systems generally contain a digital control unit [20]. This unit is responsible for receiving the trigger signal from the communication interface and generating a pulse to send to the Analog Front End (AFE). This pulse is usually sinusoidal and is at a much higher frequency than the trigger input (between 30 kHz and 5 MHz). After the digital pulse is generated, the AFE amplifies it using a transistor drive circuit. This can be at a relatively low voltage e.g. 5 V, but often high-voltage and "direct drive" amplification is used, which may allow up to 36 V.

Pulse Acquisition

After some time, the pulse may return and electrically excite the microphone transducer. It is subsequently filtered and passed through a low-noise amplifier. The signal is then converted by an ADC and enters the digital domain, where further processing is done. Finally, a DSP analyzes the signal. This includes performing the actual "time-of-flight" calculation, which it then communicates back to the control unit. The control unit is then responsible for creating the echo signal on the communication interface for the length of time sent by the DSP.

1.4. PWM to Analog Conversion

PWM (Pulse Width Modulation) is useful in that it allows analog information to be conveyed in digital signals. PWM waves are similar to square waves, however differ in that $t_{high} \neq t_{low}$. A PWM signal is defined by 3 properties:

- Frequency: The rate at which the signal oscillates. $f = \frac{1}{t_{high}+t_{low}}$ Hz.
- Amplitude: The difference between "high" and "low" voltages. $A = V_{high} - V_{low}$ V.
- Duty cycle: The ratio of the signal's "high time" to its period. $\tau = \frac{t_{high}}{t_{high}+t_{low}}$ s.

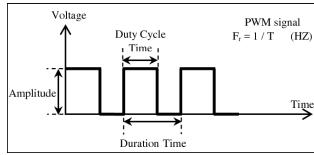


Figure 1.9: PWM Signal Voltage vs Time [11]

Often, this analog information is conveyed in a varying duty cycle (τ). To convert this varying value to analog, a low-pass filter can be used. Since the signal's average value increases with τ , filtering out all "harmonics" of the signal will result in $V_{out} = A \times \tau$ (1.2) [12]. The cutoff frequency (f_c) of the filter should be as low as possible, while maintaining an acceptable rise time, in order to minimize ripple on the filter output. Then, since $t_r \propto \frac{1}{f_c}$, $t_{r(max)}$ will determine the minimum cutoff frequency, $f_{c(min)}$. This will be based on the filter used e.g. $f_{c(min)} = \frac{3.3}{2\pi \cdot t_{r(max)}}$ for a 2nd order filter [C.1.1].

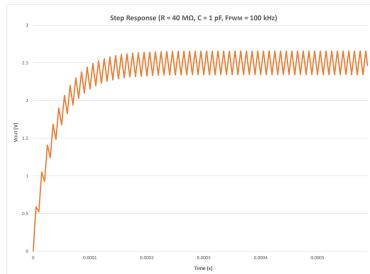


Figure 1.10: Filtered PWM Signal [12]

Assuming $f_{c(min)}$ is fixed, $f_{c(max)}$ should be determined by the maximum acceptable noise on the output of the filter. Since filtering will still leave a small "ripple" signal at frequency f_{PWM} , this will be the largest noise component. Given the following:

- A : Amplitude of the PWM signal (V)
- τ_{max} : Maximum duty cycle of the PWM signal (%)
- N_{max} : Maximum acceptable noise of the filtered output (V)

Then the required attenuation at f_{PWM} is given by $A_{dB} = 20 \log \left[\frac{A \cdot \tau_{max}}{N_{max}} \right]$ (1.3). This will determine $f_{c(max)}$, in conjunction with the type of filter used and its order.

1.5. Digital to Analog Conversion

1.5.1. Configurations

A DAC can be implemented using different summing op-amp configurations:

- *Inverting vs Non-Inverting.* Single-supply inverting amplifiers require an offset bias at V^+ to keep the output positive. Non-inverting amplifiers suffer from input source coupling (discussed in Section 1.5.2) and require a second stage to invert the output.
- *Resistor-Weighted vs R2R Ladder.* Resistor-weighted networks (RWN) use resistors continuously halving in value (e.g. in Figure 1.11). They are simple to build, but require large-valued precision resistors, or many parallel resistors. R2R Ladder networks (e.g. in Figure 1.12) solve this by re-using resistors across inputs.

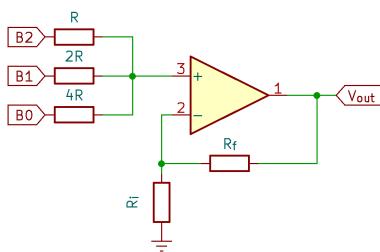


Figure 1.11: Non-Inverting Mode with Resistor-Weighted Network [22]

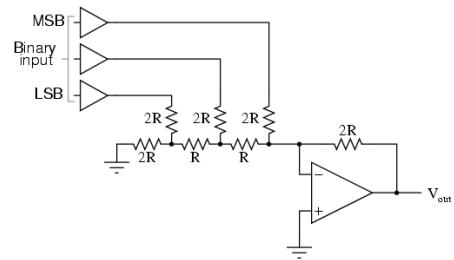


Figure 1.12: Inverting Mode with R2R Ladder Network [23]

Common-mode voltage range limitations should be considered. In inverting mode, V^- is a "virtual ground" due to negative feedback. This means common-mode voltage always equals the offset voltage at V^+ . Rail voltage can therefore be chosen using only this voltage and the output specifications. This is not true in non-inverting mode: the voltage at V^+ changes based on the source voltages. For a DAC using the MCP6242, this means $V_{dd} \geq V_{digital} - 0.3V$.

1.5.2. Impedance Requirements

For a practical source, $R_o \neq 0\Omega$, meaning amplifier input impedance should be considered. Non-inverting amplifiers do not have a "virtual ground", meaning sources are not decoupled from each other [22] causing some noise. Table 1.1 documents lowest input impedances:

Configuration	R2R	RWN
Inverting	$2R$	R
Non-Inverting	$4R$	$R \times \left(1 + \frac{1}{\frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{2^N}}\right) \approx 2R$

Table 1.1: Input impedance of various summing configurations

For a practical load, $R_L \neq \infty$, meaning amplifier output impedance should be considered. A buffer stage can be added. This lowers the output impedance of the op-amp.

Chapter 2

Detailed Design

2.1. Current Sensor

2.1.1. Configuration

The differential amplifier configuration will be used for this project for the following reasons:

- The configuration is specifically designed to reject common-mode noise, which the non-inverting amp suffers from.
- Only 1 op-amp is needed.
- The design is relatively simple compared to the instrumentation amplifier.

However, a modified version with two extra capacitors will be used. Two capacitors will be added in parallel with R_f and R_g called C_f and C_g respectively. It is important that these capacitors have the same value in order to preserve CMRR [5]. It is likely, however, that one of these will be dominant due to differing resistor values, and therefore this design will only consider the filter to be first-order. This is acceptable, however, due to the amplifier's noise-rejecting capabilities.

2.1.2. Gain and Filter Stage

Before calculating component values, both the cutoff frequency of the RC filter, and the DC gain of the amplifier, need to be determined. The gain of the amplifier should be determined such that, when the maximum current flows through the sense resistor, the maximum voltage is output.

First, the maximum current of the motor should be measured. This can be done by connecting the motor to a power supply (through an ammeter), stalling the motor, and reading the output current. With a supply voltage of 6.4 V connected, the motor for this project read 740 mA, however different motors may read between 1 and 1.5 A. The average running current, however, is between 200 mA and 300 mA. A value of $I_{max} = 1A$ will therefore be chosen to allow for more headroom and a slightly lower gain. Since a sense resistor of $10\text{ m}\Omega$ is to be used, the maximum voltage through this resistor will therefore be 8 mV. A gain of $\frac{3V}{10mV} = 300$ is therefore chosen. Although this voltage level is small, it is expected, given that the resistance value is so small. It is also desirable, as it shows that the circuit is not "stealing" too much power from the motor itself.

The cutoff frequency f_H should be selected such that the slew rate requirements are not affected, while still adequately filtering a 1 kHz noise signal. In order for the noise requirement to be satisfied, the input signal must be attenuated by $20 \log \frac{300*10mV}{250mV} \approx 22dB$. This means the cutoff should be around 100 Hz (a decade below 1 kHz). Since the specification requires a change from 0.1 to $3 \times 0.9 = 2.7V$ in less than 100 ms, the output should be capable of oscillating at $\frac{1}{50ms} = 20Hz$, which is below the designed cutoff.

Since input current of the circuit needs to be limited below 150 uA, high resistor values should be chosen:

- Assuming $i_n = 0$, choose $\frac{V_{out(max)}}{R_1+R_f} << 150uA \therefore R_1 + R_f >> 20k\Omega$. Choose $R_f = 100k\Omega$.
- $G = \frac{R_f}{R_1} = 300 \therefore R_1 = 330\Omega$
- Choose $R_2 = R_1 = 330\Omega$ and $R_g = R_f = 100k\Omega$ for differential symmetry.
- Since R_{eq} of C_f is R_f and of C_g is $R_g||R_2$, it is clear that C_f is dominant, $\therefore C_f = \frac{1}{2\pi \cdot R_f \cdot 100Hz} \approx 15nF$. Also set $C_g = 15nF$ for symmetry. It should be noted, however, that this technique (using time constants) is not always valid - especially in complex circuits such as these - and so these results should be checked using simulations.

2.1.3. Circuit Diagram

The following figure details the final circuit design for the sensor and amplifier system.

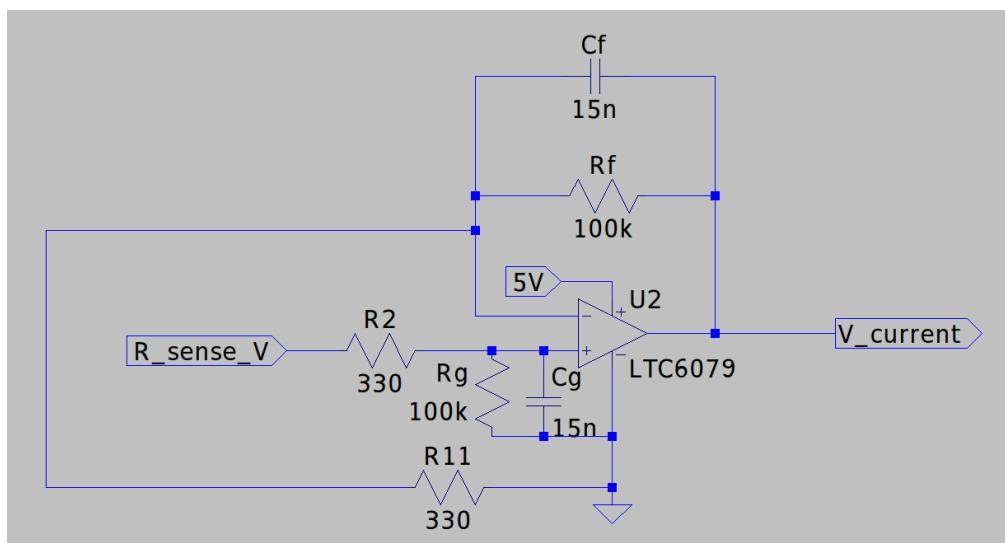


Figure 2.1: Current Sensor Circuit Diagram

A single 5 V supply will be used. Although there are benefits to a dual rail supply, that would prove impractical in the context of the larger system.

2.2. Ultrasonic Sensor

2.2.1. Power and Output Requirements

The range sensor requires 5 V_{dc} power and will draw around 15 mA. Since the LD1117V provides a stable 5.0 V output and is capable of providing up to 800 mA of current, the sensor will be powered directly from this regulator.

The sensor's echo output is a PWM wave of varying duty cycle τ and $f_{PWM} = 16$ Hz. This signal's amplitude could be as high as 5 V (TTL level). The maximum output A_{max} after unity filtering, however, will be determined by the maximum duty cycle, t_{max} . Since a distance of $D_{max} = 1$ m and $D_{min} = 5$ cm, Equations 1.1 and 1.2 can be used to calculate:

- At D_{max} , $t_{max} \approx 5.9$ ms, $\tau_{max} = \frac{5.9\text{ ms}}{1/16} \approx 9.5\%$ and $A_{max} = (5\text{ V}) \cdot (9.5\%) = 475\text{ mV}$.
- At D_{min} , $t_{min} \approx 0.29$ ms, $\tau_{min} = \frac{0.29\text{ ms}}{1/16} \approx 0.47\%$ and $A_{min} = (5\text{ V}) \cdot (0.47\%) = 23\text{ mV}$.

2.2.2. Filter Selection

To determine the filter's order, rise time and noise requirements should be considered:

- After filtering, since gain $\approx \frac{3\text{ V}}{475\text{ mV}} \approx 7\text{ V/V}$, filter ripple must be under $\frac{70\text{ mV}}{7} = 7\text{ mV}$.
- A 10% to 90% rise time (t_r) of 1.5 s should be adhered to.

These specifications result in the requirement that A_{dB} at $f_{PWM} = 20 \log \left[\frac{5\text{ V}}{7\text{ mV}} \right] \approx 60\text{ dB}$. A 3rd order filter with $f_c = 1\text{ Hz}$ will be used, as a 2nd order may be tolerance-sensitive. This provides $t_r \approx 0.63\text{s}$ and $A_{dB} \approx 72\text{dB}$ [C.1.1].

Filter type	Design Spec.	Cutoff f_c	Rise time t_r	Attenuation A_{dB}
1 st order	Rise Time	0.233 Hz	1.5 s	37 dB
	Attenuation	0.016 Hz	22 s	60 dB
2 nd order	Rise Time	0.350 Hz	1.5 s	66 dB
	Attenuation	0.505 Hz	1.038 s	60 dB
3 rd order (cascade)	Rise Time	0.420 Hz	1.5 s	95 dB
	Attenuation	1.600 Hz	0.394 s	60 dB

Table 2.1: Filter type vs Rise Time and Attenuation using [C.1.1]

2.2.3. Configuration

A "two-and-a-half" stage configuration will be used. The first stage is a gain/offset and 1st order filter, and is placed first in order to amplify the signal above the MCP's 35 mV floor. The second stage is unity-gain 2nd order filter. A non-inverting amplifier will be used for stage 1, and a Sallen-Key topology for stage 2. Since the quiescent current for each op-amp is 70 μA [2], stage 1 & 2 will be allocated 400 μA and 200 μA respectively.

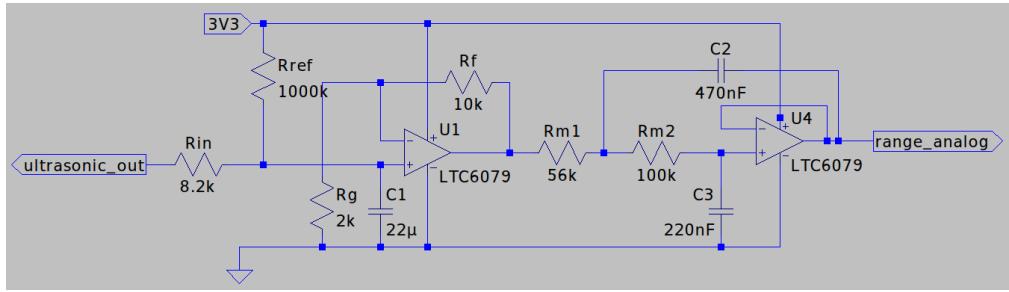


Figure 2.2: Range Sensor Amplifier Circuit Diagram

2.2.4. Gain Stage

This stage will be powered by the 3.3 V regulator. As this is a low-gain circuit, input bias voltages can be neglected. Slew rate and CMMR imbalance can also be ignored due to the low-frequency, single-ended use of the op-amp. Voltage rail saturation does not need to be considered at the circuit output, as $0.3 \text{ V} < V_{out} < 3 \text{ V}$, and has already been catered for at the input, as discussed in Section 2.2.3. Using the equations at [18], and the expected input ranges from the filter stage, gain $m = \frac{3\text{V}-0.3\text{V}}{475\text{mV}-23\text{mV}} = 5.97 \text{ V V}^{-1}$, and offset $b = 0.3 \text{ V} - m \times 23 \text{ mV} \approx 163 \text{ mV}$:

- With idle current $I_Q = \frac{V_{out}}{R_f + R_g}$, and $V_{out(max)} = 3.3 \text{ V}$, $(R_f + R_g)_{min} = \frac{3.3 \text{ V}}{400 \mu\text{A}} = 8.25 \text{ k}\Omega$.
- Since the offset voltage is low (i.e. R_{ref} will be high), first choose $R_{ref} = 820 \text{ k}\Omega + 470 \text{ k}\Omega\text{pot} \approx 1000 \text{ k}\Omega$. A potentiometer is used to tune the offset.
- Calculate $R_{in} = \frac{R_{ref} \times b}{V_{ref} \times m} \approx 8.2 \text{ k}\Omega$ with $V_{ref} = 5 \text{ V}$ and $C_1 = \frac{1}{2\pi f_c R_1} \approx 22 \mu\text{F}$.
- Choose $R_f = 10 \text{ k}\Omega$ to satisfy the current requirements.
- Calculate $R_g = \frac{R_{ref} \times R_f}{m \times (R_{in} + R_{ref}) - R_{ref}} \approx 2 \text{ k}\Omega$. To tune the gain, choose $R_g = 1.5 \text{ k} + 1 \text{ k}\Omega\text{pot}$.

2.2.5. Filter Stage

This stage will use the 3.3 V regulator to clip the circuit output for use with the MCU. This results in the 2nd order stage transfer function $H(s) = \frac{1}{1+0.2251s+0.02533s^2} = \frac{1}{1+a_1s+b_1s^2}$ with $\zeta = 0.707$. Now, component values can be chosen. Formulae from [17] will be used:

- Since both capacitors are open-circuit during DC, the idle current is very low. A maximum step input will result in a surge of current through C_2 to ground. With $V_{in(max)} = 5 \text{ V}$, $(R_{m1} + R_{m2})_{min} = \frac{5 \text{ V}}{200 \mu\text{A}} = 25 \text{ k}\Omega$.
- Since $C_3 = \frac{a_1}{2\pi f_c (R_{m1} + R_{m2})}$ [17], choose $C_3 = 220 \text{ nF}$ so that $R_{m1} + R_{m2} \approx 160 \text{ k}\Omega$.
- To meet $C_2 \geq C_3 \cdot \frac{4 \cdot b_1}{a_1^2} \approx 2C_3$ [17], choose $C_2 = 470 \text{ nF}$.
- Since $C_3 \cdot C_2 = \frac{b_1}{((2\pi f_c)^2 R_{m1} R_{m2})}$, and $R_{m1} + R_{m2} = 450 \text{ k}\Omega$, solve to obtain $R_{m1} = 61 \text{ k}\Omega$ and $R_{m2} = 99 \text{ k}\Omega$. Choose $R_{m1} = 56 \text{ k}\Omega$ and $R_{m2} = 100 \text{ k}\Omega$ as practical values.

2.3. Digital to Analog Converter

2.3.1. Configuration and Impedance Requirements

The inverting, R2R configuration will be used. The benefit of a virtual ground, high input impedance, and low component count are some reasons for this. A voltage divider will be added at V^+ to offset the negative gain, and a buffer stage will be used for better output current. The ESP32 pin output impedance is typically $30 - 40 \Omega$ [24]. In order to have less than 1% deviation of ESP voltage, R_{in} can be solved for using:

$$\frac{V_{cc} - V_{pin}}{V_{cc}} = \frac{R_{in}}{R_{in} + R_{ESP}} \leq 0.01 \therefore R_{in} \geq 3.5 \text{ k}\Omega$$

The output impedance of the MCP is $R_o \approx \frac{5.5 \text{ V}}{23 \text{ mA}} = 239 \Omega$ [2]. The MCP also has current protection, and can continuously source/sink 23 mA to a 0 ohm load. The buffer stage will decouple the negative feedback loop of the summer from the load stage, adding protection.

2.3.2. Summing Stage

All ESP pins are either 0 or 3.3 V. An amplifier current limit of $250 \mu\text{A}$ (after quiescent current), and a pin limit of $50 \mu\text{A}$ per digital input is chosen. Since an inverting configuration with a virtual ground (which will be $\ll 3.6 \text{ V}$) has been used, the common-mode range of the op-amp is not violated. Since the MCP can only reach within 35 mV of the rails, an output range of $0.1 \text{ V} < V_{out} < 3.1 \text{ V}$ will be designed for. Both stages can be powered by 5 V.

- For amplifier current, $R_f > \frac{3.3 \text{ V}}{250 \mu\text{A}} = 13.2 \text{ k}\Omega$. For input current, $2R > \frac{3.3 \text{ V}}{50 \mu\text{A}} = 66 \text{ k}\Omega$.
- Choose $2R = 100 \text{ k}\Omega$. For 1111, and using the summing amplifier formula (before offset), $V_{out} = -3 \text{ V} = - \left[\frac{R_f}{2R} \times 3.3 + \frac{R_f}{4R} \times 3.3 + \frac{R_f}{8R} \times 3.3 + \frac{R_f}{16R} \times 3.3 \right] \therefore R_f = 48.485 \text{ k}\Omega$. Choose $R_f = 47 \text{ k}\Omega + 4.7 \text{ k}\Omega\text{pot}$.
- For $V_{out} = 3.1 \text{ V}$ with 0000 input, $V^+ = V^- = 3.1 \text{ V} \times \frac{50 \text{ k}\Omega}{48.485 \text{ k}\Omega + 50 \text{ k}\Omega} \approx 1.574 \text{ V}$. For the voltage divider, choose $R_a = 47 \text{ k}\Omega \therefore R_b = 21.59 \text{ k}\Omega$. Choose $R_b = 18 \text{ k}\Omega + 10 \text{ k}\Omega\text{pot}$.

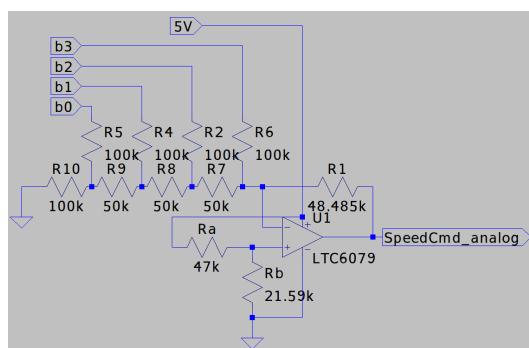


Figure 2.3: Digital to Analog Converter Circuit Diagram

2.4. Motor Controller

2.4.1. Configuration

The motor controller circuit will consist of both a subtractor stage and a power stage. The subtractor will be a differential op-amp which will receive the range sensor and DAC outputs as inputs. The output of this stage will feed the power stage with the "motor control" command. The power stage will use a common-collector circuit with a TIP31C NPN transistor to provide current gain from the control command. A second transistor, the 2N3904, will be used to create a Darlington pair configuration to increase the input impedance. A "flyback" diode will be connected from ground to the power stage's output to prevent sparking.

2.4.2. Power Stage

Since the load is a motor, current will always be sourced by the transistor (not sunk), and therefore the load can be connected directly to the emitter without any bias resistor or AC coupling capacitor. Since the subtractor stage can provide a DC bias, there is also no need for a resistor input bias network.

According to the specifications, the output voltage range across the motor/load should be at least $0.5 \text{ V} < V_L < 6.2 \text{ V}$, however a higher maximum voltage is desireable. The TIP31C saturates at $V_{be} \approx 0.7 \text{ V}$ for $I_c = 10 \text{ mA}$ and at $V_{be} \approx 0.95 \text{ V}$ for $I_c = 1 \text{ A}$ (around the motor stall current) [4]. Therefore, to ensure the motor is off, $V_{control} < 0.5 \text{ V} + 0.7 \text{ V} = 1.2 \text{ V}$, and to power the motor fully, $V_{control} > 6.2 \text{ V} + 0.95 \text{ V} = 7.15 \text{ V}$. A minimum input range of $1.2 \text{ V} < V_{control} < 7.15 \text{ V}$ is therefore chosen, however the lower/upper limits may be decreased/increased respectively during subtractor design. With $I_{c(max)} \approx 1 \text{ A}$, the source needs to be capable of providing $I_{s(max)} = \frac{1 \text{ A}}{\beta} = 40 \text{ mA}$ since $\beta \approx 10^{1.4} = 25$ [4].

2.4.3. Subtractor Stage

The input voltage ranges into this stage are $0.2 \text{ V} < V_{range} < 3.3 \text{ V}$ for the ultrasonic sensor, and $0.1 \text{ V} < V_{speed} < 3.1 \text{ V}$ for the DAC, with the output range being equal to the power stage's input range as discussed in Section 2.4.2. Since a high V_{speed} corresponds to a low output voltage, the DAC input will be connected to the inverting terminal. No offset needs to be added at the non-inverting terminal as the range sensor provides a constant 3.3 V when no object is near. A limit of $400 \mu\text{A}$ should be kept for this circuit, excluding quiescent current. Referring to the final circuit diagram in Figure below and according to [25], the equation for $V_{control}$ is given by:

$$V_{control} = (V_{ref} \cdot R_r + V_{range} \cdot R_o) \left(\frac{1 + \frac{R_f}{R_s}}{R_r + R_o} \right) - V_{speed} \cdot \frac{R_f}{R_s} \quad (2.1)$$

Equation 2.1 ultimately has 3 unknowns i.e. 3 degrees of freedom.

Component values can now be calculated:

- Maximum current will flow through the feedback loop when $V_{control} = 7.2\text{ V}$ and $V_{speed} = 0\text{ V}$, with a value of $I_{max} = \frac{7.2\text{ V}}{R_s+R_f}$. To keep feedback current $< 200\text{ }\mu\text{A}$, $(R_s + R_f)_{min} = \frac{7.2\text{ V}}{200\text{ }\mu\text{A}} = 36\text{ k}\Omega$.
- When no object close, the output voltage should be $< 1.2\text{ V}$ for $V_{speed} = 3.1\text{ V}$ and $> 7.15\text{ V}$ for $V_{speed} = 0.1\text{ V}$. This results in a minimum gain of $\frac{7.15\text{ V}-1.2\text{ V}}{3.1\text{ V}-0.1\text{ V}} = 1.98\text{ V/V}$. Choose a gain of 2 i.e. $\frac{R_f}{R_s} = 2$. Choose $R_f = 47\text{ k}\Omega$ and $R_s = 23.5\text{ k}\Omega = 18\text{ k}\Omega + 10\text{ k}\Omega\text{pot}$.
- Now, $V_{control} = 3 \cdot V_{range} \cdot \frac{R_a}{R_a+R_b} - 2 \cdot V_{speed}$, with a single DAC step resulting in $\approx 400\text{ mV}$ step. For $V_{speed} = 0.1\text{ V}$ and $V_{range} = 3.3\text{ V}$, $V_{control} \approx 7.2\text{ V}$ therefore solve for $\frac{R_a}{R_a+R_b} = 0.747$.

Chapter 3

Results

3.1. Current Sensor

3.1.1. Simulation

After running initial simulations, it was clear that the constant assumed in the design stage for the dominant capacitor C_f was too high. The capacitor value was then experimentally increased to 100nF where a satisfactory response which was reasonably below 250 mV (10-20%) was obtained. This section details the rest of the results of these simulations.

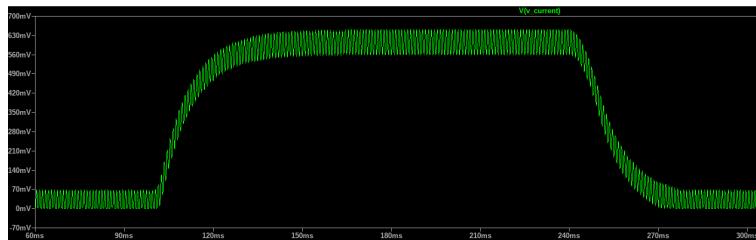


Figure 3.1: Amplifier Output in Response to Step Input

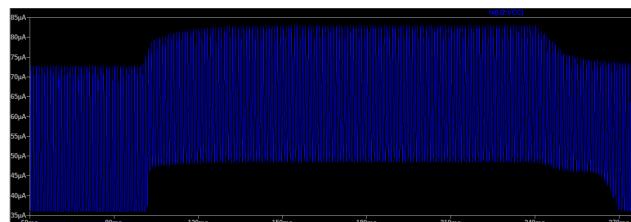


Figure 3.2: Current Draw

As can be seen, all specifications were adhered to:

- The noise level at idle is well below the 250 mV requirement.
- The step response input changes 20-25 ms, which is below the 100 ms requirement.
- The power draw of the circuit (as measure at the positive terminal of the op-amp) is less than 85 uA, which is much less than the specified 150 uA.

Lastly, the input simulation parameters were modified during testing to analyze the various output voltages for different input currents. For input currents of 400mA, 500mA, 800mA and 1A, the output voltages were 1.22V, 1.52, 2.43 and 3.024 V respectively. This matches perfectly with the initial design.

3.1.2. Implementation

Tests were conducted with a function generator to ensure the amplifier met specifications.

As can be seen in Figure 3.3, the amplifier noise requirement was satisfied. The input signal (channel 1, bottom) is a 10 mV_{pp} 1 kHz sine wave with 6 mV offset. It is required that a sinusoidal "noise" signal greater than this frequency should not be amplified to more than 250 mV_{pp}. An output of 1.13 V - 0.949 V = 181 mV was obtained - within the threshold.

In Figure 3.4, the amplifier's step response time was recorded as 4.957 ms, which is much below the 100 ms requirement. This time is 4x better than the designed/simulated circuit, presumably due to the increased resistance value and other tolerances.

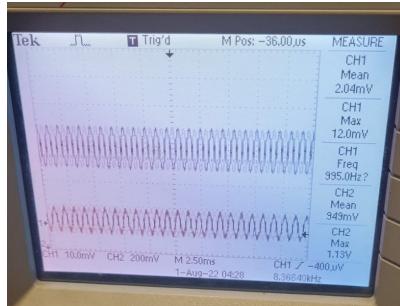


Figure 3.3: Noise Level

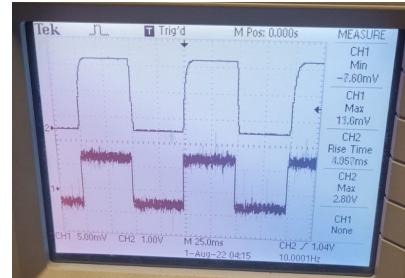


Figure 3.4: Step Response

Current measurements were then made with the motor connected, as visible in Table 3.1. As can be analyzed, there is an offset voltage of 0.42 V at the output. The actual gain can be calculated as e.g. $\frac{1.42\text{ V} - 0.42\text{ V}}{210\text{ mA} * 10\text{ m}\Omega} = 476\text{ V/V}$. With the 120 kΩ resistor, an ideal gain of $\frac{120\text{ k}\Omega}{330\text{ }\Omega} = 363.6\text{ V/V}$ was expected, however due to the nature of the circuit (which contains 4 resistors) a tolerance of 10% * 4 should be accounted for, which explains the higher gain.

Motor Condition	PSU Current (mA)	Output Voltage (V)
Stall	1200	3.31
Slight Load	305	1.96
Free Running	210	1.42
I = 150 mA	150	1.13
I = 100 mA	100	0.91
I = 50 mA	50	0.63
I = 0 mA	0	0.42

Table 3.1: Measurements of Motor Current and Voltage

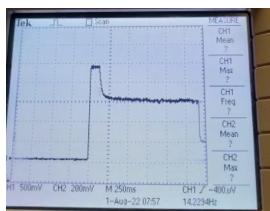


Figure 3.5: Open Circuit to Free Running

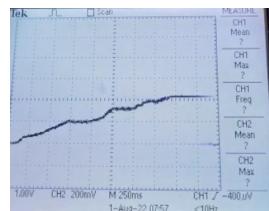


Figure 3.6: Increasing Load

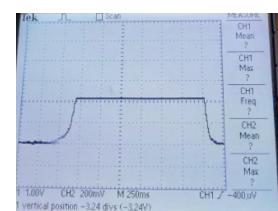


Figure 3.7: Free Running to Stall

3.2. Range Sensor

3.2.1. Simulation

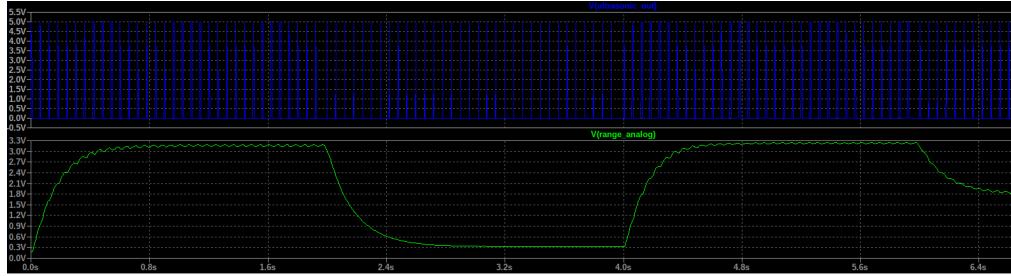


Figure 3.8: Full-Range PWM using Modified Workbench

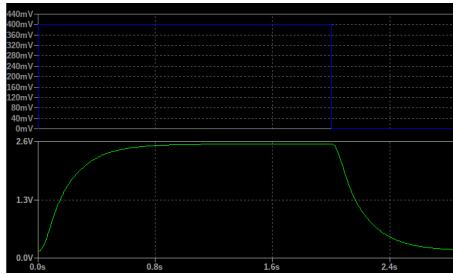


Figure 3.9: 400 mV Step Response
Input vs Output

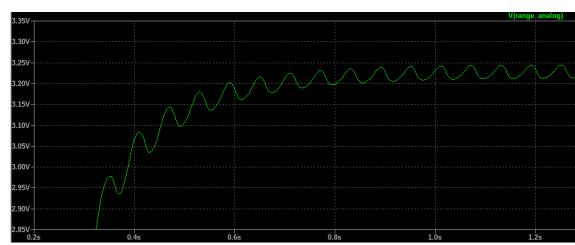


Figure 3.10: Noise Level

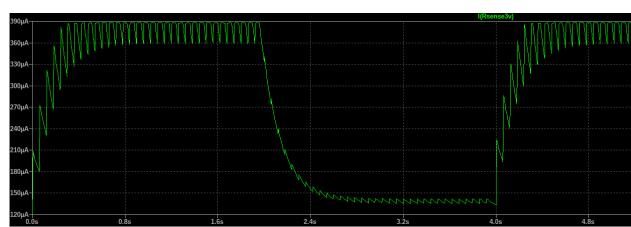


Figure 3.11: Current Draw

As seen in the above figures, all specifications were complied with:

- Figure 3.8 demonstrates the default simulation to test the distance limits with $\tau = 0.05\%$ to 9.5% , followed by the original workbench settings. As visible, the output is ≥ 3.0 V for far distances, and ≤ 300 mV for close distances.
- Figure 3.9 shows the response time of around 800 ms, much less than the required 1.5 s.
- Figure 3.10 demonstrates the low noise ripple of around 50 mV, less than the required 70 mV.
- Figure 3.11 indicates a maximum current draw of 390 μ A, less than the maximum 750 μ A.

3.2.2. Implementation

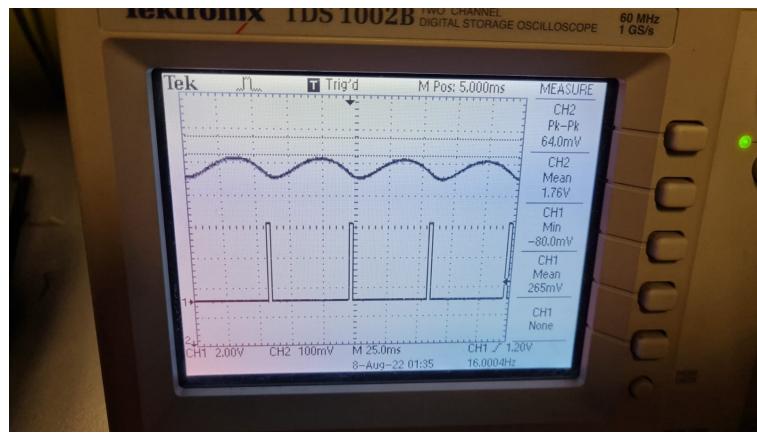


Figure 3.12: Noise Level

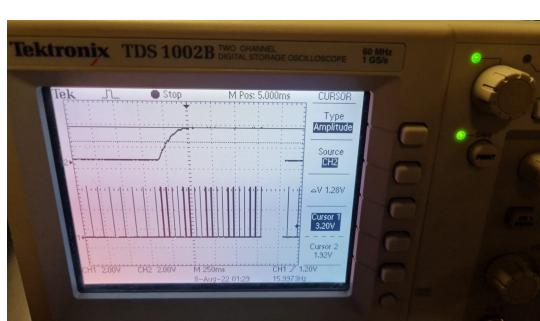


Figure 3.13: Step Response

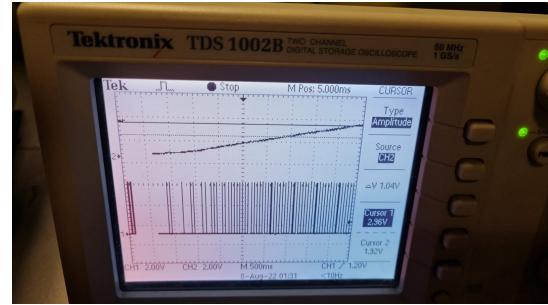


Figure 3.14: Gradual Change over Input Range

Similarly, the implementation of the circuit also complied with specifications:

- Figure 3.12 indicates a noise level of $64 \text{ mV}_{\text{pp}}$. Although this is only measured at 1.76 V output, it seems the oscilloscope was struggling to provide accurate readings and could not be zoomed in further.
- Figure 3.13 indicates a rise time of around 300 ms.
- Figure 3.14 shows the gradual response of the circuit. The cursor is on 2.96 V in the Figure, and by counting divisions it can be seen that it began at around 0.2 V . This shows a relatively linear response.

3.3. Digital to Analog Converter

3.3.1. Simulation

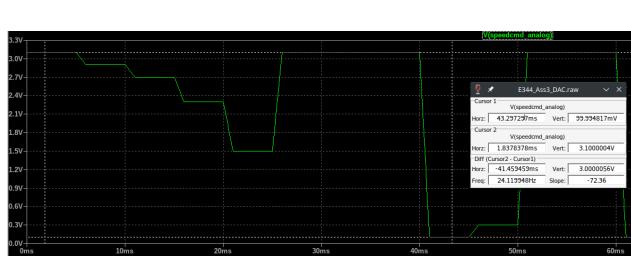


Figure 3.15: Output Range from 0000 (First Cursor) to 1111 (Second Cursor)

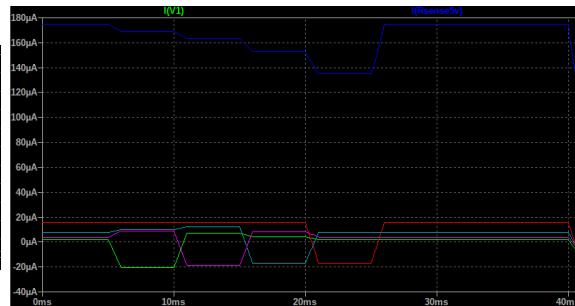


Figure 3.16: Current Draw (Amplifier and Digital Inputs)

As seen in the above figures, all specifications were complied with:

- Figure 3.15 shows that an output of 0000 produces exactly 3.1 V on the output, and that 1111 produces 100 mV.
- Figure 3.16 shows a maximum current draw of under 180 μ A, which is much under the 250 μ A specification. It also shows that each digital input draws less than 20 μ A, also under the 50 μ A specification.

3.3.2. Implementation

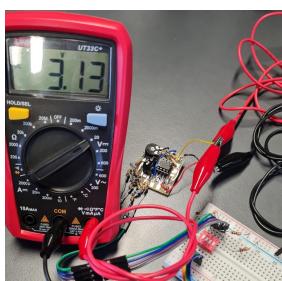


Figure 3.17: DAC Output at 0000

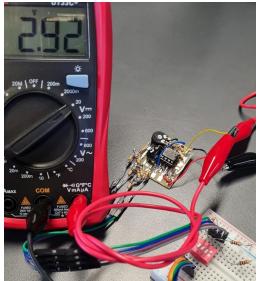


Figure 3.18: DAC Output at 0001

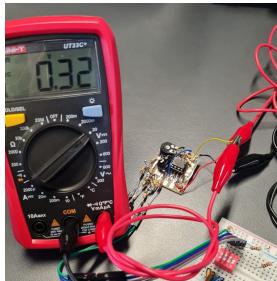


Figure 3.19: DAC Output at 1110

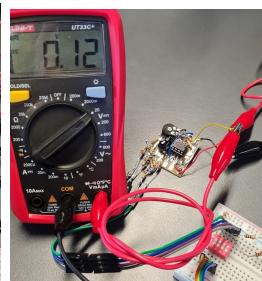


Figure 3.20: DAC Output at 1111

Figures 3.17 to 3.20 demonstrate the output voltages at specific digital input combinations. All specifications are complied with, specifically that 0000 produces > 3 V on the output, and that 1111 produces < 0.5 V.

Chapter 4

Physical Implementation

4.1. Current Sensor

The implementation of the circuit was different in two ways compared to the original design:

- 120 k Ω resistors were used instead of 100 k Ω , as they were easier to obtain, and would only result in a slightly larger gain and lower cutoff.
- The amplifier circuit was powered with regulated 3.3 V. This was done to protect the ESP's input pins by saturating the output when it would have been too large.

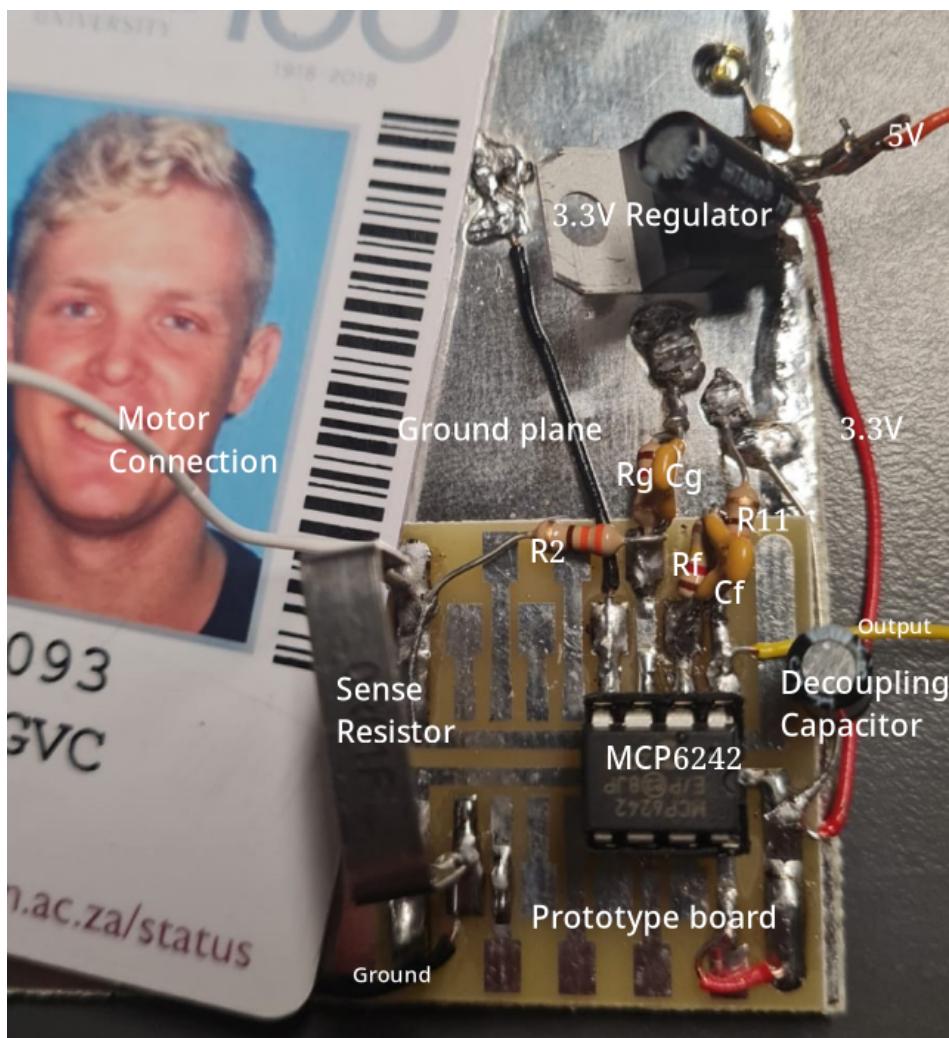


Figure 4.1: Current Sensor Physical Circuit

4.2. Range Sensor



Figure 4.2: Ultrasonics Sensor Amplifier Physical Circuit

4.3. Digital to Analog Converter



Figure 4.3: Digital to Analog Converter Physical Circuit

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Appendix A

Social contract



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jou kennisvennoot • your knowledge partner

E-design 344 Social Contract

2022

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceding the term, the lecturer (Thinus Booyens) and a few paid helpers (Rita van der Walt, Keegan Hull, and Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth, that you are enabled to learn from the module, and demonstrate and be assessed on your skills. We commit to prepare the assignments, to set the assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

I, Gary Allen have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication online of supplementary videos on specific topics, I acknowledge that I am expected to attend the scheduled lectures to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Prof. MJ (Thinus) Booyens

MJ Booyens
Signature:

Date: 1 July 2022

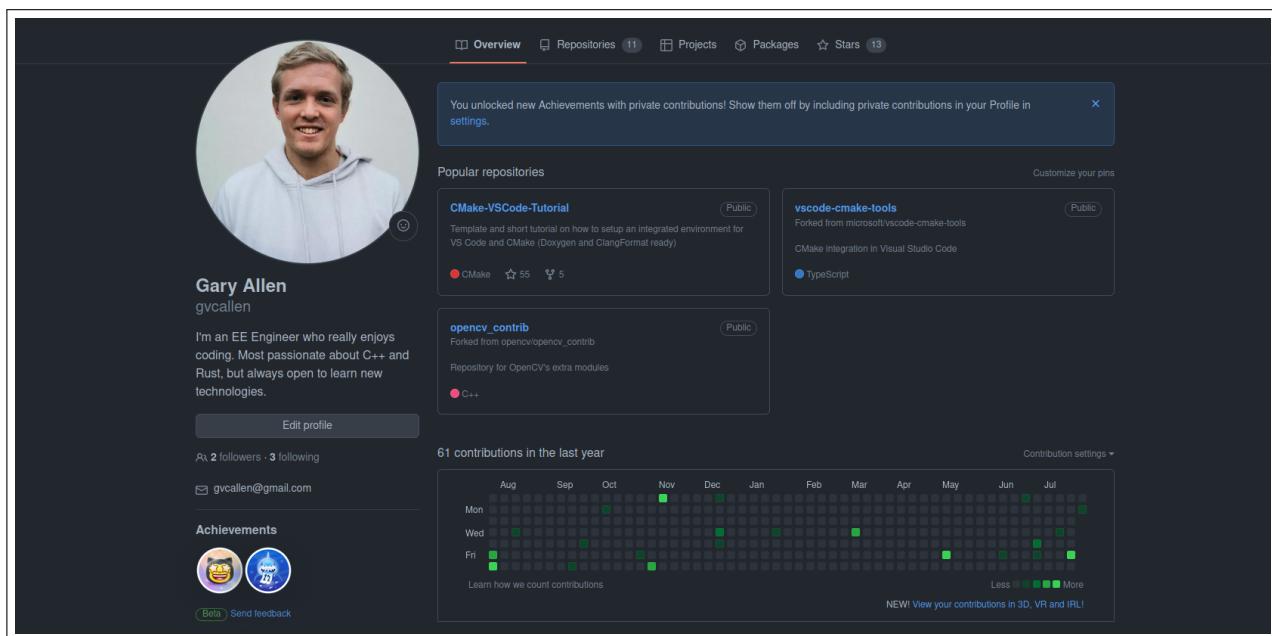
Student number: 23908083

Signature: Dale

Date: 07 / 07 / 2022

Appendix B

GitHub Activity Heatmap



Appendix C

Formulae and Derivations

C.1. Filters

C.1.1. Common Filter Formulae

In the following formulae, f_c is the filter's cutoff frequency, $w_c = 2\pi f_c$, and $H(s)$ is the Laplace transfer function of the filter.

For a 1st order filter:

- $H(s) = \frac{w_c}{s+w_c}$
- Attenuation (dB) = $-10 \log[1 + (\frac{f}{f_c})^2]$ [12]
- 10% to 90% Rise time, $t_r \approx \frac{2.2}{w_c}$ [13]

For a 2nd order filter:

- $H(s) = \frac{w_c^2}{s^2 + 2\zeta w_c s + w_c^2}$
- Attenuation (dB) = $-10 \log[1 + (\frac{f}{f_c})^4]$ with $\zeta = 0.707$ [C.2]
- 10% to 90% Rise time, $t_r \approx \frac{3.3}{w_c}$ with $\zeta = 0.707$ [14]

For a 3rd order filter (formed by cascading a 1st and 2nd order):

- $H(s) = \left(\frac{w_c}{s+w_c}\right) \left(\frac{w_c^2}{s^2 + 2\zeta w_c s + w_c^2}\right)$
- Attenuation (dB) = $-10 \log[1 + (\frac{f}{f_c})^2 + (\frac{f}{f_c})^4 + (\frac{f}{f_c})^6] \approx -60 \log \left[\frac{f}{f_c}\right]$ with $\zeta = 0.707$ and $f >> f_c$.
- 10% to 90% Rise time, $t_r \approx \frac{3.97}{w_c}$ with $\zeta = 0.707$, using $t_{ro} = \sqrt{t_{r1}^2 + t_{r2}^2}$ from [16]

C.1.2. 2nd Order Filter Attenuation

For a 2nd order filter with the following transfer function:

$$H(s) = \frac{w_c^2}{s^2 + 2\zeta w_c s + w_c^2}$$

The attenuation A_{dB} at frequency w can be calculated as follows:

$$\begin{aligned}
A_{dB} &= 20 \log \left| \frac{w_c^2}{(jw)^2 + 2\zeta w_c(jw) + w_c^2} \right| \\
&= -20 \log \left| \frac{(w_c^2 - w^2) + j(w2\zeta w_c)}{w_c^2} \right| \\
&= -20 \log \sqrt{\frac{w_c^4 - 2w_c^2w^2 + w^4 + 4\zeta^2 w_c^2 w^2}{w_c^2}} \\
&= -10 \log \left[\frac{w_c^4 + w^4}{w_c^4} + \frac{w_c^2 w^2 (4\zeta^2 - 2)}{w_c^4} \right] \\
&= -10 \log \left[1 + \left(\frac{w}{w_c} \right)^4 + \left(\frac{w}{w_c} \right)^2 (4\zeta^2 - 2) \right]
\end{aligned} \tag{C.1}$$

For the case when $\zeta = 0.707$ (i.e. when optimally damped), then C.1 simplifies to:

$$A = -10 \log \left[1 + \left(\frac{w}{w_c} \right)^4 \right] \tag{C.2}$$

C.1.3. 1st and 2nd Order Filter Cutoff vs Attenuation

Given:

- $f_n = f_{\text{cutoff}} (n^{\text{th}} \text{ order})$.
- For 1st order, attenuation (dB) @ $f = -10 \log[1 + (\frac{f}{f_c})^2]$ [12]
- For 2nd order, attenuation (dB) @ $f = -10 \log[1 + (\frac{f}{f_c})^4]$ with $\zeta = 0.707$ [C.2]

A 1st order filter will therefore always attenuate a given frequency f less than a 2nd order filter with $f_1 = f_2$. The cutoff frequency of a 2nd order filter that will attenuate f by the same amount as a 1st order filter with a given cutoff frequency f_1 can be calculated as follows:

$$\begin{aligned}
-10 \log \left[1 + \left(\frac{f}{f_1} \right)^2 \right] &= -10 \log \left[1 + \left(\frac{f}{f_2} \right)^4 \right] \\
\left(\frac{f}{f_1} \right)^2 &= \left(\frac{f}{f_2} \right)^4 \\
\therefore f_2^4 &= \frac{f^4}{f^2} f_1^2 \\
\therefore f_2^4 &= f^2 f_1^2 \\
\therefore f_2 &= \sqrt{f \cdot f_1}
\end{aligned} \tag{C.3}$$