PQ9 & CS14
Electrical and Mechanical Subsystem Interface Standard for PocketQubes and CubeSats

Description: This document defines the use and implementation PQ9 and CS14 standard.

Revision Record

Issue	Date	Author / Editor	Reviewer	Affected Sections	Description
0.1	15-5-17	J. Bouwmeester		All	Document initiation
0.2	22-5-17	J. Bouwmeester		0	Electrical characteristics added
0.3	22-5-17	J. Chia		Appendix A	Compatibility appendix added
0.4	29-5-17	M. Boerci		0, 4.7, 0	Added mechanical characteristics, reset line description and pin definition
0.5	17-10-17	S. Radu		1,3,4	Added scope and introduction; Changed mechanical characteristics – added spacers explanation.
0.5	18-10-17	S. Radu		5, appendix B	Added reference data bus architecture Added appendix with drivers
0.6	22-11-2017	J. Bouwmeester		all	Rewritten towards public standard
0.7	23-05-2018	J. Bouwmeester		5	Modifications on data link protocol
1.0	04-07-2017	J. Bouwmeester		4,5	Added missing parts on grounding, termination and updated data link protocol. Document made ready for first public release.

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1 Background

At Delft University of Technology (TU Delft), long term research in CubeSat electrical interface standards revealed many issues with the versatile adaptation of the PC/104 electrical interface standard. The main issues identified are the major amount of bus lockups on the I^2C data bus interface, the volume consumption of the relatively big 104 pin connector and the potential compatibility issues arising from different manufacturers assigning different functions to unused/general purpose pins[1]. Also for power distribution the existing standards provide limited clarity and power efficiency [2]. Similar to the PC/104 implementation on CubeSats, a versatile electrical and mechanical interfaces standard under the name PQ60 already exists [3].

The versatility of the PC/104 and PQ60 standards, having multiple data busses to choose from and the freedom to allocate custom signals or power to general purpose pins, are appreciated by many engineers. Since both standards are implemented already in commercial products at the time of initiation of this document, they are a logical option to consider as main bus standard. However, the definition of a lean and unambiguous alternative standard for PocketQubes and CubeSats was deemed necessary in attempt to overcome identified issues and be prepared for the future.

The aim in selecting the interface standard for the satellites developed at TU Delft was to have lean, small, efficient and resilient interface. For selecting the data bus, I^2C, Differential I^2C, CAN and RS-485 were taking into consideration and the main criteria were robustness, power consumption, effective data throughput and legacy support were taken into account. The details of the trade-off can be found in a journal paper [4]. The PocketQube and CubeSat community has been involved in the research and the trade-off process for the data bus with the aid of surveys. However, the detailed definition of the PQ9 and CS14 standards are performed at TU Delft to aid a rapid definition process and avoid compromising its lean philosophy.

2 Use of the Standard

The standard is open, non-proprietary and free to use for commercial and non-commercial entities. The PQ9 and CS14 standards are not trademarked. However, the logos may only be used for systems which are fully compliant to the respective standards. New (derived) standards should use a different logo and naming in order to avoid confusion and to maintain the lean philosophy and unambiguous implementation of PQ9 and CS14.

Delft University of Technology will remain the responsible entity for the maintenance of this document. In the near future, potential updates will focus on the clarity, correctness and completeness of the document. Comments from the community related to the documents and the specified details are welcome. Changes to the standard on the high level are undesired and will not occur if no major flaws will be discovered during the verification process which is expected early 2018. Future improvements of the standard will only be performed when the interface becomes a limiting factor for the state-of-the-art technology. This is not expected in upcoming years and when this is deemed necessary the aim will be to provide backwards compatibility with the existing standard.

3 Mechanical Characteristics

Each physical subsystem will be placed in a stack and has standard outer (PCB) dimensions and four holes for mechanical fixation to the rest of the systems and/or satellite body. The mechanical outline of the boards are compatible to the CubeSat Design Specification [5] and the PocketQube Standard [6].

3.1 In-Plane System Envelope

The standard Printed Circuit Board (PCB) outline of PQ9 and CS14 is provided in Figure 1 and Figure 2 respectively. The room between the edges of the PCB and the outer structure of the satellite can be used by cabling and extensions toward the outside of the satellite. It is recommended to limit in-plane extensions of components and use of flexible wiring which can be rerouted when necessary.

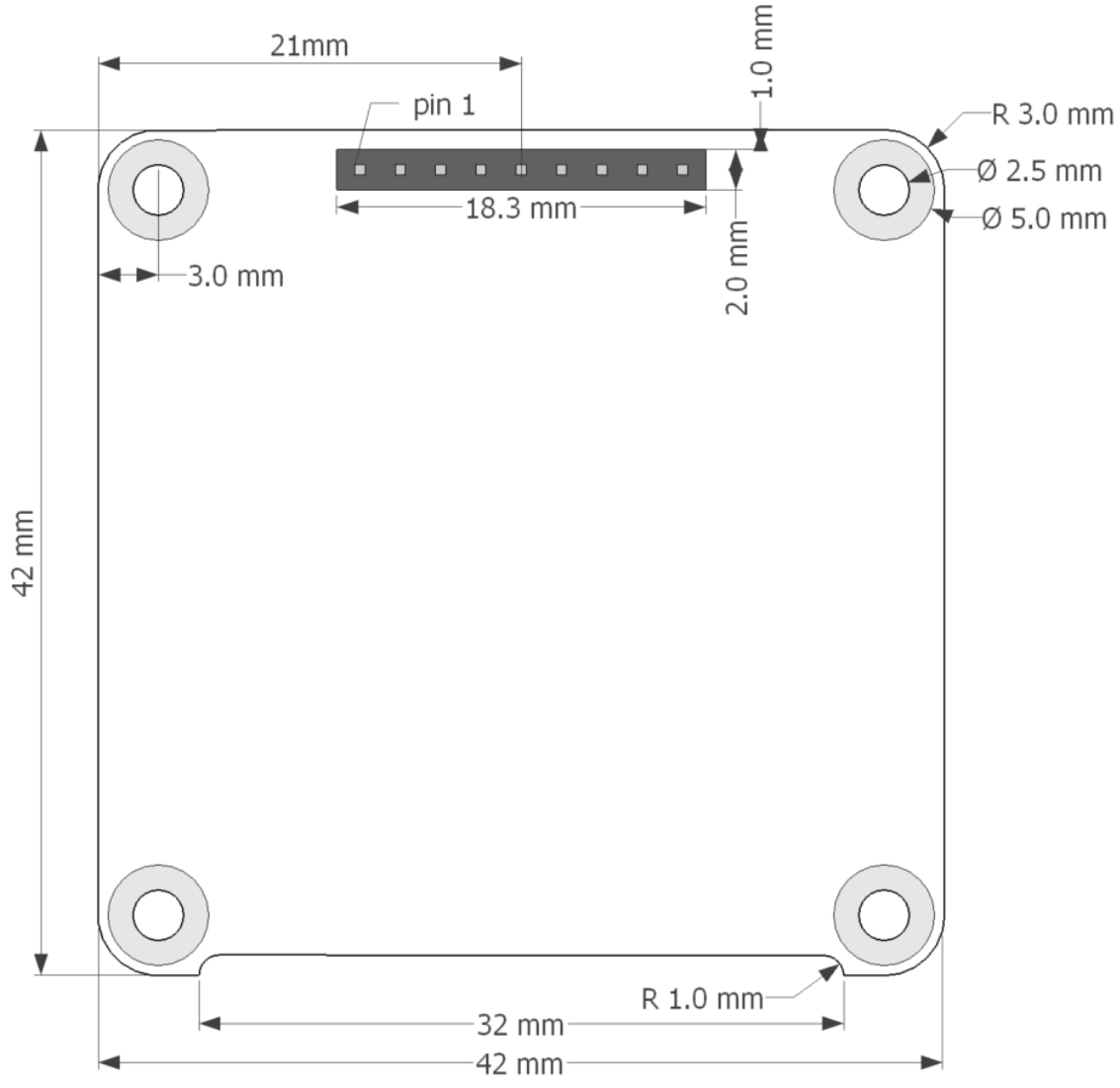


Figure 1. PQ9 printed circuit board outline

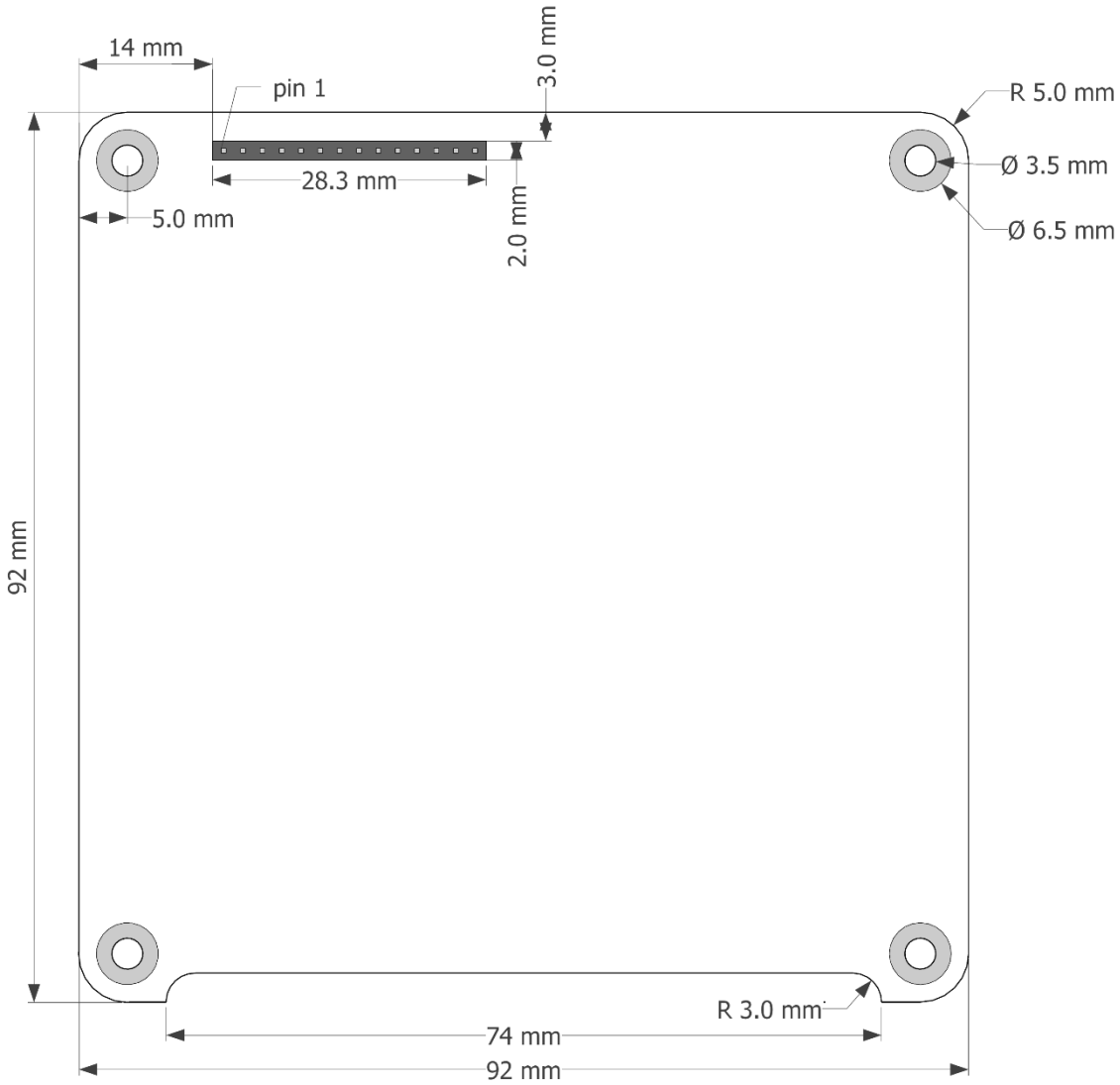


Figure 2. CS14 printed circuit board outline

3.2 Out-of-Plane System Envelope

The out of plane dimensional constraint depends on the selection of the connector(s) and possible configurations. The following requirements have to be taken into account:

- Each system has a minimum (out-of-plane) component height of 2 mm on the bottom side of the PCB. *This minimum value is used for a system with only leads on the bottom of a small connector. Note that the connector of the system below protrudes into the system envelope under consideration.*
- A 1 mm margin is required between components on the top side of the PCB and possible components on the bottom side of the next PCB.
- The PCB thickness is assumed to be 1.6mm. *In case of other PCB thickness, the potential configuration(s) need to be recalculated. Please pay attention to the minimum and maximum pin insertion depth.*

- The maximum pin soldering height is 0.65 mm.
- The rods or threaded stand-offs thread diameter is M2 for PocketQubes and M3 for CubeSats.
- The outer diameter of the spacers or stand-offs is 5 mm for PocketQubes and 7 mm for CubeSats.

The reference connector is the Samtec SQT-1xx-xx-LS series, which provides the input stated below.

- The connector height is equal to 6.35 mm [RD01]
- The pin (lead) length of the small connector (SQT-109-03-LS for PocketQubes, SQT-114-03-LS for CubeSats) is equal to 5.28 mm [RD01]
- The pin (lead) length of the large connector (SQT-109-02-LS for PocketQubes, SQT-114-02-LS for CubeSats) is equal to 15.24 mm [RD01]
- The insertion depth is required to be between 2.62 and 5.03 mm [RD01], whereas for PQ9 and CS14 the minimum and maximum considered insertion depths are respectively 3 and 5 mm.
- *Connectors if different vendors may be considered is they are fully compatible with the reference connector. In case the potential pin (lead) lengths are different, the potential configurations need to be recalculated*.

Figure 3 and Table 1 provides an example based on two systems using the small connector and a board to board distance (spacer) of 7 mm in between.

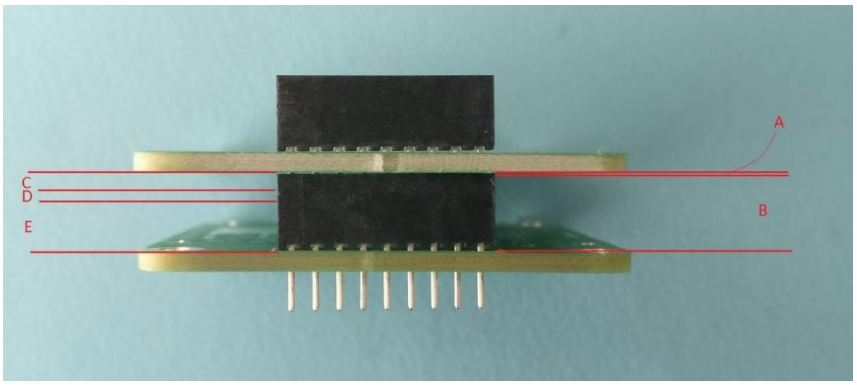


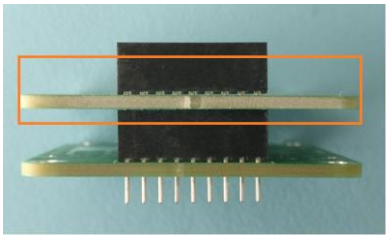
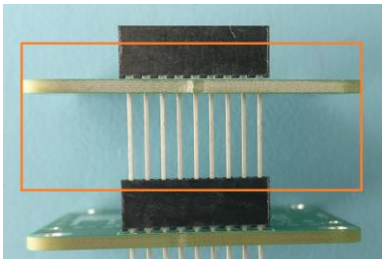
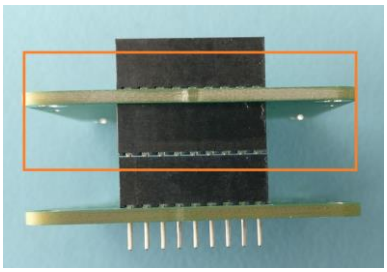
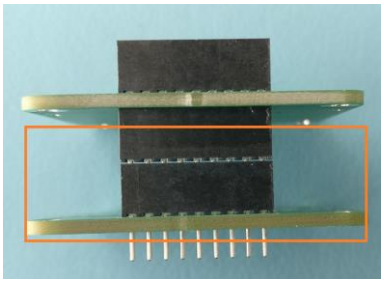
Figure 3: Out-of-plane constraints example (option I)

Table 1: Values of maximum component height and insertion depth (option I)

Symbol	Description	Value [mm]
A	Maximum soldering pad height	0.65
B	Connector height	6.35
C	Maximum height of components placed underneath upper PCB	2.00
D	Margin between components of two adjacent PCBs	1.00
E	Maximum component height	4.00
t_{PCB}	PCB thickness	1.60
$L_{pins,small}$	Pin length of the small connector	5.28
l_{depth}	Pin Insertion Depth	3.03

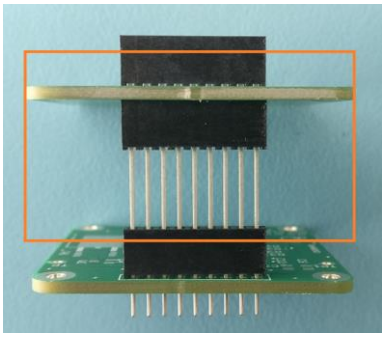
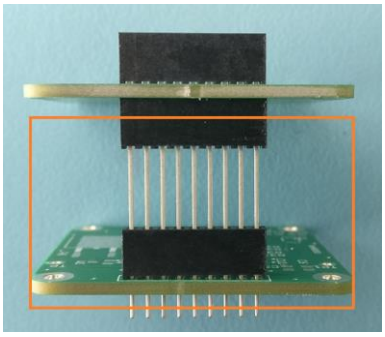
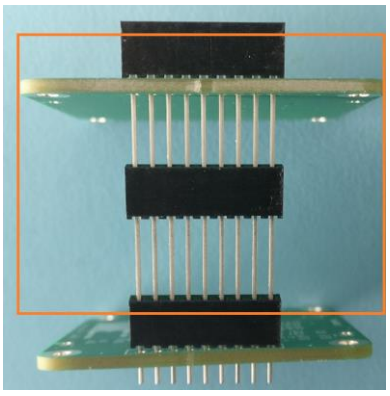
Table 2 provides the values for different configurations of the small and large reference connector. When using these values, please check if they comply with the assumptions made.

Table 2: Configuration possibilities with small and large connectors

Description	Max. comp. height above PCB [mm]	Max. comp. height below PCB [mm]	Board spacing dist.[1] [mm]	Pin insert depth [mm]	Stack height inc. 1mm margin [mm]	Example Image
Option I: single small connector on top	4.0	2.0	7.0	3.0	8.6 mm	
Option II: single large connector on top	4.0 4.0 4.0	10.0 11.0 12.0	15.0 16.0 17.0	5.0 4.0 3.0	16.6 17.6 18.6	
Option III: small connector on top, small connector glued on bottom[2]	4.0	9.0	14.0	3.9 - 4.6	15.6	
Option IV: double small connector stacked on top[3]	11.0	2.0	14.0	3.0	15.6	

1) This board spacing distance stated is the distance from the PCB surface of the largest side to the next system's PCB surface, assuming that the next system uses only a single small connector. In case the next system uses a different configuration, spacing distance needs to be calculated for this configuration.
2) fixation of bottom connector (e.g. with glue) at a spacing distance between 0.0 and 0.65 mm from the PCB is essential to prevent that this connector can slide downwards and the connector on top goes below minimum insertion depth.
3) Fixation of stacked connector at exactly 0.65mm spacing (e.g. with glue) is required to prevent that the insertion depth of the PCB above goes below minimum insertion depth.

table continued

Description	Max. comp. height above PCB [mm]	Max. comp. height below PCB [mm]	Board spacing dist.[1] [mm]	Pin insert depth [mm]	Total stack height inc. 1mm margin [mm]	Example Image
Option V: small connector on top, large connector on bottom	4.0	19.0	24.0	3.9 - 4.6	25.6	
Option VI: small connector on top, large connector stacked on top of small connector	21.0	2.0	24.0	3.9 -3.6	25.6	
Option VII: large connector on top, large connector on bottom	4.0 4.0	27.0 28.0	32.0 33.0	4.6 – 5.0 3.6 – 5.0	33.6 34.6	

1) This board spacing distance stated is the distance from the PCB surface of the largest side to the next system's PCB surface, assuming that the next system uses only a single small connector. In case the next system uses a larger sizing as well, spacing distance needs to be calculated for this configuration.

4 Electrical Characteristics

4.1 Pin Definition

Both PQ9 and CS14 are based on a single linear RS-485 data bus, several unregulated power distribution lines, a few (common) ground lines and a reset line.

The PQ-9 and CS14 interface connector pin allocations are represented in Figure 4 and Figure 5 respectively and their definition is stated in Table 3.

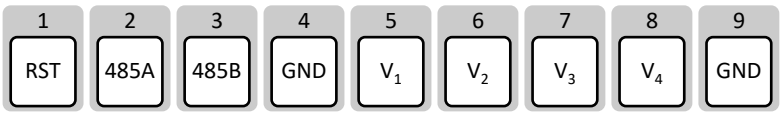


Figure 4. PQ9 (pin 1-9) interface connector

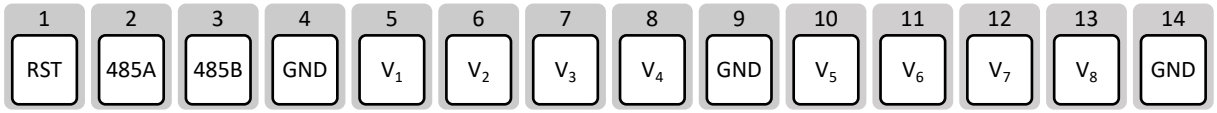


Figure 5. CS14 interface connector

Table 3. Pin allocation for PQ9/CS14 standard interface

Pin	Signal	Allocation
1	RST	system reset line (60 Ω to gnd)
2	485-B	RS-485 inverting signal
3	485-A	RS-485 non-inverting signal
4	GND	Ground
5	V_1	rec.: OBC (PQ: + Radio)
6	V_2	rec.: ADCS (PQ: + GNC)
7	V_3	rec.: propulsion
8	V_4	rec.: primary payload(s)
9	GND	Ground
10	V_5	rec.: radio
11	V_6	rec.: GNC
12	V_7	rec.: data storage & payload data transmitter
13	V_8	rec.: secondary payload(s)
14	GND	ground

4.2 RS-485 Clock Frequency

The internal microcontroller's UART will be set at a baud rate of:

500 kbit/s (500,000 bit/s) for PQ9

and

1 Mbit/s (1,000,000 bit/s) for CS14.

The clock at any subsystem may not be off by more than +/- 0.5% to ensure reliable communications. It is recommended to select the general clock frequency of the microcontroller at least 16 times higher than the baud rate (this yields 8 MHz for PQ9 and 16 MHz for CS14) .

4.3 RS-485 Compatible Microcontrollers

The microcontroller should have a UART which supports the stated clock frequency. The UART should also support 9 bits between start and stop conditions (see byte definition in section 5.1). However, it is recommend that a hardware controlled address bit detection which triggers and interrupt is included to limit the amount of data (interrupts) which need to be processed by the microcontroller. Developers using the standard should always check if a chosen microcontroller supports the byte and packet definition. Appendix A shows the compliance of a selection of microcontrollers with these requirements.

4.4 RS-485 Differential Drivers

There is a wide variety of differential drivers which can be chosen. In the current version of the standard no specific recommendations are given. An important criteria is the supported baud rates. For PQ9 this should be at least 500 kbit/s, for CS14 it should be 1 Mbit/s. Furthermore, the size of the integrated circuit and its power consumption could be important criteria to consider for which significant differences between options can be expected. Finally, slew rate limited devices are more immune to noise but it comes at the expense of a restricted supported data rate.

4.5 RS-485 Termination and Biasing

Reflection is not really a concern up to 1 MHz for PocketQubes and CubeSats, since the wavelength (~300m) in this case is orders of magnitude longer than the line length. There is thus no need to put the termination at the end of the lines to suppress reflection. For increased noise immunity however, single termination at an arbitrary point along the line is highly recommended. The chosen location for the standard is the physical board which acts as the central unit for the electrical power distribution. The reason is that such a system is always required for the CS14 and PQ9 interface standard to distribute power. A central on-board computer, being a likely master node for RS-485, is more likely to be redundant or could be integrated with another physical subsystem, yielding potential missing or redundant termination resistors in the system. The termination resistance should be 60 Ω or more. The higher the resistance, the lower the power consumption but this also reduced noise immunity.

Old generation differential drivers specify bias resistors to enforce a logic high during idle state by pulling line A to the reference voltage and line B to ground. The bias resistors can only be implemented if there is also a termination resistor and it is recommended to have a bias resistor value of 5 to 10 times the termination resistance. This forces the operation out of the undefined region between +/- 200 mV. New generation RS-485 drivers, such as the LTC1480, MAX3471 and TI SN64HVD7x have an internal fail-safe feature which do not require external biasing anymore. However, for enhanced noise immunity it can still be implemented.

4.6 Power Distribution Voltage Level and Current Limits

The distribution voltage levels are:

PQ9: 3.0 V – 4.1 V
CS14: 6.0 V – 8.2 V

These levels are based on a single Li-Ion battery cells and two in series respectively. By distributing unregulated battery voltage levels and leaving potentially required regulation to fixed voltage levels to the local subsystems, complexity is avoided and conversion efficiency losses are minimized [3].

The **absolute maximum current is 4 A** per distribution line, as determined by the connector specification assuming a maximum internal temperature of 60 °C [6]. The allowed current levels can however be lower due to the battery limitations and the power budget. It is recommended to include programmable current limiters for each distribution line.

In-rush current limits are not yet specified in this standard. Therefore, the specifications of the chosen central electrical power distribution unit needs to be followed. It is generally recommended to limit the in-rush current as much as possible at the subsystem loads.

4.7 Grounding Topology

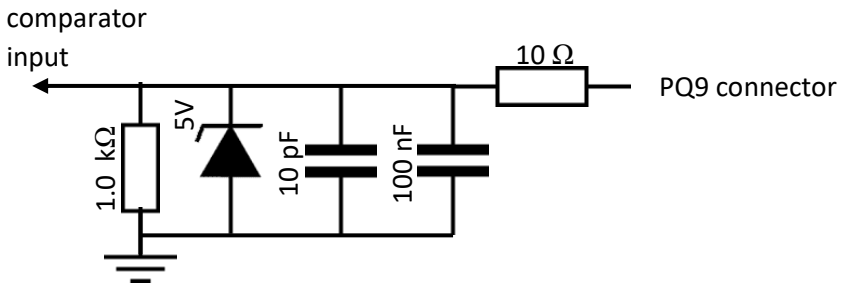
The ground pins on the PQ9 and CS14 function as common reference ground as well as power return path. This could lead to small voltage difference across a stack of physical subsystems due to their power consumption. According to [2], an extreme case of stack of 10 boards over 20 cm distance w.r.t. the electrical power distribution unit, would yield 44 mΩ resistance for one grounding path. Assuming that this should carry a return current of 4A, a maximum ground voltage offset of 200 mV can be expected. To minimize ground loops, it is important that electrically conducting structural components (for example metallic stand-offs or spacers at the corners) are only connected to the ground via a resistor of at least 1 kΩ to ensure that the electrical interface ground carries the current and not the structural elements. All electronic circuits must be connected to the PQ9/CS14 ground with a minimal path resistance.

4.8 Reset Line

A global power reset will be triggered when the line is pulled high for at least 20 ms to a minimum threshold voltage of 2 V and at maximum 5 V. At both sides of the reset line, this period should be ensured with margins appropriate for the circuit and its (thermal) environment. The driving circuit can be placed e.g. at the radio command receiver (for a tele-commanded reset) or at the on-board computer (for automatic failure detection, isolation and recovery purposes).

After a reset has been triggered, the central EPS unit is required to switch off the distribution power to all subsystems and its own microcontroller for 2000 ms. All subsystems should ensure that local power has dropped to a level which guarantees a complete power-out of volatile memory and register states within 2000 ms taking appropriate margins into account.

A standard filter and protection circuit shall be implemented close to the power reset (integrated) circuit:



The shunt bias resistor pulls the line low in idle conditions. A minimum direct current of 2 mA is required to pull the line to the threshold voltage.

The input series resistors in combination with the Zener diode protects the circuit for excessive voltage levels due to electrostatic discharge and particle radiation.

The RC filter caps have a cut-off frequency of 1.6 kHz and 16 MHz to filter out power transient and RF noise respectively.

5 Data Link Protocol

The data protocol used for PQ9 is currently only defined at the data link layer.

5.1 Byte Definition

- The chronological order is Least Significant data Bit (LSB) first
- Each byte begins and ends with a start and stop bit (UART standard)
- The address interrupt bit follows after the Most Significant data Bit (MSB). When this bit is 1, the byte contains an destination address. For any other type of byte it is 0.

This figure relates to the chronological order and not the logical order where bit 7 is on the left.. Please note that for human interpretation the 8 content bits need to be reversed in order (bit 7 on the left).

5.2 Packet Definition

- Destination/Source Address:
  - Defines the source and destination of the packet.
  - Supports up to 254 nodes (inc. master).
  - Master address: 0x00.
  - General call address: 0xFF.
  - Slave address: anything between 0x01 and 0xFE.
- Message Size:
  - Defines the length of the message in bytes.
  - Size=0x00 is used for acknowledgements.
  - Supports messages up to 255 bytes.
  - Refers only to the message content, so total packet size is message size + 5 bytes.
- CRC:
  - CRC-16 CCIT
  - Initialized on seed: 0xFFFF
  - Calculated on complete packet (so address, size + message data)
  - Calculated on least significant bit first

5.3 Data Transactions

There is only a single master node active at a time. All other devices are slave nodes and only respond upon request of the master. A redundant/back-up node which is slave or off in nominal conditions can take over the master functionality provided that the nominal master is not active on the bus anymore.

There are three types of transactions:

1. Individual message

master → slave

slave address	message size	master 0x00	one-way command/data	CRC [16 bit]

slave → master

master 0x00	ack. 0x00	slave address		CRC [16 bit]

2. Data request

master → slave

slave address	message size	master 0x00	data request command	CRC [16 bit]

slave → master

master 0x00	ack. 0x00	slave address	response data	CRC [16 bit]

3. General call

master → slave

all 0xFF	message size	master 0x00	one-way command/data	CRC [16 bit]

slaves do not respond (this should be enforced at each slave when called on the general address)

5.4 Error Handling

CRC Failure

When the CRC failed, the data packet should be discarded as a whole by the microcontroller. This minimizes the chance that slaves respond on a message which was not meant for them (e.g. bitflip on destination address) or master or slave start to interpret noise.

Time-out

The maximum time-out is 100 ms, including latency and time intervals between bytes. The counter starts at the master after the destination address byte is sent and by the slave when the it identifies its own address (or the general address). When the entire transaction is not completed within this time, both slave and master discard the information which is send. The master will internally flag that the transaction is timed-out, such that it could potentially be used by the application layer for error handling.

6 References

1. Bouwmeester J. et al., *Survey on the implementation and reliability of CubeSat electrical bus interfaces*, CEAS Space Journal Vol 9, . doi: 10.1007/s12567-016-0138-0, 2017.
2. Bouwmeester J. and Santos N., *Analysis of the Distribution of the Electrical Power in CubeSats*, The 4S symposium. ESA, Valetta, 2014.
3. Becnel E. et al., *PQ 60 Standard Document (v1.1)*, 2015.
4. Bouwmeester J. et al., *Towards an innovative electrical interface standard for PocketQubes and CubeSats*,. Adv Sp Res. doi: 10.1016/j.asr.2018.03.040, 2018.
5. California Polytechnic State University., *Cubesat design specification*, 2009.
6. Radu S. et al., *The PocketQube Standard*, 2018.

Appendix A Microcontroller-Byte Definition Compatibility

A sample selection is made of 8 microcontrollers (to be) used in PocketQubes and CubeSats, to check if the UART controller supports the byte definition, with emphasis on the address bit as interrupt. The results are provided in the following table:

Manufacturer	Microcontroller	Satellite	Can an address bit (9-bit UART) be implemented on the micro-controller?	Does the address bit trigger a dedicated interrupt?	Note
Texas Instruments	MSP432	Delfi-PQ	Y	Y	MSP432 Technical Reference manual, pg 725-753 Keyword: Address-Bit Multiprocessor Format, pg 729
Texas Instruments	MSP430	Alba Orbital OBC	Y	Y	MSP430 User's Guide, pg 571- 599 Keyword: Address-Bit Multiprocessor Format, pg 575
Atmel	AT91SAM9G20	ISISpace CubeSat OBC	Y	Y	Atmel SAM9G20 datasheet pg 354-376, 481-535 Keyword: Multidrop mode, PARE, pg 500
ARM	Cortex-M3 STM32F103C8T6	AAUSAT-3, OzQube camera module	?	Y	RM0008 Reference manual, pg 790-832 Keyword: Address mark detection, WAKE, RXNE flag, pg 806 Address bit at MSB, used 4-bit address format, the 4-bit address is at LSB
Atmel	AT32UC3C	GOMSpace CubeSat OBC	Y	Y	Atmel AT32UC3C datasheet pg 562-656 Keyword: Multidrop mode, PARE, pg 584
Atmel	ATmega328P	Arduino, OzQube, ArduiQube	Y	Y	Atmel ATmega328/P datasheet pg 225-253 Keyword: Multi-Processor Communication Mode, pg 239
ARM	Cortex-M4 MK20DX256	Ubo PocketQube, Smog-1	Y	Y	K20 Sub-Family Reference Manual pg 1201-1296 Keyword: Match address operation, pg 1274
MicroChip	PIC32MM0064FPL028	Low power, latest generation	Y	Y	PIC32MX Family Reference Manual pg 699-752 Keyword: Address Detect Mode, pg732

Appendix B Potential RS485 drivers

The list below provide a list of potential RS-485 drivers which can be used with their key specifications. Note that this list is not complete and will not be kept up to date. It focusses on the data rates required for PQ9 and CS14 and is limited to solder mounted devices.

No			Max. Data rate (Mbit/s)	Current (idle, Rx on) [mA]	Power (driving, 120Ω termination) [mA]	Package	width (mm)	length (mm)	Voltage range		Temp. Range (deg C)		Features	Datasheet
1.	Intersil	ISL32455EIUZ	1	2.1	54 or 100	8-MSOP	3.05	5.05	3	5.5	-40	85	+-60V Fault	https://www.intersil.com/content/dam/Intersil/documents/isl3/isl32450e-52e-53e-55e-57e.pdf
2.	Intersil	ISL32455EIBZ	1	2.1	54 or 100	8-SOIC	3.05	5.05	3	5.5	-40	85	+-60V Fault	https://www.intersil.com/content/dam/Intersil/documents/isl3/isl32450e-52e-53e-55e-57e.pdf
3.	Intersil	ISL32435EIUZ	1	2.1	54 or 100	8-MSOP	3.05	5.05	3	5.5	-40	85	+-40V Fault	https://www.intersil.com/content/dam/Intersil/documents/isl3/isl32450e-52e-53e-55e-57e.pdf
4.	Intersil	ISL32435EIBZ	1	2.1	54 or 100	8-SOIC	3.05	5.05	3	5.5	-40	85	+-40V Fault	https://www.intersil.com/content/dam/Intersil/documents/isl3/isl32430e-32e-33e-35e-37e.pdf
5.	Exar Corporation	XR33155	1	4	120	8-SOIC	3.05	5.05	3	5.5	-40	85	+-60V Fault	https://www.intersil.com/content/dam/Intersil/documents/isl3/isl32430e-32e-33e-35e-37e.pdf
6.	Exar Corporation	XR33038	1	0.3	120	8-NSOIC	6	5	2.8	5.5	-40	85	+-18V Fault, receiver input filtering	https://www.exar.com/ds/xr33152-xr33155-xr33156-xr33158.pdf

7.	Exar Corporation	XR33035	10	0.3	120	8-NSOIC	6	5	2.8	5.5	-40	85	+-18V Fault, receiver input filtering	https://www.exar.com/ds/xr33032-35-38_v100_022814.pdf
8.	Maxim Integrated	MAX14782EAUA	1	1.9	54 or 100	8-SO	5	6.2	3	5.5	-40	85		https://www.exar.com/ds/xr33032-35-38_v100_022814.pdf
9.	Maxim Integrated	MAX14782EATA	0.5	1.9	54 or 100	8-TDFN-EP	3.1	3.1	3	5.5	-40	125		http://datasheets.maximintegrated.com/en/ds/MAX14782E.pdf
10.	Maxim Integrated	MAX14782EASA	0.5	1.9	54 or 100	8-uMAX	3.1	5.03	3	5.5	-40	125		http://datasheets.maximintegrated.com/en/ds/MAX14782E.pdf
11.	Maxim Integrated	MAX13430EETB	0.5	1 or 2	54 or 100	10-TDFN-EP	3.1	3.1	3	5	-40	125	slew rate limited	http://datasheets.maximintegrated.com/en/ds/MAX14782E.pdf
12.	Maxim Integrated	MAX13430EEUB	0.5	1 or 2	54 or 100	10-uMAX	3.1	3.1	3	5	-40	85	slew rate limited	http://datasheets.maximintegrated.com/en/ds/MAX13430E-MAX13433E.pdf
13.	Holt Integrated Circuits	HI4850	0.5	10	54 min	8-SOIC	3.05	5.05	3	5.5	-55	125		http://datasheets.maximintegrated.com/en/ds/MAX13430E-MAX13433E.pdf