**University of Central Florida**

**Department of Computer Science**

**CDA 5106: Fall 2022**

**Machine Problem 1: Cache Design, Memory Hierarchy Design**

**by**

**Venkata Sai Kumar Ganesula**

Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student’s electronic signature: Venkata Sai Kumar Ganesula

(sign by typing your name)

MACHINE PROBLEM 1

INTERPRETATION OF RESULTS FROM EXPERIMENTS

**GRAPH 1**: (a total of 55 simulations)

Several experiments are conducted by changing the L1 cache size(l1\_cache\_size) and L1 Associativity.

L1 cache size varies as {1kb,2kb,4kb,8kb,16kb,32kb,64kb,128kb,256kb,512kb,1Mb}

L1 Associativity varies as {1(Direct), 2, 4, 8, fully associative}

Chart

Description automatically generated

**The above Plot is between L1\_miss\_rate on Y axis and LOG(L1\_Size) on X axis grouped by Associativity.**

1. Graph Trends -->

(a) For a given Associativity, the **miss rate( ↓ )** is reduced when the **cache size ( ↑ ).**

From the graph we can see the Miss rate keeps on decreasing to its lowest value, which in turn is dependent on the number of Compulsory Misses.

(b) We can also observe from graph that for given cache size, the **miss rate ( ↓ )** as the **associativity ( ↑ )**

2. Miss rate Compulsory = 0.025820 (we can interpret this from graph as well as attached results from simulations)

3. Miss rate Conflict = Miss rate – Miss rate Compulsory

(a) Direct Mapped(1- way Set Associative):

Miss rate Conflict = 0.193460 – 0.025820 = 0.16764

(b) 2-Way Set Associative:

Miss rate Conflict = 0.156030 – 0.025820 = 0.13021

(c) 4-Way Set Associative:

Miss rate Conflict = 0.142700 – 0.025820 = 0.11688

(d) 8-Way Set Associative:

Miss rate Conflict = 0.136270 – 0.025820 = 0.11045

(e) Fully – Associative:

Miss rate Conflict = 0.136960 – 0.025820 = 0.11114

**GRAPH 2:** (a total of 55 simulations)

Several experiments are conducted by changing the L1 cache size(l1\_cache\_size) and L1 Associativity.

L1 cache size varies as {1kb,2kb,4kb,8kb,16kb,32kb,64kb,128kb,256kb,512kb,1Mb}

L1 Associativity varies as {1(Direct), 2, 4, 8, fully associative}

**Chart

Description automatically generated**

**The above Plot is between AAT on Y axis and LOG(L1\_Size) on X axis grouped by Associativity.**

The lowest AAT is seen = **2.8396080629425**

For a given Associativity, the **AAT( ↓ )** is reduced when the **cache size ( ↑ ).**

Configuration corresponding to lowest AAT:

L1\_Cache\_Size = **16kb**

Assoc = **Fully Associative**

**GRAPH 3:** (a total of 27 simulations)

Several experiments are conducted by changing the L1 cache size(l1\_cache\_size) and replacement policy.

L1 cache size varies as {1kb,2kb,4kb,8kb,16kb,32kb,64kb,128kb,256kb}

Replacement policy varies as {LRU, PLRU, OPT}

Chart, line chart

Description automatically generated

**The above Plot is between AAT on Y axis and LOG(L1\_Size) on X axis grouped by Replacement policy.**

The lowest AAT is seen = **2.86925004959106**

For a given replacement policy as the **L1\_cache\_size( ↑ )** the **AAT ( ↓ )**

Configuration corresponding to lowest AAT:

L1\_Cache\_Size = **32kb**

L1\_assoc = constant (4)

Replacement Policy = **Optimal Replacement policy**

**GRAPH 4:** (a total of 12 simulations)

Several experiments are conducted by changing the L2 cache size(l2\_cache\_size) and inclusive property.

L2 cache size varies as {2kb,4kb,8kb,16kb,32kb,64kb}

Inclusive Property varies as {non-inclusive, inclusive}

Chart, line chart

Description automatically generated

**The above Plot is between AAT on Y axis and LOG(L2\_Size) on X axis grouped by Inclusive property.**

The lowest AAT is seen = **9.28164434**

Configuration corresponding to lowest AAT:

L2\_Cache\_Size = **4kb**

Inclusive property = **non inclusive property**