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PULP: A Ultra-Low Power Parallel Accelerator for Energy-Efficient and Flexible Embedded Vision

Francesco Conti, Davide Rossi, Antonio Pullini, Igor Loi, Luca Benini

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Abstract Novel pervasive devices such as smart surveillance cameras and autonomous micro-UAVs could greatly benefit from the availability of a computing device supporting embedded computer vision at a very low power budget. To this end, we propose PULP (Parallel processing Ultra-Low Power platform), an architecture built on clusters of tightly-coupled OpenRISC ISA cores, with advanced techniques for fast performance and energy scalability that exploit the capabilities of the STMicroelectronics UTBB FD-SOI 28nm technology. We show that PULP performance can be scaled over a 1x-354x range, with a peak theoretical energy efficiency of 211 GOPS/W. We present performance results for several demanding kernels from the image processing and vision domain, with post-layout power modeling: a motion detection application that can run at an efficiency up to 192 GOPS/W (90% of the theoretical peak); a ConvNet-based detector for smart surveillance that can be switched between 0.7 and 27fps operating modes, scaling energy consumption per frame between 1.2 and 12mJ on a 320x240 image; and FAST+Lucas-Kanade optical flow on a 128x128 image at the ultra-low energy budget of 14 µJ per frame at 60fps.

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Francesco Conti · Davide Rossi · Igor Loi · Luca Benini
Department of Electrical, Electronic and Information Engineering, University of Bologna
E-mail: {f.conti,davide.rossi,igor.loi,luca.benini}@unibo.it

Antonio Pullini · Luca Benini
Integrated Systems Laboratory, ETH Zurich,
E-mail: {pullinia,lbenini}@iis.ee.ethz.ch

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1 Introduction

With the introduction of cheap and powerful embedded computing devices such as Qualcomm Snapdragon 810 [7] and Nvidia Tegra K1 [5], the computer vision field has started to shift from theory and PC-based prototypes towards embedded applications such as smart cameras, self-driving cars and semi-autonomous robots. However, all current vision devices depend on the availability of a relatively abundant source of energy such as a mobile phone battery, which prevents integration of significant vision capabilities in devices that must run on very limited power and energy budgets, such as micro- or nano-UAVs that have a limited payload to host a battery or wireless sensor nodes (WSNs) that run on harvested power or must live years on a single charge [43]. These devices typically employ low power and ultra-low power microcontroller units (MCUs) that cannot cope with the heavy workloads of CV algorithms, even for very small images.

The ideal computing platform for this kind of heavily energy-constrained applications would be a low power, yet flexible fabric that is able to provide significant performance when needed and remain in a very low-consumption state when not. In particular, smart cameras, micro-UAVs and other similarly constrained applications that are designed to work with input from low-power imagers and performing vision-related algorithms need an exceptional degree of performance and energy scalability to cope both with the limited energy budget and with the frame-rate requirements of vision

applications. At the same time, a computing fabric answering to these needs should also provide a very high level of programmability with an easy-to-use model, to keep on track with the fast-moving CV field.

In this work we introduce *PULP* (Parallel processing Ultra-Low Power platform), a many-core platform answering to these demands. To achieve high performance when needed, PULP features clusters of simple, yet complete, OpenRISC [11] cores that can be used to exploit both coarse- and fine-grain data level parallelism or task level parallelism. At the same time, operating points (voltage, frequency, body biasing) can be controlled at a fine granularity and high speed to achieve high energy efficiency when the performance constraints are more relaxed or when the power budget is tighter. The proposed PULP platform exploits the capabilities of STMicroelectronics Ultra-Thin Body and Box Fully Depleted Silicon-on-Insulator (UTBB FD-SOI) technology [33] that, in contrast with deep submicron bulk technologies, allows to exploit an extended body bias range to modulate the performance/energy trade-off at different operating points.

We put our platform to test using several vision benchmarks, which were implemented in pure C code using the OpenMP programming model to express parallelism. Two benchmarks are targeted at the smart surveillance use case. The first is absolute difference motion estimation, a well known highly parallel algorithm that can be used to detect intruders in a camera stream, and is also a component of successful video compression algorithms[54]. The second benchmark is based on Convolutional Neural Networks (*CNN*s or *ConvNet*s) [40], a model that is state-of-art in many current CV benchmarks and has shown promising accuracy results in new classification, detection, and full-scene understanding tasks. CNN-based algorithms are typically computationally demanding and require a good level of performance to work at acceptable frame rates. Finally, to demonstrate the micro-UAV use case for a device such as PULP, we provide a benchmark based on Lucas-Kanade optical flow [42] that can be used as input for self-stabilization and hovering in an aerial vehicle.

The paper is organized as follows: Section 2 reports related works, introducing the state of art of research on energy-efficient embedded computing platforms, particularly those devoted to embedded vision. Section 3 overviews the architecture of the PULP platform, and its features to support low-power computing. Section 4 details our implementation results, it compares PULP with several other platforms and analyzes performance and energy efficiency in three benchmarks: motion detection, convolutional neural networks and optical flow.

2 Related work

Architectural research on many-core architectures has focused on tiled platforms; each tile contains one or more cores and communicates with other tiles through a scalable medium. The dominating paradigm is that of general-purpose and embedded GPUs such as NVIDIA Tegra [53]. GPUs feature a restricted SPMD-based execution model that can be suboptimal for CV applications, which have often an irregular structure [19][44]. Many-core platforms with clusters of RISC cores have been proposed as a more flexible model: examples include STMicroelectronics *P2012* [12], which is programmable in OpenCL [47] and OpenMP [45]; and Kalray *MPPA* [24], which supports a proprietary KPN-based programming model as well as OpenMP. All these platforms target a different power budget (from a few watts to several hundred milliwatts) with respect to the PULP platform we present in this paper.

To improve energy efficiency, many CV-targeted platforms rely on clusters of VLIW cores; for example, Movidius *Myriad* [50] features 8 SHAVE clusters, each including a VLIW core. Other examples are the TI *AccelerationPAC* [41], which includes several EVE clusters composed of a RISC processor and a VLIW coprocessor, and the Qualcomm Hexagon DSP [20] that accelerates a Snapdragon 800 with VLIW DSPs. While it is technically possible to develop new functionality for these platforms, all heavily rely on intrinsics, specialized assembly languages and other very low level programming models to deliver maximum performance and efficiency.

Trading off flexibility for additional efficiency, many CV-focused platforms rely on fixed-function HW blocks. Most of these platforms are dataflow engines, often implemented on FPGAs or CGRAs. Examples of this approach include *Vortex* [52][60] for biologically-inspired vision acceleration, and *NeuFlow* [26] and TeraDeep *nn-X* [29], which focus on ConvNet acceleration. Another high-performance platform based on a combination of coarse- and mid-grain reconfigurable blocks and embedded FPGA blocks is *Morpheus* [57], that can reach up to 50 GOPS/W energy efficiency on a variety of applications. Also some commercial products follow this path: for example the Analog Devices *Blackfin* [2] features a fixed-function Pipelined Vision Processor for CV acceleration. Another approach is to augment an existing many-core with fixed-function accelerators or coprocessors, as is done in *He-P2012* [21].

None of the platforms reported above currently targets ultra-low power operation, as their power budget ranges from hundreds of milliwatts to several watts. At the other end of the spectrum, microcontrollers can easily target power budgets of 50 mW and below, even in

the case of high performance MCUs such as the STMicroelectronics STM32F401, based on a ARM Cortex-M4 [9]. State-of-art ULP microcontrollers can work with less than 10 mW: examples include the SiliconLabs *EFM32* [8], Texas Instruments *MSP430* [10] families of MCUs, and *Ambiq Apollo* [1]. Significant efficiency can be reached by near-threshold microcontrollers such as the one shown in Ickes et al. [32], *SleepWalker* [13] and *Bellevue* [14], which also exploits SIMD parallelism to further improve performance.

Since the performance level attainable by these low-power MCUs is too low for most CV applications, many CV-focused ULP accelerators employ fixed-function HW blocks [66][34][51]. Application specific architectures for low-power computer vision include designs trying to exploit alternative approaches to computation with respect to the traditional Von-Neumann ones; examples include state-of-art ASICs implementing spiking neural networks [48][37]. In some cases computation may be performed in the analog domain, for example in mixed-signal ASICs based on cellular neural networks [18]; another example is that of integrating simple filtering capabilities directly within the vision sensor [16].

A class of designs that are more directly comparable to our PULP platform is that of parallel low-power processors. *Centip3de* [27] consists of a large scale 3D-integrated fabric of clusters of Cortex M3 cores. With 64 cores running at 10 MHz, it can reach a performance of 0.64 GOPS. *DietSODA* [62] features 128 SIMD lanes working at lower frequency (50 MHz) than the rest of the chip, reaching up to 6.4 GOPS. These multicore platforms achieve efficiency levels comparable to those of PULP, but they compromise on programmability and flexibility; moreover, to the extent of our knowledge results on their power/performance scalability have not been provided. Dogan et al. [25] explore multicore design in subthreshold for biomedical usage, with a power budget as low as 10 µW that is more than one order of magnitude the power budget of PULP; however, this comes at a huge cost in terms of performance that also hits overall energy efficiency. To the best of our knowledge, the only commercial ULP multicore microcontroller on the market is the NXP LPC51400 [6], that asymmetrically couples a Cortex-M4 powerful microcontroller with a low-power Cortex-M0 for sensor control.

The first application we chose to evaluate PULP is smart visual surveillance, with the motion estimation and CNN benchmarks. Motion estimation is a well-known algorithm that is part of video standards such as MPEG [54], with known hardware (e.g. Hsieh et al. [31]) and software (e.g. Brockmeyer[15]) implementations. Conversely, Convolutional Neural Networks (CNNs or

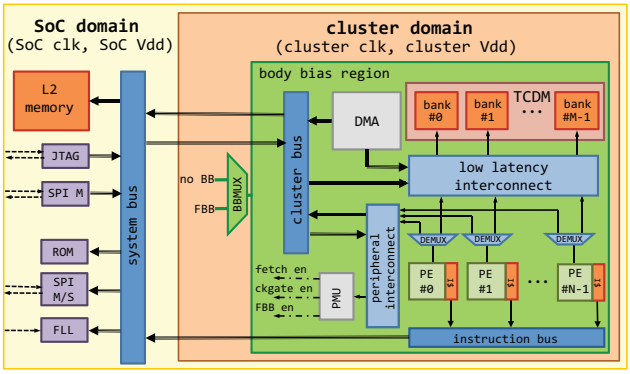


Fig. 1: PULP architecture.

ConvNets), originally proposed by LeCun et al. [40], have been object of many recent developments that were rekindled by the discovery of efficient ways to train them [39]. ConvNets have been used to obtain state-of-art accuracy results on scene labeling, video classification and object detection and interest in their applications has been shown by companies such as Google [35][64], Microsoft [23] and Facebook [67].

Future applications for scalable ultra-low power and energy computing devices are beginning to emerge in many fields, such as that of micro-UAVs and of smart and ubiquitous surveillance. State-of-art work on autonomous UAVs focuses on relatively big UAVs that are driven by full desktop-class processors and GPUs [61] [30]; to achieve full autonomy in micro-UAVs with much more limited batteries and payload a breakthrough in computing efficiency is needed. Wood et al. [65] quantify the total power budget for this kind of vehicle as 102 mW, of which only 5 mW can be dedicated to sensing and computation. In a similar fashion, smart wireless cameras acting as wireless sensor network nodes need to perform relatively complex activities in a reduced amount of time, while keeping the energy consumption at a minimum [17].

3 Architecture

3.1 PULP SoC overview

PULP (Parallel processing Ultra Low Power platform) is a scalable, clustered many-core computing platform able to operate on a large range of operating voltages, achieving in this way a high level of energy efficiency over a wide range of application workloads. Figure 1 shows the main building blocks of a single-cluster SoC. The PULP fabric is integrated in a SoC featuring a L2 memory (sized in the 32 kB to 128 kB range) shared

among all clusters through a system bus, plus IO peripherals that provide flexibility to the whole platform.

The set of peripherals integrated in the PULP platform includes two SPI (Serial Peripheral Interface) interfaces (one master and one slave), GPIOs, a bootup ROM and a JTAG interface suitable for testing purposes. Both SPI interfaces can be configured in *single* mode or *quad* mode depending on the required bandwidth, and they are suitable for interfacing the SoC with a large set of off-chip components (non volatile memories, voltage regulators, cameras...). Moreover, the SPI slave can be configured as a master, and a set of enable signals placed on both SPI interfaces allow the SoC to interface to up to 4 slave peripherals.

Thanks to its peripheral architecture the SoC is able to operate in two different modes: *slave* mode or *stand-alone* mode. When configured in slave mode, PULP behaves as a many-core accelerator of a standard *host* processor (e.g. an ARM Cortex M low-power microcontroller). In this configuration the host microcontroller is responsible for loading the application and processing data on the PULP L2 through the SPI master interface, and initiate and synchronize the computation through dedicated memory mapped signals (e.g. fetch enable) and GPIOs. When configured in stand-alone mode the SoC detects the presence of a flash memory on its SPI master interface, booting from the external flash if connected, from the L2 memory otherwise.

3.2 Cluster architecture

The cluster architecture features a parametric number of Processing Elements (*PE*s) consisting of a highly power optimized microarchitecture based on OpenRISC 32-bit ISA [11], each one with a private instruction cache (*I$*). The refill ports of all instruction caches converge on a common cluster instruction initiator port through a cluster instruction bus. The OpenRISC cores were optimized to achieve a high IPC on a wide variety of benchmarks, including control-intensive code [28]. Energy efficiency is boosted by using a flat pipeline to reduce register and clocking overhead, while the datapath was area-optimized to reduce leakage. Further, extensive architectural clock gating was employed to reduce spurious dynamic power.

The PEs do not have private data caches, avoiding memory coherency overhead and increasing area efficiency, while they all share a L1 multi-banked tightly coupled data memory (*TCDM*) acting as a shared data scratchpad memory. The TCDM has a number of ports equal to the number of memory banks providing concurrent access to different memory locations. Intra-cluster communication is based on a high bandwidth *low-latency interconnect*, implementing a word-level interleaving scheme to reduce access contention [55].

A lightweight, ultra-low-programming-latency, multi-channel DMA enables fast and flexible communication with other clusters, the L2 memory and external peripherals [56]. The DMA uses minimal request buffering and features a direct connection to the TCDM, to eliminate the need for internal buffering, which is very expensive in terms of power. A peripheral interconnect provides access to all the cluster peripherals and to all the resources external to the cluster.

3.3 Power management

In order to provide the best energy efficiency across a wide range of workloads, each cluster can work at its own voltage and frequency. To enable fine grained tuning of the SoC frequency, a FLL (Frequency-Locked Loop [49]) is included as a peripheral at SoC level. Moreover, a set of clock dividers (one for the SoC + one for each cluster) allow to further divide the clock generated by the FLL. To reduce the dynamic power consumption in idle mode, each processor can be separately disabled and clock-gated through a set of registers mapped on the peripheral interconnect. In this way, depending on the required workload, each cluster is able to work with an arbitrary number of processing elements, while the others consume zero dynamic power.

A body bias multiplexer (*BBMUX*) allows to dynamically select the back-bias voltage of the cluster, enabling ultra-fast transitions between the normal operating mode and the boost mode when temporary peaks of computation are required by the applications. To reduce the latency of the transitions between different operating modes, and making them transparent to the software, a power management unit (*PMU*) was added to generate the control signals of the processors fetch enables, clock gating units, and BBMUX.

4 Benchmarking PULP

This section examines the implementation results of the PULP platform on a reference configuration, providing an estimation of the area of the platform, of the energy efficiency at the different operating points, and a comparison with other state of the art multi-core platforms for embedded computing. It also reports the results of our evaluation of performance and energy in the motion estimation, ConvNet and optical flow benchmarks.

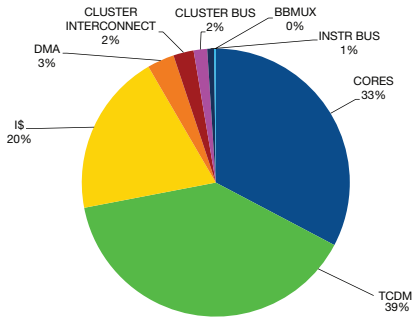


Fig. 2: PULP cluster area breakdown.

V_{DD} [V]	f_{max}[MHz] $V_{FBB} = 0V$	f_{max}[MHz] $V_{BB} = 0.5V$	f_{max}[MHz] $V_{BB} = 1V$
0.3	**2.5**	4.45	6.31
0.4	**22**	35.9	**49.1**
0.6	**200**	**277**	**350**
0.8	400	**484**	**563**
1.0	588	**650**	**705**
1.3	**775**	**836**	885

Table 1: Supply voltage and peak frequencies for the reference PULP cluster. Bold values indicate reference operating points.

4.1 Implementation results

In the context of this work we consider a single cluster PULP implementation operating in stand-alone mode. Thus, we assume the SoC connected to an external flash memory which contains the application code, a video surveillance camera periodically feeding the L2 of the SoC with a new frame, and a programmable DC/DC converter configured by the cores to switch between the idle, *search* and *follow* mode described in Section 4.4. The L2 memory was sized at 128 kB to fit both the program code and one 320x240 frame. The cluster consists of 8 cores featuring 1 kB of I$ each, while the TCDM is composed of 16 banks of 2 kB each, leading to an overall TCDM size of 32 kB. These architectural parameters were chosen to fit the constraints of the benchmarks described in Section 4, and should be sufficiently flexible for a broad variety of vision tasks. Both the TCDM banks and the processor's I$ are implemented using standard cell memory (SCM) cuts of 4 kbits each. While SRAMs may achieve a higher density than SCMs (by a factor of ∼3x), SCMs are able to work at the same voltage ranges as the rest of the logic, with the key benefit of providing much smaller energy/access (∼4x)[46].

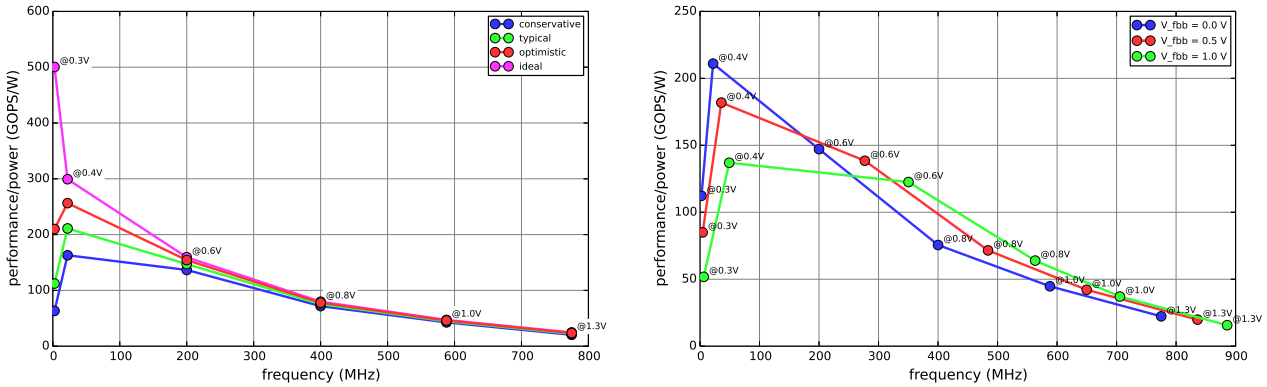
Our results refer to a post place & route implementation of the proposed SoC in STMicroelectronics 28nm UTB FD-SOI technology. Thus, they include the overheads (i.e. timing, area, power) caused by the clock tree implementation, accurate parasitic models extraction, cell sizing for setup fixing and delay buffers for hold fixing (neglecting these would cause significant underestimations in the clock tree dynamic power). The SoC was synthesized with Synopsys Design Compiler, the place & route was performed using Cadence SoC Encounter, and the signoff was performed using Synopsys StarRC for parasitic extraction and Synopsys PrimeTime for timing and power analysis.

We tested our platform with power supplies ranging from 0.3V to 1.3V and forward body biasing ranging from 0 to 1V in the typical corner case at the temperature of 25°C. Table 1 shows the peak frequency that the PULP cluster can reach at each operating point. Being the cluster composed of 8 cores, the theoretical performance of the platform can easily scale between 20 MOPS @0.3V, no BB to 7 GOPS @ 1.3V, 1.0V FBB, demonstrating the dramatic performance scalability (354x) that can be exploited on PULP.

Figure 2 shows the area breakdown of the cluster, where the overall cluster area in the considered configuration is 1.2 mm^2. It is possible to note that the TCDM and the cores I$ occupy ∼59% of the overall cluster area, mainly due to the SCM based implementation. However, this is fully compensated by the improvement in terms of dynamic power consumption of the memories, which are responsible for the ∼15% of the overall cluster dynamic power, with an improvement of ∼4x with respect to a previous implementation of the same architecture [28].

4.2 Energy efficiency analysis

This section provides an evaluation of the energy efficiency of the proposed PULP implementation at the different operating points that can be exploited on the platform. To cope with the leakage power variation in the 28nm UTB FD-SOI, cell libraries are characterized very conservatively; early silicon measurements on PULP prototypes showed that there is more than a 2x guardband on power models. For this reason, we first evaluated the energy efficiency of the platform in four scenarios, accounting for various levels of pessimism for leakage: *conservative*, where the leakage power is directly extracted from the standard cell libraries; *typical*, with leakage scaled down by 2x; *optimistic*, where it is scaled down by 5x; and *ideal* with no leakage. This experiment allowed us to quantify the impact of the leakage power model guardband over our energy efficiency estimation.



(a) GOPS/W while scaling the leakage contribution to power.

(b) GOPS/W with 0V, 0.5V and 1.0V FBB.

Fig. 3: PULP energy efficiency in GOPS/W.

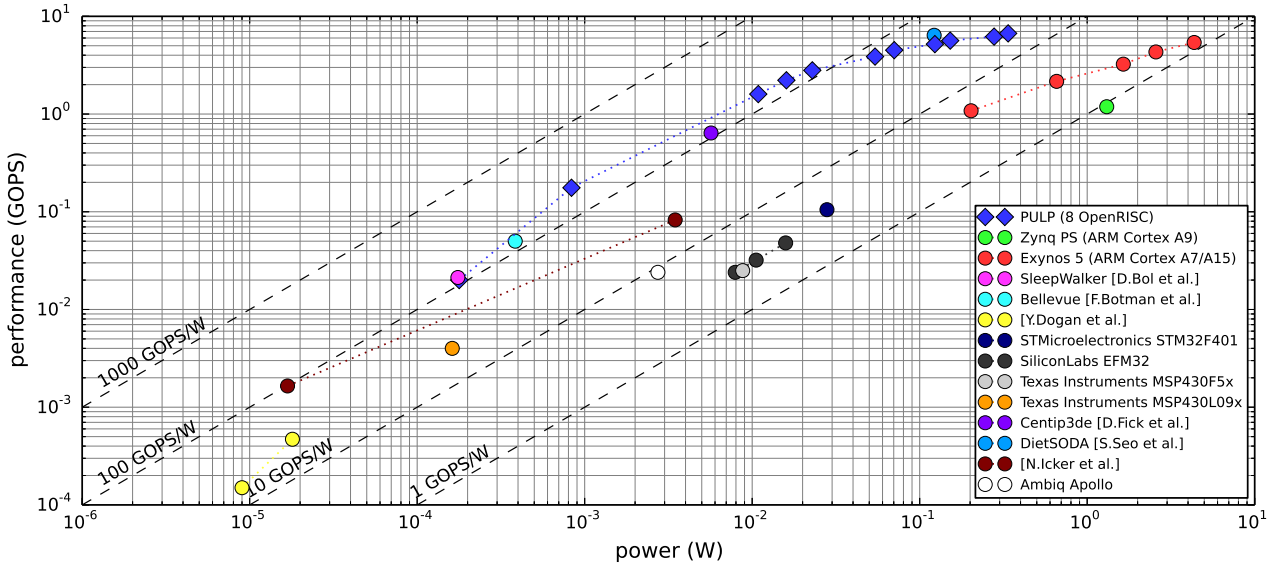


Fig. 4: Energy efficiency comparison with several platforms.

Figure 3a shows the results of this exploration; the platform is working at the maximum operating frequency achievable at each given supply voltage. The peak energy efficiency points in the four scenarios are 172 GOPS/W, 211 GOPS/W, 262 GOPS/W, and 500 GOPS/W respectively. The best energy efficiency point is around 0.4V in all the scenarios except for the ideal. In all but the ideal scenario, the impact of leakage power is huge in the 0.3V to 0.4V operating range, when the supply voltage V_{DD} is close to V_{th} (0.28V for this technology), due to the relatively slow operating frequency (2.5 MHz to 50 MHz) that causes the static contribution of leakage to be dominant. On the other hand, when working with V_{DD} larger than 0.6V, the combined effect of increased dynamic power density (which scales as V_{DD}^2), and higher operating frequency causes the impact of leakage to be smaller. In the rest of the paper we only consider the typical scenario with a twofold leakage reduction as our reference for further power estimations and comparisons; measurements on a previous batch of fabricated PULP prototypes suggest that this is the most realistic value.

Figure 3b shows what happens when forward body biasing (FBB) is introduced. By applying FBB, it is possible to dynamically modulate the V_{th} of transistors to improve the frequency without changing the supply, with only a slight increase of dynamic power in the high-V_{DD} range. On the other hand, FBB introduces an overhead in leakage power, quantifiable as a 7x increase when V_{BB} is 1V [33]. For these reasons, FBB is

an effective knob to increase the energy efficiency by up to 1.5x for workloads larger than 1.6 GOPS (200 MHz). For example, the target workload of 3.2 GOPS (400 MHz) can be achieved @0.8V with 0V FBB or @0.6V with 1V FBB, resulting in a 1.5x improvement in energy efficiency.

To further provide insight into the scaling capabilities of the PULP platform, in Figure 4 we investigate energy efficiency in terms of peak GOPS per watt. We compare the reference PULP platform with several other commercial and academic platforms: the Processing System of the Xilinx Zynq platform (i.e. a dual core ARM Cortex A9), a Samsung Exynos 5 (i.e. a ARM big.LITTLE quad-core A7 + quad-core A15), and many of the ULP platforms referenced in Section 2. PULP, providing up to 211 GOPS/W, is competitive with microcontrollers specialized for low-power (Bellevue, SleepWalker) and more performant parallel ULP platforms (Centip3de, DietSoda), and is much more efficient than mobile solutions such as the Exynos 5 due to the simpler, optimized architecture of the OpenRISC cores and to the fine-grain knobs for power management provided by the FDSOI technology. It must also be noted that both Centip3de and DietSoda do not support a programming model, whereas PULP has been designed for compatibility with standards such as OpenCL and OpenMP, to ease the exploitation of potential performance in applications.

4.3 Motion estimation benchmark

As a first test for the PULP cluster, we wrote an absolute difference motion estimation [54] benchmark composed of several simple kernels: background subtraction, absolute value, binarization, erosion, dilation and a Sobel filter. The aim of the proposed algorithm is to detect the presence of external objects on a video transmitted by a camera framing a fixed background. For each video frame the first stage performs the absolute difference between the current and the background image. The resulting maximum value is extracted and used to calculate the threshold for binarization. The binarized image is then processed by three spatial operators. Erosion and dilatation implement the opening kernel which denoises the binarized image, while edge detection is implemented through a bidimensional Sobel convolution filter to create the external object boundary. If an external object is detected, the final kernel returns the highlighting of that object on the original frame.

The motion estimation benchmark runs on an input 8-bit grayscale 176x120 QCIF image produced by a low-power camera and loaded on the PULP L2 memory along with a prerecorded background. The program code occupies 12508 bytes in the L2 memory. Since the full image cannot fit in the TCDM, we divided the input image in slices or *tiles* of 44x20 pixels that are loaded into the TCDM and processed separately. Each tile occupies 1320 bytes in the TCDM, with a total TCDM occupation of 10560 bytes (four buffers used for present tile output computation, plus four used for double buffering).

Figure 5a shows the speedup of parallel versus sequential execution. This kernel is relatively simple and linear and completely parallelizable; as a consequence, its performance scales nicely up to 16 cores. The slight gap between the theoretical and simulated performance is mainly caused by the calculation of the maximum pixel value after the binarization stage, that cannot be completely parallelized over the available cores. Even so, as that is the only sequential part of the benchmark, speedup and energy efficiency are almost ideal. Figure 5b shows that energy efficiency of the motion estimation benchmark peaks at 192 GOPS/W at the 0.4V operating point, 90% of the theoretical limit.

4.4 ConvNet benchmarks

4.4.1 Convolution-accumulation optimization

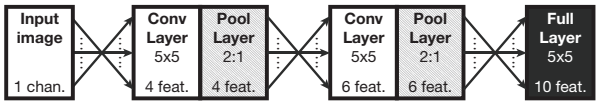
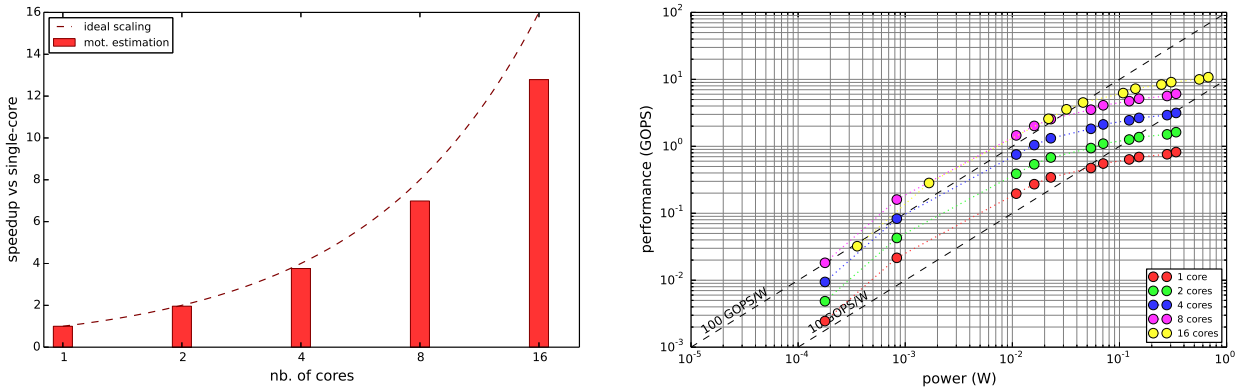


Fig. 6: Reference convolutional network.

A CNN is composed by a deep sequence of convolutional or fully-connected linear layers intermixed with pooling ones to perform a transformation on *feature maps* produced by the previous layer. Weights in convolutional and linear layers are trained by backpropagation but are used thereafter in a strictly feedforward fashion; due to their data parallel nature they are a natural candidate for acceleration in a parallel platform such as PULP. Convolutional layers in CNNs compute output feature maps of a layer as sums of convolutions over input feature maps; therefore, we chose to use a *convolution-accumulation* step as our basic kernel: $y(i,j) := y(i,j) + \Big(W * x\Big)(i,j)$. where x is the input image, W is the convolution kernel and y is the output image.

We used 16-bit fixed point numbers for inputs, kernels and outputs. We implemented three versions of convolution-accumulation: `naive` directly implements it



(a) Parallel speedup over sequential execution (1 tile).

(b) Energy efficiency (1 tile).

Fig. 5: Motion estimation benchmark results.

Implementation	**3x3**	**5x5**	**7x7**	**9x9**	**11x11**
`naive`, single thread	0.26	0.32	0.34	0.35	0.36
`1-unrolled`, single thread	0.52	0.62	0.65	**0.69**	**0.88**
`2-unrolled`, single thread	**0.80**	**0.83**	**0.76**	0.26	0.18
`naive`, 8 threads	0.26	0.31	0.34	0.35	0.36
`1-unrolled`, 8 threads	0.49	0.60	0.65	**0.69**	**0.85**
`2-unrolled`, 8 threads	**0.71**	**0.77**	**0.74**	0.27	0.18

Table 2: Convolution-Accumulation: average efficiency/core

as four nested loops (two on the output pixels and two for the convolution kernel W); `1-unrolled` uses manual loop unrolling on the innermost loop; `2-unrolled` uses loop unrolling on the two innermost loops. We benchmarked these convolutions with a single thread or 8 parallel threads[1].

Table 2 shows the efficiency/core for the various convolution-accumulation implementations on a 32x32 input image, computed as the ratio between useful (i.e. computation) cycles and the total number of cycles spent in the outermost loop. For smaller convolution kernels, unrolling both inner loops provides a much better efficiency; however, for kernels bigger than 7x7, efficiency is reduced by I$ misses due to the size of the unrolled loop. As a consequence, the tighter `1-unrolled` convolution-accumulation step is more convenient for bigger kernels. Results are similar in the multi-threaded case, as data contention on the TCDM causes on average only a small amount of efficiency decrease.

[1] We used the `or1k-elf-gcc` compiler (build `4.9.0 20140308`), with the following flags: `-O2 -nostdlib -mhard-mul -msoft-div`.

4.4.2 Use case: CNN for visual surveillance

On top of these optimized convolutions, we developed a network based on the one proposed by LeCun et al. [40] for MNIST classification, which is shown in Figure 6. This network has 2220 parameters and a footprint of 11408 bytes for data and 4400 bytes for weights on the L1 TCDM; Table 3a summarizes them. The program code uses 16768 bytes on the L2 memory. As shown in Conti et al. [22], a network of this kind can be trained for complex object detection tasks by running it on a window sliding over the input frame.

We use this CNN for visual surveillance. The platform spends most of the time in a low-power *search* mode looking for suspicious objects (as this task requires only a relatively low frame rate), and it switches to a high-performance *follow* mode to keep track of a previously detected object. Input frames are brought inside the PULP cluster by DMA transfer from the L2. This transfer is superimposed to the computation of deeper layers and has no impact on the final throughput.

Figure 7a shows the performance of the reference CNN when run on a 32x32 image patch, scaling the clock frequency of the cluster from 100 MHz to 1 GHz and the number of OpenRISC cores in the PULP cluster between 1, 2, 4, 8 or 16. As expected from a highly data-parallel algorithm such as ConvNets, execution time scales almost linearly with the number of cores. In our visual surveillance application, the ConvNet is run on a 32x32 window spanning a QVGA (320x240) image with a stride of 32 pixels. Each frame is spanned two times: one with no offset, the other with an offset of 16 pixels in both directions so that the chance of missed detections on the border of a window are reduced. PULP can be set to work at a very low frame rate (∼0.7 fps at

layer	params			memory (*bytes*)	
	# *feat.*	*filter size*	*data size*	*weights*	*data*
`input`	1	-	32x32	0	2048
`conv 0`	4	5x5	28x28	200	6272
`pool 1`	4	-	14x14	0	1568
`conv 2`	6	5x5	10x10	1200	1200
`pool 3`	6	-	5x5	0	300
`full 4`	10	5x5	1x1	3000	20

(a) *small* CNN.

layer	params			memory (*bytes*)	
	# *feat.*	*filter size*	*data size*	*weights*	*data*
`input`	1	-	32x32	0	2048
`conv 0`	8	5x5	28x28	400	12544
`pool 1`	8	-	14x14	0	3136
`conv 2`	12	5x5	10x10	4800	2400
`pool 3`	12	-	5x5	0	600
`full 4`	10	5x5	1x1	6000	20

(b) *medium* CNN.

layer	params			memory (*bytes*)	
	# *feat.*	*filter size*	*data size*	*weights*	*data*
`input`	1	-	32x32	0	2048
`conv 0`	16	5x5	28x28	800	25088
`pool 1`	16	-	14x14	0	6272
`conv 2`	24	5x5	10x10	19200	4800
`pool 3`	24	-	5x5	0	1200
`full 4`	10	5x5	1x1	12000	20

(c) *big* CNN.

layer	params			memory (*bytes*)	
	# *feat.*	*filter size*	*data size*	*weights*	*data*
`input`	1	-	64x64	0	16384
`conv 0`	4	5x5	60x60	200	28800
`pool 1`	4	-	30x30	0	7200
`conv 2`	6	5x5	26x26	1200	8112
`pool 3`	6	-	13x13	0	2028
`conv 4`	10	5x5	9x9	3000	920

(d) *small* CNN on a 64x64 image.

Table 3: Parameters and memory usage of all CNN networks.

the 0.4V operating point) in the *search* mode, and then switched to a frame rate as high as 27 fps (at the 1.3V operating point with 1V FBB) in the *follow* mode.

Figure 7b shows the energy efficiency of the ConvNet execution on a frame in terms of FPS/W; we ran the same ConvNet on the Xilinx Zynq PS and on a Samsung Exynos 5 for comparison, as this benchmark is beyond the typical performance capabilities of most ULP microcontroller architectures. Benchmark results substantially confirm the theoretical values shown in Figure 4. The energy/execution time tradeoff when switching between *search* and *follow* mode is also clearly shown: in *search* mode, PULP consumes 1.18 mJ per frame and lives at a power budget of 834 µW, whereas in *follow* mode energy consumption jumps at 12.6 mJ per frame.

4.4.3 Tiled CNNs

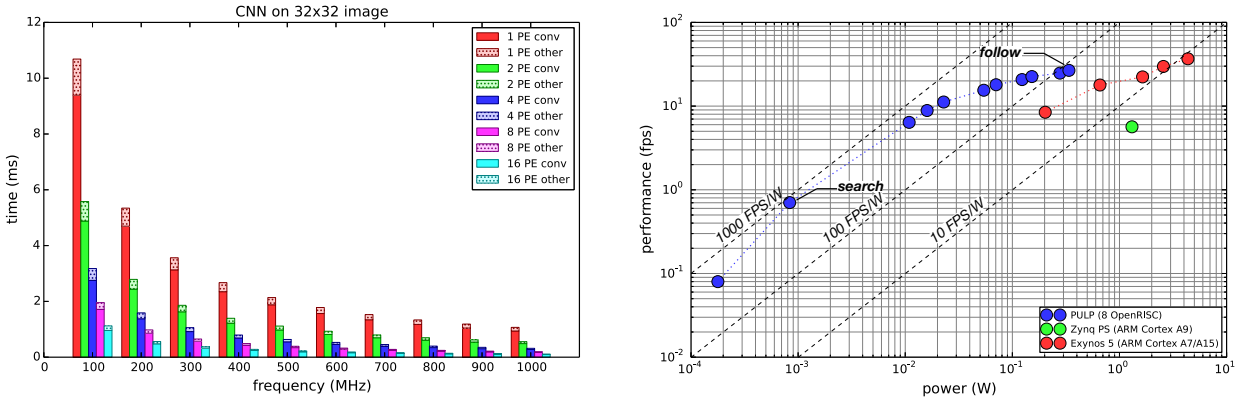
To further explore the capabilities of the PULP platform in this scenario, we considered the case that the CNN or its input image cannot fit in the TCDM. In this case, it is necessary to tile the CNN similarly to what is described in Section 4.3; also in this case, double buffering can be employed to hide the latency of the L2/L1 memory transfer.

In the case of CNNs, tiling involves some amount of recomputation as the receptive field of each output convolutional tile is partially superimposed to that of the next output tile. We can tile the same ConvNet with two distinct approaches. With a "vertical" tiling approach, the full network is applied to each input tile until the last layer, then the output is transferred to the L2 memory and a new tile is loaded; "horizontal" tiling instead is applied by dividing input of a single layer in tiles and computing all output tiles before proceeding to the following layer. In this approach, intermediate results (i.e. the outputs of intermediate layers) have to be stored in buffers in the L2 memory.

We chose to concentrate on horizontal tiling for three reasons: first, vertical tiling involves a lot of recomputation as the smaller ConvNet tile has to be moved over the input image (similarly to what we did in Section 4.4.2, but with stride of 1 pixel instead of 32). Second, the horizontal approach allows us to tile also in the input feature dimension, whereas in vertical tiling all input features are needed in the shared memory to compute the following layer. Third, although horizontal tiling involves frequent data transfers between L1 and L2, we will show in the following that the impact of these transfers scales nicely with the size of the input data and the amount of parallelism.

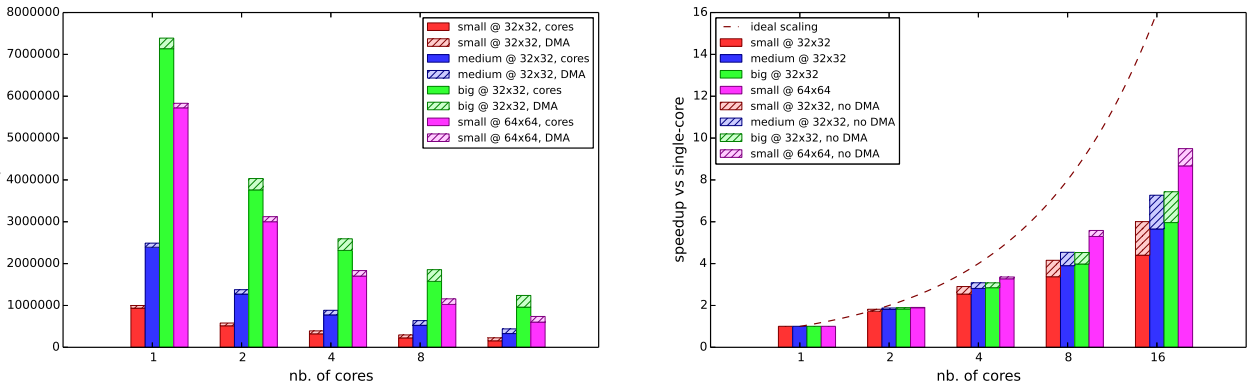
We extended the reference CNN[2] of Section 4.4.2 in the following way. The *medium* and *big* CNNs, whose parameters are reported in Tables 3b and 3c respectively, are similar to the *small* one but their intermedi-

[2] We will refer to this network as the *small* network from this point on.



(a) Execution time in ms (32x32 patch). (b) Energy efficiency in FPS/W (QVGA frame).

Fig. 7: Surveillance ConvNet benchmark results.



(a) Execution time in cycles. (b) Parallel execution speedup.

Fig. 8: Tiled CNN benchmark performance results.

ate layers have more features. The fourth CNN shares the same parameters as the *small* one, but runs on a bigger image patch of 64x64 pixels; its parameters and memory consumption are reported in Table 3d. In this network, the final linear layer is substituted by an equivalent convolutional layer using the same weights; the output is equivalent to the separate classification of all pixels (see for example Sermanet et al. [63]). In all benchmarks, we set the maximum dimension of the tiles to 4KB so that it is possible to fit two input tiles and two output tiles in the TCDM. The dimension of the program code is similar for all of these benchmarks (∼25KB loaded on the L2 memory), since we relied on the same ConvNet library extended with horizontal tiling support.

Figure 8a reports the execution time of all benchmarks in terms of cluster clock cycles. The computational complexity of the CNN raises exponentially when we double the number of feature maps used in each layer or the pitch of the input image; we observe that the *big* CNN applied on a 32x32 image and the *small* one on a 64x64 image impose similar constraints both in terms of workload and of memory occupation. To better evaluate how performance scales in all benchmarks as we vary the number of cores, Figure 8b compares speedup versus single-core execution for all benchmarks. Figure 8b also reports the theoretical speedup if we neglected all impact of DMA transfers. The main limiting factor for speedup is given by Amdahl's law: due to the small dimension of the tiles, the parallel fraction of the code is not sufficient to yield quasilinear speedup. This is clearly visible in that the same ConvNet applied to a 4x bigger input image yields much better results in terms of performance scaling. The size of the input image itself is mainly limited by the availability of L2 memory. The plot also shows that, due to the higher computation to communication ratio, the impact of data transfers on the speedup scales nicely with the size of the workload,

i.e. the bigger the input image and/or the CNN is, the less limiting impact DMA transfers have over parallel execution speedup.

To estimate how much the accuracy may vary between the *small*, *medium* and *big* CNNs, we trained them to classify the CIFAR-10 dataset [38], a well known and freely available set of 60000 32x32 images labeled in 10 classes [3]. Figure 9 shows that the difference can be significant: after 500 epochs of training the final accuracy is 70.64% for the *big* CNN, which drops to *64.38%* for the *medium* one and to 50.05% for the *small* one. The difference is greatly reduced if we compare the CNNs for a one versus all classification task over the same dataset: the final accuracy in this case is 95.1%, 94.2% and 93.3% for the *big*, *medium* and *small* CNNs respectively.

In Figure 10, we plot the energy efficiency in terms of GOPS/W for the execution of the *big* ConvNet (results are practically identical for the other benchmarks). Compared with the peak theoretical value of 211 GOPS/W, we measured a peak of 150 GOPS/W in this benchmark, which correspond to an average IPC of 0.71 per core. By comparison, average single-core IPC in the inner convolutional loops is 0.96, and average single-core overall IPC is 0.87. The IPC reduction in the multi-core tests is mainly accounted for by contention on the shared TCDM and, to a lesser extent, by contention on the I$ refill bus. Still, IPC in the inner-loops is as high as 0.90 per core when executing with 8 cores. The energy efficiency results mimic the peak ones presented in Figure 4, and peak efficiency (125 MOPS @ 834 µW) at the same operating point (0.4V without FBB) in the near-threshold region.

[3] As our CNNs work on grayscale images, the training and test samples where converted from RGB to grayscale. Training consisted in 500 epochs of mini-batch stochastic gradient descent with momentum $\mu = 0.9$ and starting learning rate $\lambda_0 = 0.01$ (dropping exponentially as $\lambda = \lambda_0 \cdot 0.995^{n_{\text{epoch}}}$), using 20% dropout [39] layers for better regularization.

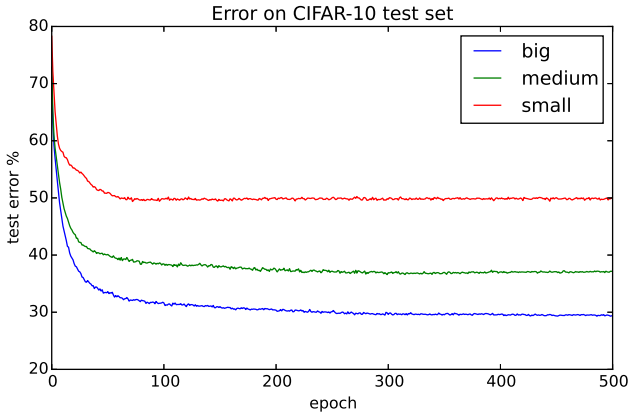


Fig. 9: Test error of *small*, *medium* and *big* CNNs on the CIFAR-10 set over 500 training epochs.

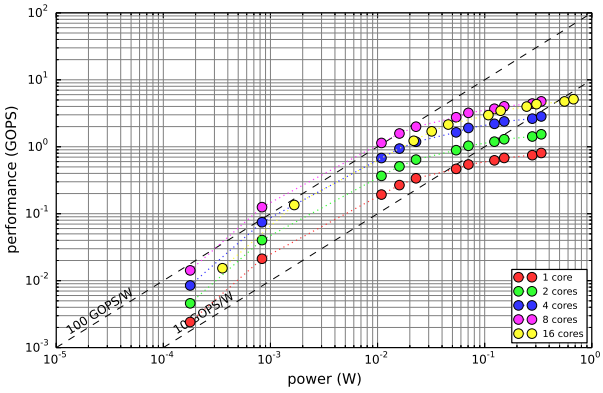
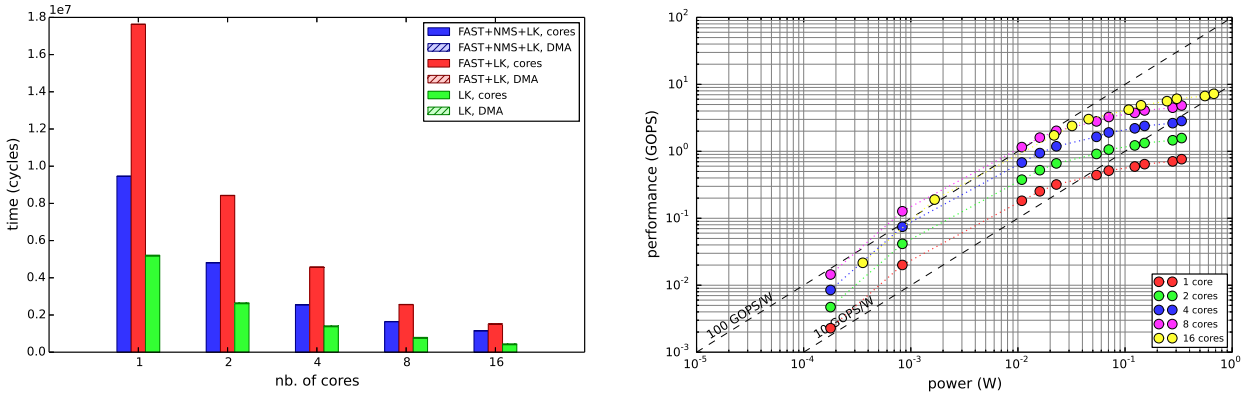


Fig. 10: Energy efficiency for execution of the *small* CNN on a 64x64 image, while sweeping the number of cores.

4.5 Optical flow benchmark

As a representative application for the usage of PULP as an accelerator for an autonomous nano-UAV, we developed an optical flow benchmark that is meant to be integrated in the drone control loop to make completely autonomous hovering and navigation possible. In this scenario, a low-resolution (e.g. 128x128 pixel) ultra-low-power imager such as a CentEye Stonyman [3] continuously feeds frames to PULP via the QSPI slave interface. On turn, PULP computes the optical flow and uses its QSPI master to report the flow vectors back to the microcontroller driving the vehicle, where they are used to estimate rotations and translations of the drone.

The benchmark is composed of three kernels: FAST corner detection [58][59], non-maximal suppression and Lucas-Kanade optical flow estimation [42]. Since Lucas-Kanade should be applied to strong corners to yield high-quality, it is generally not advisable to drop either the non-maximal suppression step or the whole corner detection. Nonetheless, since the users of the flow vectors (i.e. the aerial vehicle software developers) might want to trade off optical flow accuracy for performance and energy, we decided to explore also these non-optimal cases. Therefore, we present results for three separate implementations: *FAST+NMS+LK* that feeds corners produced by the FAST algorithm in non-maximal suppression before computing optical flow; *FAST+LK* that uses all corners produced by FAST for the optical flow; *LK* that drops corner detection and computes optical flow on all pixels.



(a) Execution time in cycles (all).

(b) Energy efficiency in GOPS/W (*FAST+NMS+LK*).

Fig. 11: Optical flow benchmark results.

The input of the optical flow application are two 128x128 8-bit grayscale frames stored in the L2 memory by the QSPI slave module. To cope with the dimension of the input frames, we divided them in stripes of 128x16 pixels; we use double buffering to transfer the stripes from the L2 to the TCDM while we are computing the optical flow of the previous stripe.

Figure 11a reports the execution time in cycles for all versions of the benchmark, sweeping the number of cores in the PULP cluster from 1 to 16. The first observation is that the *FAST+LK* benchmark is the slowest; this is due to the fact that if non-maximal suppression is dropped, the Lucas-Kanade step has to be performed on a much higher number of corners, in the order of several hundreds. The *LK* benchmark drops FAST altogether and is therefore the fastest, even if it computes optical flow on the full 16384 pixels of the image. Conversely, the *FAST+NMS+LK* benchmarks spends most of its time in computing the best corners (in the order of some tens) in the picture and much less time in the actual optical flow, as it is computed only on those corners. In all cases, optical flow computation on the 128x128 input frames takes more than 1 million cycles when performed with 8 cores: intuitively, this means that the workload to perform this task at 60fps is bigger than 60 MOPS.

Figure 11b helps to understand whether this is a feasible target, and at what power budget, by plotting energy efficiency in terms of GOPS versus watt measured by profiling the optical flow *FAST+NMS+LK* benchmark. At the most efficient operating point (0.4V with no FBB, 834 µW of power consumption) the 8-core cluster achieves a performance of 127 MOPS, with an efficiency of 152 GOPS/W. The peak efficiency is similar to that of the CNN benchmark but this is due to a different mixture of effects from the result obtained in Section 4.4.3. First, the lower internal regularity of the FAST benchmark (which is responsible for the majority of the execution time) hits the inner-loop IPC with respect to the very regular and manually optimized convolutional kernels employed in the ConvNet. At the same time, however, it also significantly lowers data contention, leading to a similar overall efficiency result. At this operating point, optical flow would be feasible for a micro-UAV application as it would add less than a mW to the total vehicle power, which nicely fits in the 5 mW budget for computing in Wood et al. [65]. The energy budget to compute a frame is 13.9 µJ; to make this measure concrete let us take for example the commercial Crazyflie Nano Quadcopter [4], that mounts a 240 mAh 3.3V battery, hosting approximately 2850 J of energy destined primarily to power DC motors. If we suppose a flight time of one hour, the battery consumption due to the PULP accelerator would amount to ∼3 J, i.e. 0.1% of the total battery, which is almost negligible with respect to the energy consumed by the vehicle actuators.

5 Conclusions

As our main contribution, we have introduced the PULP (*Parallel processing Ultra-Low Power*) platform that features clusters of tightly-coupled OpenRISC cores to achieve high energy efficiency through parallelism. We have analyzed the platform, showing that its performance can be scaled by the dramatic factor of 354x and that it features a peak energy efficiency of 211 GOPS/W.

As a use case for PULP, we show a motion estimation algorithm for smart surveillance which almost fully

exploits the available performance, with a peak energy efficiency of 192 GOPS/W, i.e. 90% of the theoretical peak. We also implemented a ConvNet-based algorithm for video surveillance, showing that it can be switched from a low-power state consuming just 1.18 mJ per frame with a rate of 0.7 fps to a high-performance state running at 27 fps and consuming 12.6 mJ per frame. Finally, we wrote a sample benchmark for applications in the nano-UAV field, where we use PULP to accelerate estimation of optical flow from frames produced by a ULP imager, with the objective of autonomous hovering and navigation; we show that it is possible to meet tight timing constraints (60fps frame rate) at the energy budget of 14 µJ per frame. These benchmarks showcase the high level of flexibility and programmability of the PULP platform, that does not come at the expense of energy efficiency: all of them were able to reach at least 70% of the peak efficiency overall, with much higher peaks in highly parallel regions such as in the motion detection and inner convolutional kernels.

A fully functional PULP test chip featuring 4 OpenRISC cores, 64 kB of L2 memory and 24 kB of TCDM has been submitted for fabrication in 28nm STMicroelectronics FD-SOI technology in December 2014. We decided to submit a 4-core version of the platform out of two main considerations: first, due to the relative novelty of the FD-SOI technology, we chose to be conservative and take into account a bigger leakage contribution to power consumption, which would level out the efficiency gap between 4- and 8-core PULP clusters. Second, the higher complexity of the shared-memory interconnect in a 8-core cluster with respect to a 4-core one coupled with the constrained wafer area allotted to our chips could make optimal placement & routing and timing closure more difficult, resulting in a slower or less energy-efficient chip.

Our work is now focusing on pushing the PULP architecture to the 1 GOPS/mW limit, making it competitive with special purpose mixed-signal accelerators such as the 1.57 TOPS/W in Kim et al. [36] in terms of energy efficiency, while also preserving general software programmability. This is being tackled with a complete redesign of the core, with microarchitectural changes to improve IPC and programmability, a new custom compiler toolchain based on LLVM and architectural improvements to the platform to improve its performance and energy efficiency, such as a more efficient instruction cache hierarchy and the addition of specialized blocks for selected macro-operations.

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