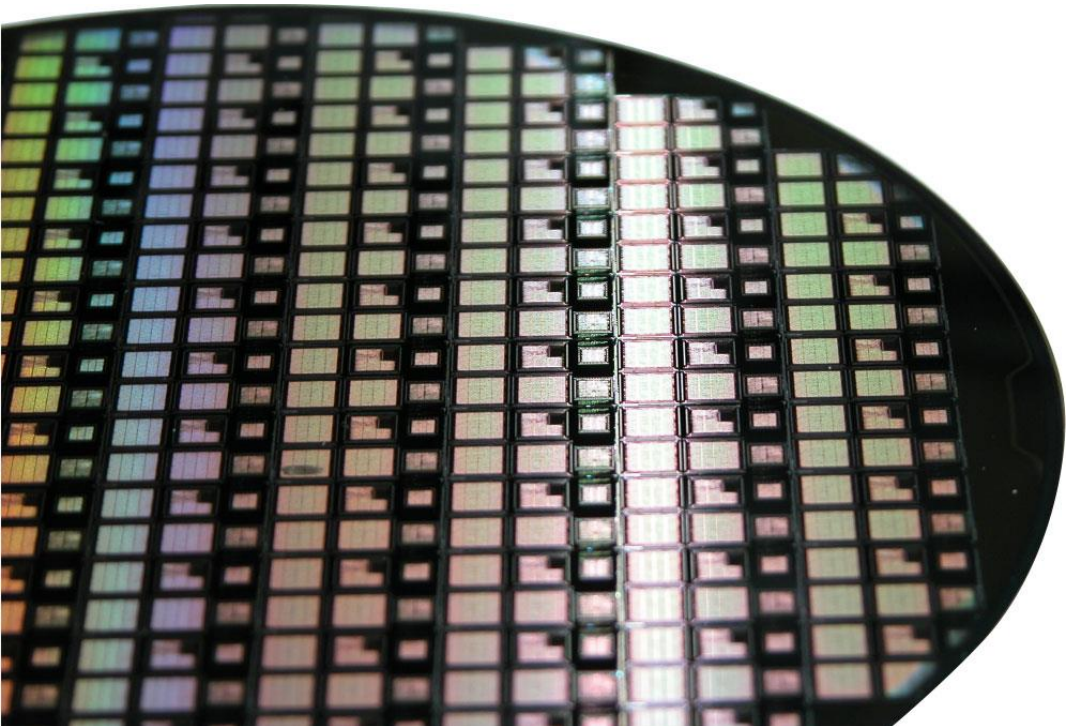
ETH zürich

Evaluating RISC-V Cores for PULP

An Open Parallel Ultra-Low-Power Platform

www.pulp.ethz.ch

30 June 2015



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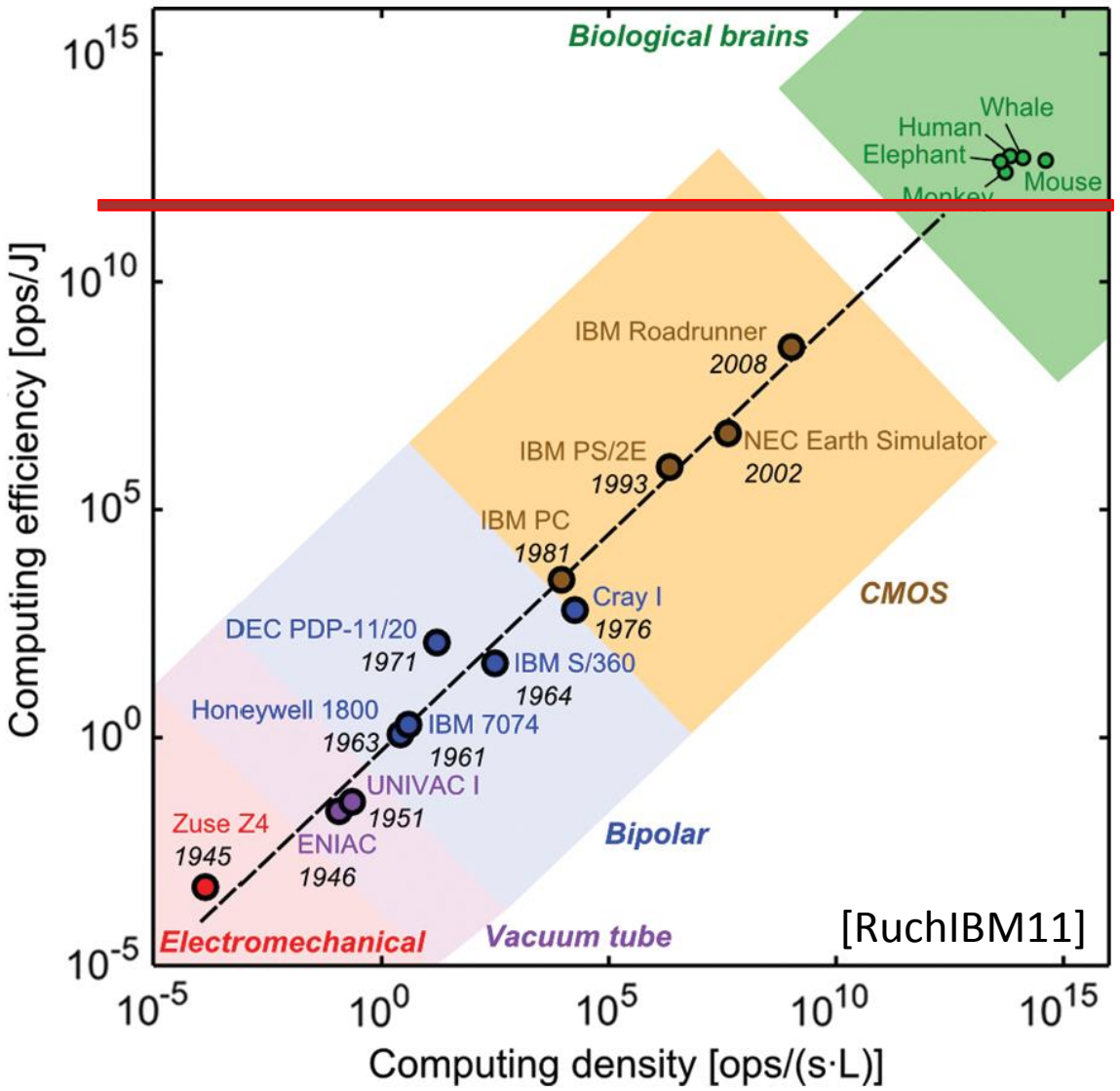
Summary

- **Background**
  - The group
- **PULP platform**
  - Goals
  - Our approach
- **RISC-V on PULP**

The Group of Prof. Luca Benini

- **Approximately 40 people**
  - ETH Zürich Integrated Systems Laboratory (IIS)
  - University of Bologna EEES
  - Many involved in PULP
- **Great experience in IC design**
  - More than 400 ICs, in-house ASIC tester
- **Close Collaborations**
  - POLIMI (compiler support)
  - CEA/LETI
  - EPFL

Our Goal: Reach 1 GOPS/mW efficiency



10^{12}ops/J

↓

1pJ/op

↓

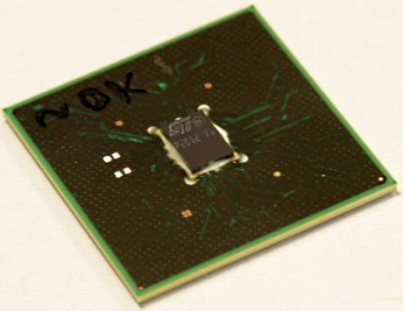
1GOPS/mW

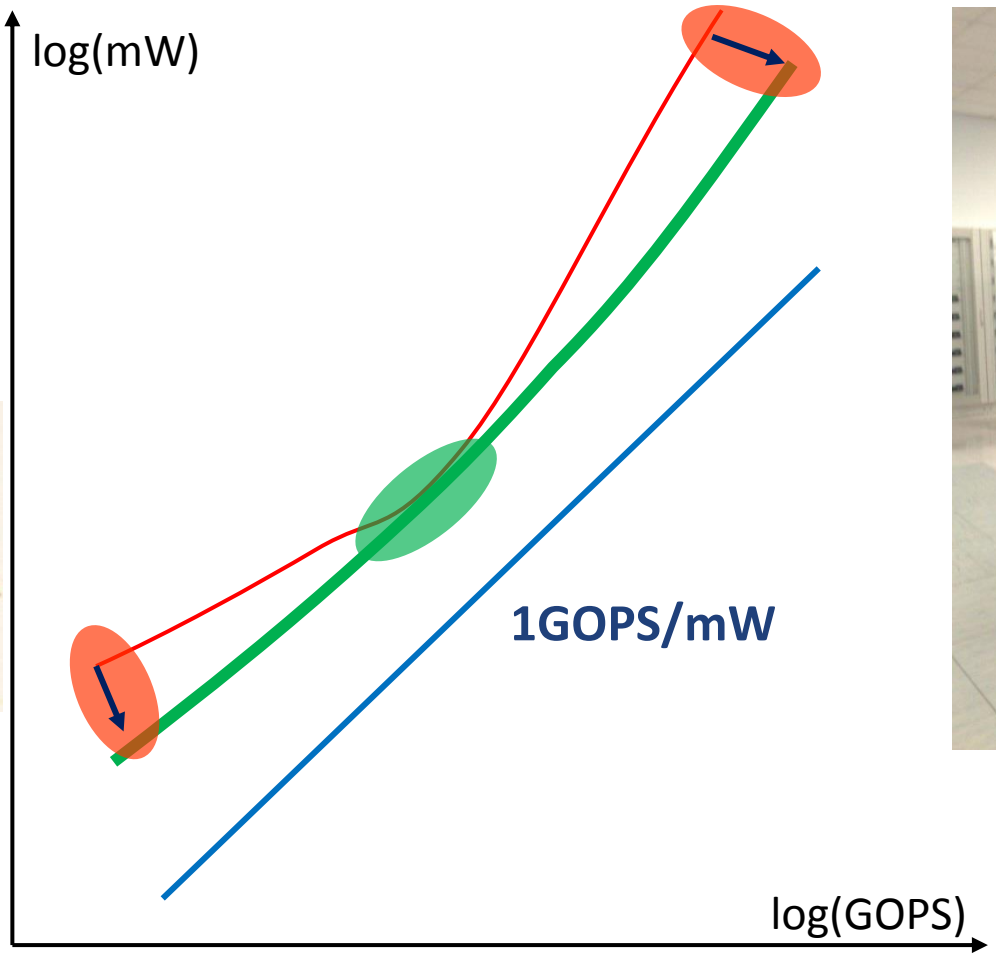
Energy Proportionality

0,003GOPS/mW – 30KW

0,03GOPS/mW

life.augmented





PULP

- **An open research platform**
- **Goals:**
  - Reach 1 GOPS/mW efficiency
  - Scalable hardware: Achieve energy proportionality
- **Research on:**
  - Efficient cores, platform innovations
  - Technology options
  - Software support

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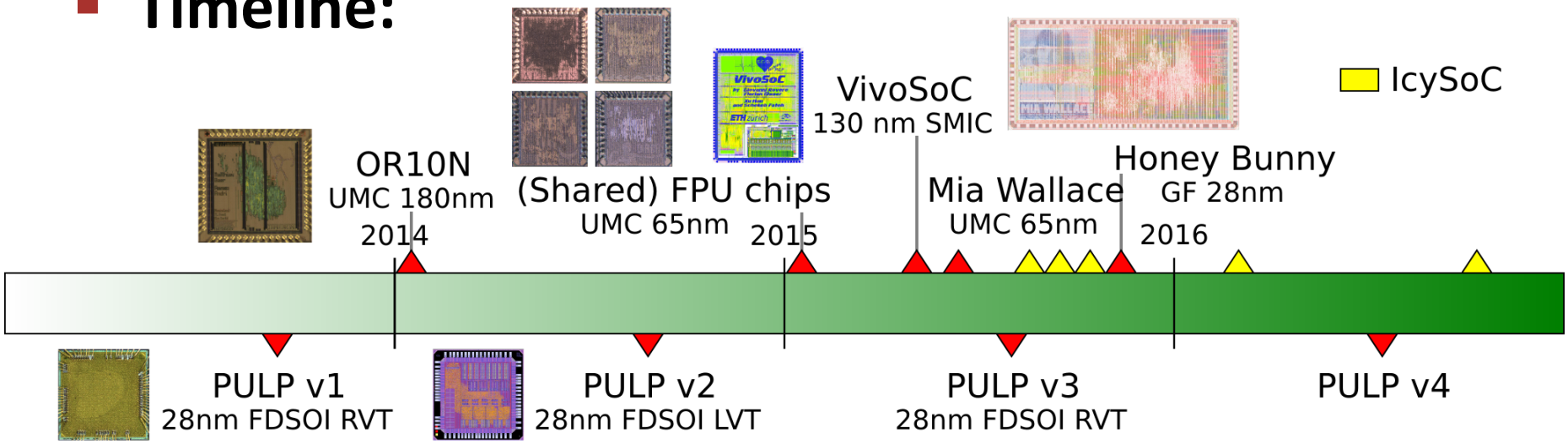
Our Approach: PULP

- **Exploit parallelism**
  - Multiple small cores organized in a cluster
  - Share memory within the cluster
- **Simple but efficient processor cores**
  - Currently: OpenRISC with ISA extensions
  - RISC-V Minion core in the work
- **Hardware optimizations**
  - Near-threshold operation
- **Dedicated accelerators**

PULP Family of Chips

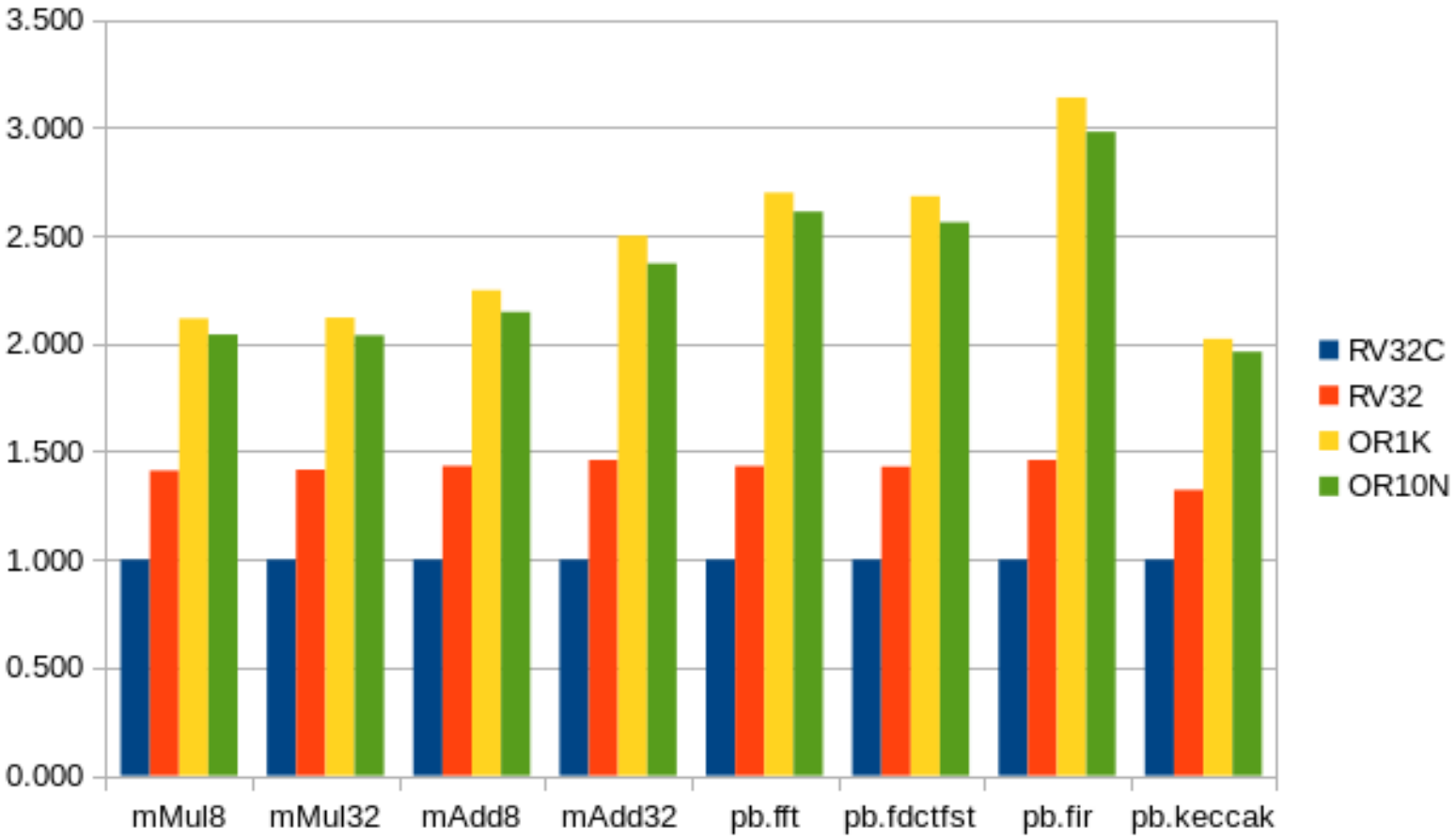
- **Silicon proven in 28nm**
- **Several tape-outs in different technologies**
  - 180nm (IcySoC project, approximate computing)
  - 130nm (Mixed-signal PULP: Vivo-SOC)
  - 65nm (Student projects, demonstrators)
  - 28nm (Flagship designs, technology options)
- **Timeline:**



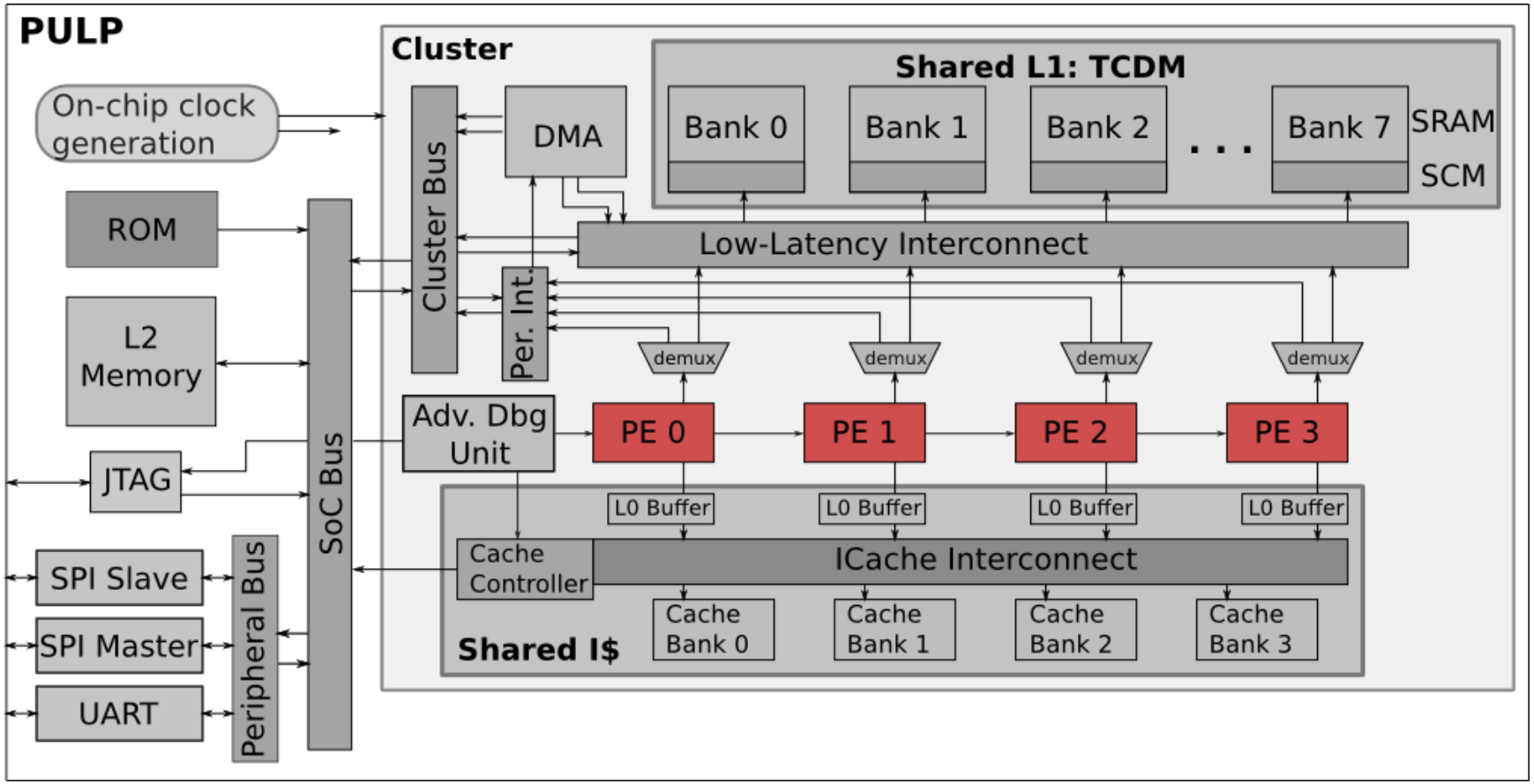
RISC-V on PULP

- **Replace OpenRISC with RISC-V core**
- **Motivation**
  - More active community
  - Compressed instruction set
- **Current status:**
  - Simple 4-stage (IF, ID, EX, WB) design
  - Support for RV32IC
  - ‘mul’ instruction from M extension
  - UMC65: 22 kGE for t_{pd} = 2.2ns @ 1.08V
  - Privileged features: M-mode, Mbare memory

RVC: Big impact on code size

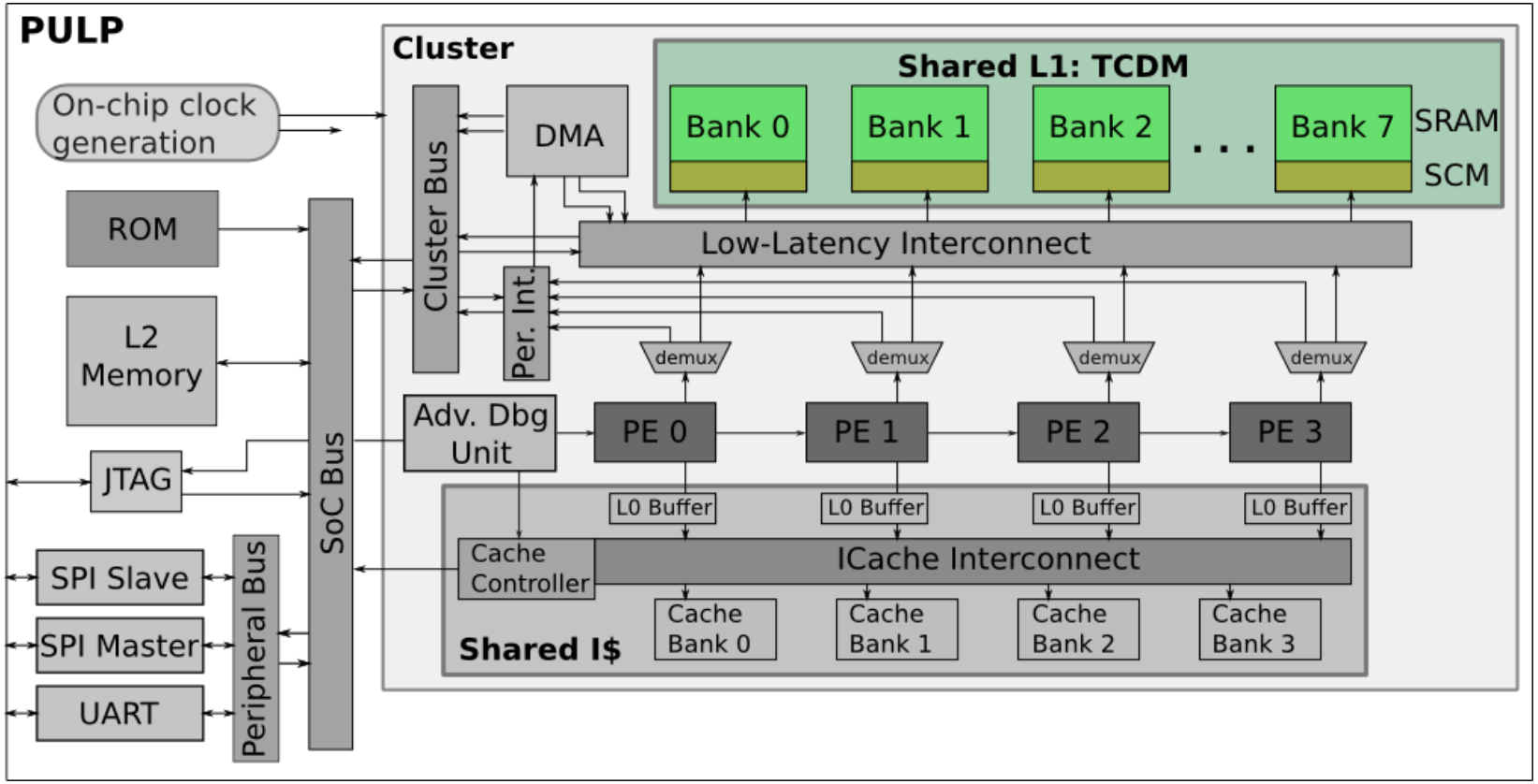


PULP Architecture



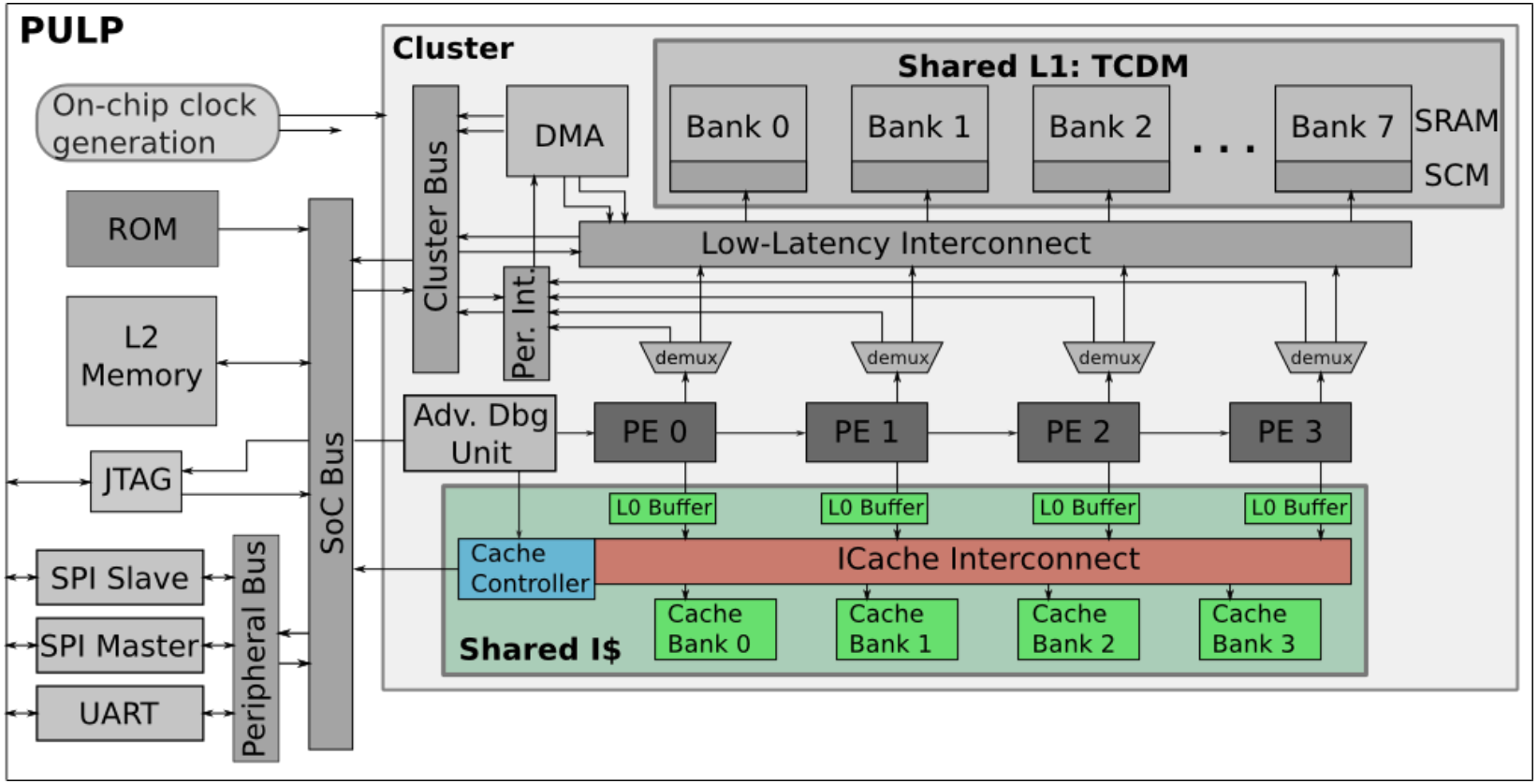
Tightly Coupled Data Memory (TCDM)

- Cluster-local data storage, explicitly managed
- Single-cycle access without contention



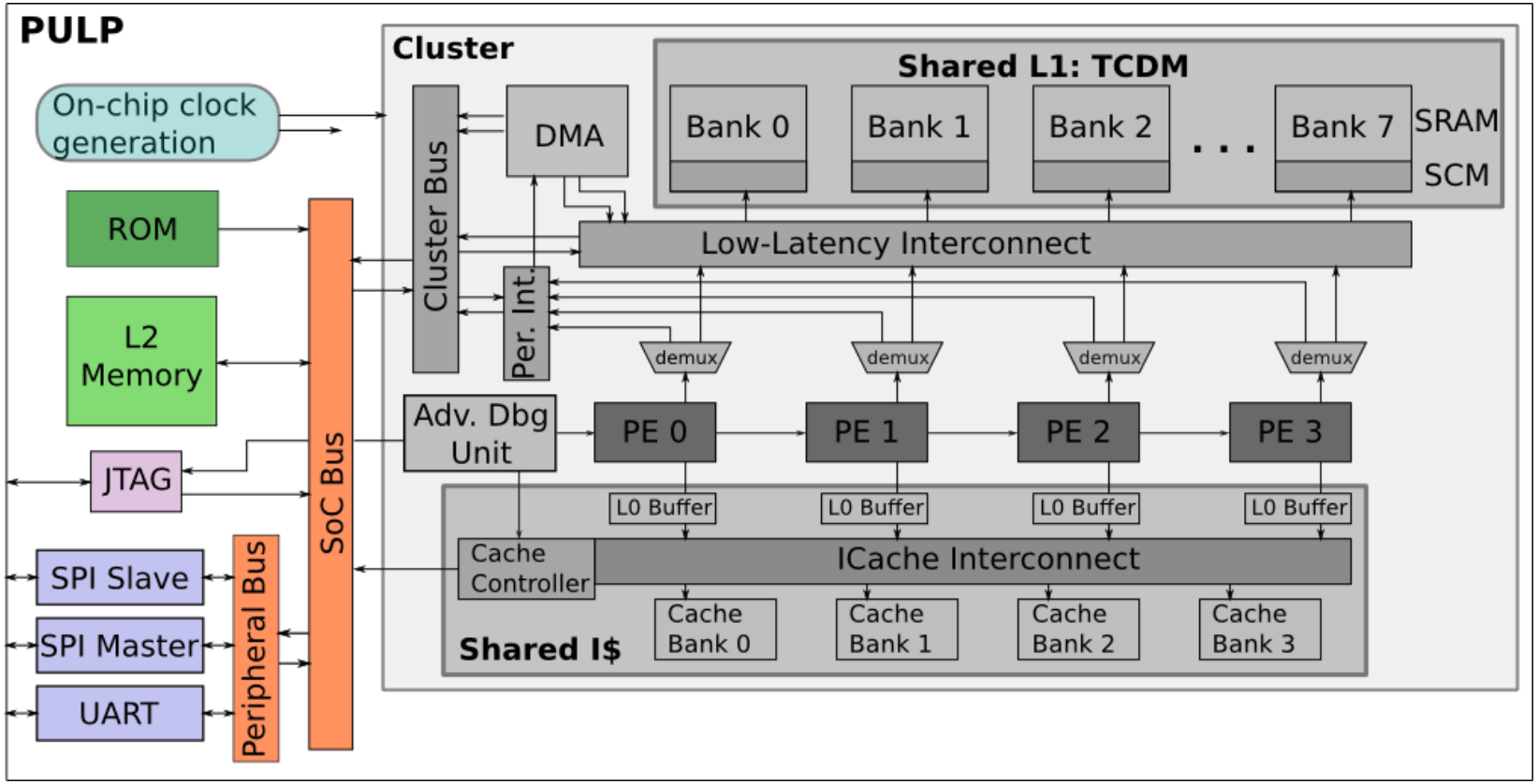
Instruction Cache

- Exploit parallelism: shared between cores



System on Chip

- Frequency-locked loop (FLL)
- Memory, (I/O) Peripherals, ROM, …



Improved OpenRISC: OR10N Core

- **OpenRISC core developed at IIS**
- **ISA extensions to improve efficiency**
  - Hardware Loops
  - Pre-/Postincrement memory access
  - Vectorial (packed SIMD) instructions
- **Custom llvm compiler**
  - No changes to C code needed to use new instructions
- **Debugging support**

RISC-V on PULP: Future Work

- **Tapeout in 4Q2015**
  - GlobalFoundries 28nm
- **Evaluate OR10N extensions for RV core**
  - Hardware loops: Smaller impact on RV
  - Vectorial instructions
- **We are open for suggestions / collaborations**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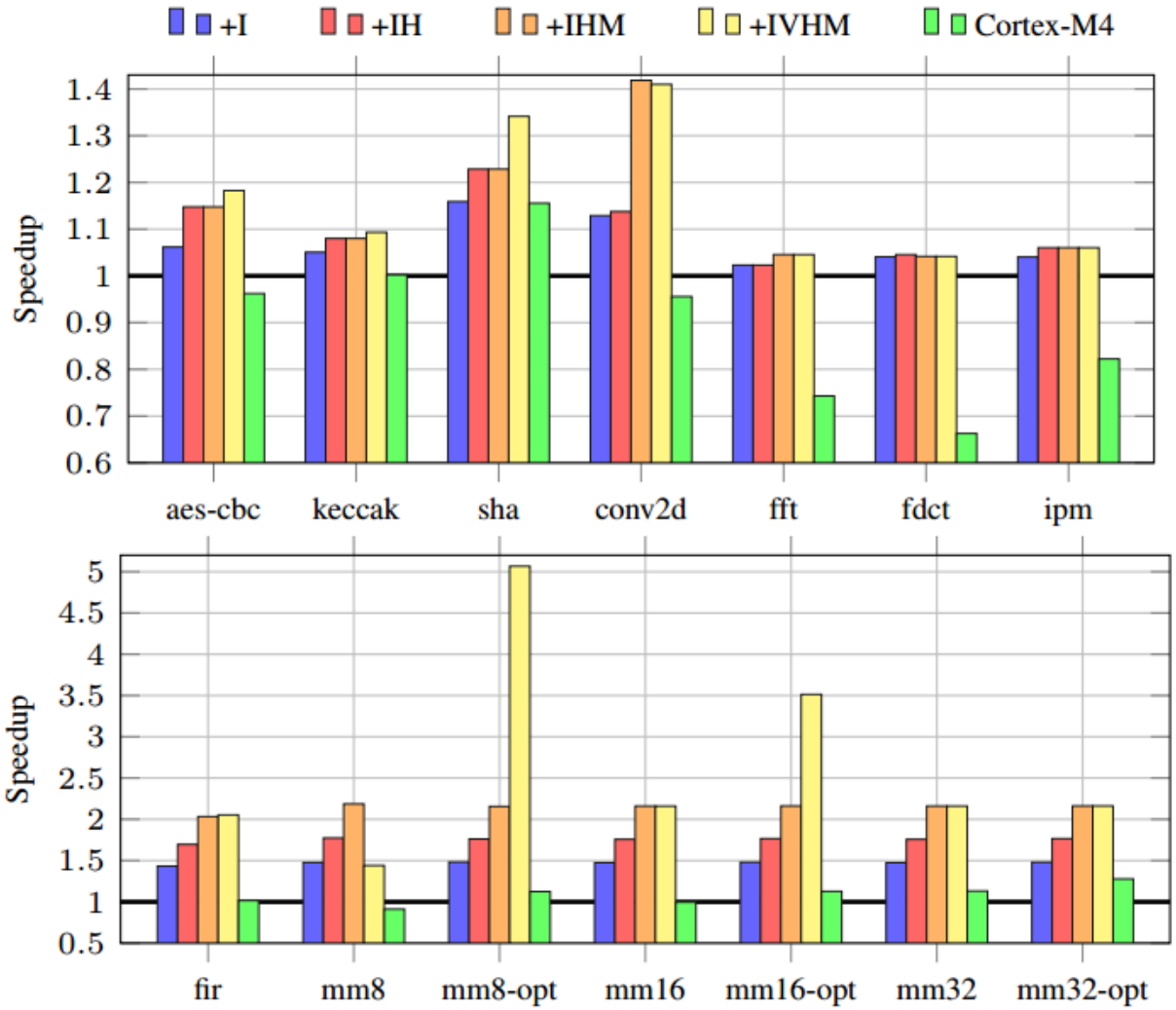
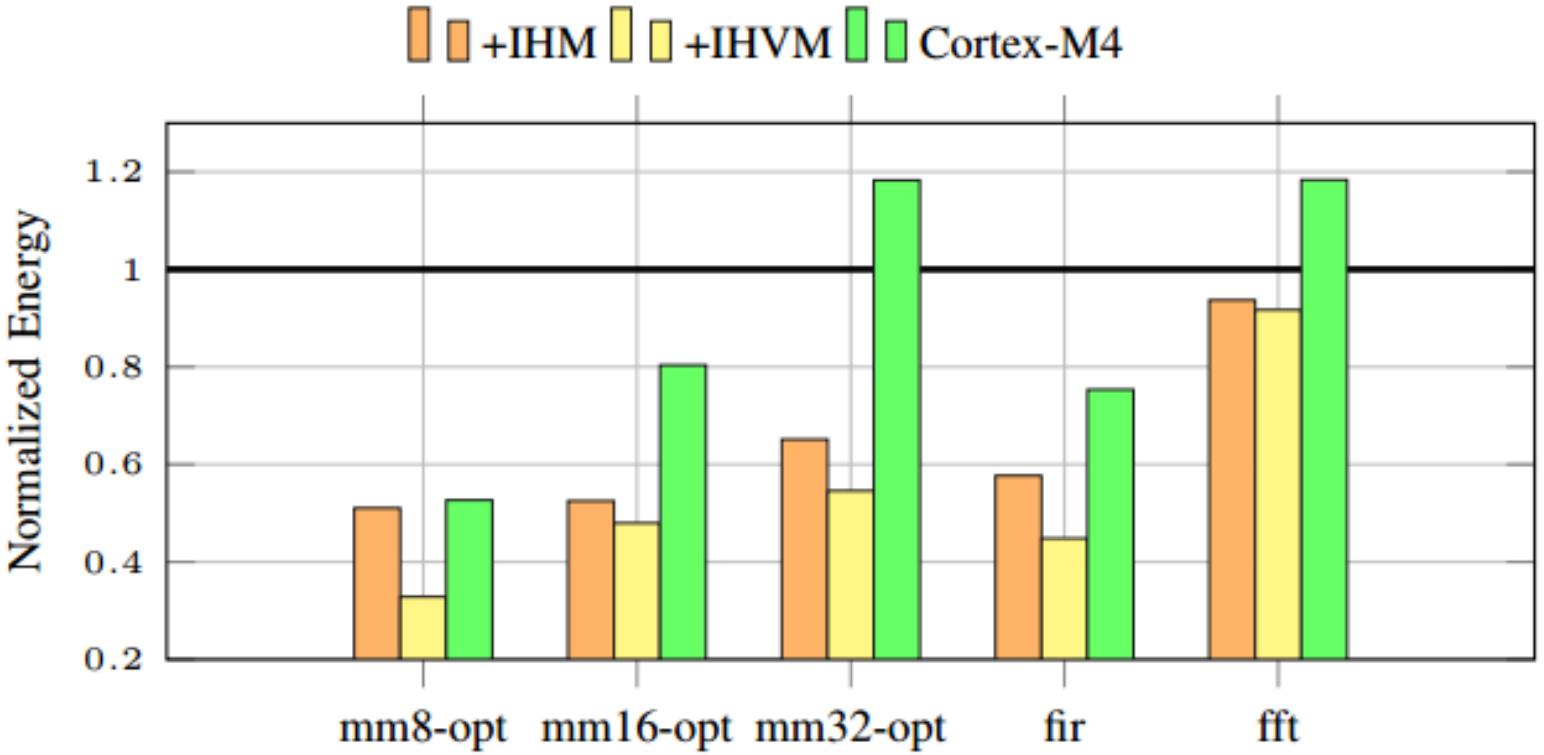
http://asic.ethz.ch
QUESTIONS?

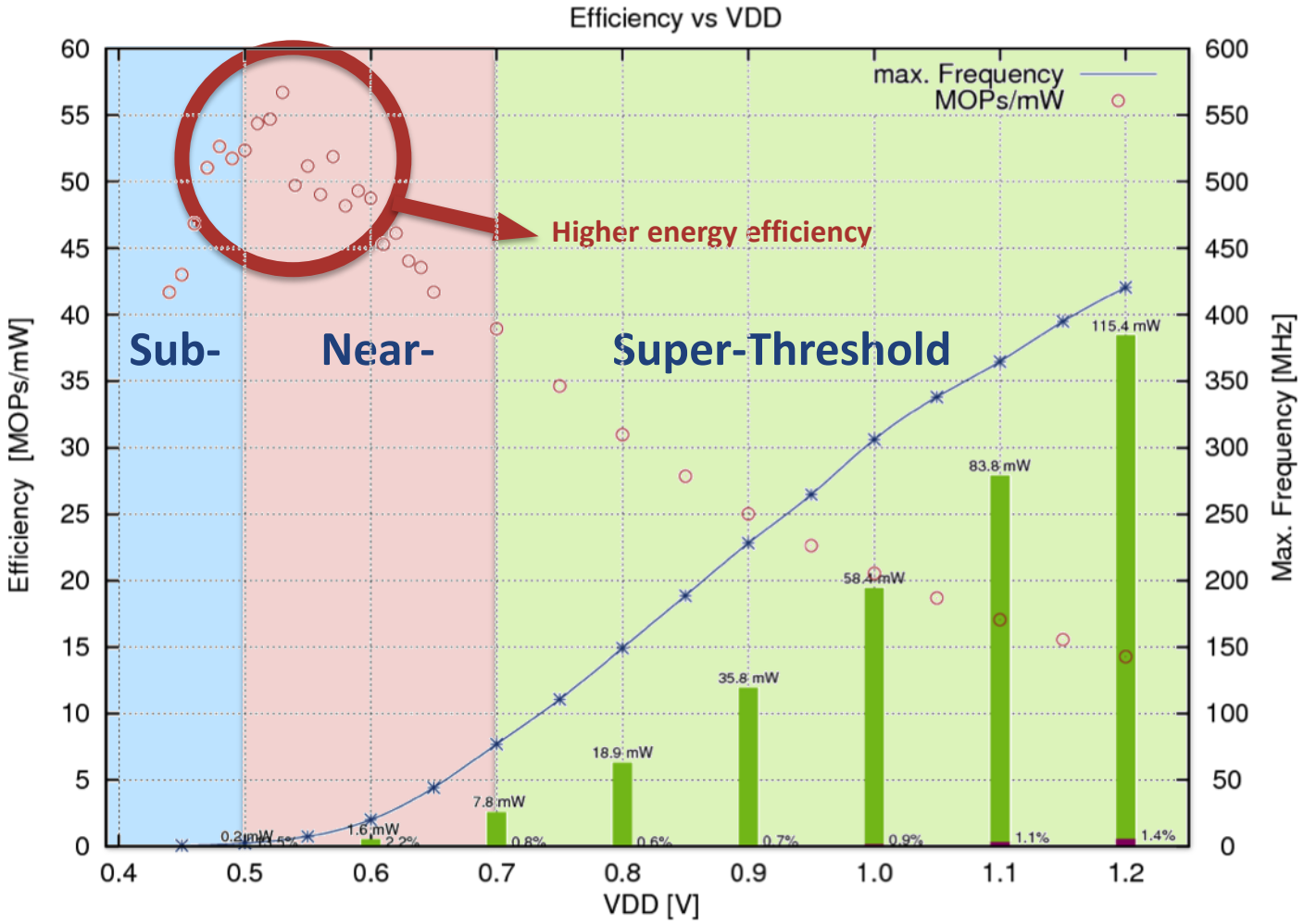
OR10N Extensions Performance Gain



OR10N Extensions Power Improvement

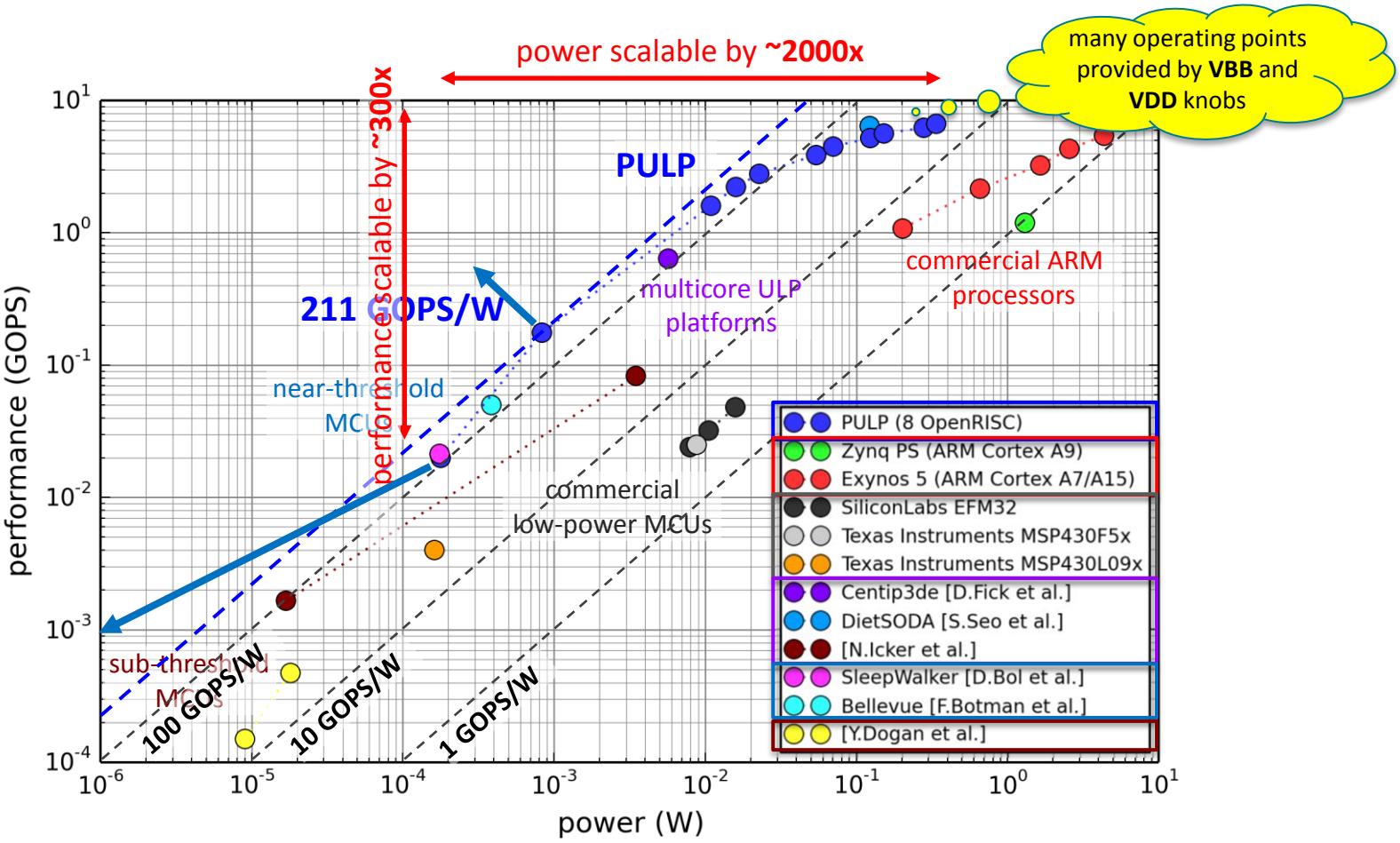


Near Threshold Operation More Efficient



Actual PULP Measurement Results

PULP v2: Best in Class



PULP v2: Best in Class