Laboratory 1 Tutorial Exercises

The first task laid out specifications for five separate layout patterns labelled a-e respectively. The specifications are stated below:

1. Two parallel POLY lines that are 2μm wide and spaced 1μm apart
2. Two parallel POLY lines that are 1μm wide and spaced 2μm apart
3. Two parallel POLY lines that are 2μm wide and spaced 2μm apart
4. Two parallel METAL1 lines that are 2μm wide and spaced 3μm apart
5. A 2μm wide POLY line that is parallel to a 3μm wide METAL1 line, with the two lines spaced 2μm apart

Below are schematic diagrams of the layouts created from the specifications above. Accompanied by highlights from the SCNA Design Rule Checker’s (DRC) output file and a discussion of the results:

Layout (a)

|  |  |
| --- | --- |
|  | 1. 3.2 Poly to Poly Spacing = 2 Microns: (-11.000,23.500)->(-10.000,23.500) 2. 3.2 Poly to Poly Spacing = 2 Microns: (-11.000,44.500)->(-10.000,44.500) |

Figure Schematic Diagram and DRC Violations of Layout (a)

Violations 1 and 2 state that DRC rule 3.2 has been violated. Rule 3.2 requires that the spacing between any two poly objects is at least 2 microns (in accordance to SCNA). The spacing of our objects here is only 1 micron (1µm) hence this is a violation. Note this violation is recorded twice. Once for the upper inside corners and once for the lower inside corners. Violations are reported like this as the objects can be any complex polygonal shape and any number of violations can be made with one object; reporting each instance can help the designer correct the layout in one pass. Adherence to the SCNA design rules is necessary to minimise avoidable design defects in MOSFETs created from layouts like this. This particular design rule helps prevent coupling or shorting of separate poly lines.

Layout (b)

|  |  |
| --- | --- |
|  | 3.1 Poly Minimum Width = 2 Microns: (8.000,13.000)->(7.000,13.000)  3.1 Poly Minimum Width = 2 Microns: (7.000,31.000)->(8.000,31.000)  3.1 Poly Minimum Width = 2 Microns: (5.000,13.000)->(4.000,13.000)  3.1 Poly Minimum Width = 2 Microns: (4.000,31.000)->(5.000,31.000) |

Figure Schematic Diagram and DRC Violations of Layout (b)

Layout (b) violates rule 3.1 which states any poly object must be a minimum width of 2 microns. It is registered four times. One for each violating edge; the two top edges and the two bottom.

Layout (c)

|  |  |
| --- | --- |
|  | No errors were present. |

Figure Schematic Diagram and DRC Violations of Layout (c)

This layout has no violations. Rules 3.1 and 3.2, minimum distance for two poly objects and minimum width respectively, have been satisfied. Should we wish to export this to a SPICE model etc. there would be no conflicts however this would be pointless as the two lines of poly-silicon are functionless by themselves. Aside: note the cross denotes the origin and all coordinates in LEdit (such as those stated in the DRC violations) are measured from here.

Layout (d)

|  |  |
| --- | --- |
|  | 7.1 Metal1 Minimum Width = 3 Microns: (8.000,2.000)->(6.000,2.000)  7.1 Metal1 Minimum Width = 3 Microns: (6.000,15.000)->(8.000,15.000)  7.1 Metal1 Minimum Width = 3 Microns: (3.000,2.000)->(1.000,2.000)  7.1 Metal1 Minimum Width = 3 Microns: (1.000,15.000)->(3.000,15.000) |

Figure Schematic Diagram and DRC Violations of Layout (d)

In this layout “metal 1” is instead of “poly”. Here the violations are caused by the lines being too thin. SCNA rule 7.1 requires all metal 1 objects to be at least 3 microns thick, here they are 2 microns. As with (b) four violations are reported, one for each violating edge.

Layout (e)

|  |  |
| --- | --- |
|  | No errors were present. |

Figure Schematic Diagram and DRC Violations of Layout (e)

The minimum width rules (3.1, 7.1) are satisfied here. There is no minimum distance between poly and metal 1 as they are on different layers and an overlap of the two layers with a poly connection is how a gate connection is made.

Task two

Task two requires you to construct a simple n-channel MOSFET in L-Edit with W' = 20µm and L' = 2µm whilst obeying the SCNA design rules, a few of which is shown above. We are then required to extract the layout as a SPICE netlist and comment on the influence the layout design has on the netlist parameters. The cell derived from the instructions is shown below; accompanied by the spice netlist and a cross sectional view of the cell.

|  |  |
| --- | --- |
|  | M1 2 1 3 4 NMOS L=2u W=20u AD=110p PD=51u AS=110p PS=51u |
|  | |

Figure Schematic Diagram, SCIPE netlist and cross section of Layout 2

Figure 6 is a simple MOSFET with dimensions W' = 20µm and L' = 2µm. You can see the cross section of this layout at the bottom of the figure. The cross section shows that the layers have generated correctly producing a working model of a MOSFET. You could probably get away with less active connections but this layout ensures better channel conductivity. It turns out that you do not even need the poly connection for the spice model as the gate port is generated over the channel anyway with only the port numbers changing. The poly dimensions over the active regions are L = 20µm and W = 2µm. The channel dimensions are L = 2µm and W = 20µm. It is easy to see that they are the same dimensions just transposed. This is because the channel’s length is measured from source to drain (or vice versa) and the gate’s length is measured from bottom to top i.e. the channel is perpendicular to the poly line. Note the areas and the perimeters of the drain and the source are also extracted so they can be used in electrical modelling.