Reg No.:_____ Name:_____

0720MCA103122403

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

MCA (Two Year) Degree S1 (R, S) Examination December 2024

Course Code: 20MCA103

Course Name: DIGITAL FUNDAMENTALS AND COMPUTER ARCHITECTURE

Max. Marks: 60 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1	Using Boolean algebra techniques, simplify (A+B+C)(A+B'+C)(A+B+C')	(3)
2	Implement priority encoder.	(3)
3	Construct SR latch using NOR gate.	(3)
4	Construct a Mod-5 asynchronous counter.	(3)
5	List the key components of a computer with a diagram.	(3)
6	Mention about indirect addressing modes with an example	(3)
7	What are the datapath elements used for Load/Store instructions?	(3)
8	What is Bus Arbitration? List two approaches for Bus Arbitration.	(3)
9	Define spatial and temporal locality.	(3)
10	What do you understand by virtual memory?	(3)

PART B

Answer any one question from each module. Each question carries 6 marks.

Module I

11	Compare SOP and POS in detail.	(6)

OR

12	Using an 8:1 MUX, implement the Boolean function: $F(A,B,C,D)=\sum(1,3,4,11,12,13,14,15)$.	(6)

Module II

13 Explain the working of an edge triggered SR Flip-Flop with the help of a circuit and timing diagram. (6)

OR

14 Draw the state diagram and logic diagram of a 3 bit up down synchronous counter. (6)

Module III

15 Consider 2 processors P1and P2 executing the same instruction set. P1 has 3 GHZ clock rate and CPI of 1.5 and P2 has 1.5GHZ clock rate and a CPI of 1.0.Which processor has the highest performance expressed in instructions/second. (6)

OR

16 Explain the different classes of instruction set architectures with an example. (6)

Module IV

17 With a neat diagram, explain the operation of DMA controllers in a computer system. (6)

OR

18 How should two or more simultaneous interrupt requests be handled? Explain with figure. (6)

Module V

19 What are the three factors related to the memory hierarchy? Compare DRAM and SRAM. Draw a pyramid structure which is used to describe the differences among memory types. (6)

OR

20 What is cache memory? Explain different cache mapping techniques with examples. (6)

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