Counters

A counter is a sequential machine that produces a specified count sequence. The count changes whenever the input clock isgiven. The output of the counter can be used to count the number of pulses.

Because of limited word length, the count sequence is limited. For an n-bit counter, the range of the count is [0, 2n-1]. The count sequence usually repeats itself. When counting up, the count sequence goes in this manner: 0, 1, 2, … 2n-2, 2n-1, 0, 1, …etc. When counting down the count sequence goes in the same manner: 2n-1, 2n-2, … 2, 1, 0, 2n-1, 2n-2, … etc.

The complement Q′ of the count sequence counts in reverse direction. If the uncomplemented output Q counts up, the complemented output counts down. If the uncomplemented output counts down,the complementedoutput counts up.

Example:

3-bit Up Counter	Complement of the Count
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

• A binary counter produces a count sequence similar to the binary numbers. A decade counter counts from 0 to 9, thus making it suitable for human interface. Other counters count to 12 making them suitable for clocks.

Uses of Counters

The most typical uses of counters are

- To count the number of times that a certain event takes place; the occurrence of event to be counted is represented by the input signal to the counter.
- To control a fixed sequence of actions in a digital system
- To generate timing signals
- To generate clocks of different frequencies

Two Classes of Counters

Counters are classified into two categories:

- Asynchronous Counters (Ripple counters)
- Synchronous Counters (Parallel counters)

Asynchronous & Synchronous

Asynchronous: The events do not have a fixed time relationship with each other and do not occur at the same time.

Synchronous: The events have a fixed time relationship with each other and do occur at the same time.

Counters are classified according to the way they are clocked. In asynchronous counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is by clocked the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all of the flip-flop so that they are clocked simultaneously.

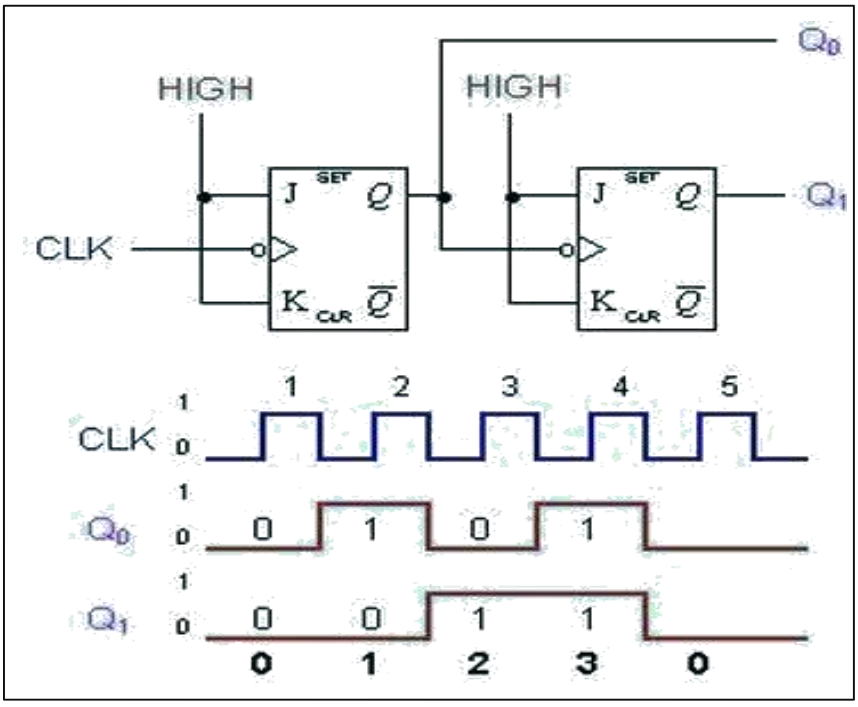
Types of Counters

Counters can be categorized into different types according to the way they are clocked. They are

Asynchronous Counters
Synchronous Counters
Asynchronous Decade Counters
Synchronous Decade Counters
Asynchronous Up-Down Counters
Synchronous Up-Down Counters

Asynchronous Counters

- The diagram of a 2-bit asynchronous counter is shown below.
- A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.
- FF1 changes only when activated by the decreasing edge of the Q0 o/p of FF0.
- FF0 changes when negative clock pulse is given



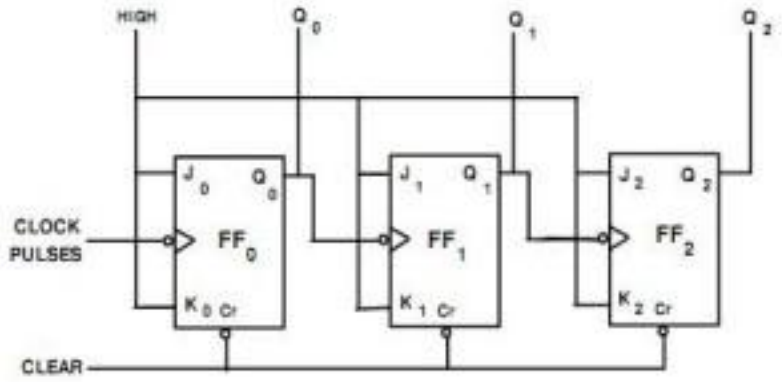
Modulus Counters, or simply MOD counters, are defined based on the number of states that the counter will sequence through before returning back to its original value. For

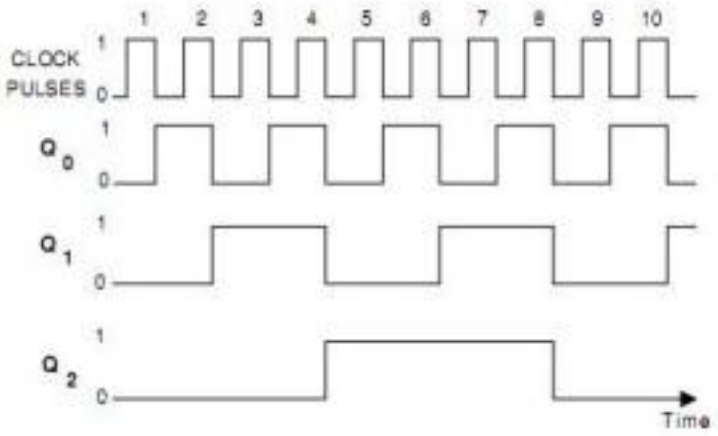
example, a 2-bit counter that counts from 002 to 112 in binary, that is 0 to 3 in decimal, has a modulus value of 4 (00 → 1 → 10 → 11, and return back to 00) so would therefore be called a modulo-4, or mod-4, counter. Note also that it has taken four clock pulses to get from 00 to 11.

3-Bit Asynchronous Binary Counter

The following is a three-bit asynchronous binary counter and its timing diagram for one cycle.

It works exactly the same way as a two-bit asynchronous binary counter mentioned above, except it has eight states due to the third flip-flop.

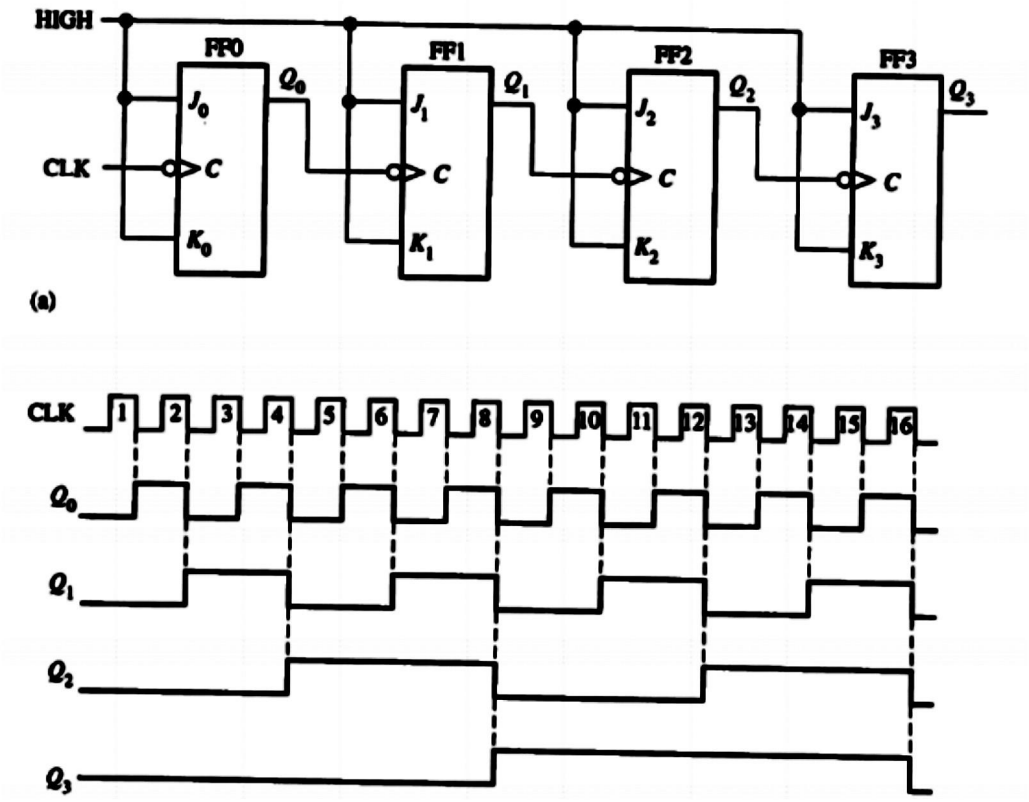




Counter State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

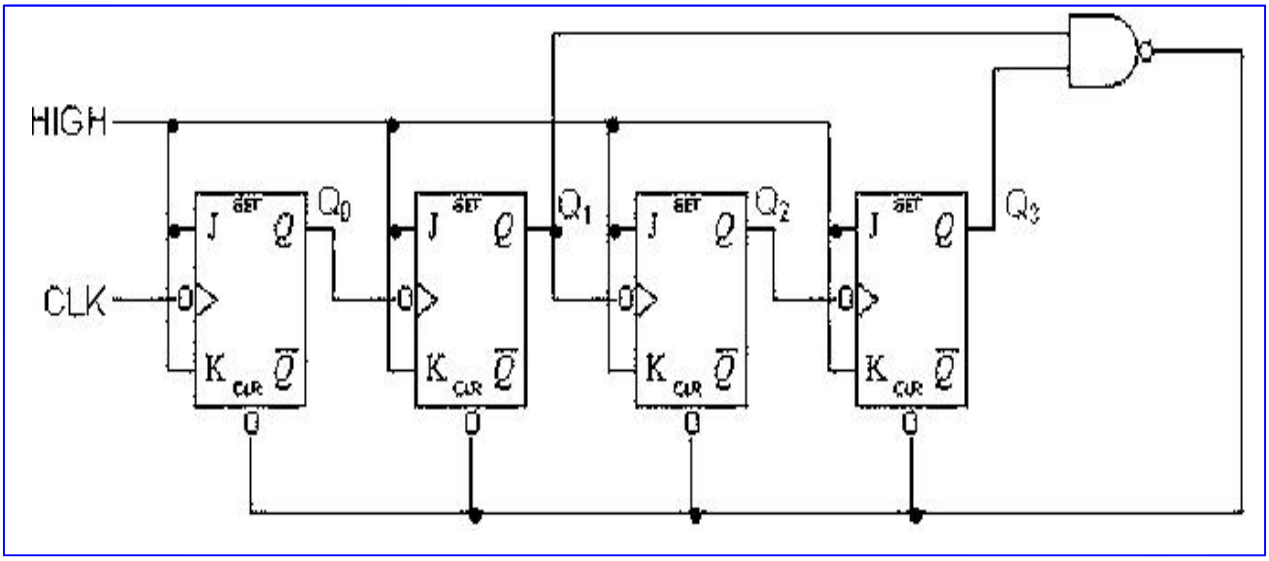
4 bit Asynchronous Binary Counter

The following is a 4-bit asynchronous binary counter and its timing diagram for one cycle. It works exactly the same way as a 2-bit or 3 bit asynchronous binary counter mentioned above, except it has 16 states due to the fourth flip-flop.



Asynchronous Decade Counters

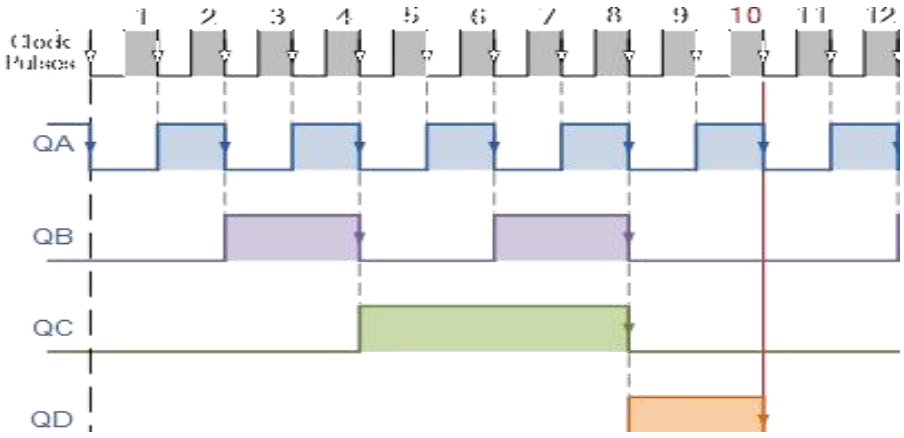
- The decade counter has four outputs producing a 4-bit binary number
- By using external AND and OR gates we can detect the occurrence of the 9th counting state to reset the counter back to zero.
- As with other mod counters, it receives an input clock pulse, one by one, and counts up from 0 to 9 repeatedly.
- Once it reaches the count 9 (1001 in binary), the counter goes back to 0000 instead of continuing on to 1010.
- The basic circuit of a decade counter can be made from JK flip-flops that switch state on the negative trailing-edge of the clock signal as shown.



This arrangement is a partial decoding, in which the two unique states, Q1 = 1 and Q3 = 1, are sufficient to decode the count of ten because none of the other states, zero through nine, have both Q1 and Q3 HIGH at the same time. When the counter goes into count ten (1010), the decoding gate output goes LOW and asynchronously resets all the flip-flops.

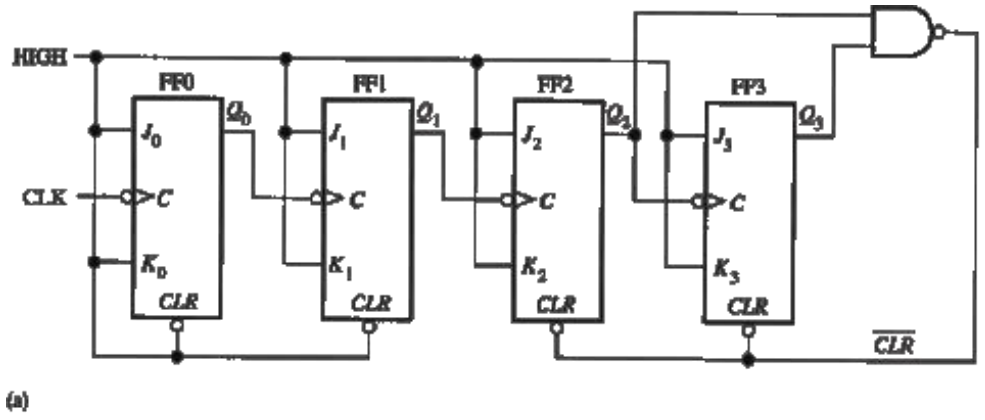
Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

Timing Diagram

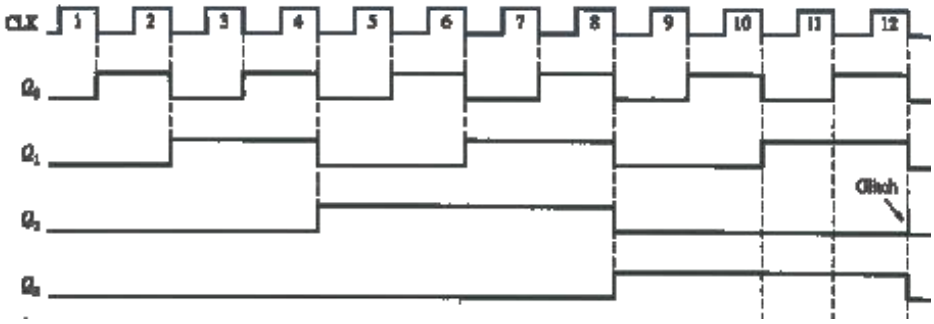


Modulus Twelve Asynchronous Counter

- An Asynchronous counter can be implemented having a modulus of 12 with a straight binary sequence from 0000 through 1011.
- The circuit diagram for a Mod-12 counter is shown below.
- It is obvious that a mod-12 counter will require 4 flip-flops which when connected as a counter, will provide 16 states. This counter counts 0, 1, 2, .., 15 and then it resets to 0. For a mod-12 counter,one may skip state 12 and return to state 0 from state 11 and the cycle should continue this way.
- For this an additional combinational logic circuit, i.e. a 2-input NAND gate is required, whose output is connected to clear terminal of all the flip flops. This will feed a reset pulse to the counter during state 12 (1100) and immediately after state 11 (1011). The flip-flops are reset and the counter starts counting again.

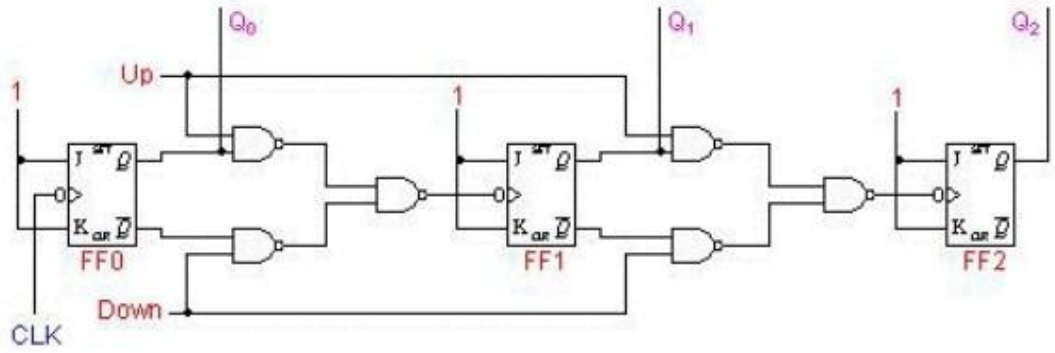


(a)



Asynchronous Up-Down Counters

In certain applications a counter must be able to count both up and down. The circuit below is a 3-bit up-down counter. It counts up or down depending on the status of the control signals UP and DOWN. When the UP input is at 1 and the DOWN input is at 0, the NAND network between FF0 and FF1 will gate the non-inverted output (Q) of FF0 into the clock input of FF1. Similarly, Q of FF1 will be gated through the other NAND network into the clock input of FF2. Thus the counter will count up.



When the control input UP is at 0 and DOWN is at 1, the inverted outputs of FF0 and FF1 are gated into the clock inputs of FF1 and FF2 respectively. If the flip-flops are initially reset to 0's, then the counter will go through the following sequence as input pulses are applied.