AN1207

Switch Mode Power Supply (SMPS) Topologies (Part II)

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INTRODUCTION

This application note is the second of a two-part series on Switch Mode Power Supply (SMPS) topologies.

The first application note in this series, AN1114 - "*Switch Mode Power Supply (SMPS) Topologies (Part I)*", explains the basics of different SMPS topologies, while guiding the reader in selecting an appropriate topology for a given application.

Part II of this series expands on the previous material in Part I, and presents the basic tools needed to design a power converter. All of the topologies introduced in Part I are covered, and after a brief overview of the basic functionality of each, equations to design real systems are presented and analyzed. Before continuing, it is recommended that you read and become familiar with Part I of this series.

CONTENTS

This application note contains the following major sections:

REQUIREMENTS AND RULES

The following requirements and rules were used to determine the various component values used in the design of a power converter.

The general design requirements are listed as follows:

- Nominal input voltage (V_{DC})
- Minimum input voltage (V_{DC}, min)
- Maximum input voltage (V_{DC}, max)
- Output voltage (V_{OUT})
- Nominal average output current (I_O, av, nom)
- Nominal minimum output current (I_O, av, min)
- Maximum ripple voltage (V_R, max)

In addition, a few common rules were used for component selection:

- MOSFETs (or switches) must be able to:
  - Withstand the maximum voltage
  - Withstand the maximum current
  - Operate efficiently and correctly at the frequency of the PWM
  - Operate in the SOA (dependant on dissipation)
- Diodes must be able to:
  - Withstand the maximum reverse voltage
  - Withstand the average current

Arrows are used in the circuit schematics to represent voltages. The voltage polarity is not directly reflected by the arrow itself (meaning if the voltage reverses, the arrow is not reversed, but that the value of the voltage is negative).

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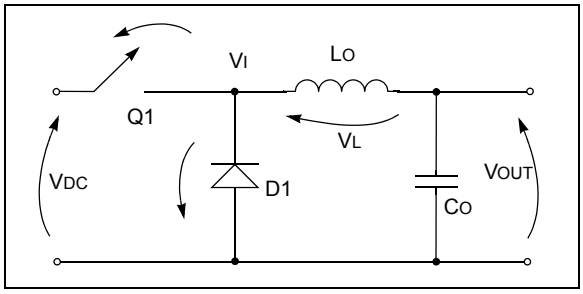
BUCK CONVERTER

The Buck Converter converts a high input voltage into a lower output voltage. It is preferred over linear regulators for its higher efficiency.

Topology Equations

Figure 1 shows the basic topology of a Buck Converter. The Q1 switch is operated with a fixed frequency and variable duty cycle signal.

FIGURE 1: BUCK CONVERTER TOPOLOGY



Accordingly, voltage VI is a square-wave $s(t)$. The Fourier series of such a signal is shown in Equation 1.

EQUATION 1:

$$s(t) = A\frac{\tau}{T} + \Sigma\sin$$

waves_with_frequency_multiple_of_the_square_wave_frequency

where:

τ = the duty cycle

T = the period

A = the square-wave amplitude

This means that the square-wave can be represented as a sum of a DC value and a number of sine waves at different, increasing (multiple) frequencies. If this signal is processed through a low-pass filter (Equation 2), the resulting output (DC value only) is received.

EQUATION 2:

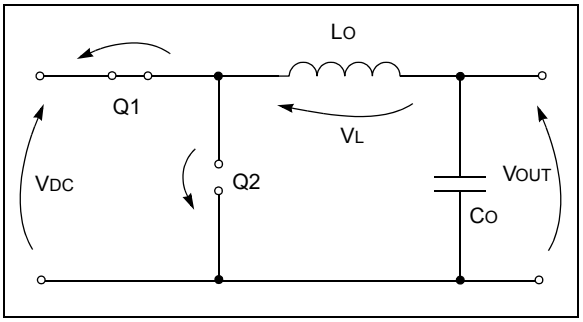
$$s_f(t) = A\frac{\tau}{T} = const$$

A LoCo low-pass filter extracts from the square-wave its DC value and attenuates the fundamental and harmonics to a desired level.

Q1 CLOSED (TON PERIOD)

In this configuration, the circuit is redrawn as shown in Figure 2. The diode is reverse-biased so that it becomes an open circuit.

FIGURE 2: BUCK CONVERTER TOPOLOGY: TON PERIOD



Based on Figure 2, the voltage on the inductor is as shown in Equation 3.

EQUATION 3:

$$V_L = V_{DC} - V_{Q,on} - V_{OUT}$$

The inductor current (having a constant time derivative value) is a ramp:

$$i_L(t) = i_L(0) + \frac{(V_{DC} - V_{Q,on} - V_{OUT})}{L_O}t$$

At time TON, equals:

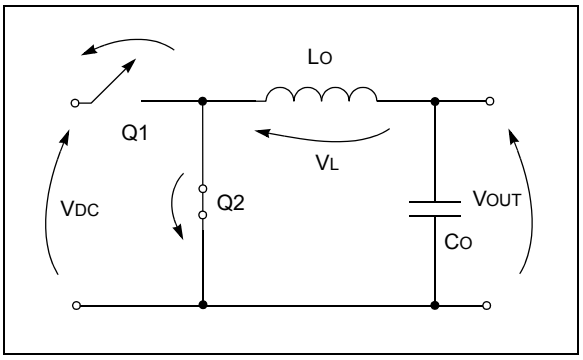
$$i_L(T_{ON}) = i_L(0) + \frac{(V_{DC} - V_{Q,on} - V_{OUT})}{L_O}T_{ON}$$

Where T_{ON} is the duration of the time interval when the switch Q1 is closed.

Q1 OPEN (TOFF PERIOD)

As shown in Figure 3, when the switch Q1 opens, the inductor will try to keep the current flowing as before.

FIGURE 3: BUCK CONVERTER TOPOLOGY: TOFF PERIOD



As a result, the voltage at the D1, LO, Q1 intersection will abruptly try to become very negative to support the continuous flow of current in the same direction (see Figure 4).

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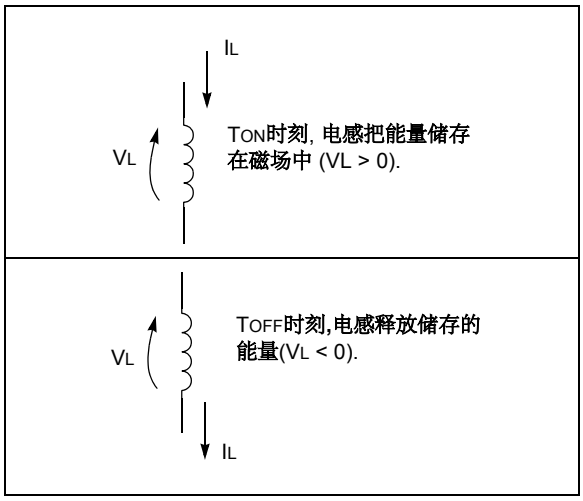
FIGURE 4: INDUCTOR BEHAVIOR



Equation 4 shows the resulting inductor voltage, while Equation 5 shows the current.

EQUATION 4:

$$V_L = -V_{OUT} - V_{D,on}$$

EQUATION 5:

$$i_L(t) = i_L(T_{ON}) + \frac{-V_{OUT} - V_{D,on}}{L_O} t$$

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

What has been described until now is called Continuous mode. To understand what it is and its importance, refer to Figure 5(G), which represents the inductor current. As previously seen, there is a ramp-up during TON and a ramp-down during TOFF.

The average current can be computed easily using Equation 6.

EQUATION 6:

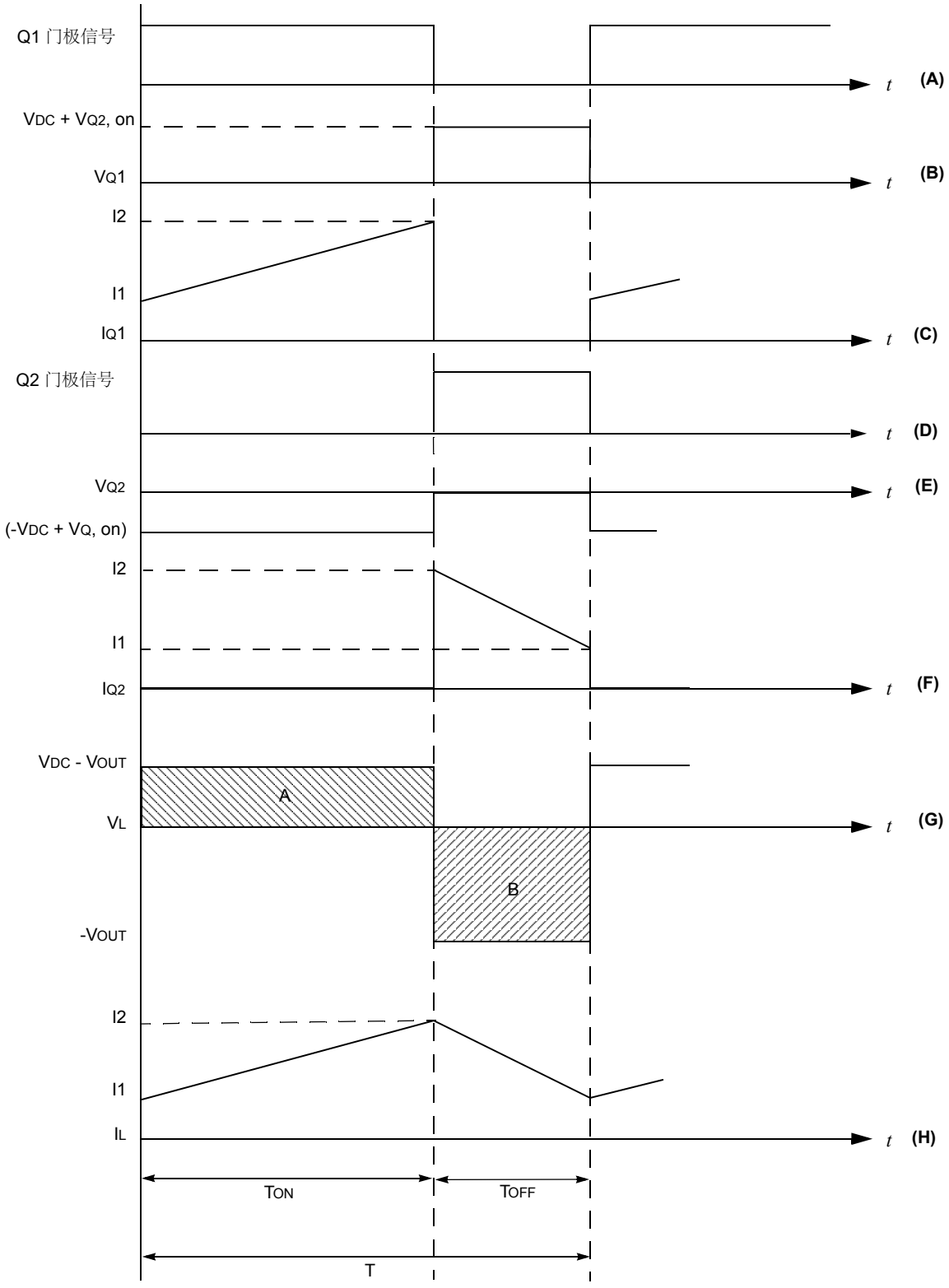
$$I_{L,av} = \frac{I_2 + I_1}{2}$$

The average inductor current is also the current flowing to the output, so the output average current is equal to Equation 7.

EQUATION 7:

$$I_{O,av} = \frac{I_2 + I_1}{2}$$

FIGURE 5: BUCK CONVERTER WAVEFORMS



(A) = Q1门极控制信号
(B) = Q1漏极、源极电压
(C) = Q1电流
(D) = Q2门极控制信号
(E) = Q2漏极、源极电压
(F) = Q2电流
(G) = 电感Lo电压
(H) = 电感Lo电流

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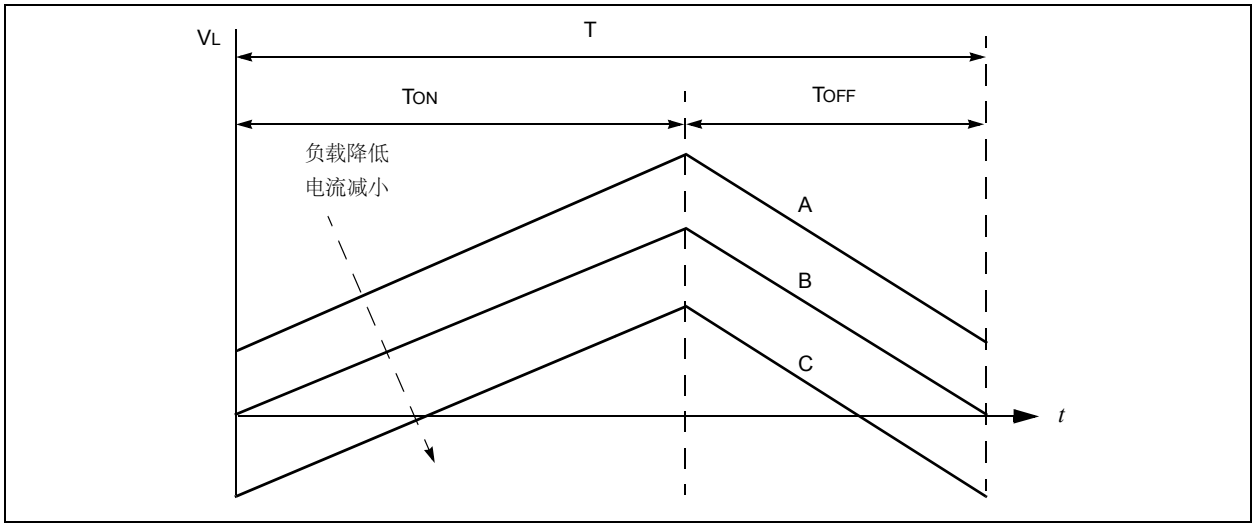
Supposing the output load RO (connected in parallel to the output capacitor CO) changes by increasing, this change has the effect of reducing the average output current. As shown in Figure 6, current moves from line A for the nominal load, to line B for a larger load. What should be noted is that the slopes of the two ramps, both during TON and TOFF, do not change because, they only depend on VDC, VOUT and L, and they have not been changed. As a consequence, increasing the load results in RO becoming greater. Since VO equals constant (the control loop explained earlier handles this) and RO increases, the current diminishes.

FIGURE 6: INDUCTOR CURRENT AT DIFFERENT LOADS



CONTINUOUS MODE

Operating in the Continuous mode is so named since the current in the inductor never stops flowing (goes to zero).

As shown in Figure 6, if the load continues to increase (reducing IO, av), at some time the inductor current plot will touch the x-axis (line C). This means the initial and final current (at the beginning and the end of the switching period) in the inductor is zero. At this point, the inductor current enters what is considered as Critical mode.

If the load is further increased, the current during the down-ramp will reach zero before the end of the period T (line D), which is known as Discontinuous mode.

Note:	In Discontinuous mode, the only way to further decrease the inductor current is to reduce the ON time (TON).

One key point is that the inductor current at the end of the TOFF period must equal the inductor current at the beginning of the TON period, meaning the net change in current in one period must be zero. This must be true at Steady state, when all transients have finished, and the circuit behavior is no longer changing.

Using the value of IL(TON) derived from Equation 3 and Equation 5 creates the relationship shown in Equation 8.

EQUATION 8:

$$\Delta I_L \propto (V_{DC} - V_{Q,on} - V_{OUT})T_{ON} = (V_{OUT} + V_{D,on})T_{OFF}$$

Neglecting VD, on and VQ, on, Equation 8 can be solved for VOUT, as shown in Equation 9.

EQUATION 9:

$$V_{OUT} = V_{DC}D$$

where $D = Ton / T$ (duty cycle), or

$$D = \frac{V_{OUT}}{V_{DC}}$$

The maximum duty cycle is achieved when the input voltage is at its minimum, as shown in Equation 10.

EQUATION 10:

$$D_{max} = \frac{V_{OUT}}{V_{DC,min}}$$

Therefore, D must obviously be between '0' and '1'.

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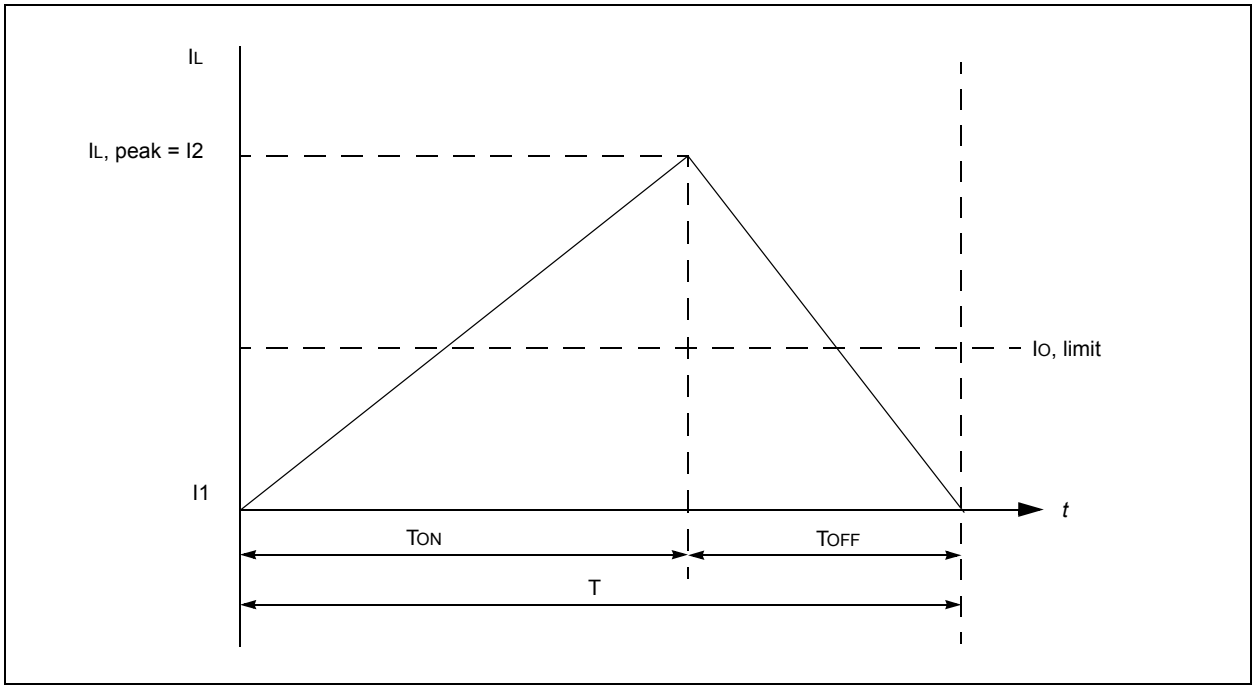
DISCONTINUOUS MODE

In Discontinuous mode, the inductor current goes to zero before the period T ends.

The inductor (output) average current (I_O, av, min) that determines the edge between Continuous and Discontinuous mode can be easily determined, as shown Figure 7.

FIGURE 7: INDUCTOR CURRENT AT THE EDGE OF DISCONTINUOUS MODE



Based on Figure 7, the inductor current limit is equal to Equation 11.

EQUATION 11:

$$I_{O,limit} = \frac{1}{2}I_{L,peak} = \frac{1}{2}(I_2 - I_1) = \frac{1}{2}I_2$$

From this point on, the behavior of the Buck Converter changes radically.

If the load continues to increase, the only possibility the system has to reduce the current, is to reduce the duty cycle (Figure 6). However, this means that a linear relationship, as shown in Equation 9, no longer exists between input and output.

The relationship between V_{DC}, V_{OUT} and D can be obtained with some additional effort, as shown in Equation 12.

EQUATION 12:

$$D = \frac{V_{OUT}}{V_{DC}}\sqrt{\frac{\frac{I_O}{I_{O,limit}}}{1-\frac{V_{OUT}}{V_{DC}}}}$$

Figure 8 illustrates this relationship.

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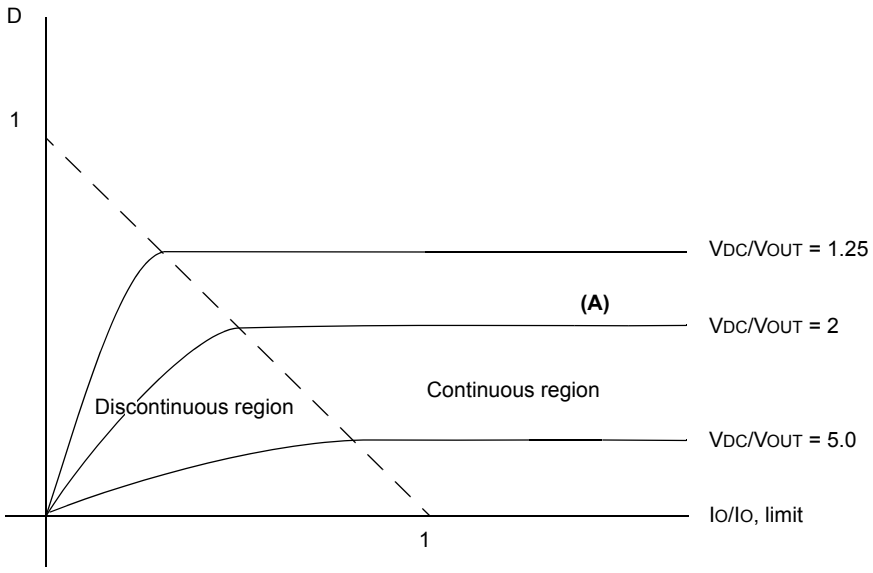
FIGURE 8: DUTY CYCLE IN CONTINUOUS AND DISCONTINUOUS REGIONS



As shown in Figure 8, starting from the continuous region and moving along line (A), where D = 0.5, as soon the boundary between continuous and discontinuous regions (dotted line) is crossed, to keep the same output voltage (V_{DC}/V_{OUT} = 2), D changes according to the nonlinear relation in Equation 12.

Design Equations and Component Selection

This section determines the equations that enable the design of a Continuous mode Buck Converter.

INDUCTOR

The average minimum current (I_O, av, min) is set as the average output current at the boundary of Discontinuous mode (Figure 7). This way, for any current larger than I_O, av, min, the system will operate in Continuous mode. Usually it is a percentage of I_O, av, nom, where a common value is 10%, as shown in Equation 13.

EQUATION 13:

$$I_{o,av,min} = I_{O,limit} = 0.1I_{o,av,nom} = \frac{1}{2}I_2 = \frac{(V_{DC,nom} - V_{OOUT})}{2L_O}T_{ON}$$

Solving Equation 13 with respect to L_O results in Equation 14.

EQUATION 14:

$$L_O = \frac{5(V_{DC,nom} - V_{OUT})V_{OUT}}{V_{DC,nom}F_{PWM}I_{O,av,nom}}$$

where F_{PWM} is the PWM frequency (F_{PWM} =1/T)

Power Losses In The Inductor

Power losses in the inductor are represented by Equation 15.

EQUATION 15:

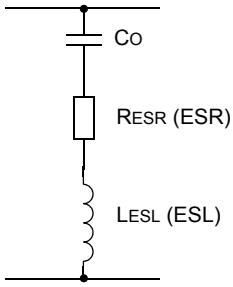
$$P_{LOSS,inductor} = (I_{O,av,nom})^2 ESR$$

where ESR is the equivalent inductor resistance

OUTPUT CAPACITOR

The current ripple generates an output voltage ripple having two components, as shown in Figure 9.

FIGURE 9: MODEL OF THE OUTPUT CAPACITOR Co



The first component of the ripple voltage (VR) is caused by the effect series resistance (ESR) of the output capacitor. This resistance is shown in Figure 9 as RESR.

The second component, VR,CO, comes from the voltage drop caused by the current flowing through the capacitor, which results in Equation 16.

EQUATION 16:

$$V_{R,\,ESR} = R_{ESR}(I_2 - I_1) = R_{ESR}\Delta I_L$$

where (I_2 - I_1) is the ripple current flowing in the inductor and to the output (at the edge of Discontinuous mode, which is: $\Delta I_L = 2\,I_O$, *limit*), and

$$V_{R,\,C_O} = \frac{1}{C_O}\int i_C(t)\;dt$$

The two contributions are not in phase; however, considering the worst case, if they are summed in phase, this results in one switching period, as shown in Equation 17.

EQUATION 17:

$$\Delta V_{R,\,total} = R_{ESR}\Delta I_L + \frac{1}{C_O}\Delta I_L\frac{D}{F_{PWM}}$$

By rearranging terms, the required capacitor value needed to guarantee the specified output voltage ripple is shown in Equation 18.

EQUATION 18:

$$C_O = \frac{\Delta I_L D}{F_{PWM}[\Delta V_{R,\,total} - R_{ESR}\Delta I_L]}$$

Power Losses in the Capacitor

Power losses dissipated in the capacitor are shown in Equation 19.

EQUATION 19:

$$P_{LOSS,\,capacitor} = \Delta I_L{}^2 R_{ESR}$$

DIODE

Referring to Figure 5(E), the current flowing through the diode during TOFF is the inductor current. It is easy then to compute the average diode current using Equation 20.

EQUATION 20:

$$I_{D,\,av} = I_{O,\,av,\,nom}(1 - D)$$

The maximum reverse voltage the diode has to withstand is during TON (see Figure 5(D)), as shown in Equation 21.

EQUATION 21:

$$V_{R,\,max} = -V_{DC,\,max} + V_{Q,\,on}$$

Power Dissipation Computation in the Diode

Because voltage on the diode is non-zero (VR), but the current is zero, dissipation during TON is equal to Equation 22.

EQUATION 22:

$$P_{D,\,T_{ON}} = 0$$

Dissipation during TOFF is equal to Equation 23.

EQUATION 23:

$$P_{D,\,T_{OFF}} = V_f I_{O,\,av,\,nom}\frac{T_{OFF}}{T} = V_f I_{O,\,av,\,nom}(1 - D)$$

MOSFET

The maximum voltage on the switch (see Figure 5(B)) during TOFF is shown in Equation 24.

EQUATION 24:

$$V_{Q,\,max} = V_{DC,\,max} + V_{D,\,on}$$

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The average current (Figure 5(C)) during TON is shown in Equation 25.

EQUATION 25:

$$I_{Q,av} = I_{O,av,nom}D$$

MOSFET Power Losses Computation

Static Dissipation

During TON, the average current flowing in Q1 is IO, av, nom • D and the voltage is V = V*f*, the switch forward voltage, which results in Equation 26. This value is small since VF is relatively small.

EQUATION 26:

$$P_{Q1,static,T_{ON}} = V_f I_{O,av,nom}\frac{T_{ON}}{T} = DV_f I_{O,av,nom}$$

This same loss can be expressed using the RDS(ON) of the MOSFET, taking care to determine from the component data sheet the value of RDS(ON) at the expected junction temperature (RDS(ON) grows with temperature). This term can be written as shown in Equation 27.

EQUATION 27:

$$P_{Q1,static,T_{ON}} = D(I_{O,av,nom})^2 R_{DS(ON)}\Big|_{hightemp}$$

During TOFF, the voltage on Q1 is VDC + VD, on (Figure 5(B)), but the current is zero. As shown in Equation 28, there is no contribution to the dissipated power.

EQUATION 28:

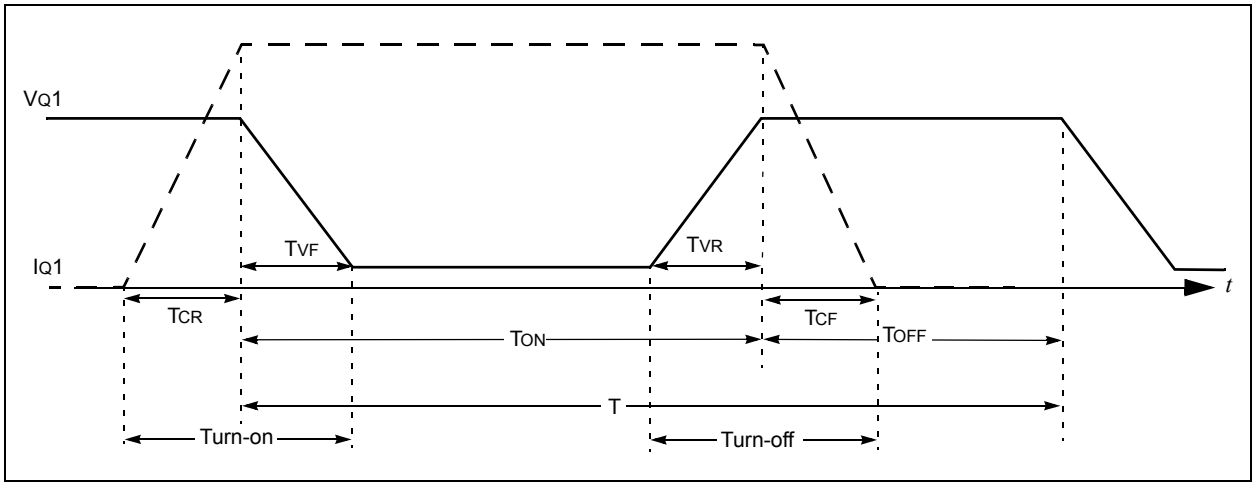
$$P_{Q1,static,T_{OFF}} = 0$$

Switching Dissipation

Figure 10 illustrates what occurs during switching. There are two events to consider: turn-on (Q1 closes) and turn-off (Q1 opens).

In both cases, voltage and current do not change abruptly, but have a linear behavior. The representation in Figure 10 is the worst-case possibility where at turn-on the voltage VQ1 remains constant at VDC, while the current is ramping up from zero to its maximum value. Only at this moment does the voltage start falling to its minimum value of VF. In reality, the two ramps will somehow overlap; however, since this is the worst case, this depicted situation is considered the current switching event. Therefore, at turn-on the power is equal to Equation 29.

FIGURE 10: MOSFET SWITCHING LOSS COMPUTATION WAVEFORMS



EQUATION 29:

$$P_{Q1,switching,turnon} =$$

$$= \frac{1}{T}\int V_{Q1}I_{Q1}dt \cong \frac{1}{T}\int_0^{T_{CR}} V_{DC}\frac{I_{O,av,nom}}{T_{CR}}tdt + \frac{1}{T}\int_0^{T_{VF}} I_{O,av,nom}\left(\frac{V_{DC}}{T_{VF}}\right)tdt = \frac{V_{DC}I_{O,av,nom}}{2}\frac{T_{CR}}{T} + \frac{V_{DC}I_{O,av,nom}}{2}\frac{T_{VF}}{T}$$

If TCR is equal to Equation 30, the result of Equation 29 can be simplified, as shown in Equation 31.

EQUATION 30:

$$T_{CR} = T_{VF} = T_{SW}$$

EQUATION 31:

$$P_{Q1,\,switching,\,turnon} = V_{DC} I_{O,\,av,\,nom} \frac{T_{SW}}{T}$$

At turn-off the switching loss can be calculated using Equation 32.

EQUATION 32:

$$P_{Q1,\,switching,\,turn-off} =$$

$$= \frac{1}{T}\int V_{Q1} I_{Q1} dt \cong \frac{1}{T}\int_{0}^{T_{VR}} I_{O,\,av,\,nom} \frac{V_{DC}}{T_{VR}} t dt + \frac{1}{T}\int_{0}^{T_{CF}} V_{DC} \frac{I_{O,\,av,\,nom}}{T_{CF}} t dt = \frac{V_{DC} I_{O,\,av,\,nom}}{2} \frac{T_{VR}}{T} + \frac{V_{DC} I_{O,\,av,\,nom}}{2} \frac{T_{CF}}{T}$$

Again, if TVR is equal to Equation 33, this computation results in Equation 34.

EQUATION 33:

$$T_{VR} = T_{CF} = T_{SW}$$

EQUATION 34:

$$P_{Q1,\,switching,\,turn-off} = V_{DC} I_{O,\,av,\,nom} \frac{T_{SW}}{T}$$

The total dissipation in the MOSFET is shown in Equation 35.

EQUATION 35:

$$P_{Q1,\,total} = P_{Q1,\,static,\,T_{ON}} + P_{Q1,\,switching,\,turn-on} + P_{Q1,\,switching,\,turn-off} = D V_f I_{O,\,av,\,nom} + 2 V_{DC} I_{O,\,av,\,nom} \frac{T_{SW}}{T}$$

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Buck Converter Design Example

This section shows how the equations previously discussed are to be used in the design process of a Buck Converter. In addition, the typical design requirements and how they influence the design are also discussed.

DESIGN REQUIREMENTS.

The design requirements are:

- Input voltage: V_{DC} = 12V ±30%
- Output voltage: V_{OUT} = 5V
- I_O nominal = I_O, av, nom = 2A
- I_O limit = 0.1 I_O, av, nom = 0.2A
- (I2 - I1) = ΔI_L = 2 I_O, limit = 0.4A
- Switching frequency = 200 kHz
- Output ripple voltage = 50 mV
- Input ripple voltage = 200 mV

DESIGN PROCESS

Duty Cycle Computation

The converter is supposed to operate in Continuous mode, so that Equation 9 holds and:

- Dnominal = V_{OUT}/V_{DC} = 5/12 = 0.42.

In addition, the maximum and minimum available input voltages will be computed:

- Minimum input voltage = 8.5V
- Maximum input voltage = 15.5V

Inductor

According to Equation 14, the nominal value of the inductor (Continuous mode) is equal to Equation 36.

EQUATION 36:

$$L_o = \frac{5(V_{DC} - V_{OUT})}{I_{O,\,av,\,nom}} \frac{V_{OUT}}{V_{DC}} \frac{1}{F_{PWM}} = \frac{5 \cdot (12-5)}{2} \cdot \frac{5}{12} \cdot \frac{1}{200K} = 36\mu H$$

The inductor required to place the system in Continuous mode with the maximum input voltage is shown in Equation 37.

EQUATION 37:

$$L_{O,M} = \frac{V_{DC} - V_{OUT}}{0.2 I_{O,\,av,\,nom}} \frac{V_{OUT}}{V_{DC}} \frac{1}{F_{PWM}} = \frac{15.5-5}{0.2 \cdot 2} \cdot \frac{5}{15.5} \cdot \frac{1}{200K} = 42\mu H$$

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The required inductor with the minimum input voltage is shown in Equation 38.

EQUATION 38:

$$L_{O,m} = \frac{V_{DC} - V_{OUT}}{0.2 I_{O,av,nom}} \frac{V_{OUT}}{V_{DC}} \frac{1}{F_{PWM}} = \frac{8.5 - 5}{0.2 \cdot 2} \cdot \frac{5}{8.5} \cdot \frac{1}{200K} = 26\mu H$$

An inductor of at least 42 µH will prevent the converter from going discontinuous over the full input voltage range.

In fact, if the smallest inductor, L = 26 µH is selected, the maximum input voltage (V_{DC} = 15.5V) would result in a current ripple of I2 - I1 = 0.85A. Conversely, the inductor L = 42 µH with an input voltage of 8.5V gives a current ripple of 0.17A. This means that any inductor greater than 42 µH will fit.

Output Capacitance

Equation 39 is supposing to select a capacitance having ESR = 30 mΩ.

EQUATION 39:

$$C = \frac{\Delta I_L D}{F_{PWM}[V_{RIPPLE} - R_{ESR}\Delta I_L]} = \frac{0.4 \cdot 0.42}{200K[50 \cdot 10^{-3} - 30 \cdot 10^{-3} \cdot 0.4]} = 22\mu F$$

Input Capacitor

Using the same approach to compute the output capacitance, the input capacitance is then calculated using Equation 40.

EQUATION 40:

$$C = \frac{\Delta I_L D}{F_{PWM}[V_{RIPPLE} - R_{ESR}\Delta I_L]} = \frac{0.4 \cdot 0.42}{200K[0.2 - 30 \cdot 10^{3} \cdot 0.4]} = 4.5\mu F$$

Free-Wheeling Diode Selection

Based on Equation 21 (see also Figure 5(D)), the maximum reverse voltage on the diode during TON is then calculated, as shown in Equation 41.

EQUATION 41:

$$V_{R,max} = -V_{DC,max} + V_{Q,on} \approx -15.5V$$

According to Equation 20, the average current in the diode is calculated, as shown in Equation 42.

EQUATION 42:

$$I_{D,av} = I_{O,av,nom}(1 - D) = 2 \cdot (1 - 0.42) = 1.16A$$

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MOSFET selection

The key parameters for the selection of the MOSFET are the average current and the maximum voltage (referring to Equation 24 and Equation 25). The resulting calculations are shown in Equation 43 and Equation 44.

EQUATION 43:

$$V_{Q,max} = V_{DC,max} + V_D \approx 15.5V$$

EQUATION 44:

$$I_{Q,av} = I_{O,av,nom} D = 2 \cdot 0.42 = 0.84A$$

The power dissipated in the MOSFET can be computed with Equation 35, which results in Equation 45, where typical values of V_F = 1V and Tsw = 100 ns are used.

EQUATION 45:

$$P_{LOSS,max} = DV_f I_{O,av,nom} + 2V_{DC} I_{O,av,nom} \frac{T_{SW}}{T} = 0.42 \cdot 1V \cdot 2A + 2 \cdot 15.5V \cdot 2A \cdot \frac{100ns}{5\mu s} = 0.84 + 1.24 = 2.08W$$

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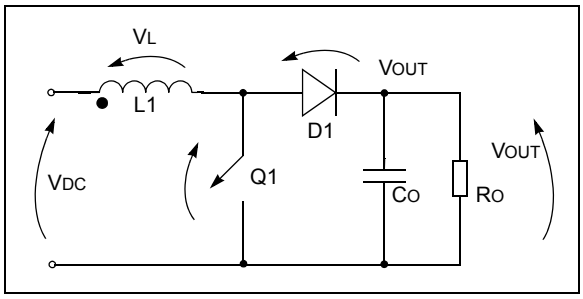
BOOST CONVERTER

A Boost Converter converts a lower input voltage to a higher output voltage.

Topology Equations

Figure 11 shows the essential topology of a Boost Converter.

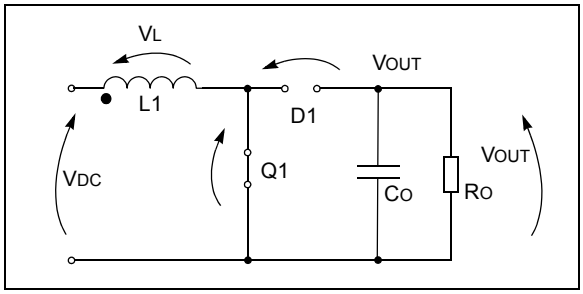
FIGURE 11: BOOST CONVERTER TOPOLOGY



Q1 CLOSED (TON PERIOD)

In this configuration, the circuit is redrawn as shown in Figure 12.

FIGURE 12: BOOST CONVERTER TOPOLOGY: TON PERIOD



The resulting voltage on the inductor is shown in Equation 46.

EQUATION 46:

$$V_L = V_{DC} - V_{Q,on}$$

Based on the inductor equation (Equation 46) the current results are shown in Equation 47.

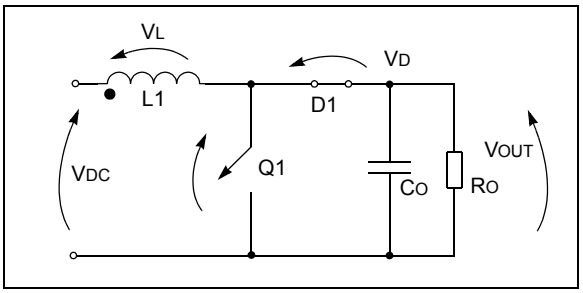
EQUATION 47:

$$I_L(t) = I_L(0) + \frac{(V_{DC} - V_{Q,on})}{L_1} t$$

Q1 OPEN (TOFF PERIOD)

When the switch opens (Figure 13), and since the inductor current cannot change abruptly, the voltage must change polarity. Current then begins flowing through the diode, which becomes forward-biased.

FIGURE 13: BOOST CONVERTER TOPOLOGY: TOFF PERIOD



The resulting inductor voltage is shown in Equation 48.

EQUATION 48:

$$V_L = V_{DC} - V_{D,on} - V_{OUT} < 0$$

The current flowing into the inductor during TOFF, which is ramping down, is computed using Equation 49.

EQUATION 49:

$$I_L(t) = I(T_{ON}) + \frac{V_{DC} - V_{D,on} - V_{OUT}}{L_1} t$$

OPERATING MODES

Like the Buck Converter, the Boost Converter can also be operated in Continuous and Discontinuous modes. The difference between the two modes is in the inductor current. In Continuous mode it never goes to zero, whereas in Discontinuous mode, the falling inductor current in the TOFF period reaches zero before the start of the following PWM period.

As in the case of the Buck Converter, the Boost Converter can be used in both modes. In either case, the control loop must be considered. A solution for one mode does not necessarily work well with the other.

Continuous Operating Mode

As usual, the two areas below the inductor voltage during TON and TOFF must be equal. This means that the current at the beginning of the PWM period equals the current at the end (Steady state condition) of the PWM period. Using Equation 47 and Equation 49, the relation shown in Equation 50 can be made.

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EQUATION 50:

$$V_{OUT} = \frac{V_{DC}}{1 - D}$$

where D is the duty cycle of the PWM signal.

It is important to note that this is a nonlinear relationship (Figure 14), unlike the Buck transfer function.

If a lossless circuit is assumed, $P_O = P_{DC}$, $V_O I_O = V_{DC} I_{DC}$, resulting in Equation 51.

EQUATION 51:

$$\frac{I_O}{I_{DC}} = (1 - D)$$

Discontinuous Operating Mode

To find the I/O relationship, a different approach is used where energy is considered, which differs from the approach used for Buck Converters.

The total power (P_T) delivered to the load comes from the contribution of the magnetic field in the inductor and, during T_{OFF}, from the input voltage V_{DC}.

The power delivered from the inductor (assuming 100% efficiency) is shown in Equation 52.

EQUATION 52:

$$P_L = \frac{L_1 I_P^2}{2T}$$

where Ip is the inductor peak current

The power delivered to the load by the input during T_{OFF} is shown in Equation 53.

EQUATION 53:

$$P_{DC} = V_{DC} \frac{I_P T_F}{2T}$$

where T_F, as indicated in Figure 15(G), is the portion of the T_{OFF} period from T_{ON} to when the inductor current reaches zero.

The total power delivered to the load is the sum of Equation 52 and Equation 53. The peak current is derived from Equation 47. If $T_{ON} + T_F = kT$, the results are that of Equation 54.

EQUATION 54:

$$V_{OUT} = V_{DC} \sqrt{\frac{kR_O T_{ON}}{2L_1}}$$

where R_O is the output load resistor

FIGURE 14:

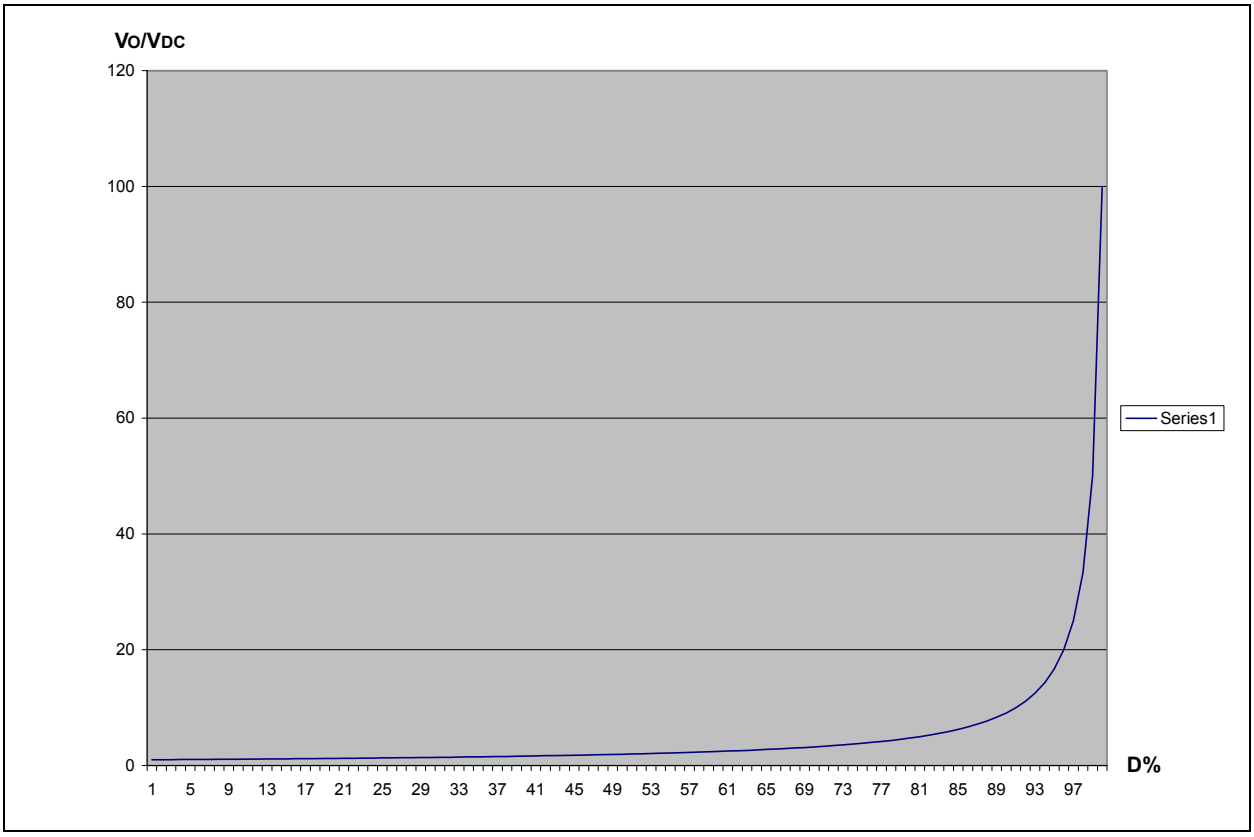
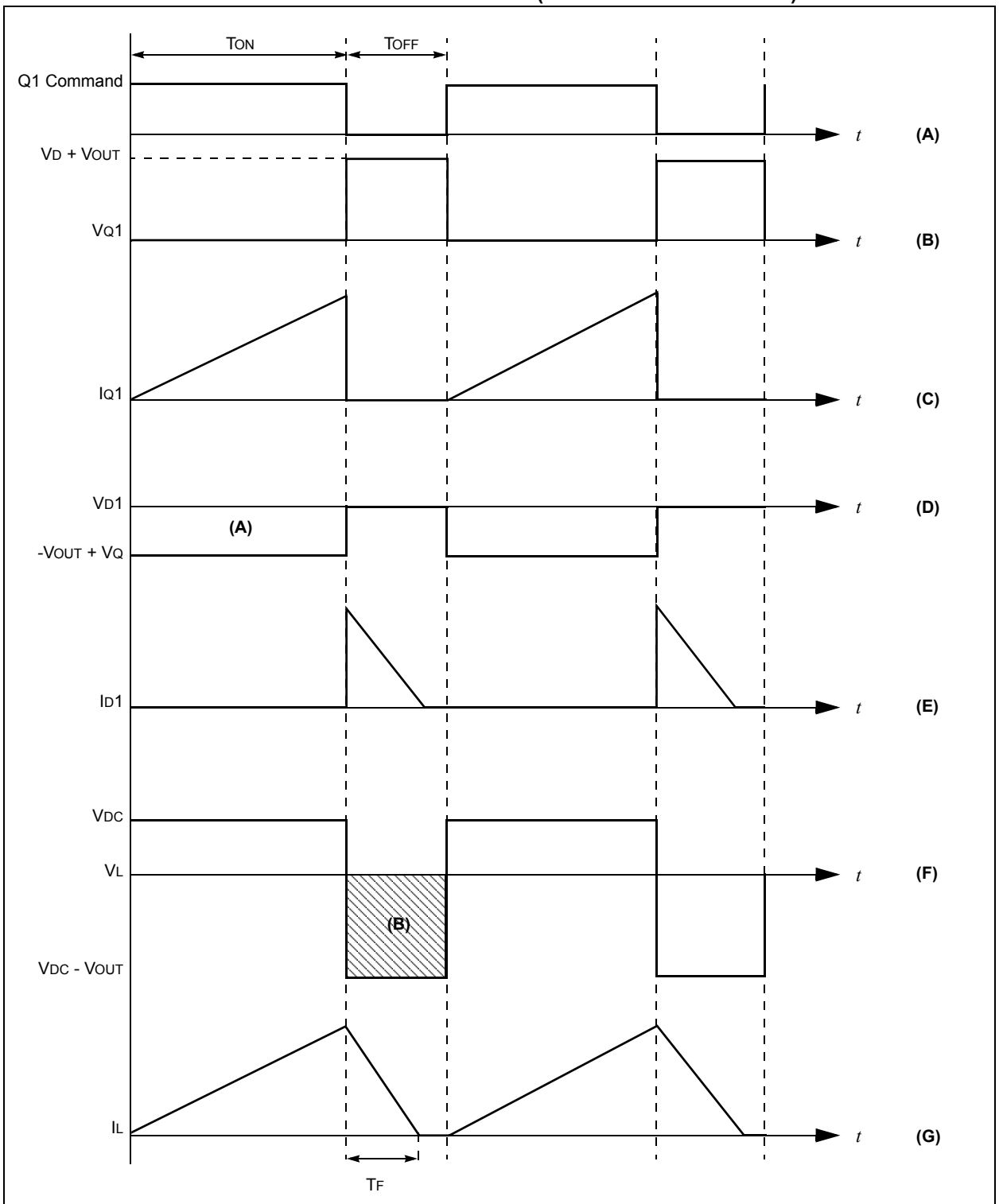


FIGURE 15: BOOST CONVERTER WAVEFORMS (DISCONTINUOUS MODE)



(A) = Command signal on Q1 MOSFET gate
(B) = Voltage on Q1 MOSFET
(C) = Current flowing into Q1 MOSFET
(D) = Voltage on D1 diode
(E) = Current in D1 diode
(F) = Voltage on LO inductor
(G) = Current in LO inductor

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Design Equations and Component Selection

As previously discussed, in Continuous mode, the input/output relationship is equal to Equation 50. In Discontinuous mode, this relationship is equal to Equation 54. The maximum ON time will correspond to the minimum input voltage, VDC.

The duty cycle can be chosen so that in Equation 54 TON + TF = kT < T, with 0 < k < 1.

Combining Equation 47 and Equation 49, and using the previous definition for TON + TF, gives an equation for TON, max, as shown in Equation 55. The resulting maximum duty cycle is shown in Equation 56.

EQUATION 55:

$$T_{ON,max} = \frac{kT(V_{OUT} - V_{DC,min})}{V_{OUT}}$$

EQUATION 56:

$$D_{max} = \frac{k(V_{OUT} - V_{DC,min})}{V_{OUT}}$$

INDUCTOR.

It is possible to compute the inductor L1 using Equation 54. The maximum TON, minimum VDC and minimum RO are assumed, which results in Equation 57.

EQUATION 57:

$$L_1 = \frac{kR_{O,min}D_{max}}{2F_{PWM}}\left(\frac{V_{DC,min}}{V_{OUT}}\right)^2$$

OUTPUT CAPACITOR

The output capacitor must be able to supply the output current during TON, without having a voltage drop greater than the maximum allowed output ripple.

Since the capacitor is large, it is possible to approximate the exponential discharge with a linear behavior. The current drawn from the capacitor is the average output current (IO, av, nom) and the charge lost during TON is equal to Equation 58. Therefore, the voltage drop is equal to Equation 59.

EQUATION 58:

$$Q_{ON} = I_{O,av,nom}T_{ON}$$

EQUATION 59:

$$V_{DROP,on} = \frac{I_{O,av,nom}T_{ON}}{C} < V_{RIPPLE}$$

A simplified representation is shown in Equation 60.

EQUATION 60:

$$C > \frac{I_{O,av,nom}T_{ON}}{V_{RIPPLE}}$$

DIODE

During TON, the diode D1 is open with the maximum reverse voltage, as shown in Equation 61.

EQUATION 61:

$$V_{R,max} = -V_{OUT} + V_{Q,on}$$

The average current in D1 during TOFF is shown in Equation 62.

EQUATION 62:

$$I_{D,av} = I_{O,av,nom}\frac{T_F}{T_T}$$

MOSFET

The average current represented in Figure 13 is shown in Equation 63.

EQUATION 63:

$$I_{Q1,av} = I_{O,av,nom}\frac{T_{ON}}{T}$$

The maximum voltage represented in Figure 12 is shown in Equation 64.

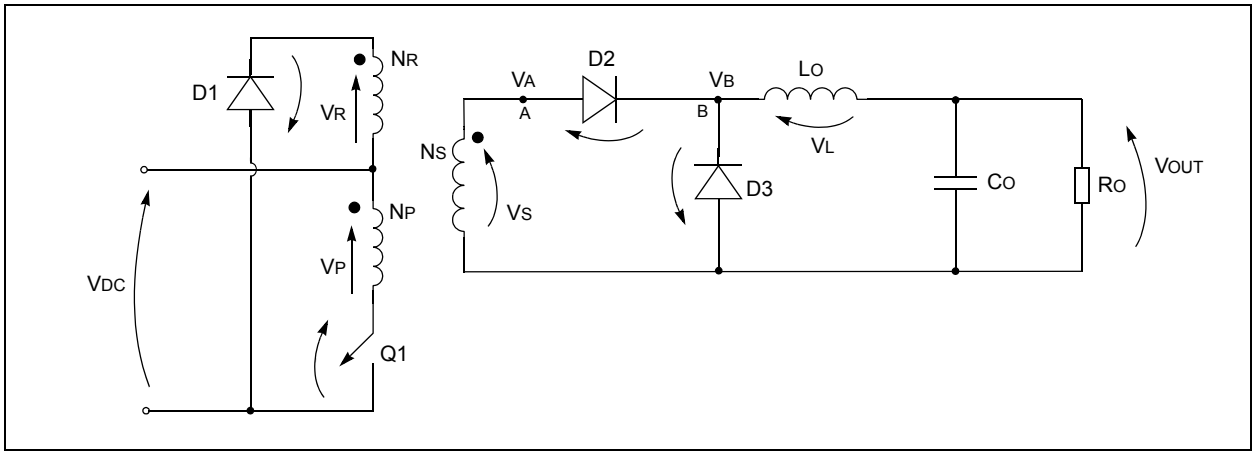
EQUATION 64:

$$V_{Q,max} = V_{OUT} + V_D$$

FORWARD CONVERTER

The topology of a Forward Converter, shown in Figure 16, can be considered a direct derivative of the Push-Pull Converter, where one of the switches is replaced by a diode. As a consequence, the cost is usually lower, which makes this topology very common.

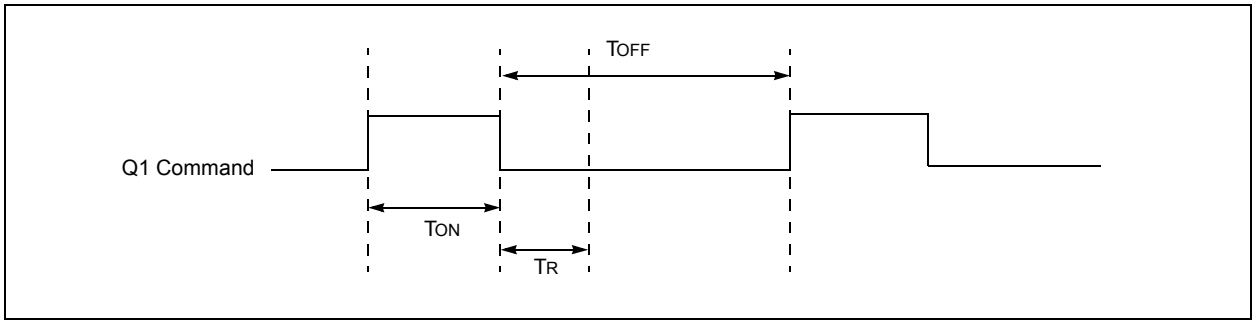
FIGURE 16: FORWARD CONVERTER TOPOLOGY



Topology Equations

Referring to the section on Forward Converters in AN1114 (see **"Introduction"**), the behavior of the system can be quickly summarized. The switch is driven by a waveform, whose duty cycle must be less than 50%, as shown in Figure 17.

FIGURE 17: Q1 MOSFET COMMAND SIGNAL TIMING



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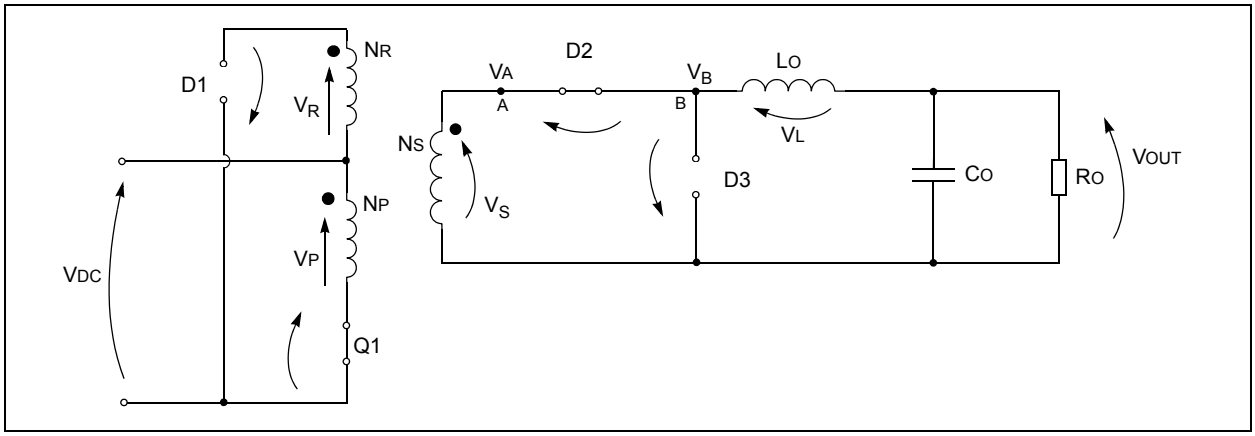
Q1 ON (INTERVAL 0 - TON)

For this configuration, the circuit is redrawn as shown in Figure 18.

FIGURE 18: FORWARD CONVERTER TOPOLOGY: INTERVAL 0 - TON



Input Circuit Behavior

The input voltage is directly connected to the winding NP, and consequently, the dot end of this winding is positive respect to the non-dot end. Similarly the dot end of NR has a higher voltage than the non-dot end. Diode D1 is reverse-biased and no current flows into the winding NR. The voltage on the winding NP is shown in Equation 65.

EQUATION 65:

$$V_{P,on} = V_{DC} - V_{Q,on}$$

The voltage on winding NR is shown in Equation 66.

EQUATION 66:

$$V_R = \frac{N_R}{N_P} V_{P,on} = \frac{N_R}{N_P}(V_{DC} - V_{Q,on})$$

The magnetizing current flowing into the NP windings and the switch Q1 circuit (current that would be flowing into the transformer if the secondary winding were open), is equal to Equation 67.

EQUATION 67:

$$I_M(t) = \frac{V_P}{L_M} t = \frac{V_{DC} - V_{Q,on}}{L_M} t$$

A positive-slope ramp whose maximum value is reached at TON is shown in Equation 68.

EQUATION 68:

$$I_M(T_{ON}) = \frac{V_{DC} - V_{Q,on}}{L_M} T_{ON}$$

The total current flowing into NP is the sum of the magnetizing current and the output current reflected to the primary through the transformer.

Output Circuit Behavior

Because of the voltage polarity on the primary windings, the dot end of the secondary winding is positive compared to its non-dot end. Consequently, D2 is forward-biased, while D3 is reverse-biased.

The secondary winding voltage is shown in Equation 69.

EQUATION 69:

$$V_S = \frac{N_S}{N_P}(V_{DC} - V_{Q,on})$$

The voltage to the right of the rectifying diode D2 is shown in Equation 70.

EQUATION 70:

$$V_B = V_S - V_{D,on} = \frac{N_S}{N_P}(V_{DC} - V_{Q,on}) - V_{D,on}$$

The voltage on the output inductor is shown in Equation 71.

EQUATION 71:

$$V_L = \frac{N_S}{N_P}(V_{DC} - V_{Q,on}) - V_{D,on} - V_{OUT}$$

The current flowing through the output inductor and through D2 is shown in Equation 72.

EQUATION 72:

$$I_L(t) = I_L(0) + \frac{\frac{N_S}{N_P}(V_{DC} - V_{Q,on}) - V_{D,on} - V_{OUT}}{L_O} t$$

At this point, the total current flowing into the primary can be computed. It has two contributions: the magnetizing current (see Equation 67) and the load current reflected back into the primary, as shown in Equation 73.

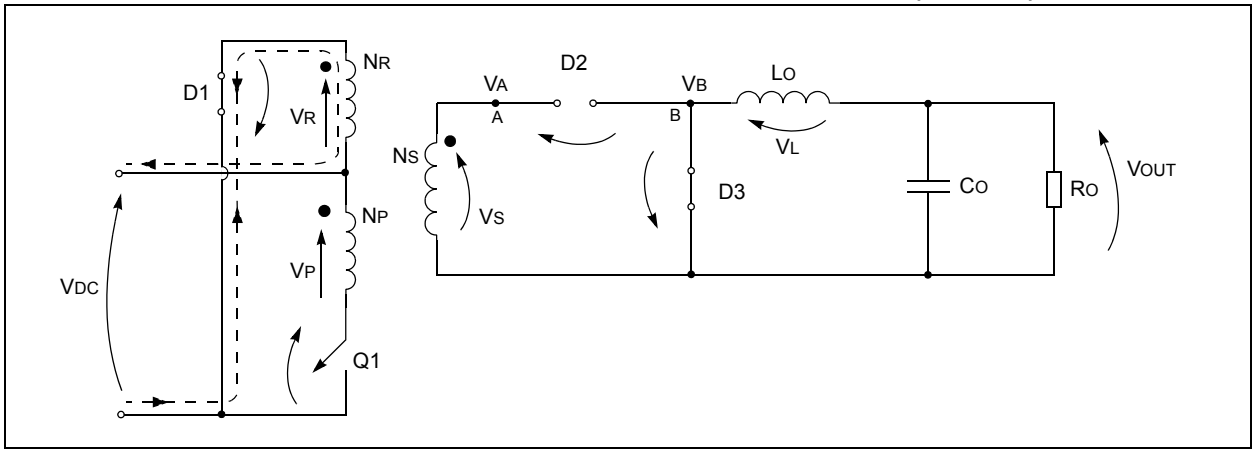
EQUATION 73:

$$I_{P,total} = I_L(0) + \frac{V_{DC} - V_{Q,on}}{L_M} t + \frac{N_S}{N_P} \frac{\frac{N_S}{N_P}(V_{DC} - V_{Q,on}) - V_{D,on} - V_{OUT}}{L_O} t$$

Q1 OFF [INTERVAL TON - (TON + TR)]

Based on this configuration, the circuit is redrawn, as shown in Figure 19.

FIGURE 19: FORWARD CONVERTER TOPOLOGY: INTERVAL TON - (TON + TR)



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Input Circuit Behavior

Before the switch Q1 was opened, the magnetizing current was flowing in N_P. When the switch opens, it reverses all the voltages to continue the flow. The dot end of N_R becomes negative in respect to the non-dot end, and a similar behavior is experienced by the winding N_P. Because of the polarity on N_R, diode D1 becomes forward-biased and keeps the voltage at the dot end of N_R, one diode drop below ground. Magnetizing current can now flow through N_R and diode D1 into the power supply V_{DC}, as shown in Figure 19. The voltage V_R on N_R is shown in Equation 74.

EQUATION 74:

$$V_R = -(V_{DC} + V_{D,on}) < 0$$

The voltage on N_P is shown in Equation 75.

EQUATION 75:

$$V_{P,off} = -\frac{N_P}{N_R}(V_{DC} + V_{D,on}) < 0$$

When t = T_{ON}, the current in the reset winding equals the magnetizing current I_M multiplied by the windings ration, as shown in Equation 76.

EQUATION 76:

$$I_R = \frac{N_P}{N_R} I_M$$

During T_R, this current has a down-slope and reaches zero when t = T_{ON} + T_R.

Output Circuit Behavior

As previously mentioned, the magnetizing current reverses all voltages when the switch Q1 turns off. As a result, the dot end of the secondary winding is more negative than the non-dot end and diode D2 becomes reverse-biased.

The secondary voltage is shown in Equation 77.

EQUATION 77:

$$V_{S,off} = -\frac{N_S}{N_R}(V_{DC} + V_{D,on})$$

To keep the current flowing into inductor L_O, its voltage reverses so that the left end of the inductor is more negative than the right end, and it would continuously decrease; however, the freewheeling diode D3, becoming forward-biased and sets VB to a diode voltage drop below ground. The voltage on the inductor is now equal to Equation 78.

EQUATION 78:

$$V_L = -V_{OUT} - V_{D,on}$$

Consequently the inductor current will decrease according to Equation 79:

EQUATION 79:

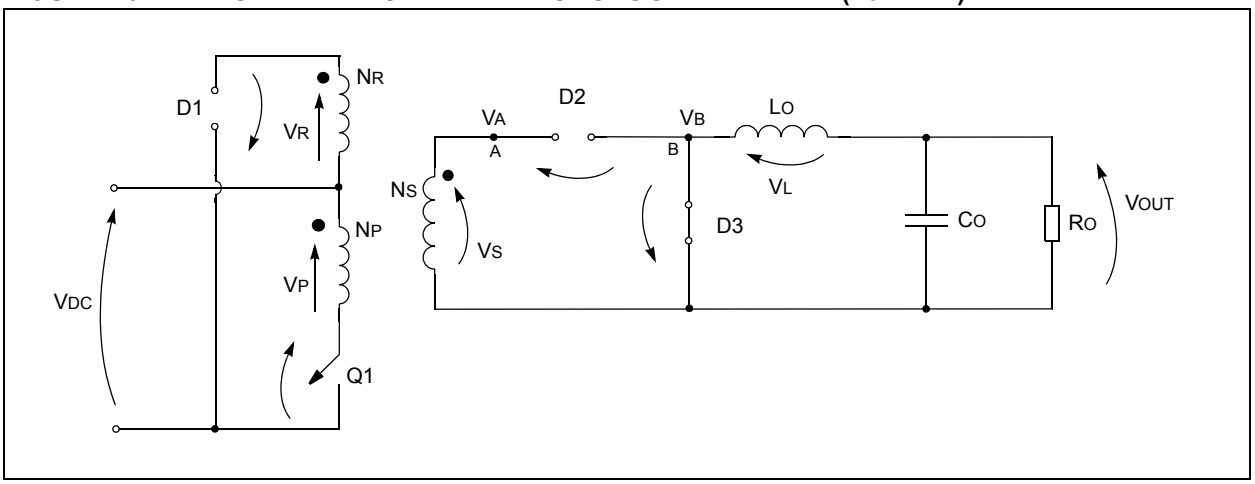
$$I_L(t) = I(T_{ON}) - \frac{V_{OUT} + V_{D,on}}{L_O} t$$

This current is the same current that is flowing into the free-wheeling diode D3.

Q1 OFF [INTERVAL (T_{ON} + T_R) TO T]

In this configuration, the circuit is redrawn as shown in Figure 20.

FIGURE 20: FORWARD CONVERTER TOPOLOGY: INTERVAL (T_{ON} + T_R) - T



Input Circuit Behavior

As soon as the magnetizing current reaches zero (at T_{ON} + T_R), all of the energy that had been stored into the transformer when T_{ON} has been released and diode D1 opens. Consequently, the voltage drop on N_R becomes zero and the voltages at both the dot end and the non-dot end of N_R equal V_{DC}. The voltage drop on N_P equally becomes zero, so that now the voltage applied to the switch is V_{DC}.

Output Circuit Behavior

Nothing changes compared to the previous time interval.

Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

At the output, at steady state, the current in the inductor L_O at t = 0, must equal the current at t = T. Expressing the inductor voltage as a function of the inductor current based on Equation 72 and Equation 78, results in Equation 80, which in turn solves Equation 81.

EQUATION 80:

$$\frac{\frac{N_S}{N_P}(V_{DC}-V_{Q,on})-V_{D,on}-V_{OUT}}{L_O}T_{ON}=$$

$$=\frac{V_{OUT}+V_{D,on}}{L_O}T_{OFF}$$

EQUATION 81:

$$V_{OUT}=\frac{N_S}{N_P}(V_{DC}-V_{Q,on})D-V_{D,on}$$

The magnetizing current, at time t = 0 and t = T_{ON} + T_R is zero (at Steady state). Therefore, ΔI_M during T_{ON} must equal ΔI_M during T_R, which is represented by Equation 82 (refer to Equation 65 and Equation 75).

EQUATION 82:

$$\frac{V_{DC}}{L_M}T_{ON}=\frac{N_P}{N_R}\frac{V_{DC}}{L_M}T_R \Rightarrow T_{ON}=\frac{N_P}{N_R}T_R$$

The circuit is now running at the maximum duty cycle when T_R equals T_{OFF}, which means the full T_{OFF} period is needed to nullify the magnetizing current. In this case, in Equation 82, T_R is replaced with its maximum theoretical value T_{OFF}, so that T_{ON}, max, as shown in Equation 83, is derived from Equation 84.

EQUATION 83:

$$T_{ON,max}=\frac{N_P}{N_R}T_{OFF} \Rightarrow T_{ON,max}=\frac{N_P}{N_R}(T-T_{ON,max})$$

EQUATION 84:

$$D_{max,theoretical}=\frac{1}{1+\frac{N_R}{N_P}}$$

In the case of N_R = N_P, Dmax, theoretical = 0.5.

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TRANSFORMER: PRIMARY

The core of the transformer during operation moves in the first quadrant of the hysteresis curve.

The change in flux, according to the Faraday law, as shown in Equation 85, is proportional to the product of the applied voltage VP, and the time Tx, during which this voltage is present.

EQUATION 85:

$$\Delta B = \frac{V_P \cdot T_X}{N_P A_{core}}$$

where the units are *Tesla* for ΔB and m^2 for A_{core}

During TON, this product equals (VDCTON), while during TR the product is NPVDC(TR)/NR, based on Equation 65 and Equation 75, neglecting VQ, on and VD, on.

In Figure 22(F), the product (VDCTON) equals area A1, while VDCNPTR/NR equals area A2.

It is preferable to have a net ΔB = 0, so that in the hysteresis plane, the operating point at the end of the PWM period has come back to the initial point. This guarantees that the system will never drift toward saturation.

The point is that the condition can easily be fulfilled, with different values of the ratio NP/NR by selecting a different number of turns on the two windings (see Figure 21). This provides an additional degree of freedom in the design of the system.

In general, TON + TR = kT; the maximum value for TON is chosen as TON, max = kT/2 when NP = NR. As indicated in Figure 21, the maximum value of TON is also dependent on the ration NP/NR. Based on the characteristics of the transformer core, ΔB is defined. From Equation 85, the primary number of turns can be determined, considering the minimum value of VDC and consequently, the maximum duty cycle as shown in Equation 86.

EQUATION 86:

$$N_P = \frac{D_{max}}{F_{PWM} A_{core} \Delta B}(V_{DC,min} - V_{Q,on})$$

Replacing NP in Equation 81 and neglecting VD, on, results in Equation 87.

EQUATION 87:

$$N_S = \frac{V_{OUT}}{F_{PWM} A_{core} \Delta B}$$

NR can be determined by considering the behavior described in Figure 21.

FIGURE 21: FORWARD CONVERTER: VOLTAGE ON THE MOSFET FOR DIFFERENT VALUES OF PRIMARY AND RESET WINDING TURNS

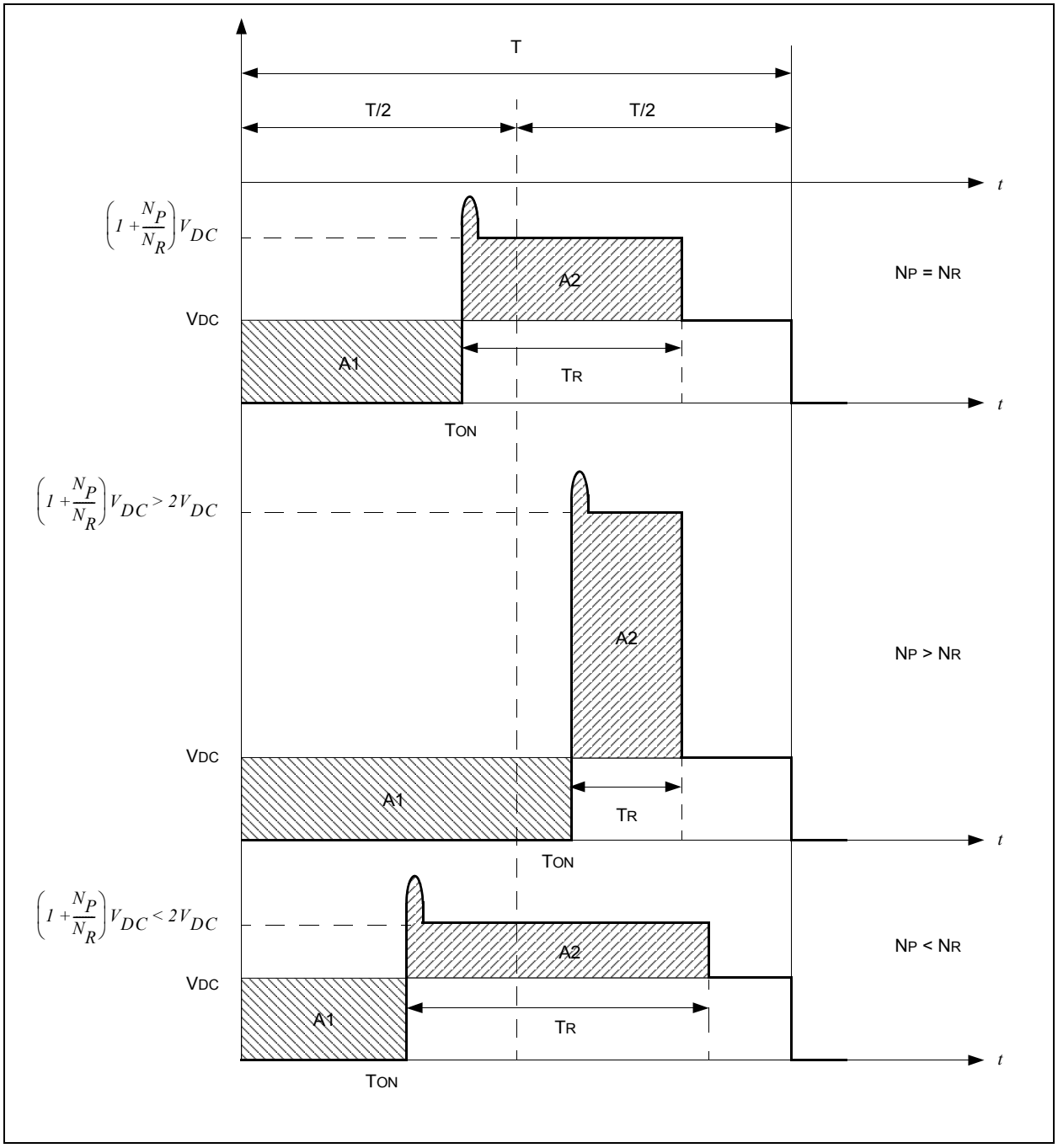

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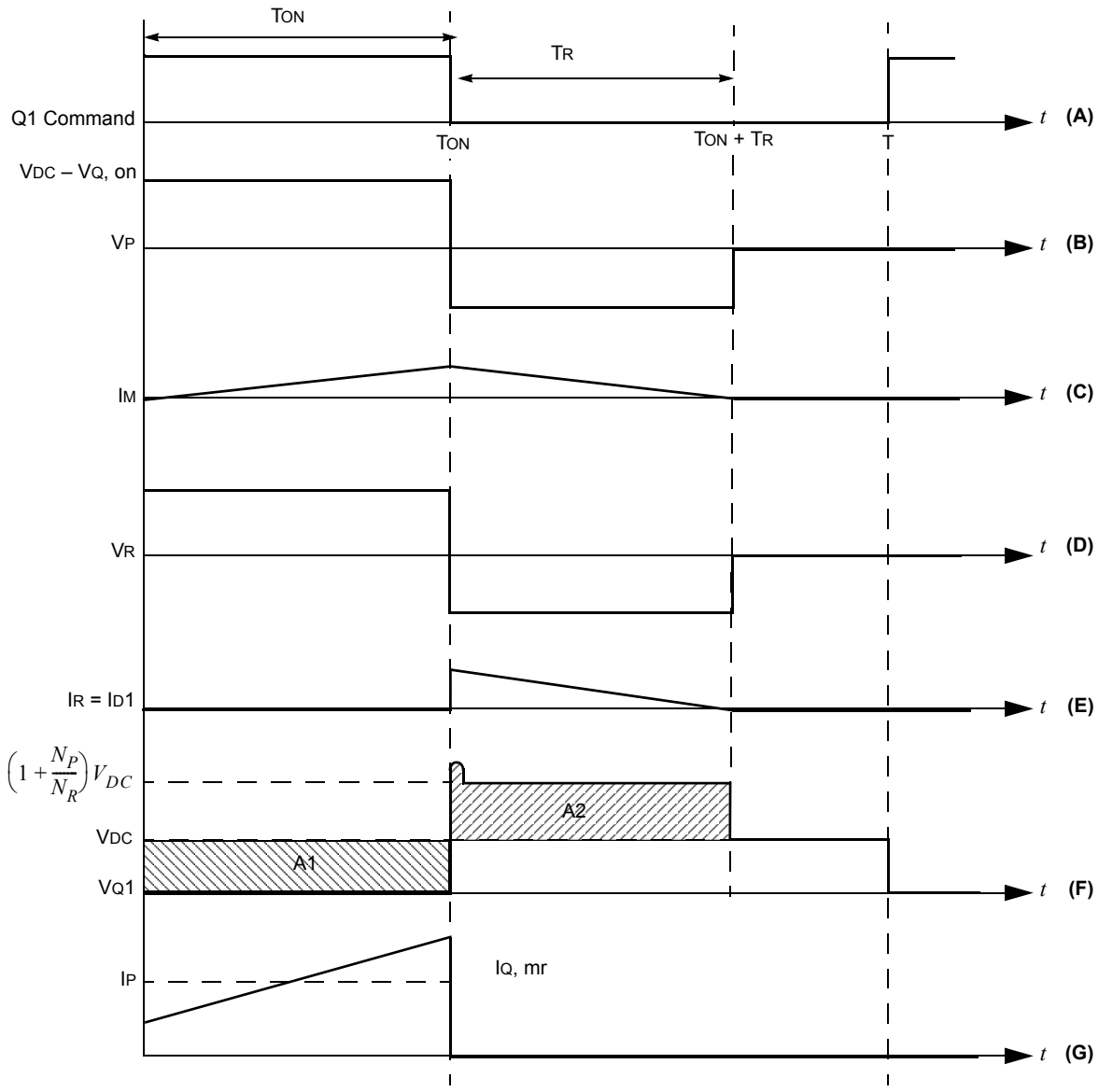
FIGURE 22: FORWARD CONVERTER WAVEFORMS ($N_P = N_R$): PRIMARY SIDE



(A) = Command signal on Q1 MOSFET gate

(B) = Voltage V_P on primary winding N_P

(C) = Magnetizing current I_M

(D) = Voltage V_R on reset winding N_R

(E) = Reset winding current, equal to diode D1 current

(F) = Voltage on Q1 MOSFET

(G) = Primary winding current, equal to Q1 MOSFET current

TRANSFORMER: PRIMARY, WIRE SIZE

As shown in Figure 22(G) the total current flowing into the primary has two contributions: the magnetizing current (Equation 67) and the load current (Equation 72) reflected back into the primary, resulting in Equation 88.

EQUATION 88:

$$I_{P,\,total} = \frac{V_{DC} - V_{Q,\,on}}{L_M}t + \frac{N_S}{N_P}\frac{\frac{N_S}{N_P}(V_{DC} - V_{Q,\,on}) - V_{D,\,on} - V_{OUT}}{L_O}t$$

The primary wire size can then be computed by first referring to Figure 22(G), and then replacing the real current waveform with a pulse having a square shaped waveform, with the same width and whose amplitude is the value in the middle of the ramp ($I_{Q,\,mr}$). The current is expressed as a function of known (design requirements) data.

Note that in these computations, magnetizing current is neglected since the transformer is designed to make it about one-tenth of the load reflected current. Therefore, the input power P_I equals Equation 89.

EQUATION 89:

$$P_I = V_{DC,\,min} I_{Q,\,mr} D_{max}$$

The output power is shown in Equation 90.

EQUATION 90:

$$P_O = \eta P_I = \eta V_{DC,\,min} I_{Q,\,mr} D_{max}$$

where η is the converter efficiency

Solving Equation 90 results in Equation 91.

EQUATION 91:

$$I_{Q,\,mr} = \frac{1}{\eta}\left(\frac{P_O}{V_{DC,\,min}}\right)\frac{1}{D_{max}}$$

This is the equivalent current flowing in the primary wires when T_{ON} is at its maximum allowed value. The rms value is computed in Equation 92.

EQUATION 92:

$$I_{Q,\,rms} = I_{Q,\,mr}\sqrt{D_{max}} = \frac{1}{\eta}\left(\frac{P_O}{V_{DC,\,min}}\right)\frac{\sqrt{D_{max}}}{D_{max}}$$

The correct AWG (wire size) can be determined accordingly.

TRANSFORMER: SECONDARY, WIRE SIZE

As shown in Figure 24(C), the secondary current equals the inductor current ($I_{O,\,av}$) during T_{ON}. Again, as for the primary current, the actual current waveform is replaced with a current pulse having a square shaped wave form whose amplitude equals the mid-ramp inductor current in the up-slope, $I_{O,\,av,\,nom}$.

Therefore, the secondary average current is equal to Equation 93.

EQUATION 93:

$$I_{S,\,av} = I_{O,\,av,\,nom}$$

The rms value is computed as Equation 94.

EQUATION 94:

$$I_{S,\,rms} = I_{O,\,av,\,nom}\sqrt{D_{max}}$$

TRANSFORMER: RESET WINDING, WIRE SIZE

The reset winding is not involved in carrying any current reflected back into the primary from the secondary. The only current it has to carry is the magnetizing current, which is plotted in Figure 22(C). The magnetizing peak current computed in Equation 67 is shown in Equation 95.

EQUATION 95:

$$I_{M,\,pk} = \frac{V_{D(C,\,min)} - V_{Q,\,on}}{L_M}T_{ON}$$

The rms value is the peak value multiplied by the square root of the duty cycle and divided by radix 3, as shown in Equation 96.

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EQUATION 96:

$$I_{M,rms} = \frac{(V_{DC,min} - V_{Q,on})}{L_M}\frac{\sqrt{D_{max}}}{\sqrt{3}}T_{ON}$$

MOSFET

During TOFF, the voltage on the Q switch is equal to Equation 97.

EQUATION 97:

$$V_{Q,off} = \left(1 + \frac{N_P}{N_R}\right)V_{DC}$$

At t = TON, a spike due to leakage current appears. It can safely be estimated to be 30% of the peak value, as shown in Equation 98.

EQUATION 98:

$$V_{Q,off,max} = 1.3 \cdot \left(1 + \frac{N_P}{N_R}\right)V_{DC,max}$$

The average current flowing through the switch has been computed in Equation 92.

DIODES

Table 1 summarizes the values of average current and voltage the diodes have to cope with.

TABLE 1: DIODE CURRENT AND VOLTAGE

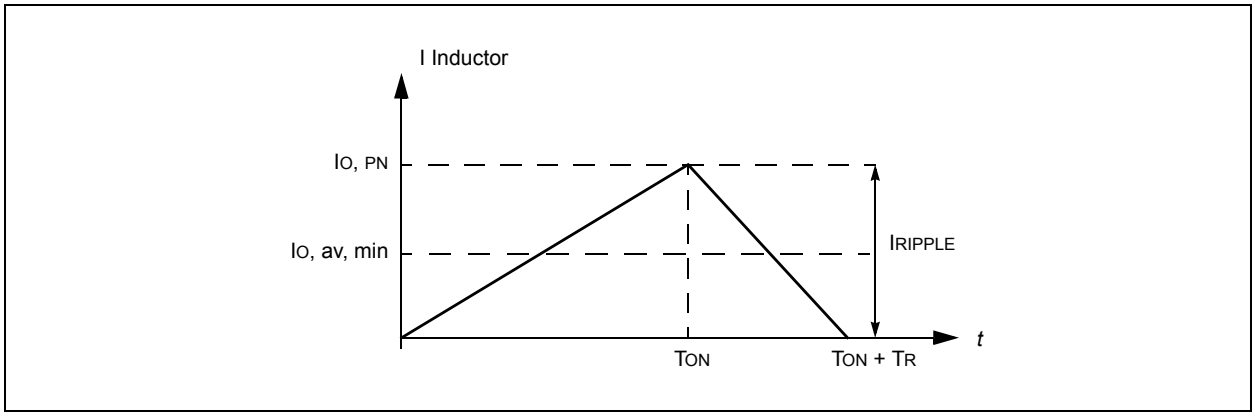
Diode	Configuration		
	0 - TON	**TON - (TON + TR)**	**(TON + TR) - T**
D1	$V_{D,max} = -\left(1 + \frac{N_R}{N_P}\right)V_{DC,max}$	V_F	$V_{D,max} = -V_{DC,max}$
D2	V_F	$V_{D,max} \approx -\frac{N_S}{N_R}V_{DC,max}$	$V_{D,max} \approx 0$
D3	$V_{D,max} \approx -\frac{N_S}{N_P}V_{DC,max}$	V_F	V_F

Legend: VF is the diode forward voltage.

OUTPUT FILTER INDUCTOR

As in all other topologies with an LC low-pass filter at the output, the inductor is selected to not operate the system in Discontinuous mode. The inductor is calculated just at the edge between Continuous and Discontinuous mode (i.e., Critical mode), where the inductor current starts from zero at the beginning of the PWM period and returns to zero before the PWM period ends. In this condition, the average current equals 0.5 the peak current (or current ripple), as shown in Figure 23.

FIGURE 23: INDUCTOR CURRENT: PEAK CURRENT, RIPPLE CURRENT AMPLITUDE AND OUTPUT CURRENT AT THE EDGE OF DISCONTINUOUS MODE



In Critical mode, the minimum acceptable output current (defined by design requirements) is made coincident with the average current, as shown in Equation 99.

EQUATION 99:

$$I_{O,\,av,\,min} = \frac{I_{O,\,ripple}}{2}$$

Using Equation 72 to compute IO, ripple, results in Equation 100.

EQUATION 100:

$$L_O = \frac{\frac{N_S}{N_P}V_{DC,\,min} - V_{OUT}}{2F_{PWM}I_{O,\,av,\,min}}D_{max}$$

OUTPUT CAPACITOR

The output voltage ripple is mainly due to the capacitor ESR. The inductor current ripple flowing through it, determines a voltage drop. Therefore, a capacitor with an ESR equal to Equation 101 must be selected.

EQUATION 101:

$$ESR < \frac{V_{OUT,\,ripple}}{I_{O,\,ripple}}$$

where $I_{O,\,ripple}$ is computed as in Equation 98

The capacitor value itself can then be computed with Equation 102, which describes the value of the voltage ripple taking into account all components.

EQUATION 102:

$$V_{ripple} = I_{ripple}\left(ESR + \frac{D_{max}}{F_{PWM}C} + \frac{ESL \cdot F_{PWM}}{D_{max}}\right)$$

Neglecting ESL, since it is normally very small (at least for PWM frequencies less than 400 kHz), results in Equation 103.

EQUATION 103:

$$C_O = \frac{I_{O,\,ripple}D_{max}}{F_{PWM}(V_{OUT,\,ripple} - I_{O,\,ripple}ESR)}$$

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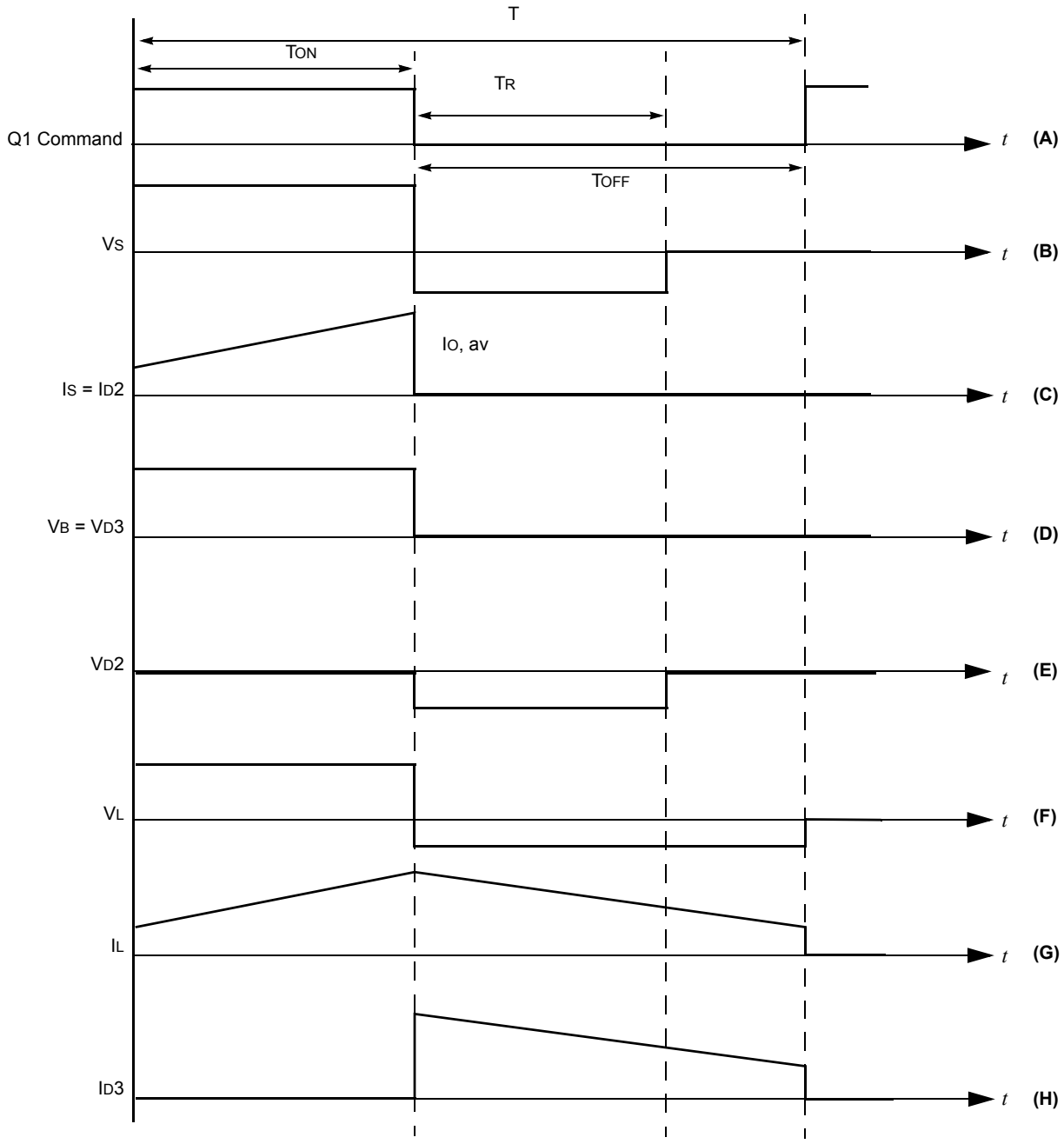
FIGURE 24: FORWARD CONVERTER WAVEFORMS: SECONDARY SIDE

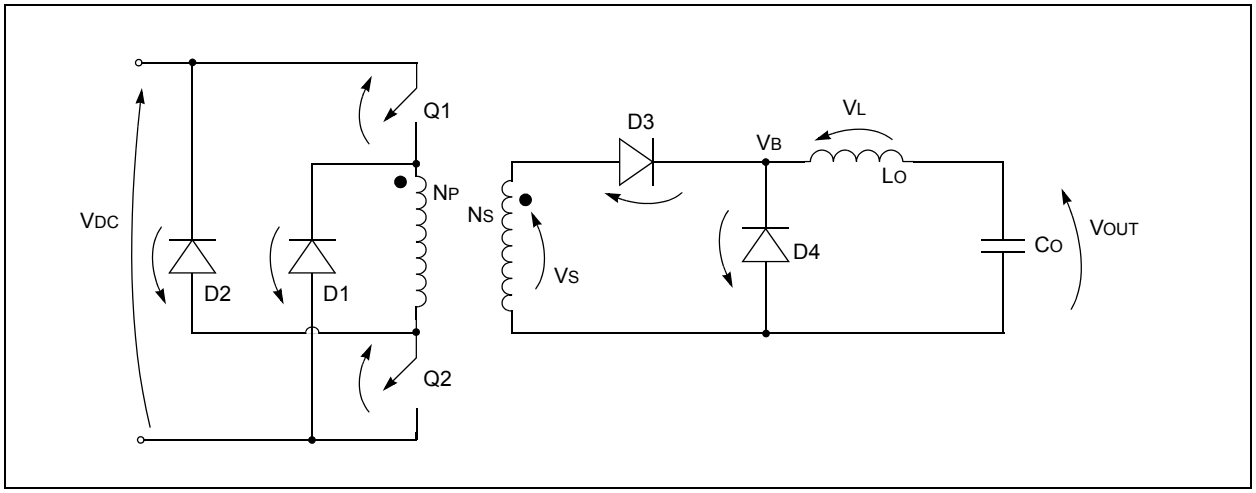


(A) = Command signal on Q1 MOSFET gate
(B) = Voltage VS on secondary winding NS
(C) = Secondary winding current, equal to diode D2 current
(D) = Voltage at node B
(E) = Voltage on diode D2
(F) = Voltage on LO inductor
(G) = Current in LO inductor
(H) = Current in diode D3

TWO-SWITCH FORWARD CONVERTER

Clearly derived from the single-ended topology (Forward Converter), this circuit has significant advantages over single-ended forward converters. A schematic of this topology is shown in Figure 25.

FIGURE 25: TWO-SWITCH FORWARD CONVERTER TOPOLOGY

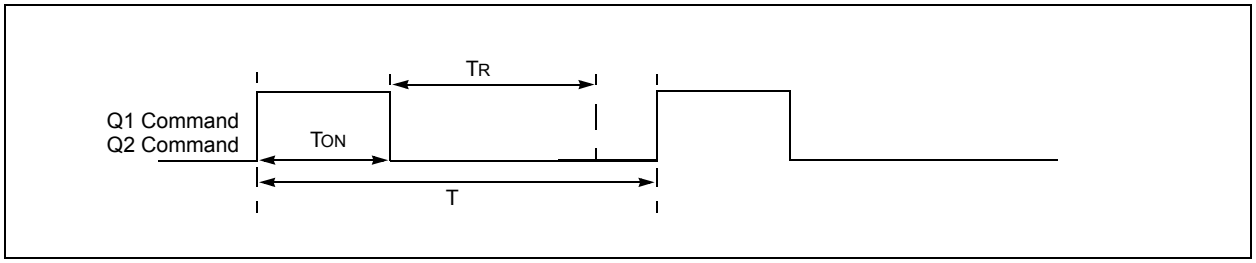


Topology Equations

Referring to the section on Two-Switch Forward Converters in AN1114 (see **"Introduction"**), the basic equations are reviewed first followed by the selection of circuit components.

Both switches, Q1 and Q2, are simultaneously driven by a square wave signal with a duty cycle less than 0.5, as shown in Figure 26.

FIGURE 26: SIGNAL DRIVING SWITCHES Q1 AND Q2



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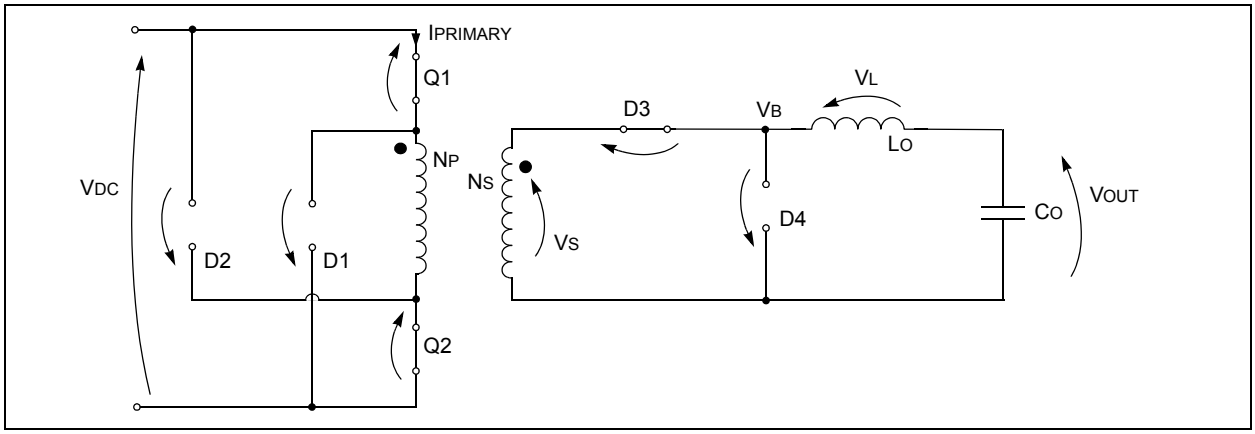
Q1 ON, Q2 ON (INTERVAL 0 - TON)

In this configuration, the circuit is redrawn, as shown in Figure 27.

FIGURE 27: TWO-SWITCH FORWARD CONVERTER TOPOLOGY: INTERVAL 0 - TON



Input Circuit Behavior

The transformer is connected between VDC and ground; the dot end is more positive than the non-dot end and the magnetizing current is flowing through it. Both diodes at the primary are reverse-biased and do not contribute to the operation.

The voltage on the primary is equal to Equation 104.

EQUATION 104:

$$V_P = V_{DC} - 2V_{Q,on}$$

The magnetizing current in the transformer has a positive slope increase as shown in Figure 30(C):

EQUATION 105:

$$I_M(t) = \frac{(V_{DC} - 2V_{Q,on})}{L_M} t$$

The total current in the primary is this magnetizing current plus the secondary current reflected by the transformer back to the primary.

Output Circuit Behavior

Similar to the primary, the secondary winding experiences a voltage that is higher at the dot end compared to the non-dot end. Therefore, diode D3 is forward-biased and conducting the current to the inductor, while diode D4 is reversed-biased.

The secondary voltage is equal to Equation 106.

EQUATION 106:

$$V_S = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on})$$

Equation 107 shows the voltage on the inductor.

EQUATION 107:

$$V_L = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D,on} - V_{OUT}$$

As shown in Equation 108, the current in the inductor has a linearly growing behavior (see also Figure 31(E)).

EQUATION 108:

$$I_L(t) = I_L(0) + \frac{\frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D,on} - V_{OUT}}{L_O} t$$

At this point, the total current in the primary windings can be computed as the sum of the magnetizing current and the secondary current reflected back into the primary (see Figure 30(F)), as shown in Equation 109.

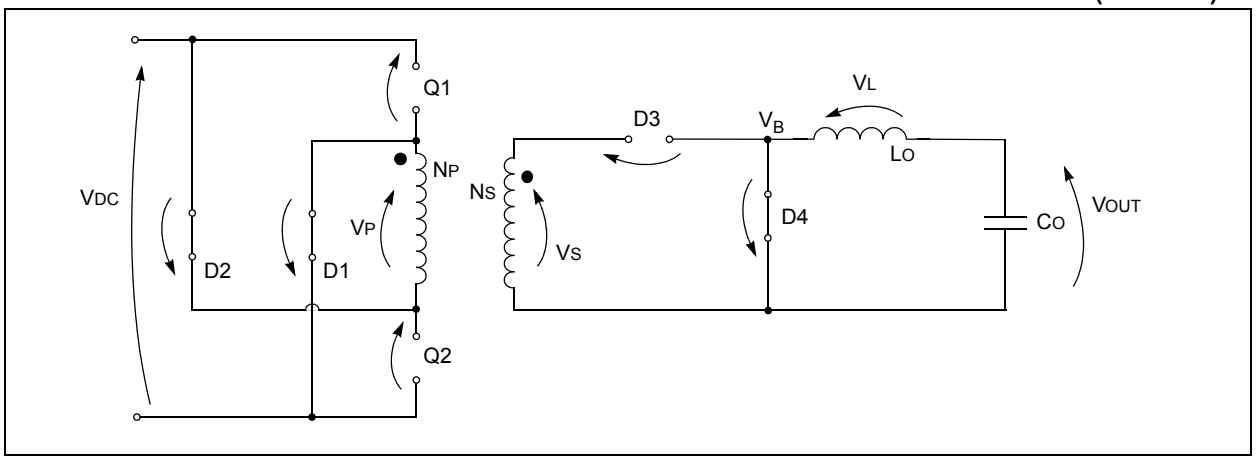
EQUATION 109:

$$I_{P,total}(t) = I_L(0) + \frac{(V_{DC} - 2V_{Q,on})}{L_M} + \frac{N_S}{N_P}\frac{\frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D,on} - V_{OUT}}{L_O} t$$

Q1 OFF Q2 OFF
(INTERVAL TON TO (TON + TR))

When both switches turn off, the magnetizing current in NP reverses all the voltages in the system. At the primary, the non-dot end part of the inductor becomes more positive than the dot end (see Figure 28). Both diodes are forward-biased, which provides a path for the leakage current, from the non-dot end of the primary, through D2 into the positive of VDC out of its negative wire, through diode D1, and back again to the transformer.

FIGURE 28: TWO-SWITCH FORWARD CONVERTER TOPOLOGY: INTERVAL TON - (TON + TR)



The voltage on the primary is equal to Equation 110.

EQUATION 110:

$$V_{P,off} = -(V_{DC} + 2V_{D,on})$$

The magnetizing current can be expressed as Equation 111.

EQUATION 111:

$$I_M(t) = \frac{-(V_{DC} + 2V_{D,on})}{L_M}t$$

The magnetizing current reaches zero (that is, all the energy stored into the transformer primary during TON has been delivered back to the VDC input) at time TON + TR, being (TON + TR) < T.

Output Circuit Behavior

Because of the change in polarity of the voltages due to the magnetizing current, the polarity of the induced secondary voltage is such that the non-dot end of the winding is more positive than the dot end. In the meanwhile, the voltage on the output inductor changes polarity as well, and its left side tries to go very negative, but is clamped to a diode voltage drop below ground by diode D4, which is forward-biased. D3 on the contrary becomes reverse-biased. The inductor current has its path through diode D4 and into the load and the output capacitor.

Equation 112 shows the secondary voltage.

EQUATION 112:

$$V_S = -\frac{N_S}{N_P}(V_{DC} + 2V_{D,on})$$

Equation 113 shows the inductor voltage.

EQUATION 113:

$$V_L = -V_{OUT} - V_{D,on}$$

Equation 114 shows the current.

EQUATION 114:

$$I_L(t) = \frac{-(V_{OUT} + V_{D,on})}{L_O}t$$

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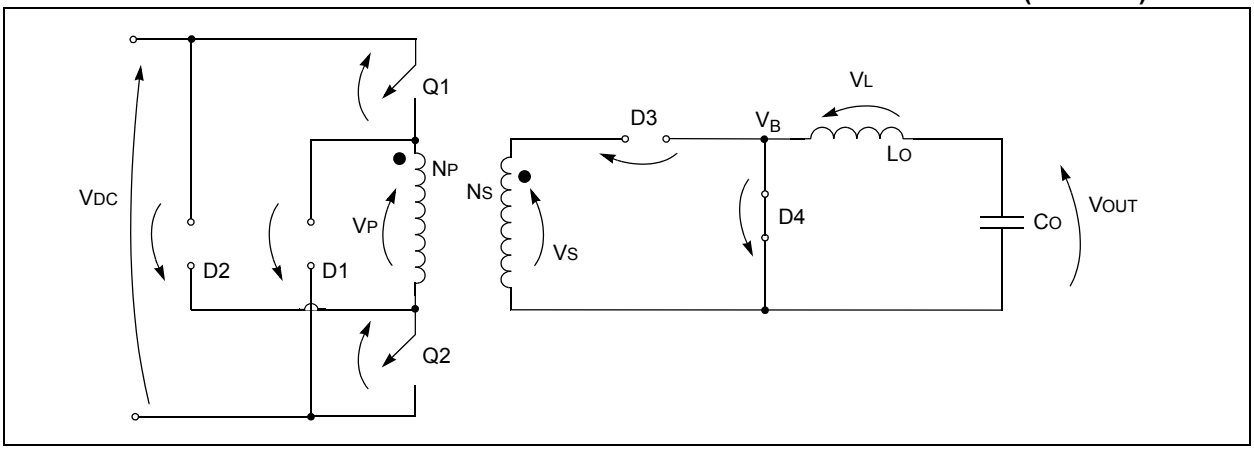
Q1 OFF Q2 OFF (INTERVAL (TON + TR) TO T)

As seen previously from (TON + TR) to T, there is no more energy in the transformer primary, the magnetizing current is zero and consequently the two diodes D1 and D2 are not conducting any more, as they are reverse-biased.

In this configuration, the circuit is redrawn as shown in Figure 29. Voltage VP and VS are both zero and voltage on the switch will be less than VDC. Nothing changes at the secondary.

FIGURE 29: TWO-SWITCH FORWARD CONVERTER TOPOLOGY: INTERVAL (TON + TR) - T



Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

The input/output relationship is shown in Equation 115, and is obtained by equating Equation 108 with Equation 114, where t = TON and t = TOFF, respectively.

EQUATION 115:

$$V_{OUT} = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on})D - V_{D,on}$$

Neglecting VD and VQ, the duty cycle can be determined, as shown in Equation 116.

EQUATION 116:

$$V_{OUT} = \frac{N_S}{N_P}V_{DC}D$$

The maximum theoretical duty cycle (Equation 117) can be obtained equating the two magnetizing currents (Equation 105 and Equation 111), considering that TR can be at maximum TR = TOFF.

EQUATION 117:

$$D_{max,\,theoretical} = 0.5$$

Of course the real duty cycle will be somewhat smaller than the maximum, theoretical value, to take into account tolerances in the computations.

TRANSFORMER: PRIMARY

The number of primary turns is determined from the Faraday equation shown in Equation 118, which results in Equation 119.

EQUATION 118:

$$\Delta B = \frac{V_P T_{ON}}{N_P A_{core}}$$

EQUATION 119:

$$N_P = \frac{(V_{DC,min} - 2V_{Q,on})D_{max}}{F_{PWM}A_{core}\Delta B}$$

TRANSFORMER: PRIMARY, WIRE SIZE

The current flowing through the transformer can be computed replacing the current in Figure 30(F), with an equivalent waveform having a constant amplitude ($I_{P, mr}$), corresponding to the mid-ramp value.

Considering the relationship of Equation 120 (between the input power) and Equation 121 (the output power), this results in Equation 122. Therefore, the rms value is then equal to Equation 123.

EQUATION 120:

$$P_O = \eta P_I$$

EQUATION 121:

$$P_I = V_{DC, min} I_{P, mr} D_{max}$$

EQUATION 122:

$$I_{P, mr} = \frac{P_O}{\eta V_{DC, min} D_{max}}$$

EQUATION 123:

$$I_{P, rms} = I_{P, mr} \sqrt{D_{max}}$$

TRANSFORMER: SECONDARY

The number of turns are determined by Equation 115 and Equation 119 and results in Equation 124.

EQUATION 124:

$$N_S = \frac{V_{OUT}}{F_{PWM} A_{core} \Delta B}$$

TRANSFORMER: SECONDARY, WIRE SIZE

By referring to Figure 31(C), the current flowing into the secondary winding can be determined, and the ramp on a step current waveform can be approximated with a constant amplitude signal, being the amplitude $I_{O, av, nom}$. Based on these, the corresponding rms value is equal to Equation 125.

EQUATION 125:

$$I_{SECONDARY, rms} = I_{O, ar, nom} \sqrt{D_{max}}$$

MOSFET

The maximum voltage the switches must be able to withstand during T_{OFF}, is shown in Equation 126.

EQUATION 126:

$$V_{Q, max} \approx V_{DC, max}$$

The maximum current during T_{ON} is shown in Equation 127, which is the same current flowing into the transformer.

EQUATION 127:

$$I_{P, mr} = \frac{P_O}{\eta V_{DC, min} D_{max}}$$

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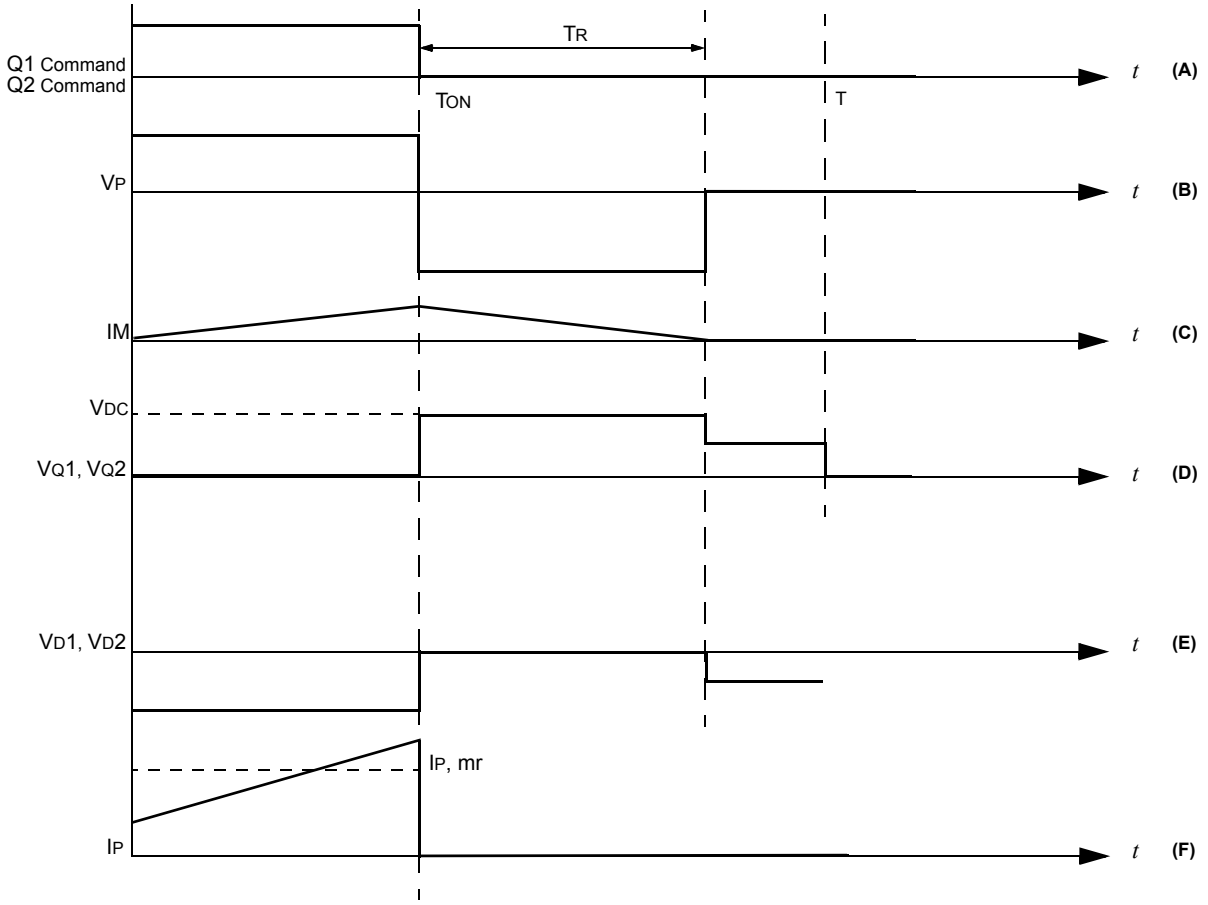
FIGURE 30: TWO-SWITCH FORWARD CONVERTER WAVEFORMS: PRIMARY SIDE



(A) = Command signal on Q1 and Q2 MOSFET gates

(B) = Voltage V_P on primary winding N_P

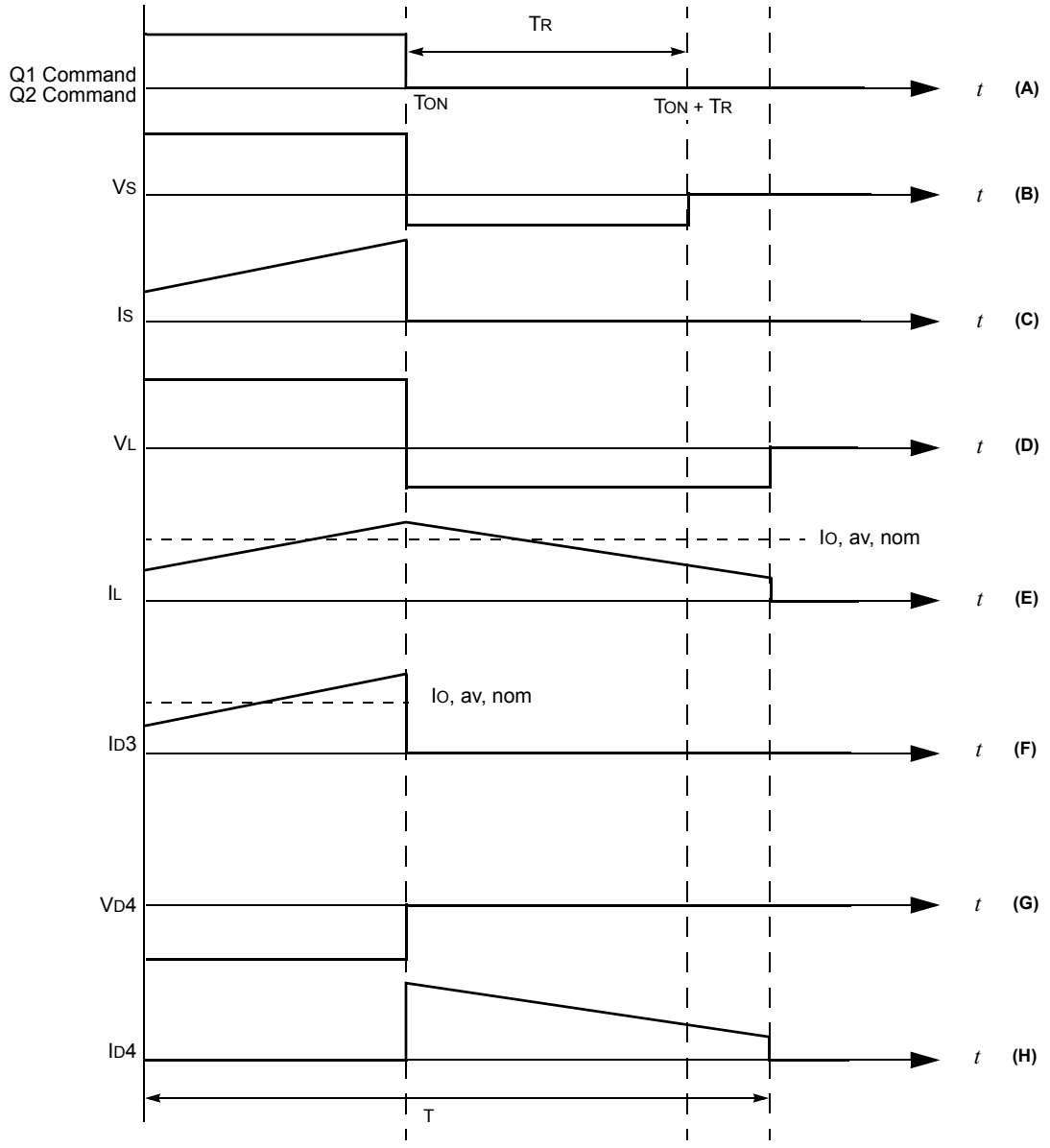
(C) = Magnetizing current I_M

(D) = Voltage on Q1 and Q2 MOSFETS

(E) = Voltage on diodes D1 and D2

(F) = Total primary current I_P (magnetizing current and load current reflected back to the primary side of the transformer)

FIGURE 31: TWO-SWITCH FORWARD CONVERTER WAVEFORMS: SECONDARY SIDE



(A) = Command signal on Q1 and Q2 MOSFET gates

(B) = Voltage V_S on secondary winding N_S

(C) = Current flowing into the secondary winding N_S

(D) = Voltage on inductor L_O

(E) = Current in inductor L_O

(F) = Current flowing in diode D3

(G) = Voltage on diode D4

(H) = Current in diode D4

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DIODES

Table 2 provides calculations for determining diode voltage.

TABLE 2: DIODE VOLTAGE

Diode	Configuration		
	0 - TON	**TON -> (TON + TR)**	**(TON + TR) -> T**
D1	$V_R = -V_{DC,max} + V_{Q,on}$	V_F	$V_R = \frac{-V_{DC,max}}{2}$
D2	$V_R = -V_{DC,max} + V_{Q,on}$	V_F	$V_R = \frac{-V_{DC,max}}{2}$
D3	V_F	$V_R = \frac{N_S}{N_P}(V_{DC,max} + 2V_{D,on}) + V_{D,on}$	$\cong V_F$
D4	$V_R = \frac{N_S}{N_P}(V_{DC,max} - 2V_{Q,on}) + V_{D,on}$	V_F	V_F

Legend: VF is the diode forward voltage.

Table 3 provides calculations for determining average diode current.

TABLE 3: DIODE CURRENT

Diode	Configuration		
	0 - TON	**TON -> (TON + TR)**	**(TON + TR) -> T**
D1	0	$\frac{P_O}{\eta V_{DC,min} D_{max}}$	0
D2	0	$\frac{P_O}{\eta V_{DC,min} D_{max}}$	0
D3	$I_{O,av,nom}$	0	0
D4	0	$I_{O,av,nom}$	$I_{O,av,nom}$

OUTPUT INDUCTANCE

The output inductor is computed so that the output inductor is at the edge of the Discontinuous mode when the output current is the minimum required (IO, av, min).

Using the same approach used for the Forward Converter (see Figure 26 and Equations 99 and 100), from Equation 108 and Equation 128 (neglecting the voltage drops on the MOSFETS and diodes) results in Equation 129.

EQUATION 128:

$$I_{O,\,av,\,min} = \frac{I_{O,\,ripple}}{2}$$

EQUATION 129:

$$L_O = \frac{\left(\frac{N_S}{N_P}V_{DC,\,min} - V_O\right)D_{max}}{2F_{PWM}I_{O,\,av,\,min}}$$

OUTPUT CAPACITANCE

The capacitance should present the lowest possible impedance at the frequency of the current ripple, to achieve the lowest output voltage ripple.

The voltage ripple is determined by the ESR of the output capacitor and by the voltage drop on CO due to the current flowing through it (see Equation 130).

EQUATION 130:

$$V_{OUT,\,ripple} = ESR \cdot I_{O,\,ripple} + \frac{1}{C_O}I_{O,\,ripple}\frac{D}{F_{PWM}}$$

The output capacitor value can be determined from Equation 131.

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HALF-BRIDGE CONVERTER

Design Equations

Figure 32 presents the schematic of a Half-Bridge Converter. Please refer to the section on Half-Bridge Converters in AN1114 (see **"Introduction"**) for a detailed description of the operation of the system.

The waveforms (two pulses, with adjustable width and a 180° phase delay) used to drive the gates of the two Q transistors are represented in Figure 33. Some margin is needed after the falling edge of one pulse before the rising edge of the other. These time intervals are called T_R. If not implemented, a short circuit exists and the switches will be destroyed by the very high current flowing through the path from V_{DC} to ground. Initially, C_B is replaced with a short circuit.

FIGURE 32: HALF-BRIDGE CONVERTER TOPOLOGY

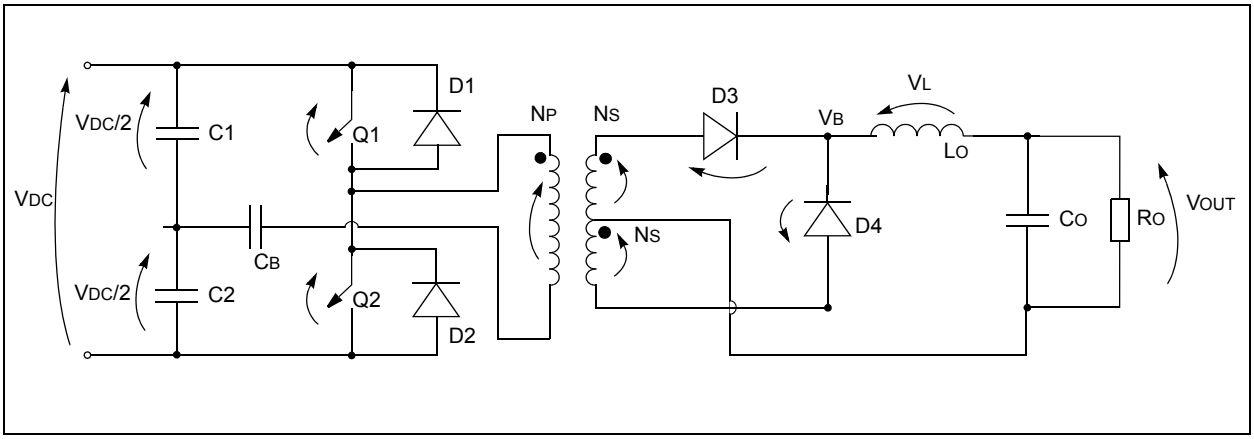
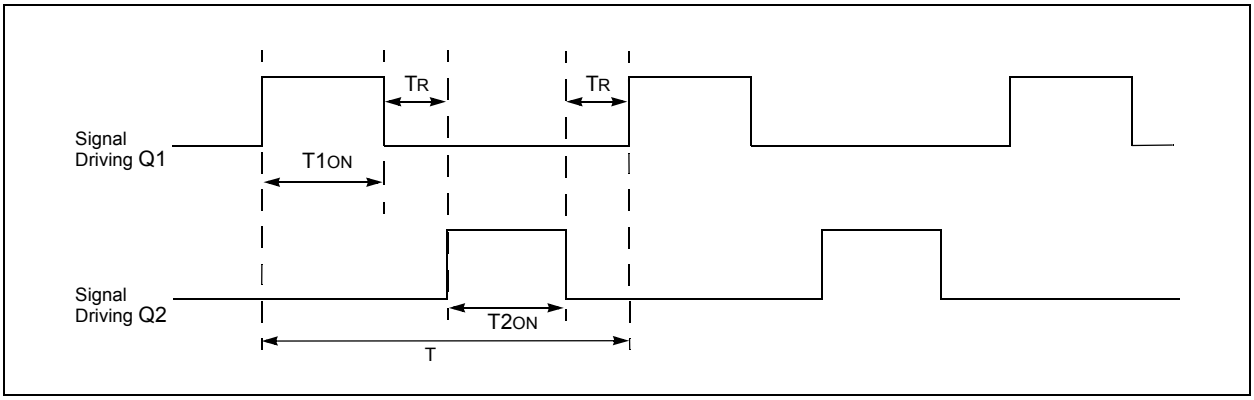


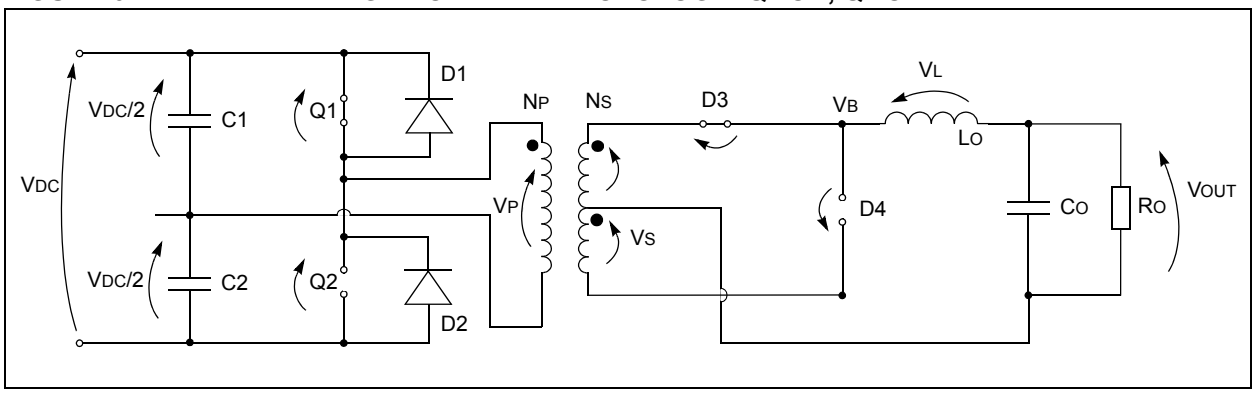
FIGURE 33: Q1 AND Q2 COMMAND SIGNALS



Q1 ON, Q2 OFF

In this configuration, the circuit is redrawn as shown in Figure 34.

FIGURE 34: HALF-BRIDGE CONVERTER TOPOLOGY: Q1 ON, Q2 OFF



Input Circuit Behavior

The voltage on capacitor C1 develops a voltage on the primary circuit where the dot end is more positive than the non-dot end.

Equation 132 shows the voltage at the primary.

EQUATION 132:

$$V_P = \left(\frac{V_{DC}}{2} - V_{Q1,on}\right)$$

Equation 133 shows the magnetizing current.

EQUATION 133:

$$I_M(t) = \frac{\frac{V_{DC}}{2} V_{Q1,on}}{L_M} t$$

Output Circuit Behavior

Because of the voltage polarity on the primary, the dot-end edge of the secondary is more positive than the non-dot end. Diode D4 is then reverse-biased and D3 is forward-biased.

Equation 134 shows the voltage at the secondary.

EQUATION 134:

$$V_S = \frac{N_S}{N_P}\left(\frac{V_{DC}}{2} - V_{Q1,on}\right)$$

Equation 135 shows the voltage on the inductor.

EQUATION 135:

$$V_L = \frac{N_S}{N_P}\left(\frac{V_{DC}}{2} - V_{Q1,on}\right) - V_{D3,on} - V_{OUT} > 0$$

Equation 137 shows the current.

EQUATION 136:

$$I_L(t) = I_L(0) + \frac{\frac{N_S}{N_P}\left(\frac{V_{DC}}{2} - V_{Q1,on}\right) - V_{D3,on} - V_{OUT}}{L_O} t$$

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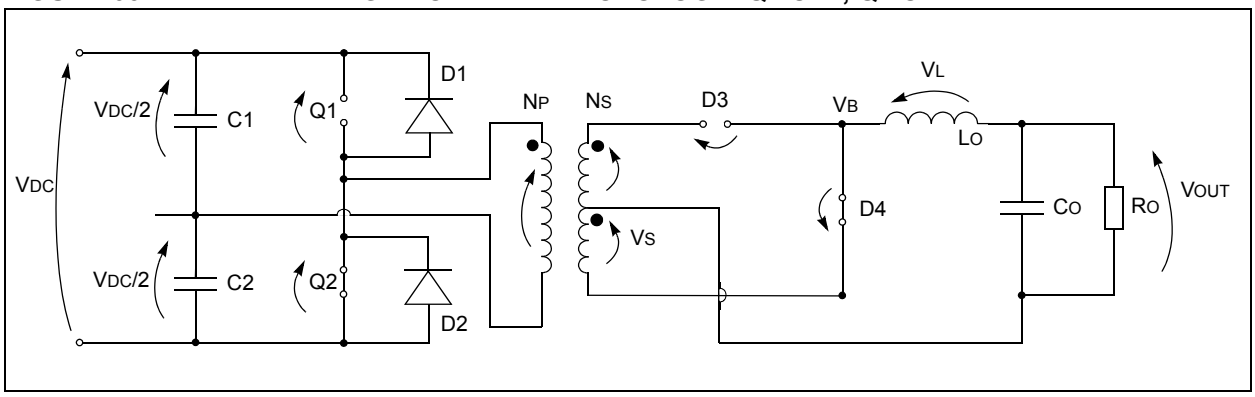
Q1 OFF, Q2 ON

In this configuration, the circuit is redrawn as shown in Figure 35.

FIGURE 35: HALF-BRIDGE CONVERTER TOPOLOGY: Q1 OFF, Q2 ON



Input Circuit Behavior

In this instance, the dot end of the primary winding has a voltage that is more negative than the non-dot end.

Equation 137 shows the primary winding voltage.

EQUATION 137:

$$V_P = -\frac{V_{DC}}{2} + V_{Q,on}$$

Equation 138 shows the magnetizing current.

EQUATION 138:

$$I_M(t) = \frac{-\frac{V_{DC}}{2} + V_{Q,on}}{L_M} t$$

Output Circuit Behavior

As with the primary, the dot end of the secondary winding has a voltage more negative than the non-dot end. As a consequence, D3 in open and D4 is forward-biased.

Equation 139 shows the secondary voltage.

EQUATION 139:

$$V_S = \frac{N_S}{N_P}\left(-\frac{V_{DC}}{2} + V_{Q,on}\right)$$

Equation 140 shows the inductor voltage.

EQUATION 140:

$$V_L = \frac{N_S}{N_P}\left(\frac{V_{DC}}{2} - V_{Q,on}\right) - V_{D,on} - V_{OUT}$$

Equation 141 shows the current.

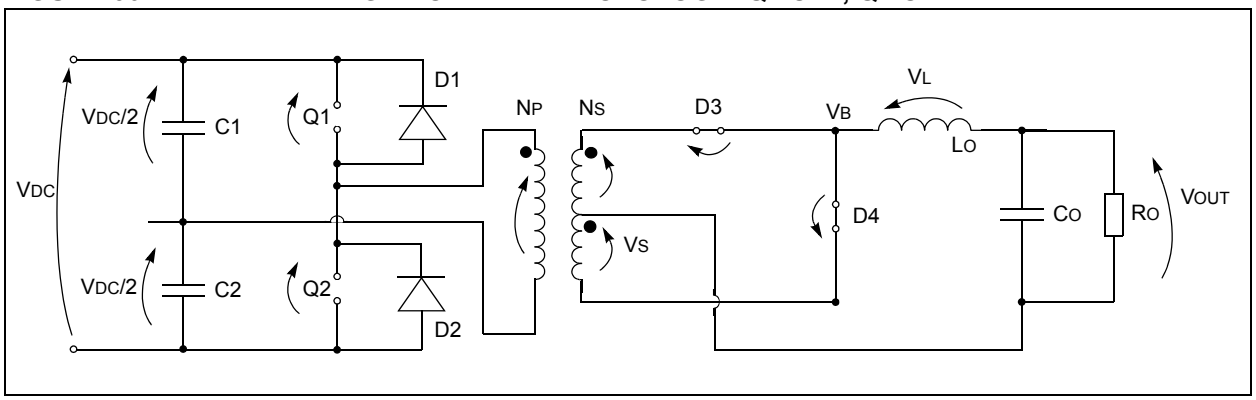
EQUATION 141:

$$I_L(t) = I_L(T_{ON}) + \frac{\frac{N_S}{N_P}\left(\frac{V_{DC}}{2} - V_{Q,on}\right) - V_{D,on} - V_{OUT}}{L_O} t$$

Q1 OFF, Q2 OFF (PERIOD TR)

In this configuration, the circuit is redrawn as shown in Figure 36.

FIGURE 36: HALF-BRIDGE CONVERTER TOPOLOGY: Q1 OFF, Q2 OFF



Input Circuit Behavior

In this instance, the current path in the primary side when Q1 turns off (Figure 37) and when Q2 turns off (Figure 38).

FIGURE 37: HALF-BRIDGE CONVERTER: CURRENT PATH IN THE PRIMARY SIDE WHEN Q1 TURNS OFF

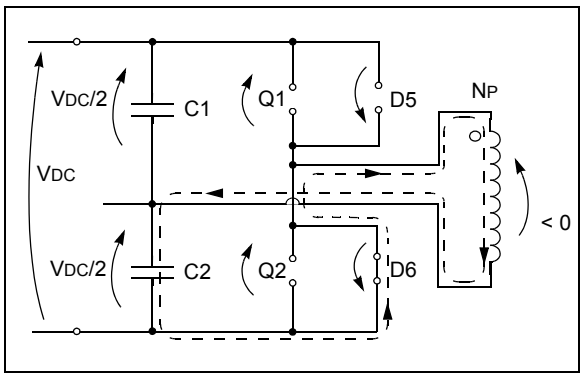
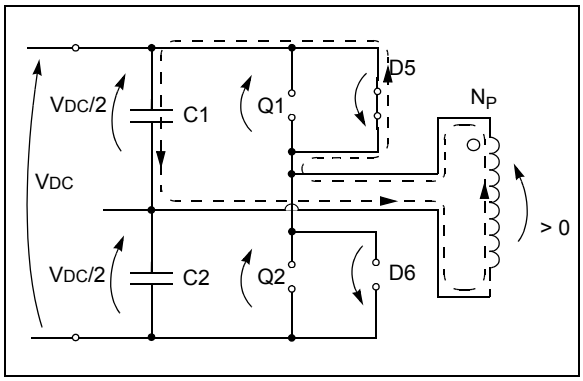


FIGURE 38: HALF-BRIDGE CONVERTER: CURRENT PATH IN THE PRIMARY SIDE WHEN Q2 TURNS OFF



Output Circuit Behavior

When both switches are off, the voltage on the two secondary windings are such that both D1 and D2 are forward-biased and are conducting. The current is split equally between them, so that each of them is conducing one half of the current flowing into the inductor. The resulting current waveforms are shown in Figure 40.

Equation 142 shows the inductor voltage.

EQUATION 142:

$$V_L = -V_{OUT}$$

Equation 143 shows the current flowing through it.

EQUATION 143:

$$I_L(t) = \frac{-V_{OUT}}{L_O} t$$

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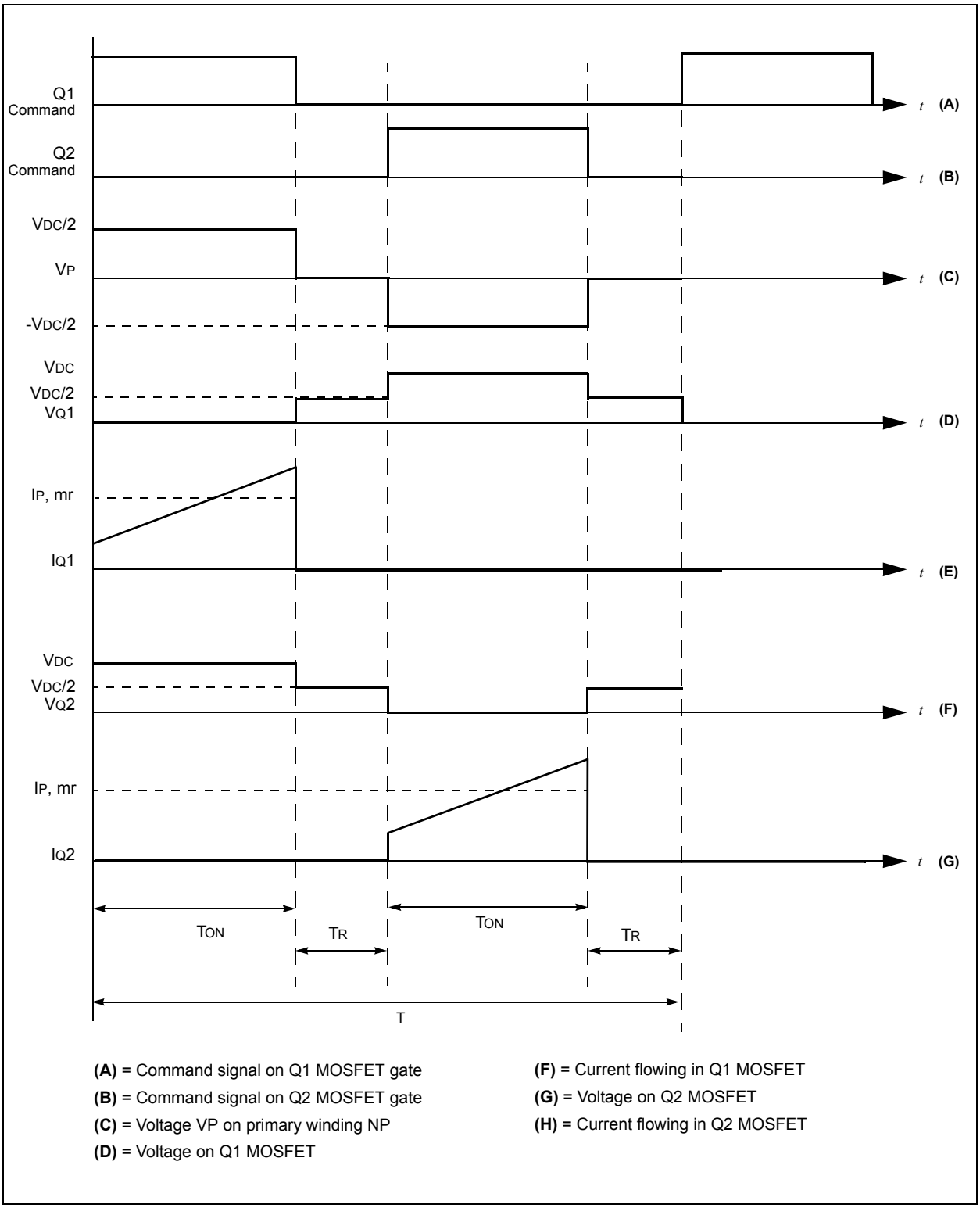
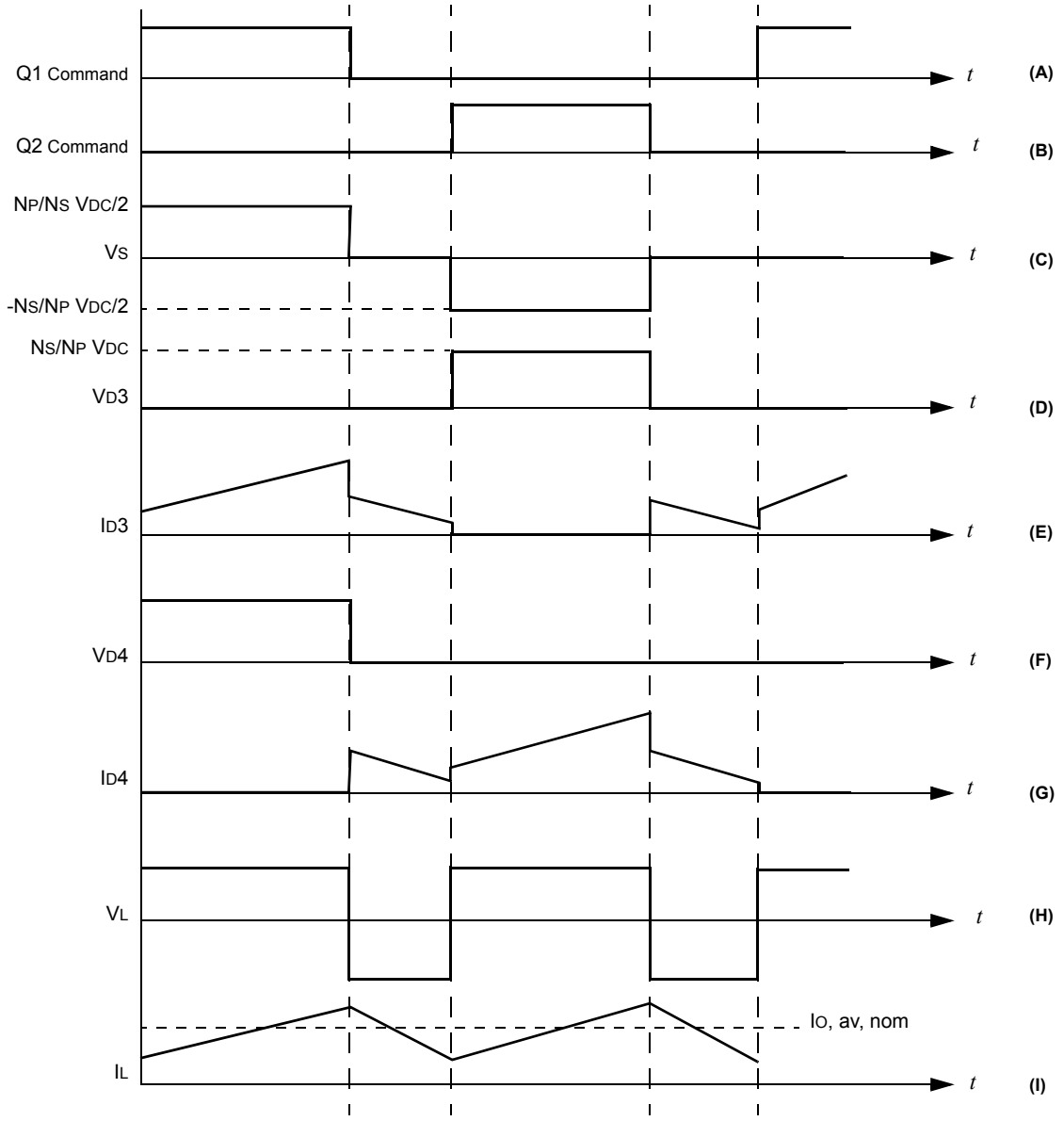
FIGURE 39: HALF-BRIDGE CONVERTER WAVEFORMS: PRIMARY SIDE



(A) = Command signal on Q1 MOSFET gate
(B) = Command signal on Q2 MOSFET gate
(C) = Voltage VP on primary winding NP
(D) = Voltage on Q1 MOSFET
(F) = Current flowing in Q1 MOSFET
(G) = Voltage on Q2 MOSFET
(H) = Current flowing in Q2 MOSFET

FIGURE 40: HALF-BRIDGE CONVERTER WAVEFORMS: SECONDARY SIDE



(A) = Command signal on Q1 MOSFET gate
(B) = Command signal on Q2 MOSFET gate
(C) = Voltage V_S on secondary winding NS
(D) = Voltage on diode D3
(E) = Current flowing in diode D3
(F) = Voltage on diode D4
(G) = Current flowing in diode D4
(H) = Voltage on inductor LO
(I) = Current in inductor LO

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Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

At the Steady state, the increase in inductor current during TON must equal its decrease during TR (neglecting the forward drop on the diode), as shown in Equation 144.

EQUATION 144:

$$V_{OUT} = \frac{N_S}{N_P} V_{DC} D$$

where $D = \frac{T_{ON}}{T}$, and $(T_{ON} + T_R) = \frac{T}{2}$

Consequently, knowing that there are two pulses in the PWM period, the maximum theoretical duty cycle is Dmax, theoretical = 0.5. Of course, to avoid the shoot-through in the two switches, the maximum duty cycle corresponding to the minimum input voltage, will be less.

TRANSFORMER: PRIMARY

As soon as the transformer core has been defined, the primary turns number can be computed from Faraday's law as shown in Equation 145, resulting in Equation 146.

EQUATION 145:

$$\Delta B = \frac{V_P T_{ON}}{N_P A_{core}}$$

EQUATION 146:

$$N_P = \frac{V_{DC,min} D_{max}}{2 F_{PWM} A_{core} \Delta B}$$

TRANSFORMER: PRIMARY, WIRE SIZE

Current flowing in the primary windings is plotted in Figure 39(E and G). It is the sum of the magnetizing current flowing into the primary windings and the secondary load current reflected back by the transformer turn ratio.

To make computations simpler, the real current waveforms can be replaced with the mid-ramp value (IP, mr) and determine its value considering the input (PI) and output (PO) power.

Equation 147 shows the input power.

EQUATION 147:

$$P_I = \frac{V_{DC}}{2} I_{P,mr} 2D$$

Equation 148 shows the output power.

EQUATION 148:

$$P_O = \eta P_I$$

where η is the efficiency

Operating on these two equations results in Equation 149.

EQUATION 149:

$$I_{P,mr} = \frac{P_O}{\eta V_{DC,min} D_{max}}$$

Equation 150 shows the rms value.

EQUATION 150:

$$I_{P,rms} = I_{P,mr} \sqrt{D_{max}}$$

TRANSFORMER: SECONDARY, NUMBER OF TURNS, WIRE SIZE

The secondary turns number shown in Equation 151, can be obtained from Equation 144 and Equation 146.

EQUATION 151:

$$N_S = \frac{V_{OUT}}{2 F_{PWM} A_{core} \Delta B}$$

The average output current, shown as IO, av, nom in Figure 40(I), is the average output current the converter is designed for. The rms secondary current (IS) results in Equation 152.

EQUATION 152:

$$I_{S,rms} = I_{O,av,nom} \sqrt{D_{max}}$$

SWITCHES

Referring to section on Half-Bridge Converters in AN1114 (see **"Introduction"**), one of the main advantages of the Half-Bridge Converter topology is that the switches must withstand a maximum voltage that is V_{DC}, compared to 2 V_{DC} as in push-pull topologies. During T_{ON} and T_R, the Q1 and Q2 switches are subject to a maximum voltage of V_Q, max = V_{DC}, max.

The maximum current flowing through the switches has already been computed in Equation 150.

OUTPUT INDUCTANCE

The inductor is selected in such a way as to prevent the output inductor current from becoming discontinuous.

The computations are performed at the edge between continuous and discontinuous operation, when the output starts from zero at the beginning of the T_{ON} period and goes back to zero at the end of the T_R period. In other words, the inductor current peak (which is also the current ripple, D_I) is twice the output average current (see Equation 153).

EQUATION 153:

$$I_{O,ripple} = 2I_{O,a(v,min)} = \frac{\frac{N_S}{N_P}\frac{V_{DC,min}}{2} - V_{OUT}}{L_O} T_{ON}$$

Equation 154 shows the results.

EQUATION 154:

$$L_O = \frac{\frac{N_S}{N_P}\frac{V_{DC,min}}{2} - V_{OUT}}{2F_{PWM}I_{O,av,min}} D_{max}$$

OUTPUT CAPACITOR

The output voltage ripple is mainly due to the ESR, which results in Equation 155.

EQUATION 155:

$$V_{OUT,ripple} = ESR \cdot I_{O,ripple} + \frac{1}{C_O} I_{O,ripple} \frac{D}{F_{PWM}}$$

As previously seen in other topologies, the output capacitor value can be determined from the relation shown in Equation 156.

EQUATION 156:

$$C_O = \frac{I_{O,ripple} D_{max}}{F_{PWM}(V_{OUT,ripple} - I_{O,ripple} ESR)}$$

CAPACITOR C_B

Capacitor C_B (see Figure 32) is used to block the DC component of the current flowing into the transformer to avoid core saturation. Small differences between C1 and C2 create an unbalance of the voltage at the point between them and causes the core to walk along the hysteresis loop onto saturation.

The presence of the small capacitor causes a droop in the primary voltage. The voltage during T_{ON} will decay almost linearly with time.

Assuming ΔV_D is the maximum acceptable droop voltage, which results in Equation 157.

EQUATION 157:

$$C_B > \frac{I_{P,mr}}{\Delta V_D} T_{ON}$$

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PUSH-PULL CONVERTER

The Push-Pull Converter uses a transformer to isolate the input from the output circuit.

Topology Equations

Figure 41 shows the schematic of a Push-Pull Converter. Refer to AN1114 (see **"Introduction"**) for a detailed description of the system operation.

The waveforms (two pulses, with adjustable width and with a 180° phase delay) used to drive the gates of the two Q transistors are shown in Figure 42. T is the period of the waveform, with two pulses in T, one on Q1 and the second one on Q2. This means that the duty cycle must be less than 0.5 to prevent overlap of the two pulses. Some margin is needed after the falling edge of one pulse before the rising edge of the other. These time intervals are called TR.

FIGURE 41: PUSH-PULL CONVERTER TOPOLOGY

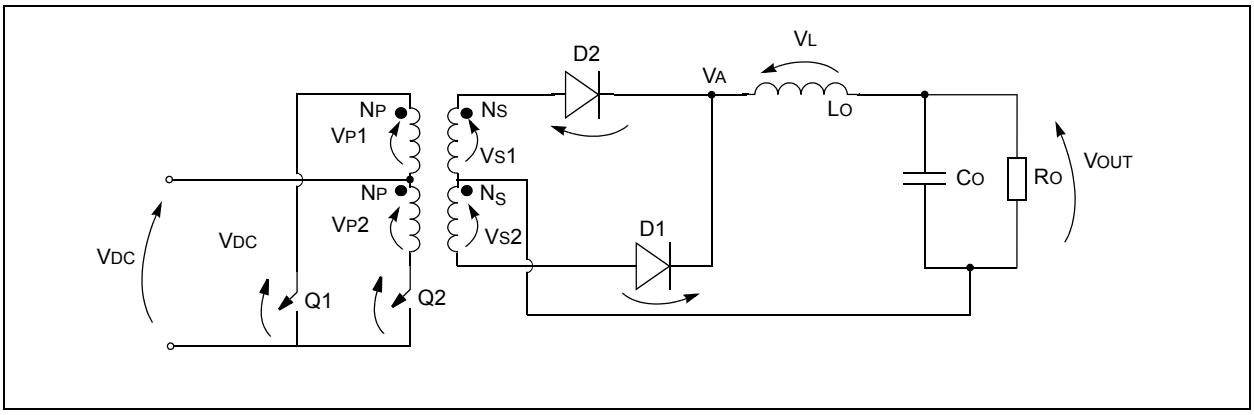
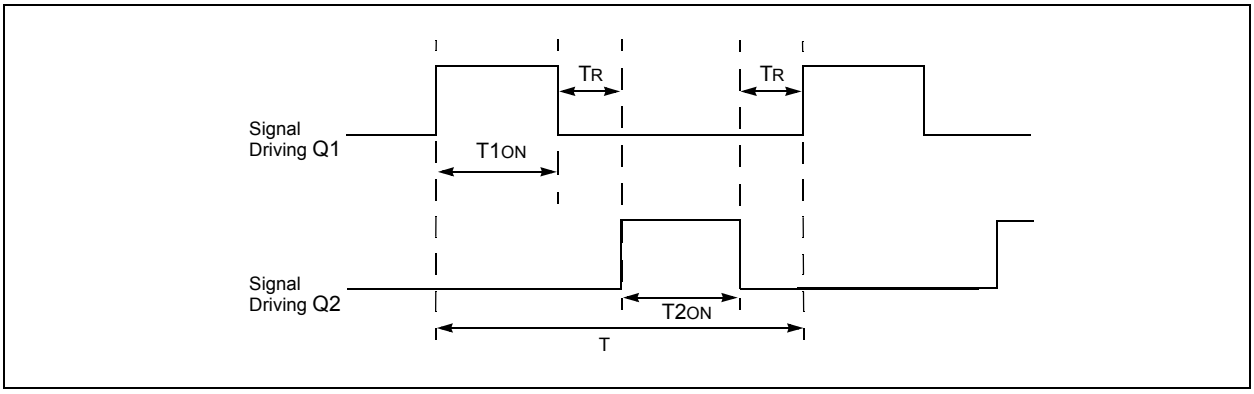


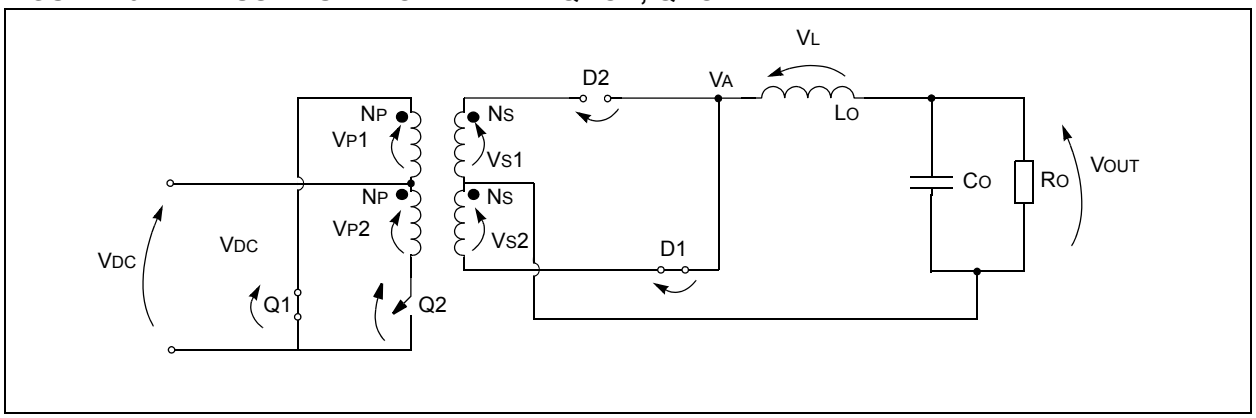
FIGURE 42: SIGNALS DRIVING Q1 AND Q2 MOSFET GATES



Q1 ON, Q2 OFF

In this configuration, the circuit is redrawn as shown in Figure 43.

FIGURE 43: PUSH-PULL CONVERTER: Q1 ON, Q2 OFF



Input Circuit Behavior

The input voltage V_{DC} gives place to a voltage on the primary winding where the non-dot ends are more positive than the dot-ends.

Equation 158 shows the voltage at the primary.

EQUATION 158:

$$V_P = -(V_{DC} - V_{Q1,on})$$

This same voltage is present on the lower primary winding (supposing $N_{P1} = N_{P2}$), so that the total voltage on Q2 switch is equal to Equation 159.

EQUATION 159:

$$V_{Q2,off} = 2V_{DC} - V_{Q1,on}$$

Equation 160 shows the magnetizing current.

EQUATION 160:

$$I_M(t) = \frac{-V_{DC} + V_{Q,on}}{L_M}t$$

Output Circuit Behavior

Because of the voltage polarity on the primary, the dot ends of the secondary is more negative that the non-dot end. Diode D2 is then reverse-biased and D1 is forward-biased.

Equation 161 shows the voltage at the secondary.

EQUATION 161:

$$V_S = -\frac{N_S}{N_P}(V_{DC} - V_{Q1,on})$$

Equation 162 shows the voltage on the inductor.

EQUATION 162:

$$V_L = \frac{N_S}{N_P}(V_{DC} - V_{Q1,on}) - V_{D1,on} - V_{OUT} > 0$$

Equation 163 shows the current.

EQUATION 163:

$$I_L(t) = I_L(0) + \frac{\frac{N_S}{N_P}(V_{DC} - V_{Q1,on}) - V_{D1,on} - V_{OUT}}{L_O}t$$

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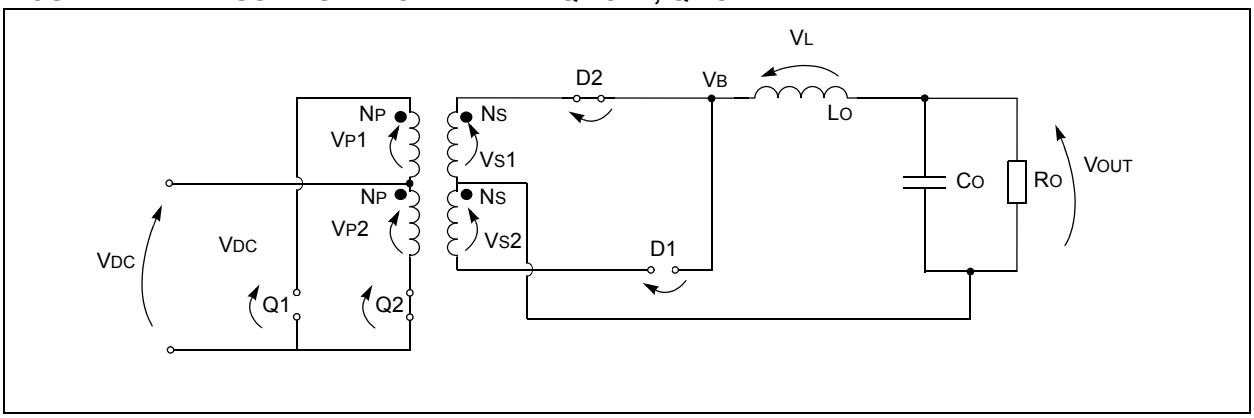
Q1 OFF, Q2 ON

In this configuration, the circuit is redrawn as shown in Figure 44.

FIGURE 44: PUSH-PULL CONVERTER: Q1 OFF, Q2 ON



Input Circuit Behavior

In this instance, the dot end of the primary windings has a voltage more positive than the non-dot end.

Equation 164 shows the primary winding voltage.

EQUATION 164:

$$V_P = V_{DC} - V_{Q2,on}$$

Equation 165 shows the magnetizing current.

EQUATION 165:

$$I_M(t) = \frac{V_{DC} - V_{Q,on}}{L_M} t$$

Output Circuit Behavior

As with the primary, the dot end of the secondary windings has a voltage more positive than the non-dot end. As a consequence, D1 is open and D2 is forward-biased.

Equation 166 shows the secondary voltage.

EQUATION 166:

$$V_S = \frac{N_S}{N_P}(V_{DC} - V_{Q2,on})$$

Equation 167 shows the inductor voltage.

EQUATION 167:

$$V_L = \frac{N_S}{N_P}(V_{DC} - V_{Q2,on}) - V_{D2,on} - V_{OUT} > 0$$

Equation 168 shows the current.

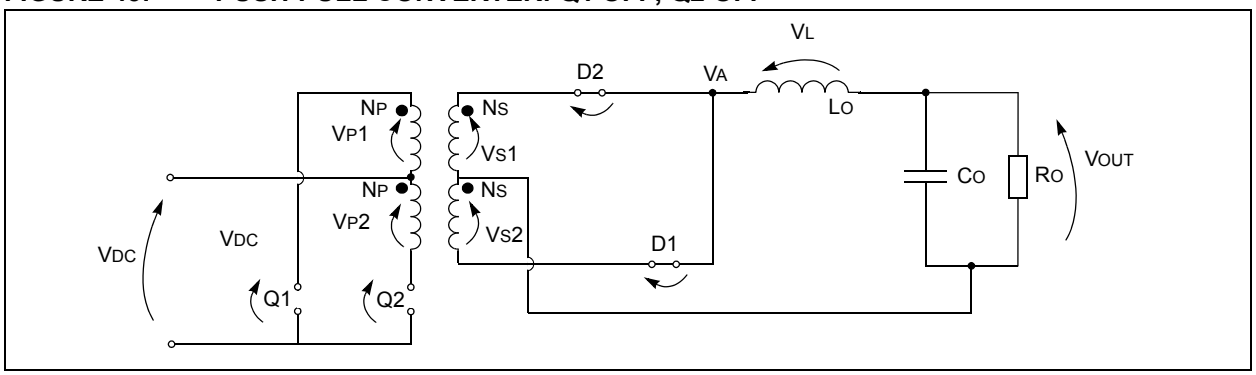
EQUATION 168:

$$I_L(t) = I_L(0) + \frac{\frac{N_S}{N_P}(V_{DC} - V_{Q2,on}) - V_{D2,on} - V_{OUT}}{L_O} t$$

Q1 OFF, Q2 OFF (PERIOD TR)

In this configuration, the circuit is redrawn as shown in Figure 45.

FIGURE 45: PUSH-PULL CONVERTER: Q1 OFF, Q2 OFF



Input Circuit Behavior

Equation 169 shows the voltage on each switch.

EQUATION 169:

$$V_Q = V_{DC}$$

Output Circuit Behavior

When both switches are off, since the current in the inductor continues to flow in the same direction as before, the voltage on the two secondary windings are such that: Vs2 = -Vs1, and D1 and D2 are forward-biased and are conducting. They split the current equally, so that each of them is conducting one half of the current flowing into the inductor. The resulting current waveforms are plotted in Figure 47(G and H) for the two secondary windings currents.

Equation 170 shows the inductor voltage.

EQUATION 170:

$$V_L = -V_{OUT} - V_{D,on} + V_{S1}$$

where V_{SI} is IL times the resistance of the windings (almost zero).

Based on Equation 170, the current flowing through the inductor LO is equal to Equation 171.

EQUATION 171:

$$I_L(t) = I_L(t) + \frac{-V_{OUT} - V_{D,on}}{L_O} t$$

Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

At the Steady state, the increase in inductor current during TON must equal its decrease during TR. Using Equation 168 and Equation 171 (neglecting the forward drop on the diode) and since (TON + TR) = T/2, results in Equation 172.

EQUATION 172:

$$V_{OUT} = 2\frac{N_S}{N_P}(V_{DC} - V_{Q1,on})D$$

where $D = \frac{T_{ON}}{T}$

Consequently, knowing there are two pulses in the PWM period, the maximum theoretical duty cycle can be Dmax = 0.5.

Starting from the input/output relationship shown in Equation 173, the feedback control loop keeps the output voltage VOUT constant against changes in the input voltage VDC, and if VDC decreases, TON will increase to compensate.

EQUATION 173:

$$V_{OUT} = 2\frac{N_S}{N_P}(V_{DC} - V_{Q1,on})\frac{T_{ON}}{T}$$

Therefore, for the system design, a maximum duty cycle (Dmax) can be defined that corresponds to the minimum input voltage (VDC, min) and if less than the maximum, theoretical is equal to Equation 174.

EQUATION 174:

$$D_{max} = \frac{N_P V_{OUT}}{2N_S V_{DC,min}}$$

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TRANSFORMER: PRIMARY, NUMBER OF TURNS

As clearly stated in the Push-Pull Converter section in AN1114 (see **"Introduction"**), the operating point of the core transformer moves between points that are in the first and third quadrant of the hysteresis loop.

Once the maximum allowable ΔB has been defined (based on PWM frequency and geometrical dimensions of the core and bobbins), using the Faraday equation shown in Equation 158 and Equation 175, results in the number of primary turns, as shown in Equation 176.

EQUATION 175:

$$\Delta B = \frac{V_P T_{ON}}{N_P A_{core}}$$

EQUATION 176:

$$N_P = \frac{(V_{DC,min} - V_{Q,on})}{A_{core} F_{PWM} \Delta B} D_{max}$$

TRANSFORMER: PRIMARY, WIRE SIZE

Current flowing in the primary windings and into the switches are plotted in Figure 46(G and H).

To simplify computations, the real current waveforms can be replaced with the mid-ramp value ($I_{P,mr}$) and determine its value considering the input (P_I) and output (P_O) power.

The input power is shown in Equation 177.

EQUATION 177:

$$P_I = V_{D(C,min)} I_{P,mr} 2 D_{max}$$

where D is the duty cycle

The output power is shown in Equation 178.

EQUATION 178:

$$P_O = \eta P_I$$

where η is the efficiency

Operating on these two equations results in Equation 179.

EQUATION 179:

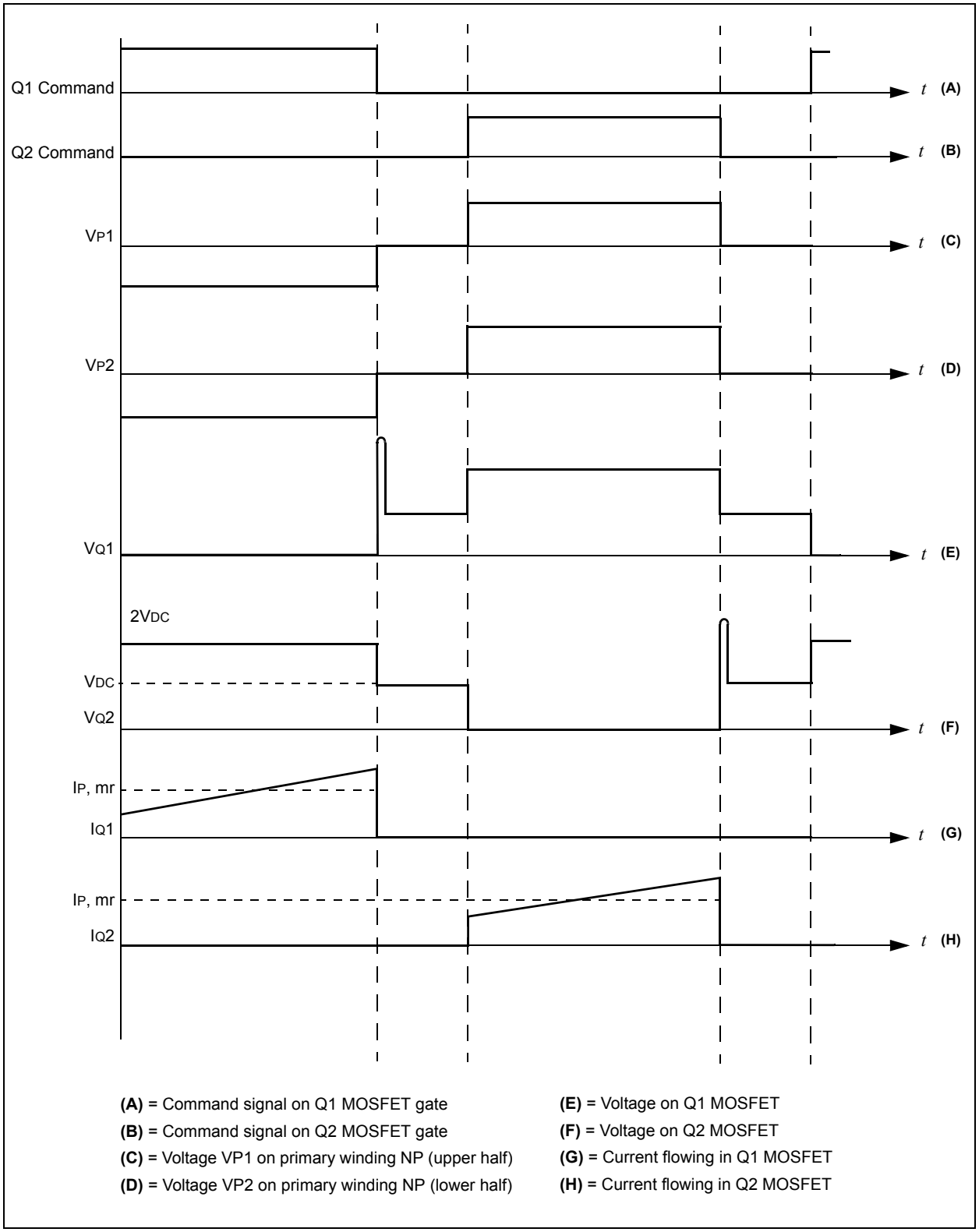
$$I_{P,mr} = \frac{P_O}{2\eta V_{DC,min} D_{max}}$$

The rms value is shown in Equation 180.

EQUATION 180:

$$I_{P,rms} = I_{P,mr} \sqrt{D_{max}}$$

FIGURE 46: PUSH-PULL CONVERTER WAVEFORMS: PRIMARY SIDE



(A) = Command signal on Q1 MOSFET gate
(B) = Command signal on Q2 MOSFET gate
(C) = Voltage VP1 on primary winding NP (upper half)
(D) = Voltage VP2 on primary winding NP (lower half)
(E) = Voltage on Q1 MOSFET
(F) = Voltage on Q2 MOSFET
(G) = Current flowing in Q1 MOSFET
(H) = Current flowing in Q2 MOSFET

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TRANSFORMER: SECONDARY, NUMBER OF TURNS

Once the primary number of turns has been defined, NS can be determined using Equation 173 and Equation 176, as shown in Equation 181.

EQUATION 181:

$$N_S = \frac{V_{OUT}}{2A_{core}F_{PWM}\Delta B} \cdot 10^8$$

TRANSFORMER: SECONDARY, WIRE SIZE

As previously seen, the secondary current waveform is quite complex (refer to Figure 47(G and H). However, to simplify computations, a contribution to the current only during TON is considered. The average current, shown as IO, av, nom, is the average output current the converter is designed for. The rms secondary current (IS) results in Equation 182.

EQUATION 182:

$$I_{S, rms} = I_{O, av, nom}\sqrt{D_{max}}$$

DIODES

During TON (Q1 ON, Q2 OFF), diode D2 is reverse-biased. The maximum voltage it can tolerate is equal to Equation 183.

EQUATION 183:

$$V_{R, D2} = -2\frac{N_S}{N_P}(V_{DC, max} - V_{Q1, on}) + V_{D1}$$

The average current flowing in D1 is the same current that is flowing into the inductor, and its value is IO, av, nom.

During the other TON period (Q1 OFF, Q2 ON), things are reversed; now D1 is reverse-biased and D2 is conducting. The same values as before apply.

MOSFETS

In Equation 159 (repeated in Equation 184) the voltage the switch must be able to withstand (considering the maximum input voltage) twice the maximum input voltage.

EQUATION 184:

$$V_{Q2, off} = 2V_{DC, max} - V_{Q1, on}$$

The maximum voltage the switches have to withstand must also take into account the spike that is generated by leakage inductance on the falling edges of the switch control signal. The spike is generally estimated to be 30% higher than the voltage on the switch. Therefore, at the end of the TON time interval, the maximum voltage is equal to Equation 185.

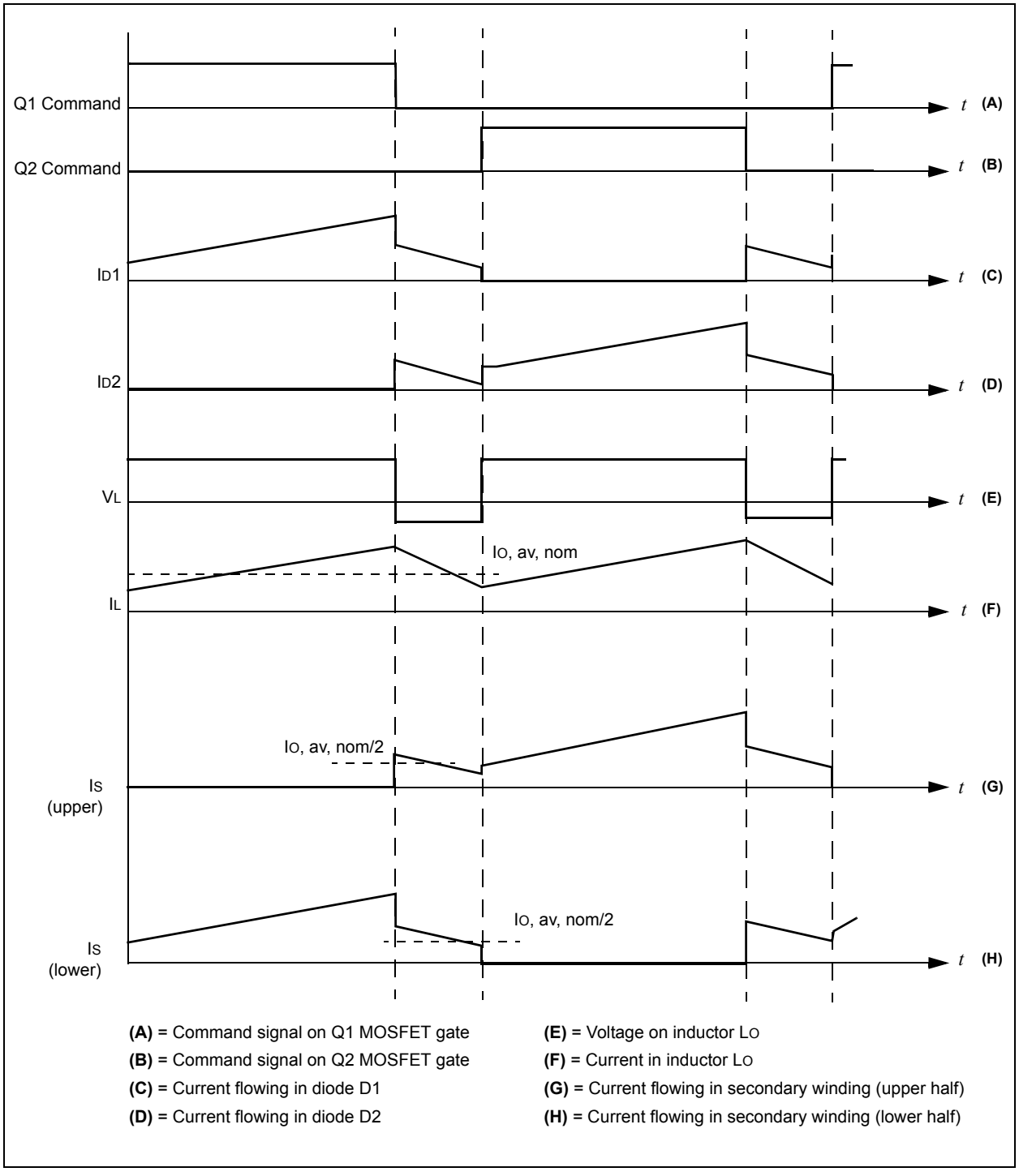
EQUATION 185:

$$V_{Q, max} \approx 2.6V_{DC, max}$$

The maximum current flowing through the switches has been already computed in Equation 179.

The maximum VQ, max and IP, mr are now obtained. Therefore, almost all that is needed to make the best device choice is known. All that remains is to add the analysis of the power dissipated in the switch, which are switching and DC losses.

FIGURE 47: PUSH-PULL CONVERTER WAVEFORMS: SECONDARY SIDE



(A) = Command signal on Q1 MOSFET gate
(B) = Command signal on Q2 MOSFET gate
(C) = Current flowing in diode D1
(D) = Current flowing in diode D2
(E) = Voltage on inductor LO
(F) = Current in inductor LO
(G) = Current flowing in secondary winding (upper half)
(H) = Current flowing in secondary winding (lower half)

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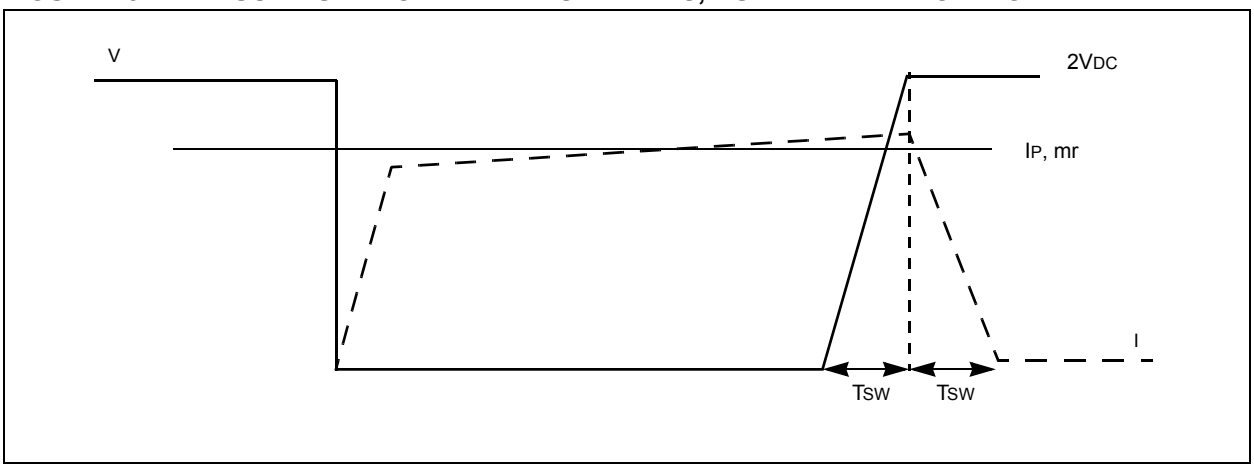
Switching Losses

Figure 48 plots the current and voltage in the switch at the switching instance. When the switch is turned on, the voltage falls rapidly, while the current has a smooth up-slope since current cannot change abruptly in an inductor. As seen in Figure 48, power dissipation is zero.

Things are completely different when the switch is turned off. Both the voltage and the current have a smooth slope (an up-slope the former, a down-slope the latter), and there is a significant overlap and some non-zero power is dissipated.

FIGURE 48: PUSH-PULL CONVERTER: SWITCHES, CURRENT AND VOLTAGE



Its value can be easily computed using Equation 186.

EQUATION 186:

$$P_{Q,ac,max} = I_{P,mr}\frac{2V_{DC,max}T_{SW}}{2T} + 2V_{DC,max}\frac{I_{P,mr}T_{SW}}{2T} = 2I_{P,mr}V_{DC,max}\frac{T_{SW}}{T}$$

where T_{SW} equals the rise and fall times

The DC losses can then be computed, as shown in Equation 187.

EQUATION 187:

$$P_{Q,dc,max} = I_{P,mr}V_{Q,on}D_{max}$$

The total power dissipated in the switch is then equal to Equation 188.

EQUATION 188:

$$P_{Q,total,max} = P_{Q,ac} + P_{Q,dc} = 2I_{P,mr}V_{DC,max}\frac{T_{SW}}{T} + I_{P,mr}V_{Q,on}D_{max}$$

OUTPUT INDUCTOR

The inductor is selected in such a way as to prevent the output inductor current from becoming discontinuous. The computations are performed at the edge between continuous and discontinuous operation, meaning when the output current starts from zero at the beginning of the TON period and goes back to zero at the end of the TR period. In other words, the inductor current peak, which is also the current ripple DL, is twice the output average current, as shown in Equation 189.

EQUATION 189:

$$I_{O,ripple} = 2I_{O,av,min} = \frac{\frac{N_S}{N_P}(V_{D(C,min)} - V_{OUT})}{L_O} T_{ON}$$

Solving Equation 189 results in Equation 190.

EQUATION 190:

$$L_O = \frac{\frac{N_S}{N_P}V_{DC,min} - V_{OUT}}{2F_{PWM}I_{O,av,min}} D_{max}$$

OUTPUT CAPACITOR

As with the Buck Converter design, the output voltage ripple is mainly due to the ESR, resulting in Equation 191.

EQUATION 191:

$$V_{OUT,ripple} = ESR \cdot I_{O,ripple}$$

As seen in previous topologies, the output capacitor value can be determined from the relationship shown in Equation 192.

EQUATION 192:

$$C_O = \frac{I_{O,ripple}D_{max}}{F_{PWM}(V_{OUT,ripple} - I_{O,ripple}ESR)}$$

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FULL-BRIDGE CONVERTER

A Full-Bridge Converter, which is capable of managing higher power levels, requires some additional components compared to the Half-Bridge Converter.

Topology Equations

The basic Full-Bridge Converter topology is shown in Figure 49. Transistors Q1, Q4 and Q2, Q3 are always operated together, driven by the waveform shown in Figure 50. Care must be taken so that Q1, Q2 or Q3, Q4 are not ON at the same time; otherwise, a low impedance path is created from V_{DC} to ground. This imposes a maximum value on the T_{ON} interval as is discussed in a later section.

FIGURE 49: FULL-BRIDGE CONVERTER TOPOLOGY

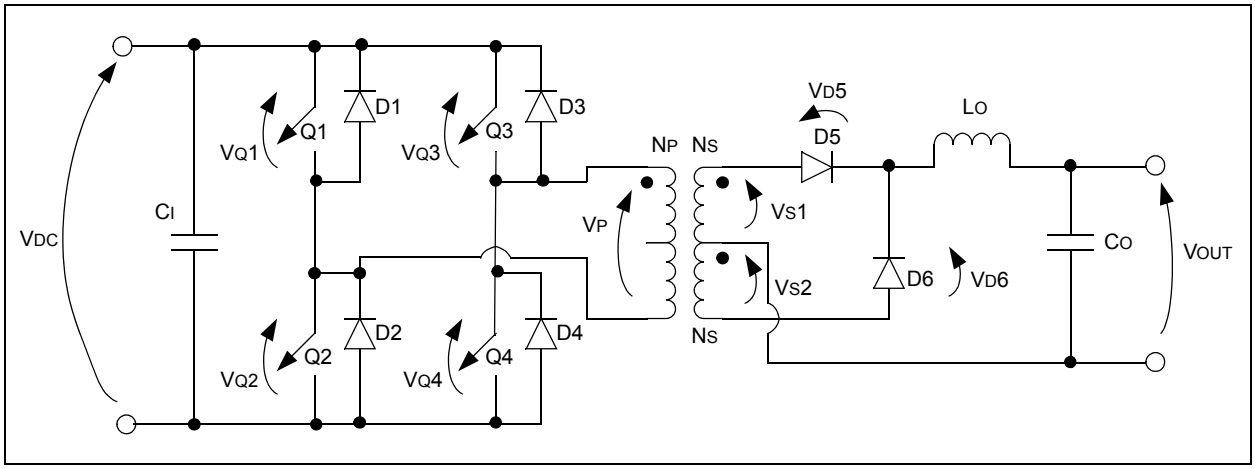
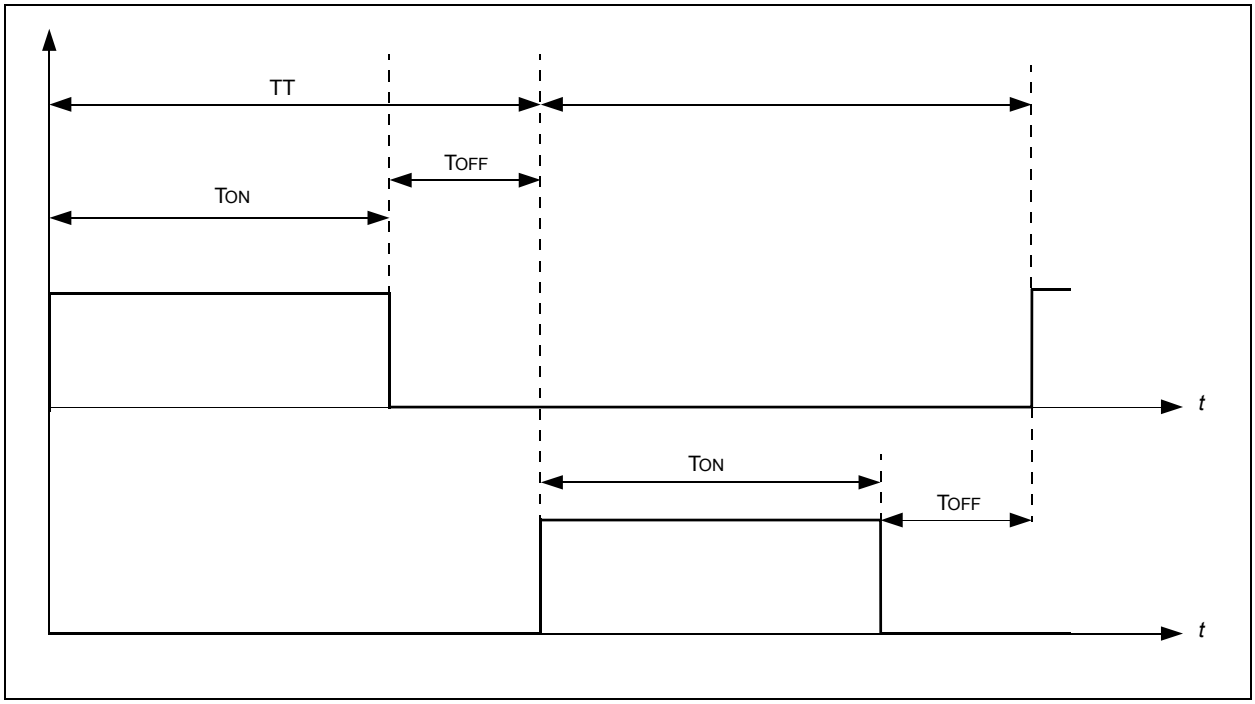


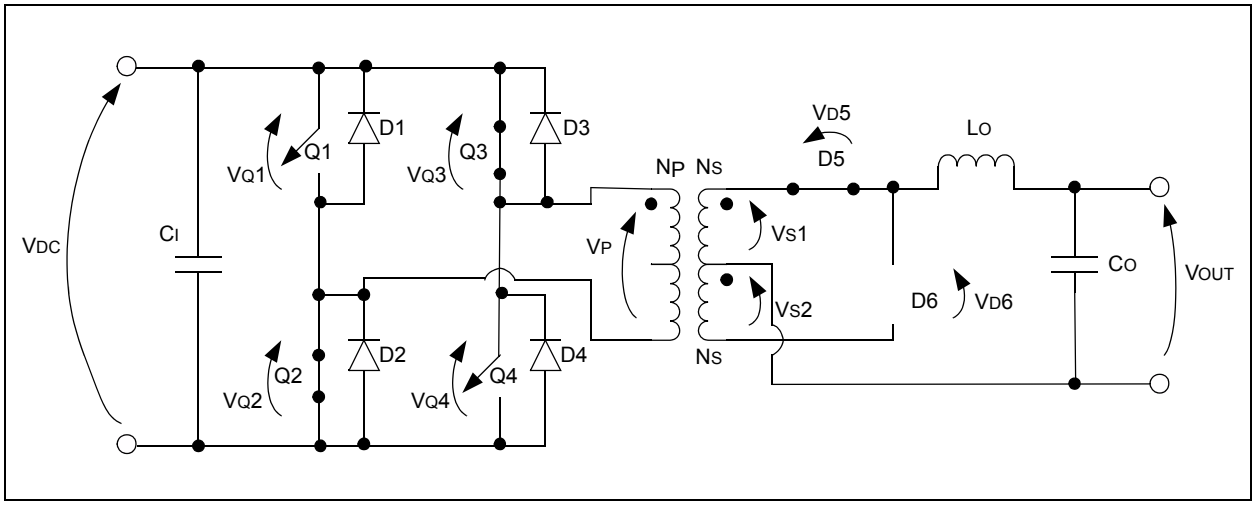
FIGURE 50: FULL-BRIDGE CONVERTER WAVEFORM



Q2 ON, Q3 ON; Q1 OFF, Q4 OFF
(INTERVAL 0-TON)

As shown in Figure 51, current flows through Q3, the transformer primary and Q2 back to the input. The dot end of the transformer is more positive than the non-dot end.

FIGURE 51: FULL-BRIDGE TOPOLOGY: Q2 AND Q3 ON



Input Circuit Behavior

The voltage on the primary is shown in Equation 193.

EQUATION 193:

$$V_P = V_{DC} - V_{Q2,on} - V_{Q3,on} = V_{DC} - 2V_{Q,on}$$

The magnetizing current increases according to the law shown in Equation 194.

EQUATION 194:

$$i_M(t) = \frac{V_P}{L_P}t = \frac{V_{DC} - 2V_{Q,on}}{L_P}t$$

Output Circuit Behavior

As for the primary winding, the dot ends of the two secondary windings are more positive that the two non-dot ends. This implies that diode D5 is conducting while diode D6 is not conducting.

The secondary voltage can be computed as shown in Equation 195.

EQUATION 195:

$$V_{S1} = \frac{N_S}{N_P}V_P = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on})$$

Equation 196 shows the current flowing into the inductor.

EQUATION 196:

$$i_L(t) = i_L(0) + \frac{\frac{N_S}{N_P}V_{DC} - V_O}{L_O}t$$

The voltage on the output capacitor LO is shown in Equation 197.

EQUATION 197:

$$V_L = V_{S1} - V_{D5,on} - V_O = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D5,on} - V_O \approx \frac{N_S}{N_P}V_{DC} - V_O > 0$$

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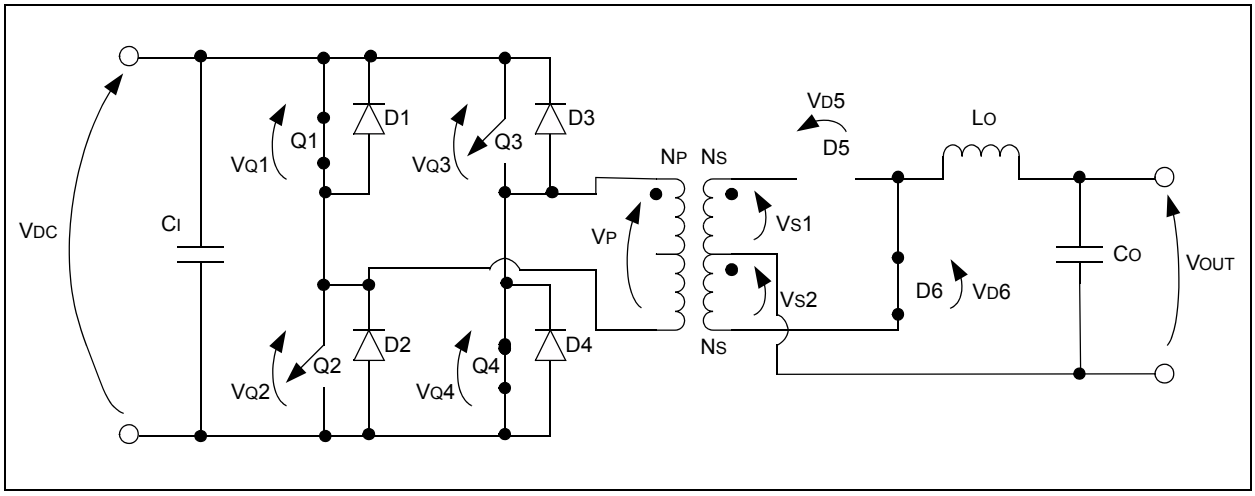
Q1 ON, Q4 ON; Q2 OFF, Q3 OFF
(INTERVAL 0-T_{ON})

As shown in Figure 52, current flows through Q1, the transformer, and Q4 back to the input. The dot end of the transformer is now more negative than the non-dot end.

FIGURE 52: FULL-BRIDGE CONVERTER TOPOLOGY: Q1 AND Q4 ON



Input Circuit Behavior

The primary voltage is shown in Equation 198.

EQUATION 198:

$$V_P = -V_{DC} + V_{Q1,on} + V_{Q4,on} = -V_{DC} + 2V_{Q,on}$$

The magnetizing current is shown in Equation 199.

EQUATION 199:

$$i_M(t) = \frac{V_P}{L_P}t = \frac{-V_{DC} + 2V_{Q,on}}{L_P}t$$

Output Circuit Behavior

In this instance, as at the primary, the dot ends are more negative than the non-dot ends, which results in Equation 200.

EQUATION 200:

$$V_{S2} = \frac{N_S}{N_P}V_P = -\frac{N_S}{N_P}(V_{DC} - 2V_{Q,on})$$

The output inductor voltage is shown in Equation 201.

EQUATION 201:

$$V_L = \frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D6,on} - V_O$$

The current flowing through it is shown in Equation 202.

EQUATION 202:

$$i_L(t) = i_L(0) + \frac{\frac{N_S}{N_P}V_{DC} - V_O}{L_O}t$$

Q2 AND Q3 HAVE JUST SWITCHED OFF; Q1 AND Q4 ARE OFF

When the switches are open, the magnetizing current continues to flow, reversing all voltages. At the primary, the dot end becomes more negative than the non-dot end. The magnetizing current flows through D4, the transformer, and D1 as seen in Figure 53.

The voltage on the primary is zero, and as shown in Equation 203 the voltage on the secondary is:

EQUATION 203:

$$V_{S1} = -V_{S2}$$

Consequently, both diodes D5 and D6 are ON and the inductor current is split in half between the two diode paths (see Figure 53 and Figure 54).

The voltage on the inductor is shown in Equation 204.

EQUATION 204:

$$V_L = -V_{S2} - V_O - V_{D6,\,on} \approx -V_O - V_{D6,\,on}$$

Since Vs2 is very low, its magnitude is given by the voltage drop on the secondary winding resistance due to one half of the inductor current flowing through it.

Q2 AND Q3 HAVE JUST SWITCHED OFF; Q1 AND Q4 ARE OFF

The behavior is similar to the previous condition. The current path in the primary is shown in Figure 54.

FIGURE 53: FULL-BRIDGE TOPOLOGY: Q2 AND Q3 HAVE JUST SWITCHED OFF; Q1 AND Q4 ARE OFF (PRIMARY CURRENT PATH)

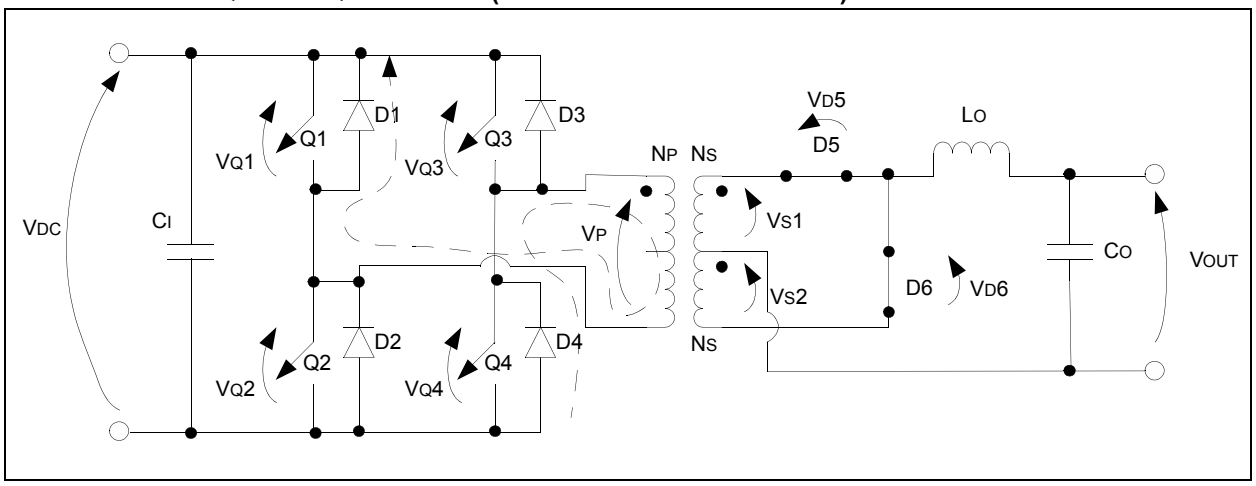
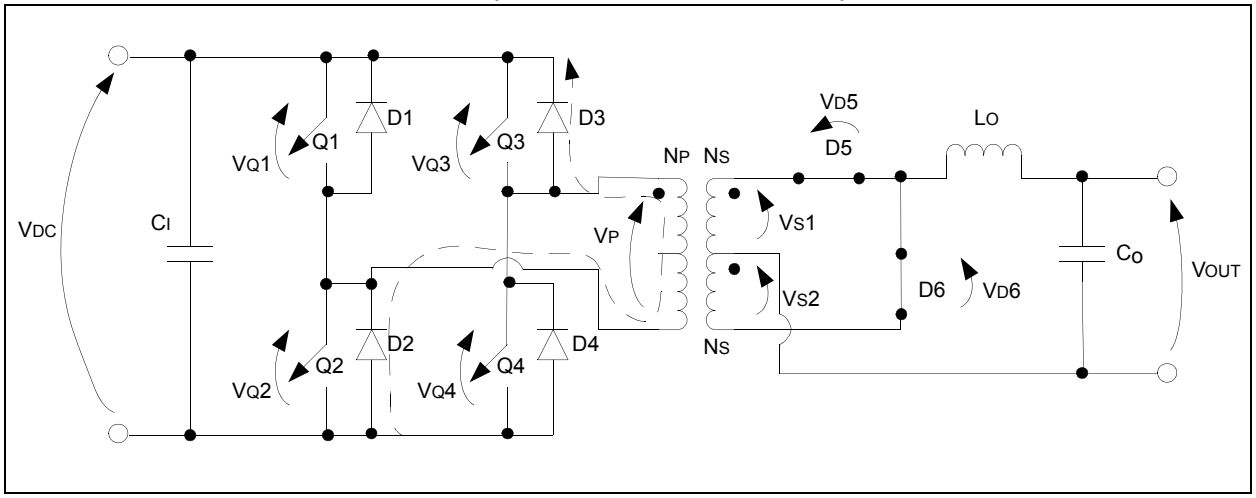


FIGURE 54: FULL-BRIDGE TOPOLOGY: Q1 AND Q4 HAVE JUST SWITCHED OFF; Q2 AND Q3 ARE OFF (PRIMARY CURRENT PATH)



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Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

The product of the primary voltage multiplied by TON must equal the product of the voltage multiplied by TOFF.

Computing Equation 197 and Equation 204 results in Equation 205.

EQUATION 205:

$$V_O = \left[\frac{N_S}{N_P}(V_{DC} - 2V_{Q,on}) - V_{D5,on}\right]D$$

where D = TON/T and the relationship TON + TOFF = T is used (see Figure 50)

To guarantee that the two switches of a leg are never ON at the same time, TON is limited to be at a maximum percentage of T, as shown in Equation 206.

EQUATION 206:

$$T_{ON,max} = \delta T$$

where, δ equals 0.8

The resulting maximum duty cycle is shown in Equation 207.

EQUATION 207:

$$D_{MAX} = \frac{T_{ON,max}}{T}$$

TRANSFORMER WINDING TURN RATIO

The maximum TON period will occur when the input voltage is at its minimum. Using Equation 205 and Equation 206 results in Equation 207.

EQUATION 208:

$$\frac{N_S}{N_P} = \frac{(V_O + V_{D5,on})\frac{T_{ON,max}}{T}}{(V_{DC,min} - 2V_{Q,on})\frac{T_{ON,max}}{T}}$$

The primary winding turn can be computed from the equation that relates the core flux change (ΔB), the voltage across the winding (VP) and the geometrical entity (A_e), as shown in Equation 209.

EQUATION 209:

$$N_P = \frac{V_{P,max}T_{ON,max}}{\Delta BA_e} \approx \frac{V_{DC,min}D_{MAX}}{\Delta BF_{PWM}A_e}$$

TRANSFORMER: PRIMARY, WIRE SIZE

Since the design specification POUT is known, the input power can be computed considering a converter efficiency of η, as shown in Equation 210.

EQUATION 210:

$$P_{OUT} = \eta P_{IN} = \eta V_{DC,min} I_{IN,av} \delta$$

where $I_{IN,av}$ is the average input current (see Figure 55 (E,G,I,K)) and δ = 0.8

Solving Equation 210 results in Equation 211.

EQUATION 211:

$$I_{I(N,av)} = \frac{P_{OUT}}{\eta V_{DC,min}\delta}$$

With some approximation, and replacing the real current waveform (ramp on a step) with a constant value equal to IIN, av, results in Equation 212.

EQUATION 212:

$$I_{IN,av,rms} = I_{IN,av}\sqrt{D_{MAX}}$$

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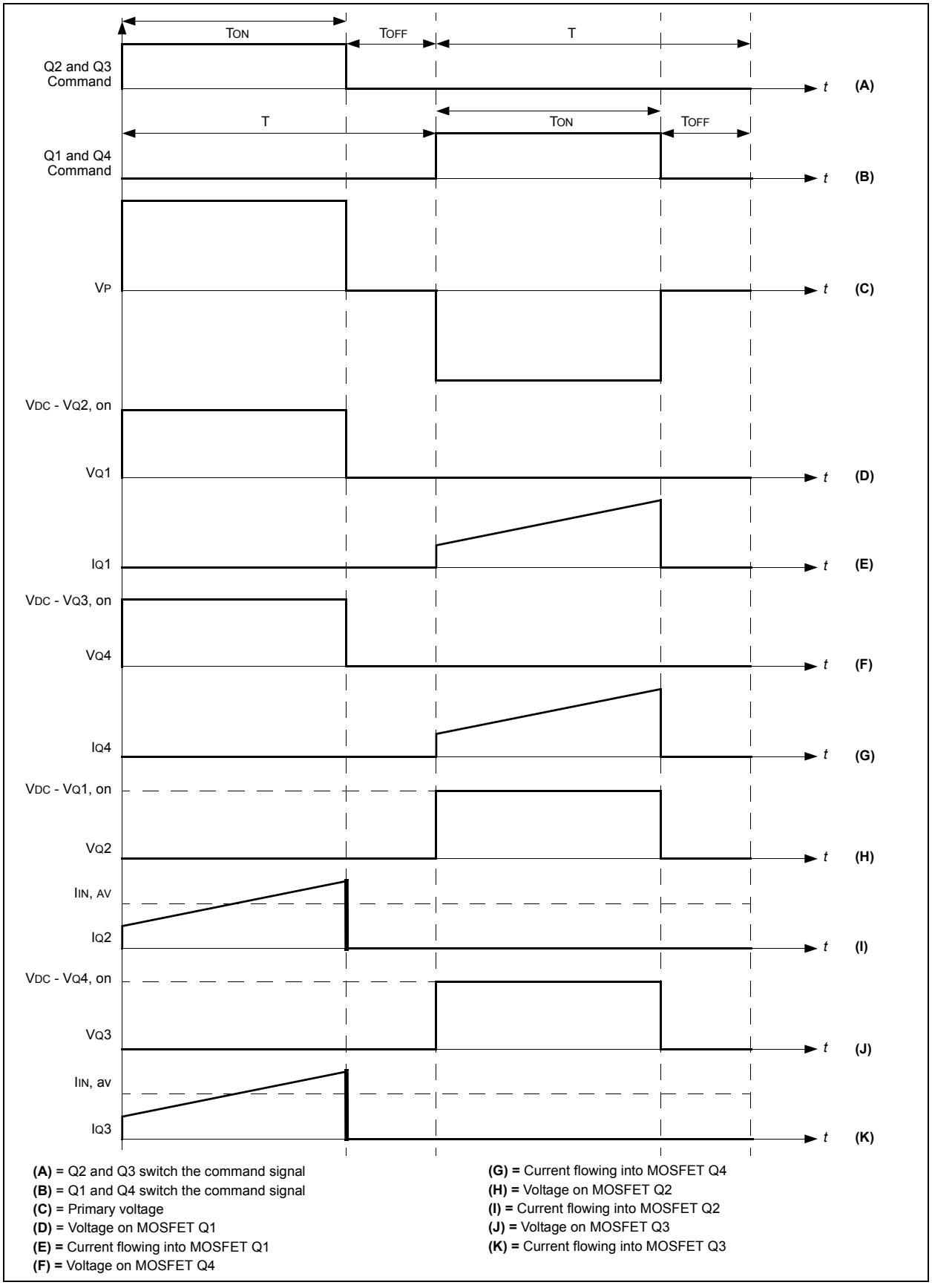
FIGURE 55: FULL-BRIDGE CONVERTER TOPOLOGY: INPUT CIRCUIT



(A) = Q2 and Q3 switch the command signal
(B) = Q1 and Q4 switch the command signal
(C) = Primary voltage
(D) = Voltage on MOSFET Q1
(E) = Current flowing into MOSFET Q1
(F) = Voltage on MOSFET Q4
(G) = Current flowing into MOSFET Q4
(H) = Voltage on MOSFET Q2
(I) = Current flowing into MOSFET Q2
(J) = Voltage on MOSFET Q3
(K) = Current flowing into MOSFET Q3

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TRANSFORMER: SECONDARY, NUMBER OF TURNS, WIRE SIZE

The secondary number of turns can be computed from Equation 208 and Equation 209 (see also Figure 56(D and E)).

To simplify the computation of the secondary rms current value, we do not consider that the contribution to the current value during TOFF is not calculated (this is due to the relatively short interval and small value of the currents). The average value as the medium value during the ramp current is considered (see Figure 56(D and E)).

Using the previous approximation results in Equation 213.

EQUATION 213:

$$I_{O,\,av,\,rms} = I_{O,\,nom}\sqrt{D_{MAX}}$$

SWITCHES

During TON, the maximum voltage drop on Q1 and Q4 are that of Equation 214.

EQUATION 214:

$$V_{Q1,\,off,\,max} = V_{DC,\,max} - V_{Q2,\,on}$$

and

$$V_{Q4,\,off,\,max} = V_{DC,\,max} - V_{Q3,\,on}$$

Similarly, the maximum voltage drop on Q2 and Q3 are that of Equation 215.

EQUATION 215:

$$V_{Q2,\,off,\,max} = V_{DC,\,max} - V_{Q1,\,on}$$

and

$$V_{Q3,\,off,\,max} = V_{DC,\,max} - V_{Q4,\,on}$$

Equation 216 shows the maximum voltage drop in Q2 and Q3 in more general terms.

EQUATION 216:

$$V_{Q,\,off,\,max} = V_{DC,\,max} - V_{Q,\,on}$$

DIODES

Equation 217 shows the voltage drop on diode D6, when Q2 and Q3 are ON.

Similarly, Equation 218 shows the maximum drop on D5, when Q1 and Q4 are ON.

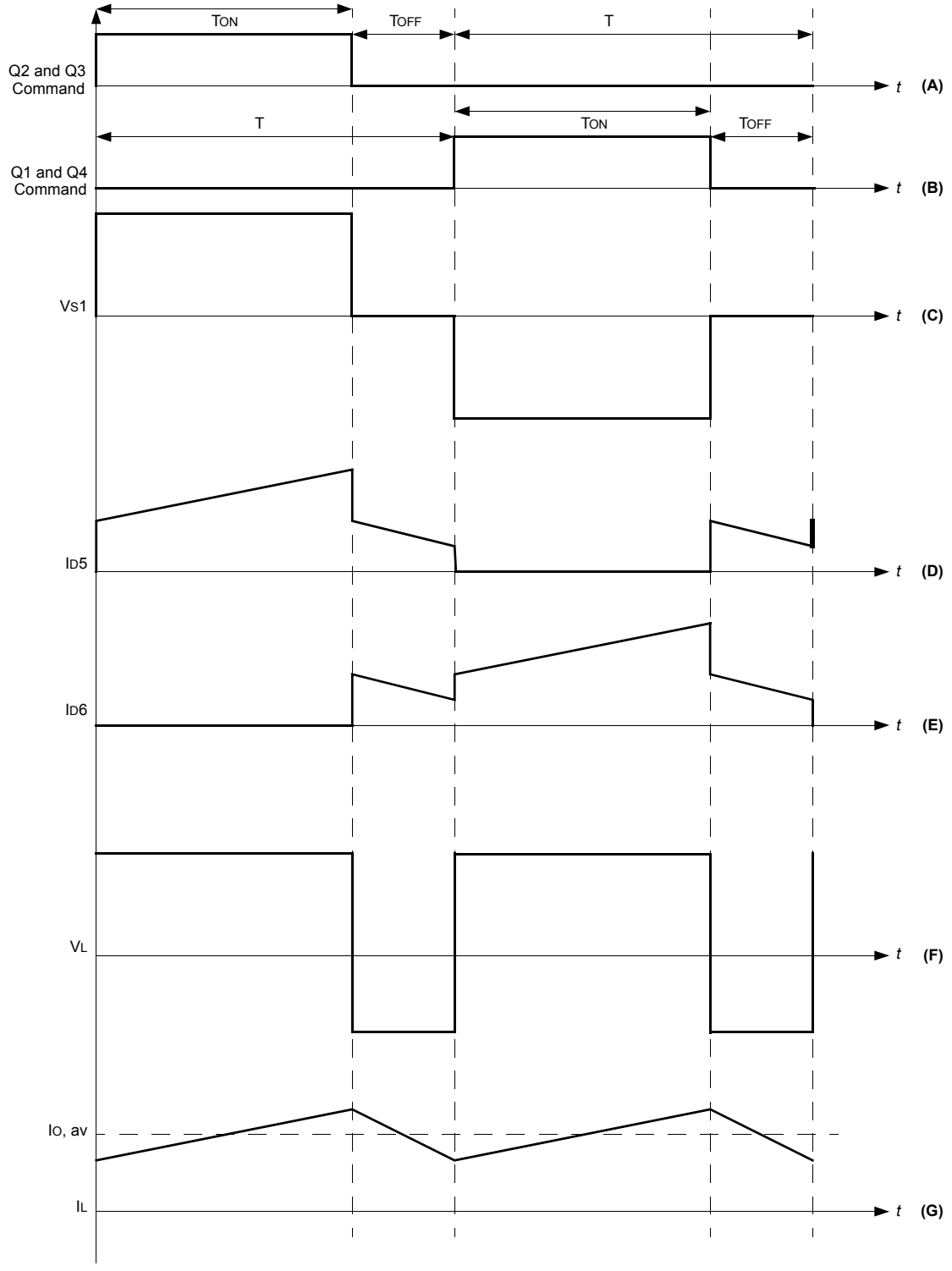
EQUATION 217:

$$V_{D6,\,off,\,max} = -V_{S1} - V_{S2} + V_{D5,\,on} \approx -2\frac{N_S}{N_P}(V_{DC,\,max} - 2V_{Q,\,on}) + V_{D5,\,on}$$

EQUATION 218:

$$V_{D5,\,off,\,max} = V_{S1} + V_{S2} - V_{D6,\,on} \approx -2\frac{N_S}{N_P}(V_{DC,\,max} - 2V_{Q,\,on}) + V_{D6,\,on}$$

FIGURE 56: FULL-BRIDGE CONVERTER TOPOLOGY: OUTPUT CIRCUIT



(A) = Q2 and Q3 switch the command signal
(B) = Q1 and Q4 switch the command signal
(C) = Secondary voltage
(D) = Diode D5 current
(E) = Diode D6 current
(F) = Inductor voltage
G) = Output inductor voltage

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OUTPUT INDUCTOR

The minimum inductor can be computed, considering the system at the edge of the discontinuous mode, as shown in Equation 219.

EQUATION 219:

$$I_{O,av} = \frac{I_{O,peak}}{2} = \frac{\Delta I_O}{2} \approx \frac{V_O}{2L_O} T_{OFF}$$

Solving Equation 219 results in Equation 220.

EQUATION 220:

$$L_O = \frac{V_O(1 - D_{MAX})}{2I_{O,av,nom} F_{PWM}}$$

OUTPUT CAPACITOR

The output capacitor is selected to get the specified output ripple. The greatest contribution to voltage ripple comes from the capacitor ESR, and the inductor current ripple, flowing through it, determines a voltage drop.

The capacitor value itself can then be computed using Equation 221, which describes the value of the voltage ripple taking into account all the components.

EQUATION 221:

$$V_{RIPPLE} = I_{RIPPLE}\left(ESR + \frac{D_{MAX}}{F_{PWM} C_O} + \frac{ESL \cdot F_{PWM}}{D_{MAX}}\right)$$

Neglecting ESL, since it is normally very small, results in Equation 222.

EQUATION 222:

$$C_O = \frac{I_{O,ripple} D_{MAX}}{F_{PWM}(V_{O,ripple} - I_{O,ripple} ESR)}$$

where,

$$I_{O,ripple} = \frac{V_O(1 - D_{MAX})}{L_O F_{PWM}}$$

FLYBACK CONVERTER

As presented in AN1114 (see **"Introduction"**), Flyback Converters are widely used in applications where an isolated conversion is required, for low-power ranges (5W to 150W), and since high output voltages can be quite easily obtained because there is no inductor in the output section.

Topology Equations - Discontinuous Mode

A Flyback Converter can be easily used in either Continuous or Discontinuous mode. In Discontinuous mode, the output winding current goes to zero before the end of the TOFF period, so that all the stored energy is transferred to the load. In Continuous mode, there is some residual energy stored in the transformer at the end of the ON and OFF periods.

Both of these modes will be analyzed, starting with the Discontinuous mode.

Figure 57 shows the basic flyback circuit. The switch is driven by a signal like the one presented in Figure 58.

FIGURE 57: BASIC FLYBACK CONVERTER TOPOLOGY

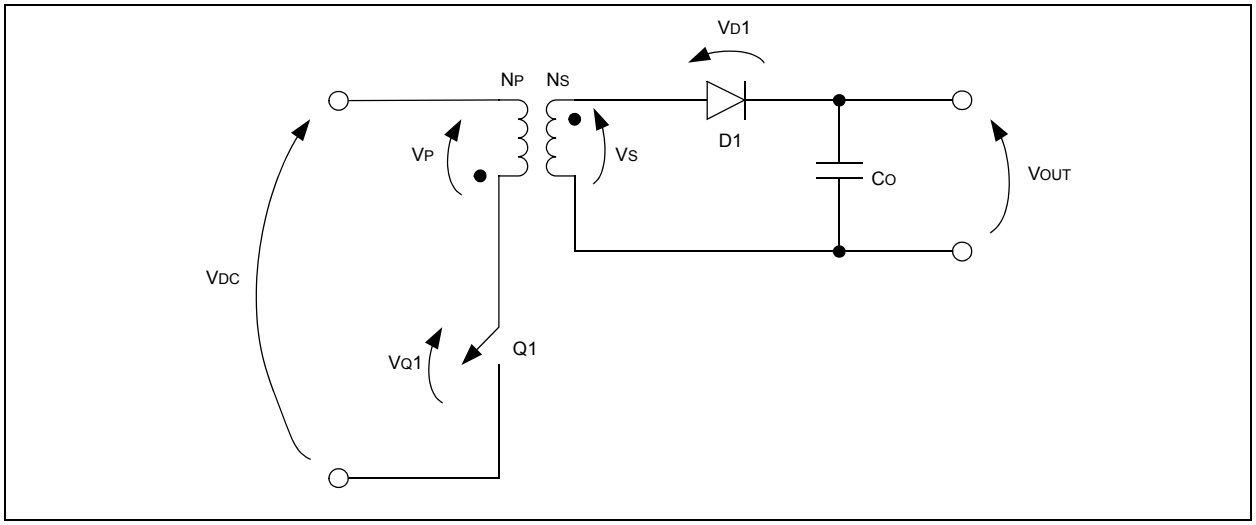
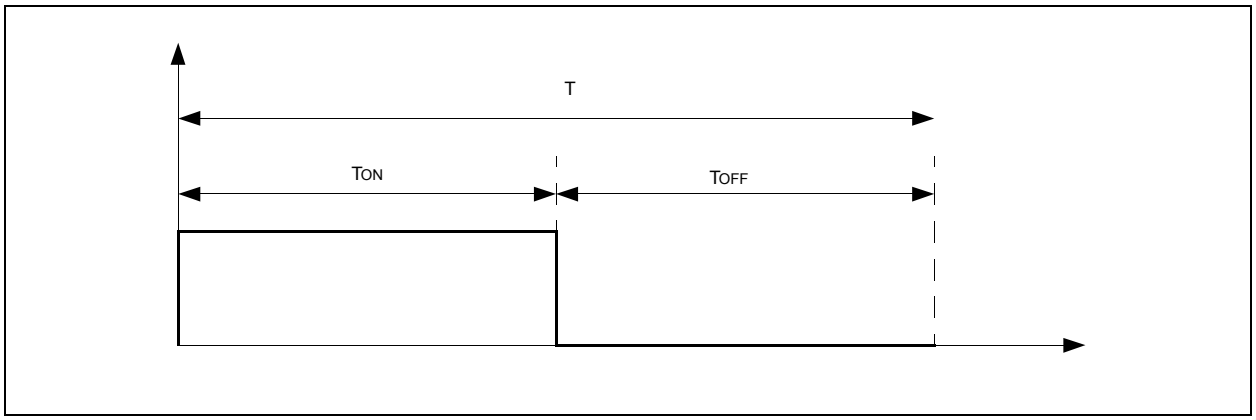


FIGURE 58: SWITCH Q1 COMMAND SIGNAL



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Q1 ON (INTERVAL 0 – TON)

Figure 59 shows the topology for this circuit.

Input Circuit Behavior

Equation 223 shows the voltage on the primary when the switch is closed.

EQUATION 223:

$$V_P = V_{DC} - V_{Q1,on}$$

The dot end is more negative than the non-dot end. The transformer behaves as an inductor accumulating energy in its windings. The current flowing in the primary is shown in Equation 224.

EQUATION 224:

$$I_P = \frac{V_P}{L_P}t = \frac{V_{DC} - V_{Q1,on}}{L_P}t$$

The increasing current, starting from zero and with a peak value reached at t = TON, is equal to Equation 225.

EQUATION 225:

$$I_{P,peak} = \frac{V_{DC} - V_{Q1,on}}{L_P}T_{ON}$$

The stored energy can be easily computed using Equation 226.

EQUATION 226:

$$E = \frac{1}{2}L_P I_{P,peak}^2$$

Output Circuit Behavior

The voltage on the secondary winding is shown in Equation 227.

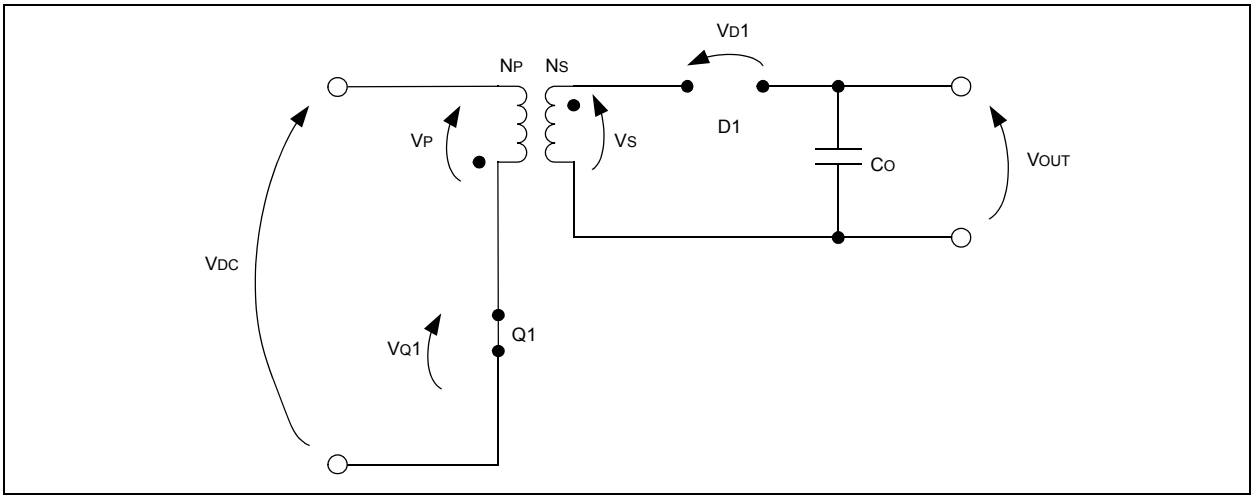
EQUATION 227:

$$V_S = -\frac{N_S}{N_P}(V_{DC} - V_{Q1,on})$$

where the minus sign is due to the fact that the dot end is more negative than the non-dot end terminal.

Therefore, the diode D1 is reverse-biased and no current flows into the output circuit. The output current is supplied by the output capacitor CO.

FIGURE 59: FLYBACK CONVERTER TOPOLOGY: INTERVAL 0 - TON



Q1 OFF (INTERVAL TON – (TON + TR))

The circuit topology is shown in Figure 60.

Input Circuit Behavior

Q1 is now open and current can no longer flow in the primary winding. As described in AN1114 (see **"Introduction"**), some circuitry to dissipate the energy in the winding is required (snubber network); however, it will not be analyzed here.

The voltage on the primary can be computed as Equation 228, in which VS is given by Equation 230, and the minus sign is due to the dot conversion.

EQUATION 228:

$$V_P = -\frac{N_P}{N_S} V_S$$

Output Circuit Behavior

As described in AN1114 (see **"Introduction"**), all voltages change sign so that in the secondary, the dot end becomes more positive that the non-dot end and the diode starts conducting current. The current that was flowing into the primary no longer flows because Q1 is now open, and transfers to the secondary as an initial current equal to Equation 229 with a down slope, so that it reaches zero at time TON + TR.

EQUATION 229:

$$I_{S,peak} = \frac{N_P}{N_S} I_{P,peak} = \frac{N_P}{N_S} \frac{V_{DC} - V_{Q1,on}}{L_P} T_{ON}$$

The voltage at the secondary is shown in Equation 230.

EQUATION 230:

$$V_S = V_O + V_{D1,on}$$

Q1 OFF (INTERVAL (TON +TR) - T)

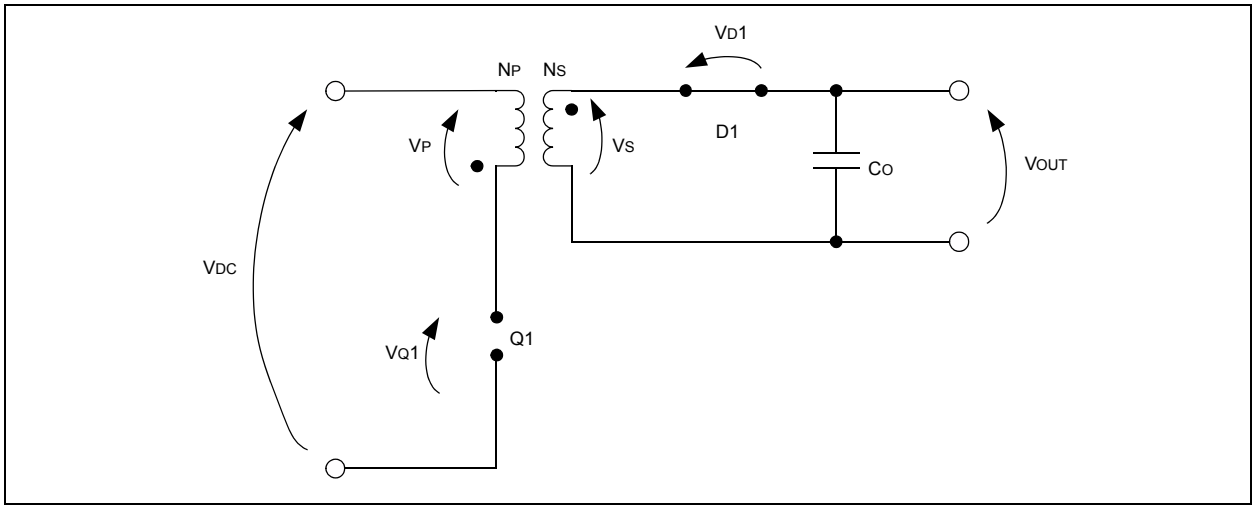
As previously stated, at time TON + TR, the current in the secondary has reached zero. To keep the system working in Discontinuous mode, some time (TF) must be added, as shown in Equation 232.

EQUATION 231:

$$T = T_{ON} + T_R + T_F$$

This is because the TON interval depends on the input voltage VDC and the output load and if, for instance, VDC decreases or the output current increases, the ON duration must be longer. TF will be consequently reduced, but will allow the system to be discontinuous.

FIGURE 60: FLYBACK CONVERTER TOPOLOGY: INTERVAL TON - TR



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Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

The input/output relationship is computed considering the power flow from input to output.

From Equation 226 the power stored in the primary can be computed, as shown in Equation 232.

EQUATION 232:

$$P = \frac{E}{T} = \frac{(V_{DC} - V_{Q1,on})^2 T_{ON}^2}{2TL_P}$$

The relationship between input and output power is shown in Equation 233.

EQUATION 233:

$$P_{OUT} = \eta P_{IN}$$

By combining Equation 232 and Equation 233, the output voltage as a function of the input voltage can be determined, as shown in Equation 234.

EQUATION 234:

$$V_O = V_{DC} T_{ON} \sqrt{\frac{\eta R F_{PWM}}{2L_P}}$$

Since the TON interval is a function of the input voltage VDC, the maximum TON (TON, max) corresponds to the minimum input voltage (VDC, min). Using these values, (VDC, min is a design spec and TON, max is usually set to some value so that TON, max + TR = 0.8T), Equation 234 can be revised, as shown in Equation 235.

EQUATION 235:

$$V_O = V_{DC,min} T_{ON,max} \sqrt{\frac{\eta R F_{PWM}}{2L_P}}$$

Two other equations, primary peak current (Equation 225) and secondary peak current (Equation 229), can be revised to take into account the VDC, min and TON, max relationship, as shown in Equation 236 and Equation 237, respectively.

EQUATION 236:

$$I_{P,peak} = \frac{V_{DC,min} - V_{Q1,on}}{L_P} T_{ON,max}$$

EQUATION 237:

$$I_{S,speak} = \frac{N_P}{N_S} \frac{V_{DC,min} - V_{Q1,on}}{L_P} T_{ON,max}$$

TRANSFORMER WINDINGS TURN RATIO

To determine the ratio (NP/NS) we can have a look at the maximum voltage the Q1 MOSFET has to be able to sustain.

Considering Figure 57, the maximum voltage on the switch is equal to that of Equation 238.

EQUATION 238:

$$V_{Q1,off,max} = V_{DC,max} - V_P$$

The primary voltage, VP, is calculated using Equation 228 and Equation 230, which results in Equation 239.

EQUATION 239:

$$V_{Q1,off,max} = V_{DC,max} + \frac{N_P}{N_S}(V_O + V_{D1,on})$$

If a MOSFET is selected with a sufficiently high voltage rating, VQ1, off is considered as a datum so that in Equation 239, the only unknown value is (NP/NS); therefore, NP/NS is equal to that of Equation 240.

EQUATION 240:

$$\frac{N_P}{N_S} = \frac{V_{Q1,off,max} - V_{DC,max}}{(V_O + V_{D1,on})}$$

MAXIMUM ALLOWABLE TON

To determine the maximum TON, the fact that the core should never saturate is considered. This means the voltage-time interval product during energy storage must equal the voltage-time interval product during the delivery of energy to the load. In simpler terms, area A1 must equal area A2, as shown in Figure 61. Considering that TON, max + TR = βT with β < 1, as shown in Equation 241, which after computation, results in Equation 242.

EQUATION 241:

$$T_{ON,\,max} + T_R = \beta T$$

EQUATION 242:

$$T_{ON,\,max} = \frac{\frac{N_P}{N_S}(V_O + V_{D1,\,on})\beta}{\left[(V_{Dc,\,min} - V_{Q1,\,on}) + \left(\frac{N_P}{N_S}\right)(V_O + V_{D1,\,on})\right]F_{PWM}}$$

TRANSFORMER PRIMARY

The value of the transformer primary inductance can be easily computed using Equation 235, replacing TON, max with the computed value from Equation 242, where the design specification, POUT, max = V_O^2/R_O, results in that of Equation 243.

EQUATION 243:

$$L_P = \frac{V_{DC,\,min}^2 T_{ON,\,max}^2 R\eta F_{PWM}}{2V_O^2} = \frac{V_{DC,\,min}^2 T_{ON,\,max}^2 \eta F_{PWM}}{2P_{OUT,\,max}}$$

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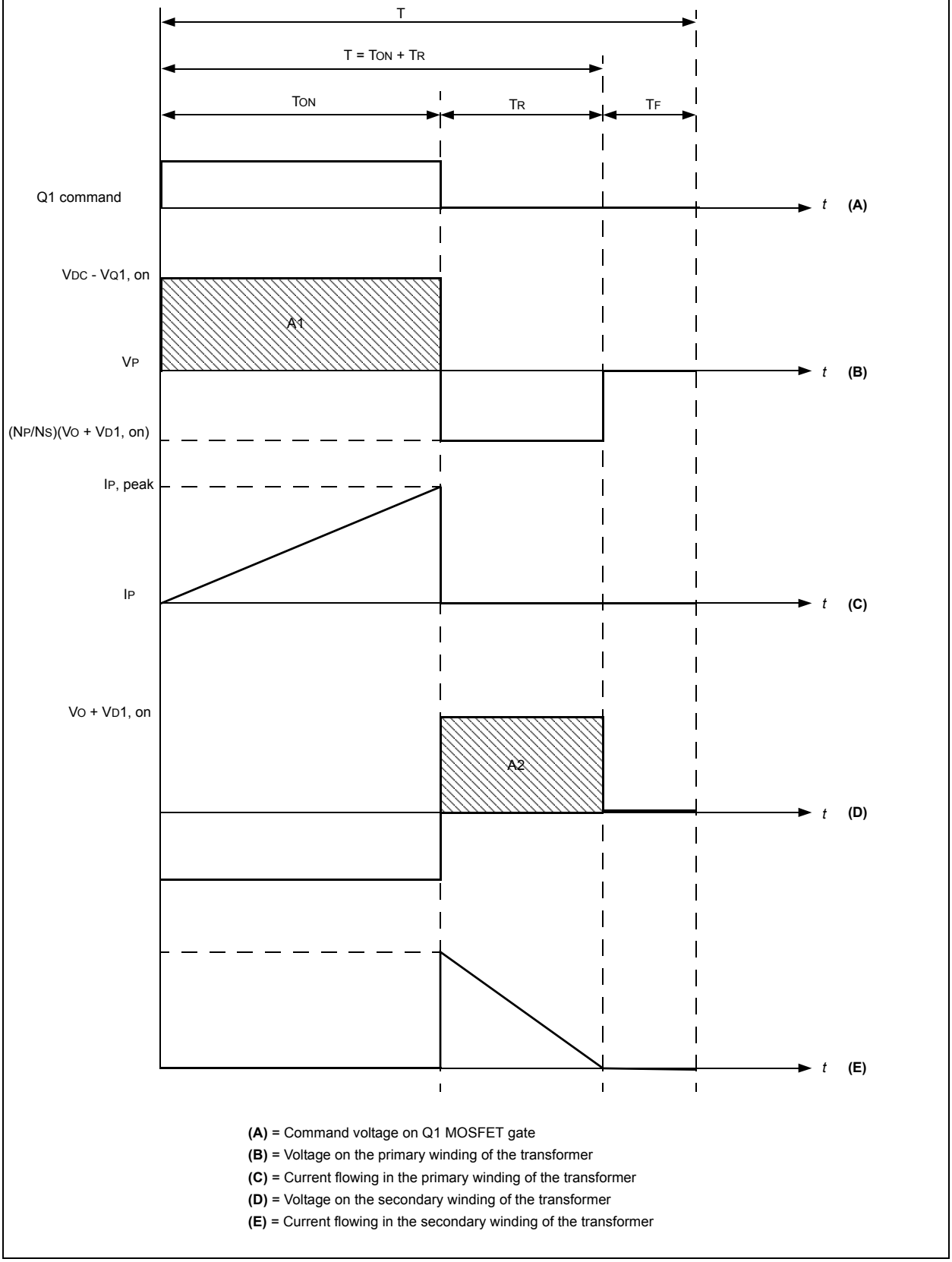
FIGURE 61: FLYBACK CONVERTER TOPOLOGY WAVEFORMS: DISCONTINUOUS OPERATION



(A) = Command voltage on Q1 MOSFET gate
(B) = Voltage on the primary winding of the transformer
(C) = Current flowing in the primary winding of the transformer
(D) = Voltage on the secondary winding of the transformer
(E) = Current flowing in the secondary winding of the transformer

TRANSFORMER: PRIMARY, WIRE SIZE

As can be seen in Figure 61(C), the current in the primary has a triangular shape, with a peak at t = TON. Based on this, the rms value can be computed as shown in Equation 244.

EQUATION 244:

$$I_{PRIMARY,rms} = \frac{I_{P,peak}}{\sqrt{3}}\sqrt{T_{ON,max}F_{PWM}}$$

In Equation 244, IP, peak is calculated from Equation 225, and TON, max, is calculated from Equation 242, which results in that of Equation 245.

EQUATION 245:

$$I_{P,peak} = \frac{V_{DC,min} - V_{Q1,on}}{L_P}T_{ON,max}$$

TRANSFORMER: SECONDARY, WIRE SIZE

From Figure 61(E), the current in the secondary similarly has a triangular shape. The rms value is then calculated using Equation 246.

EQUATION 246:

$$I_{SECONDARY,rms} = \frac{I_{S,peak}}{\sqrt{3}}\sqrt{T_R F_{PWM}} = \frac{N_P}{N_S}\frac{I_{P,peak}}{\sqrt{3}}\sqrt{T_R F_{PWM}}$$

OUTPUT DIODE

The current flowing through the output diode is the same current flowing into the secondary, with its peak value computed in Equation 228. The average current can be computed as shown in Equation 247.

EQUATION 247:

$$I_{D1,av} = \frac{1}{2}I_{S,peak}\frac{T_R}{T}$$

The maximum reverse voltage on the diode, during TON can be computed as shown in Equation 248.

EQUATION 248:

$$V_{Q1,off,max} = -\frac{N_S}{N_P}(V_{DC,max} - V_{Q1,on}) - V_O$$

OUTPUT CAPACITOR

The output capacitor can be computed considering that it has to supply the whole current to the load during TON. The criteria to be used is that the voltage droop should be less than the acceptable output voltage ripple. Since the voltage droop is equal to Equation 249, the capacitor value can be computed as shown in Equation 250.

EQUATION 249:

$$V_{DROOP} = \frac{I_{O,max}T_{ON,max}}{C_O}$$

EQUATION 250:

$$C_O = \frac{I_{O,max}T_{ON,max}}{V_{ACCEPTABLE\_RIPPLE}}$$

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Topology Equations – Continuous Mode

In Continuous mode applications, the basic circuit does not change (refer to Figure 57); however, the essential difference is that the current (both in the primary winding and the secondary winding) will not start and reaches zero during the PWM period, T. This means that some energy is still stored in the system when the PWM period is over.

The period T is now made up of TON and TOFF only. The basic topology equations are exactly the same as before, so they are presented without repeating all of the previous explanations.

Q1 ON (INTERVAL 0 – T_{ON})

Input Circuit Behavior

Equation 251 shows the voltage on the primary winding.

EQUATION 251:

$$V_P = V_{DC} - V_{Q1,on}$$

The current in the primary is shown in Equation 252.

EQUATION 252:

$$I_P = \frac{V_{DC} - V_{Q1,on}}{L_P} t$$

Equation 253 shows the peak current at the end of TON.

EQUATION 253:

$$I_{P,peak} = \frac{V_{DC} - V_{Q1,on}}{L_P} T_{ON}$$

Output Circuit Behavior

The voltage on the secondary is shown in Equation 254.

EQUATION 254:

$$V_S = -\frac{N_S}{N_P}(V_{DC} - V_{Q1,on})$$

Q1 OFF (INTERVAL T_{ON} – T)

Input Circuit Behavior

The voltage on the primary is shown in Equation 255.

EQUATION 255:

$$V_P = -\frac{N_P}{N_S} V_S$$

Output Circuit Behavior

Equation 256 shows the voltage on the transformer secondary winding.

EQUATION 256:

$$V_S = V_O - V_{D1,on}$$

The initial current (reflected from the primary), is shown in Equation 257.

EQUATION 257:

$$I_{S,peak} = \frac{N_P}{N_S} I_{P,peak} = \frac{N_P}{N_S} \frac{V_{DC} - V_{Q1,on}}{L_P} T_{ON}$$

Design Equations and Component Selection

INPUT/OUTPUT RELATIONSHIP AND DUTY CYCLE

Looking at Figure 62(B), the areas A1 and A2 must be equal so that the initial and final points on the transformer core hysteresis curve coincide, as shown in Equation 258.

EQUATION 258:

$$(V_{DC} - V_{Q(1,on)}) T_{ON} = \frac{N_P}{N_S}(V_O + V_{D(1,on)}) T_{OFF} \Rightarrow$$

$$V_O = \frac{N_S}{N_P}(V_{DC} - V_{Q1,on}) \frac{D}{1 - D}$$

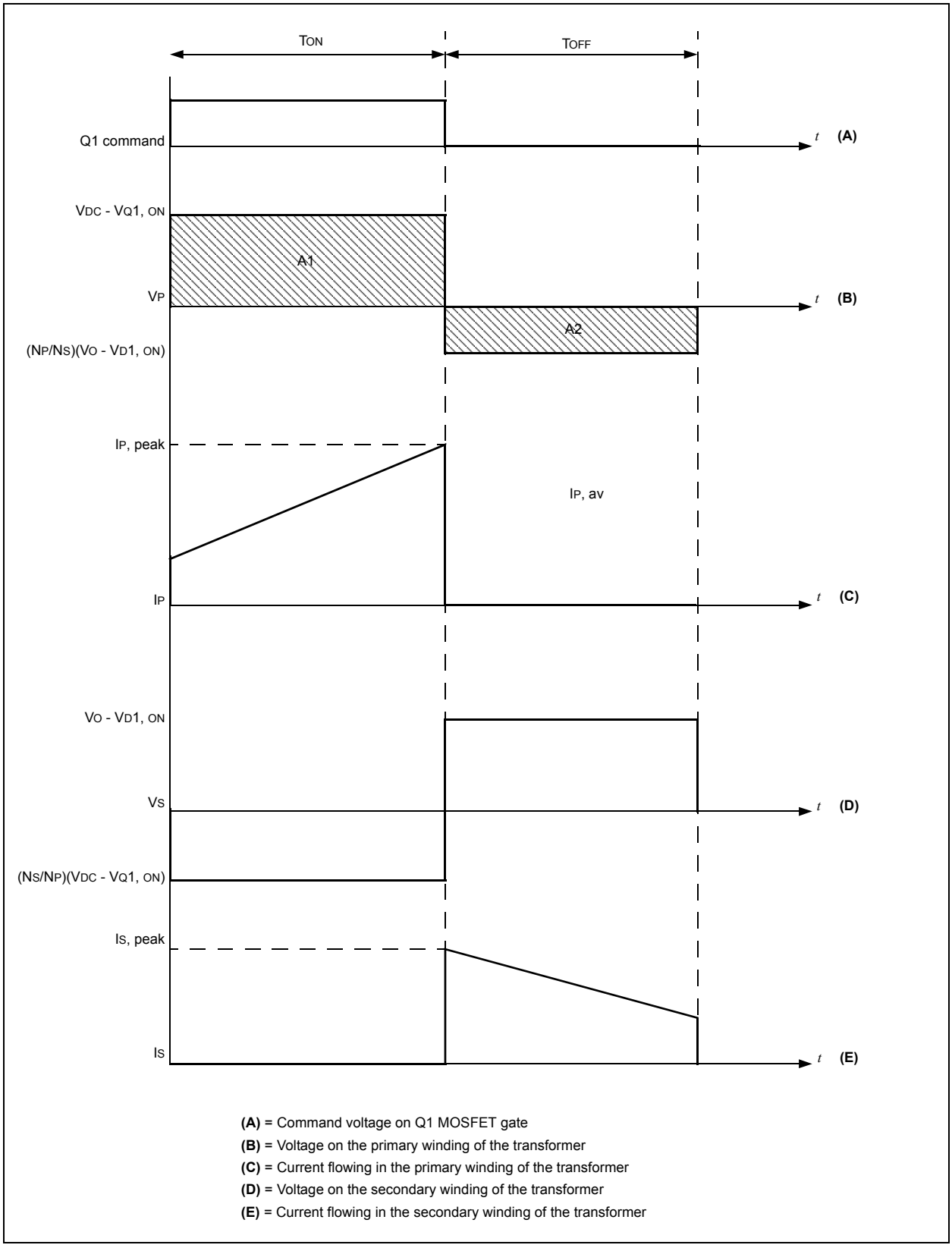
$$D = \frac{T_{ON}}{T}$$

The maximum TON/T value, can be computed from Equation 258 to occur with VDC, min (where NP/NS is computed in Equation 260), which results in Equation 259.

EQUATION 259:

$$\frac{T_{ON,max}}{T} = \frac{\frac{N_P}{N_S}(V_O + V_{D1,on})}{(V_{DC,min} - V_{Q1,on}) + \frac{N_P}{N_S}(V_O + V_{D1,on})}$$

FIGURE 62: FLYBACK CONVERTER TOPOLOGY WAVEFORMS: CONTINUOUS OPERATION



(A) = Command voltage on Q1 MOSFET gate
(B) = Voltage on the primary winding of the transformer
(C) = Current flowing in the primary winding of the transformer
(D) = Voltage on the secondary winding of the transformer
(E) = Current flowing in the secondary winding of the transformer

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TRANSFORMER WINDINGS TURN RATIO

To determine the ratio (N_P/N_S), the maximum voltage the Q1 MOSFET can sustain must be calculated, as shown in Equation 260.

EQUATION 260:

$$\frac{N_P}{N_S} = \frac{V_{Q1,off,max} - V_{DC,max}}{(V_O + V_{D1,on})}$$

TRANSFORMER: PRIMARY, WIRE SIZE

Considering a desired output power P_O, as shown in Equation 261, the rms value can be computed replacing the real current (RAM on a step) with a constant value, equal to I_P, av. The rms value is then equal to Equation 262.

EQUATION 261:

$$P_{OUT} = \eta P_{IN} = \eta I_{P,av}(V_{DC} - V_{Q1,on})\frac{T_{ON,max}}{T} \Rightarrow$$

$$I_{P,av} = \frac{P_{OUT}}{\eta(V_{DC} - V_{Q1,on})\frac{T_{ON}}{T}}$$

EQUATION 262:

$$I_{P,rms} = I_{P,av}\sqrt{D_{MAX}}$$

TRANSFORMER: SECONDARY, WIRE SIZE

The output average current (I_O, av) must be determined. To do so, the output power (which is one of the design data) is considered, as shown in Equation 263.

EQUATION 263:

$$I_{O,av} = \frac{P_{OUT}}{(V_O + V_{D1,on})\left(1 - \frac{T_{ON,max}}{T}\right)}$$

Correspondingly the rms value is that of Equation 264.

EQUATION 264:

$$I_{O,rms} = I_{O,av}\sqrt{D_{MAX}}$$

TRANSFORMER: PRIMARY INDUCTANCE

The minimum L_P inductance can be easily computed if the system at the edge of the Discontinuous mode is considered. This means that the I_P, peak is exactly one half of the increment in primary current during T_{ON}.

Therefore, the minimum average input current is that of Equation 265.

EQUATION 265:

$$I_{P,av,min} = \frac{P_{OUT}}{\eta(V_{DC,min} - V_{Q1,on})\frac{T_{ON,max}}{T}} = \frac{\Delta I_P}{2} = \frac{(V_{DC,min} - V_{Q1,on})}{2L_P}T_{ON,max}$$

Solving L_P, results in Equation 266.

EQUATION 266:

$$L_P = \eta(V_{DC,min} - V_{Q1,on})(V_{DC,min} - V_{D1,on})\,T_{ON,max}^2 F_{PWM}$$

OUTPUT CAPACITOR

The output capacitor is computed as in the Discontinuous mode, as shown in Equation 267.

EQUATION 267:

$$C_O = \frac{I_{O,max}T_{O(N,max)}}{V_{ACCEPTABLE\_RIPPLE}}$$

VOLTAGE AND CURRENT TOPOLOGIES

In this section, control loops and voltage and current modes are analyzed. A Buck Converter is used, but these techniques are valid for any topology.

In all topologies, it has been seen that an input/output relationship can be easily obtained. So long as the desired input and output voltages are known, all that remains is to compute the PWM duty cycle. In a perfect world, this would be more than enough.

Unfortunately, in the real world, things behave differently. The input voltage can change, the load can vary (i.e., switching the output load On and Off), components have their tolerances, aging and temperature drift and, of course, noise is always present. As a result, performances can differ from expectations.

To keep the behavior of the system under control during unexpected situations, a “control loop” (hardware and/or firmware) must be added to perform the operation of “controlling” the output voltage. Control loops allow the design of a circuit where the output voltage will vary as little as possible when any environmental condition changes. Moreover, in some cases, control loops help in preventing dangerous operational situations. Current control loops can prevent flux walking in the transformers.

In the following sections, the voltage and current modes of operation will be described for each topology, keeping the following two basic questions in mind:

1. What happens to the system output voltage when the input voltage suddenly changes?
2. What happens to the output voltage when the load changes?

Voltage Loop

Figure 63 presents the Buck Converter previously studied in detail, with some additional circuitry. A couple of series resistors (R1 and R2) connected to the output take a reduced amplitude copy (V_{FB}) of V_{OUT}. This voltage is compared in the error amplifier (EA) with a reference voltage (V_{REF} – the voltage value desired at the output). The output signal (V_X) is used to trim the duty cycle of the PWM signal that drives the switch.

To understand how the PWM block works, the technique that is commonly used in the analog implementation of such systems will be used initially. This does not mean that this is the only possible implementation. Later, how to digitally implement the same features with a dsPIC® DSC device is discussed. The analog version is instead quite easy and intuitive and allows for a simple explanation of how things work.

The PWM block can be replaced by a comparator that compares the V_X voltage to a sawtooth signal, generated by a local oscillator (see Figure 64). Its frequency is the PWM frequency.

FIGURE 63: BUCK CONVERTER - BASIC VOLTAGE LOOP

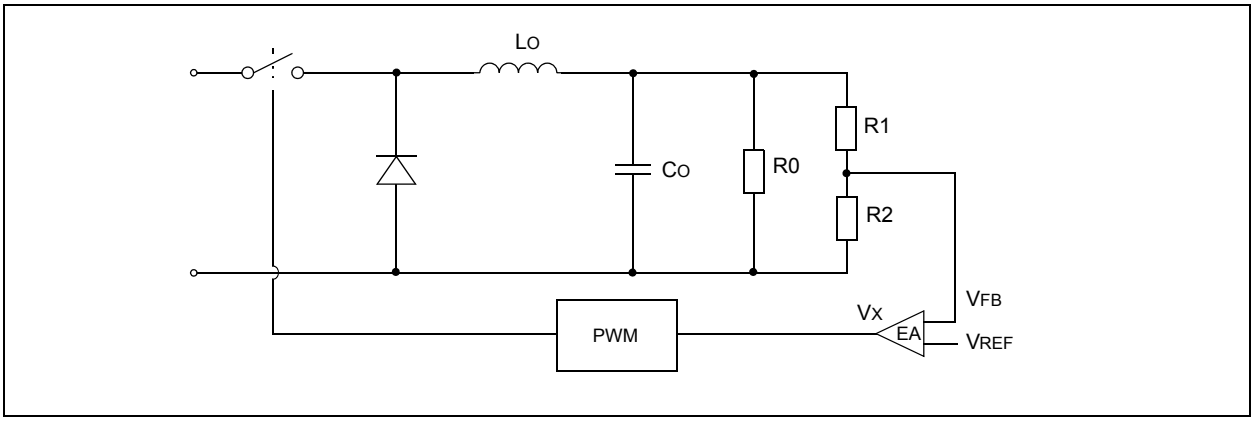

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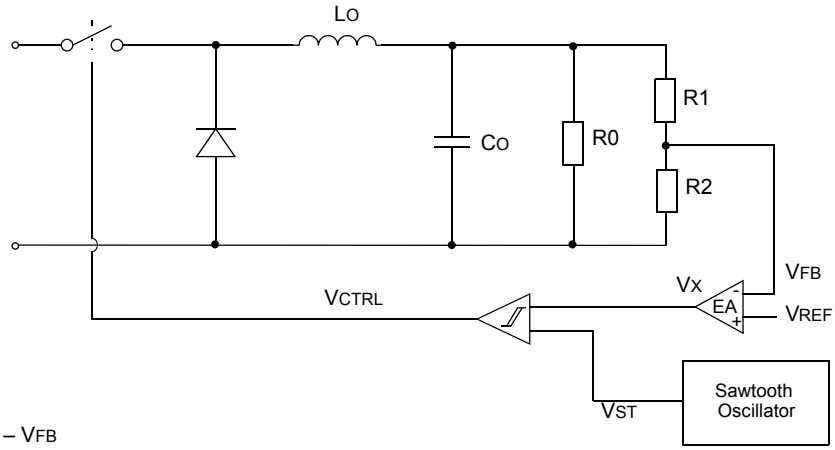
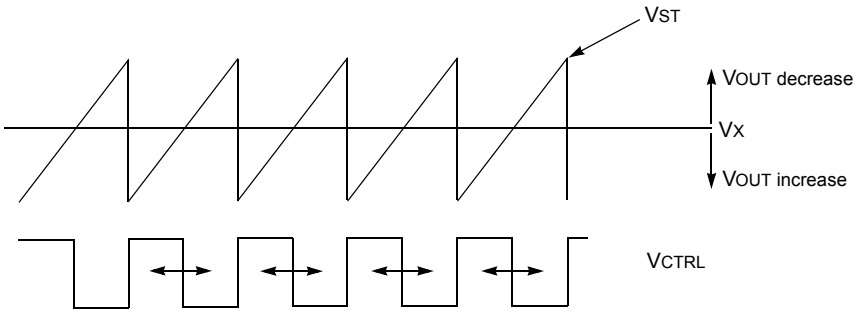
FIGURE 64: BUCK CONVERTER - BASIC ANALOG VOLTAGE LOOP



Note: VX = VREF – VFB

Here is how the system works. The VFB voltage, representing the current output voltage, is subtracted in the error amplifier EA from the reference voltage VREF. So, at least for now, the function of the EA block is just to perform a subtraction. Signal VX represents the error between the desired voltage and the "real" voltage the system is generating at that instant in time. The VX signal at Steady state, has a very slow moving average value. In the comparator, this signal is compared to the locally generated sawtooth, as shown in Figure 65, which results in VCTRL = 1, if VST < VX, or VCTRL = 0, if VST > VX.

FIGURE 65: CONTROL VOLTAGE (VCTRL) GENERATED BY COMPARISON BETWEEN ERROR VOLTAGE (VX) AND THE SAWTOOTH WAVEFORM



Note: VX = VREF – VFB

Since VCTRL is the PWM signal used to drive the switches, and is based on the value of VX, the duty cycle will either be small or large.

The operation in the EA is such that when the output voltage increases, the VX voltage decreases, so that the PWM duty cycle is reduced and vice versa. The falling edge of VCTRL moves according to the position of VX relative to VST.

LINE REGULATION

The question now is: how does this system react when the input voltage changes? In answering this question, consider that the ultimate goal is to keep the output as stable as possible against any variation of the input.

In addition, a couple of basic equations, derived previously must be taken into consideration, which describe the behavior of the Buck Converter.

Equation 268 shows the current in the inductor during TON, while during TOFF the current is equal to Equation 269.

EQUATION 268:

$$I_{L,\,on}(t) = \frac{(V_{DC} - V_{OUT})}{L_O} t$$

EQUATION 269:

$$I_{L,\,off}(t) = -\frac{V_{OUT}}{L_O} t$$

At Steady state, the current value at t = 0 equals the current value at t = T. This is represented in Figure 66, in the event of a Continuous operating mode. The output average current (IO, av) (see Equation 270) is also plotted.

EQUATION 270:

$$I_{O,\,av} = I_L(0) + \frac{I_{L,\,peak} - I_L(0)}{2}$$

So, what happens if the input voltage VDC increases? Since the up-slope of the inductor current is proportional to VDC, its slope will increase during TON.

With some delay, due to the LC low-pass filter, the output voltage will change (increase), and with some additional delay introduced by the EA, the VX signal will decrease. Therefore, the duty cycle of VCTRL will then be smaller (see Figure 65). This will reduce the TON time, reducing as a consequence VOUT and so, after some time, the output will again be at the nominal value, with a shorter duty cycle. Note that only the slope of IL during TON changes. The slope during TOFF, in the new Steady state condition, must be equal to the original one, since the system is keeping VOUT constant.

Figure 67 presents the inductor current before the change in VDC (dashed line) and after the transients have settled down in a new Steady state (solid line). The initial and final current values (at t = 0 and t = T) are lower, but at the same time the peak (point B) is higher. The average current (IO, av) has not changed as it was expected since the average output voltage has not changed. Of course, point B corresponds to a shorter on period (TON).

FIGURE 66: INDUCTOR CURRENT IN CONTINUOUS MODE

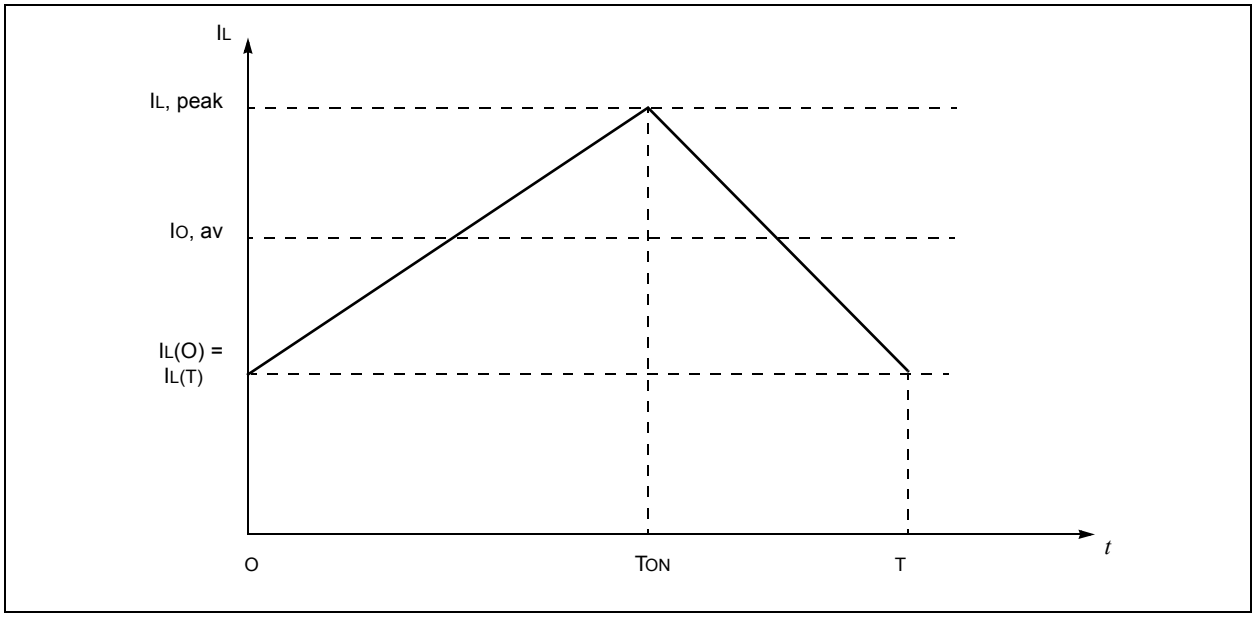


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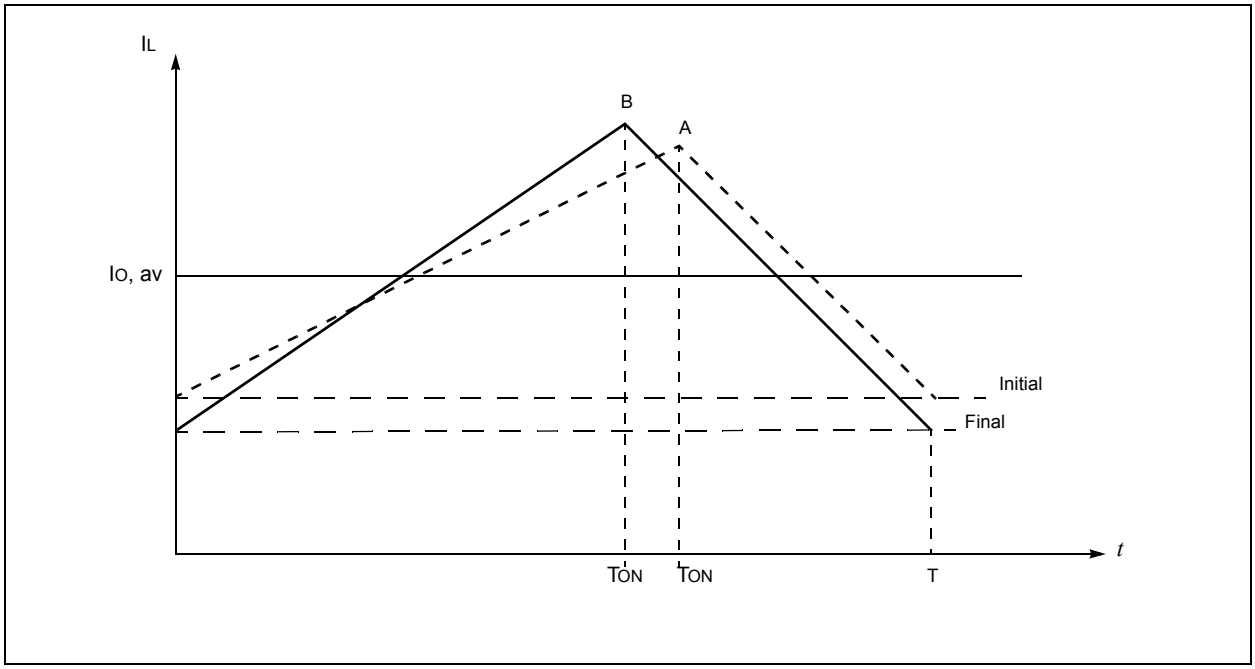
FIGURE 67: VOLTAGE MODE CONTROL - LINE REGULATION



LOAD REGULATION

The question now is: what happens if the load changes?

For example, if the R_O value changes by diminishing, at the very beginning (because of delays in the system) the output current will remain as before. This means that the output voltage will decrease only slightly. As a consequence, referring again to Figure 64 and Figure 65, the V_X signal will be higher and the duty cycle will increase. The behavior of the system can be analyzed using Figure 68, which again represents the inductor currents, before (dashed line) and after (solid line) the load change. This time both slopes, during T_{ON} and T_{OFF}, will remain the same, since the input voltage has not changed and the output voltage is kept constant by the loop itself.

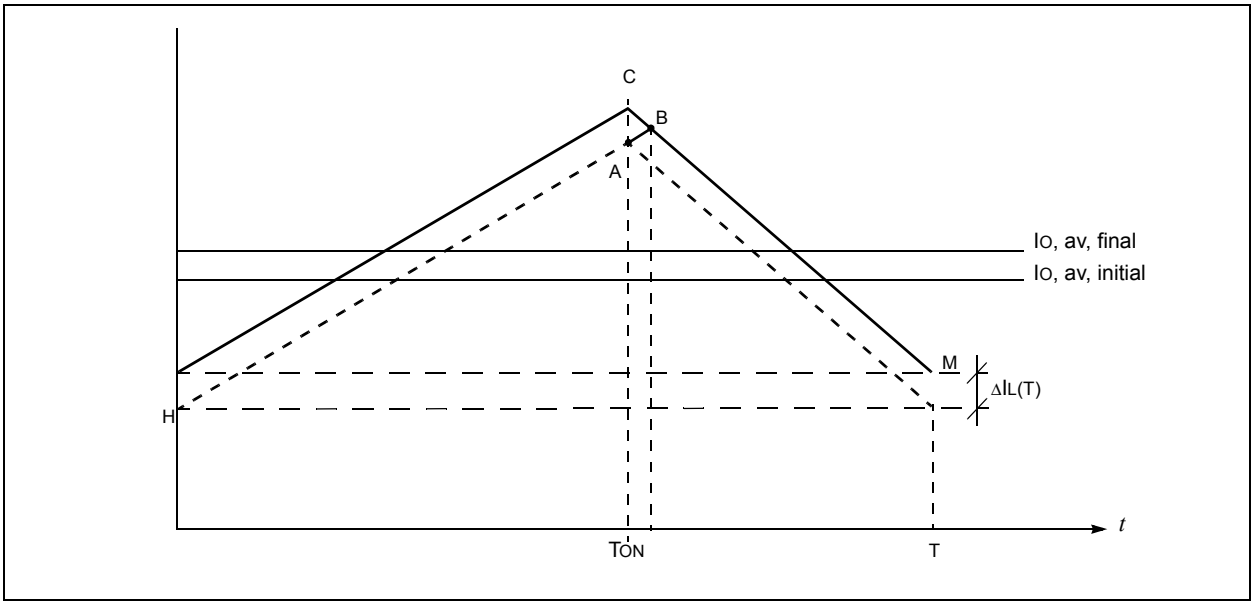
At the beginning, since V_X increases, the duty cycle will increase, moving from the original point A to point B. This means that the current at the end of the PWM period (point M, current at t = T) will be a bit larger than the initial current (point H, current at t = 0). The effect is that at the end of each PWM period, the current step is greater than zero, as shown in Equation 271.

EQUATION 271:

$$\Delta I_L(t) = I_L(T) - I_L(0)$$

When the transient ends, the loop has managed to bring the output voltage V_{OUT} back to its nominal value and consequently, the duty cycle is back to its initial value (there was no change in input voltage V_{DC}). This means that, in Figure 68, point B has moved to point C, in the new Steady state. The output average current has correspondingly increased from I_O, av, initial to I_O, av, final, as it was supposed to do since the load R_O has diminished.

FIGURE 68: VOLTAGE MODE CONTROL - LOAD REGULATION



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ADVANTAGES AND DISADVANTAGES OF VOLTAGE MODE

As is clearly seen from the previous explanation, the implementation of a voltage mode control is quite straightforward. The mechanisms of line and load regulation are also quite easy to understand. This is certainly one of the main advantages of this approach. Moreover, large amplitude signals are usually being dealt with, which is a benefit because of their good noise margin.

The key disadvantage of this mode is the delay, which is always added in reacting to any change of operating conditions. A change in V_{DC} is only detected because of its influence on the output voltage, so that from the original event (change in V_{DC}), detection makes it necessary to wait for the group delay of the low-pass filter. Moreover, once the change in output is detected, an additional delay is introduced by the EA. All of these delays must be taken into account; otherwise, a system is built that is not functional.

A change in the load is immediately detected, but again, there is a delay introduced by the EA before the countermeasure can be effective on the switch timing.

Current Mode

The current mode has been introduced to solve the disadvantages of the voltage control and, specifically, to reduce the reaction time of the system.

It also has some very specific advantages when needing to keep the current flowing into an inductor/transformer winding under control. A typical example application where the current mode is efficiently used is a PFC, which is a circuit whose task is to force the current drawn from the AC voltage source to be sinusoidal. In this case, the current mode control directly operates on the variable (current) of interest.

As seen in Figure 69, a current mode implementation has in reality two loops: one external controlling the output voltage (like the one studied in the previous paragraph) and the second one (internal) controlling the inductor current. The basic idea of the current mode is to directly monitor the quantity that is more directly responsible for the power conversion. Moreover, controlling the current allows to have a much faster response time.

Referring to Figure 69, the EA as before, monitors the output voltage. Its output is used as a reference signal to a second amplifier that compares the peak current flowing into the inductor to the reference signal from the previous stage.

Remember that when switch Q is closed, the inductor current has a positive slope waveform (Figure 70). At the beginning of the PWM period (t0), the PWM output is set active and the inductor current continues to grow until the current reaches the value of V_X. When they match (t0 + T_{ON}), the PWM signal is reset and remains low until the next PWM period starts. This system keeps the peak inductor current under control. However, this is not the only possible approach, as will be seen later.

FIGURE 69: CURRENT MODE CONTROL LOOP

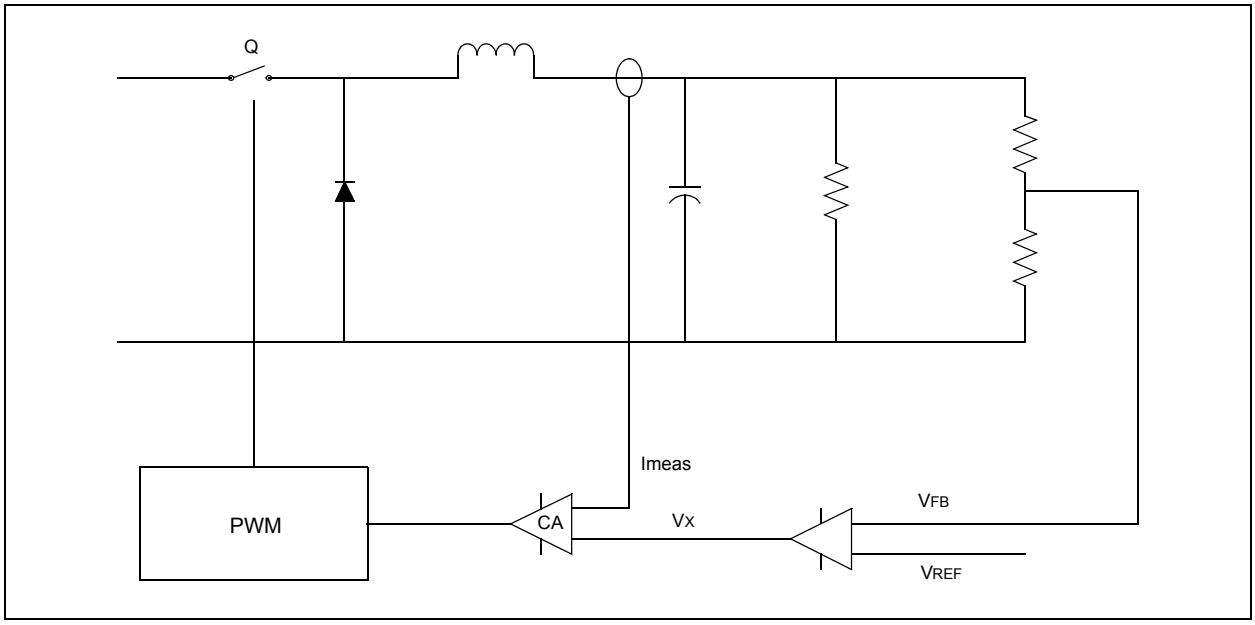
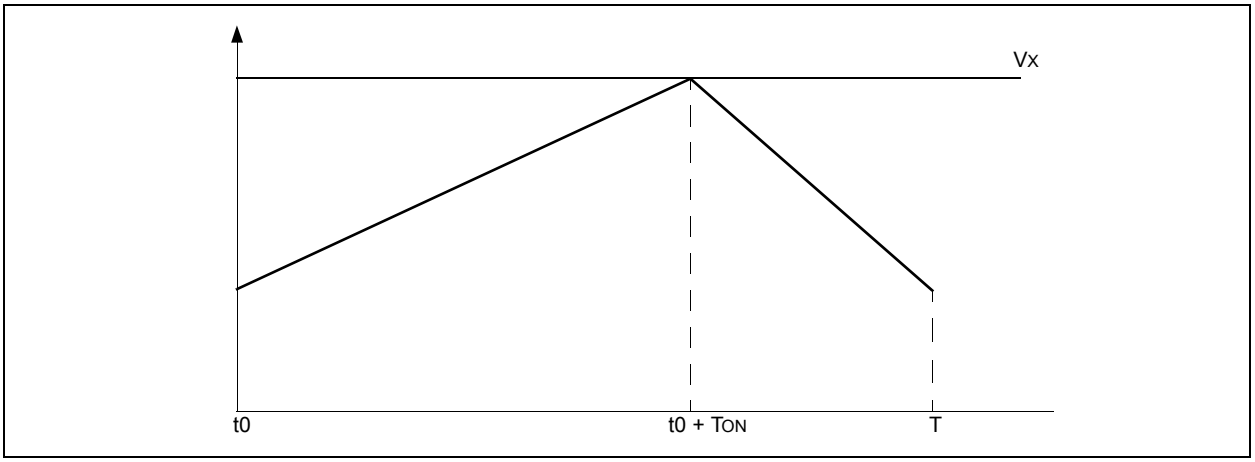


FIGURE 70: INDUCTOR CURRENT



The key point is that in the Buck Converter, the inductor current is also the output current, so that controlling it has the direct control of the quantity of relevance (VOUT). As previously seen in other systems, for instance, in a PFC, the inductor current is the input current and it should be shaped in a sinusoidal way.

In this configuration, the externally generated sawtooth signal that was used in the voltage mode control is replaced by the inductor current signal and its peak value is controlled (limited).

The system is relatively simple but also has a couple of drawbacks:

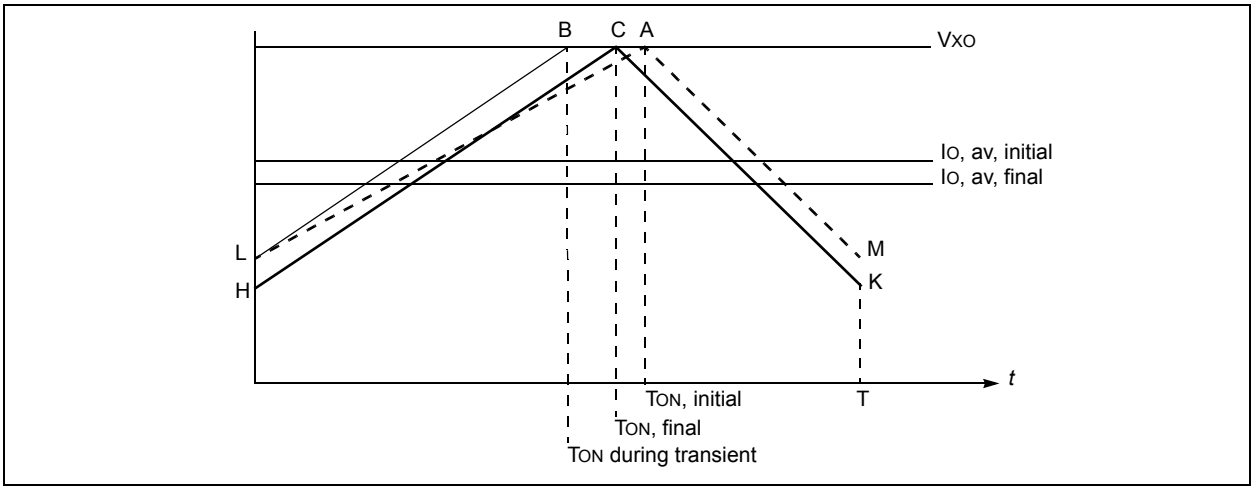
- It is preferred to be able to control the average output current, not the peak current (this is because the output voltage is proportional to the average current, not the peak current)
- There are some stability issues

LINE REGULATION

What happens when, being in Steady state, the input voltage changes? How does the system respond?

This behavior can be best understood by looking at Figure 71 (dashed lines represent the original Steady state). For example, as soon as VDC changes by increasing, the slope of the inductor current changes (see Equation 268). In this case it will increase. Meanwhile, the output has not yet changed, because of the delay of the output LOCO filter. Consequently, VFB has not changed and VX is the same as before. The loop is still imposing the same inductor peak current as before. This means that the up-slope current signal will cross the VX signal before, in point B compared to the Steady state point A (the transient behavior of the inductor current is shown with line from point L to point B). The duty cycle is reduced as it should be because of the increased input voltage. The final, new Steady state condition is point C, still on the VX line (the peak current is always the same), having steeper up-slope and the same down-slope. The important thing is that the reaction to the input voltage change is immediate, without having to wait for the change to propagate along the loop. In other words, the system response is much faster.

FIGURE 71: PEAK CURRENT MODE CONTROL - LINE REGULATION



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PROBLEMS

As seen in Figure 71, while the input voltage regulation works fine (an increase in V_{DC} brings about a reduction of the duty cycle), there is a drawback as seen in Equation 272. This is due to the fact that the peak voltage is being kept constant, while the output voltage V_{OUT} is proportional to the average inductor voltage.

EQUATION 272:

$$V_{OUT,\,av} = R_O I_{O,\,av}$$

However, as observed in Figure 71, the new condition is such that the inductor current initial and final values (points H and K) are lower than before (L and M). This means that the final average inductor (output) current is lower, as shown in Equation 273.

EQUATION 273:

$$I_{O,\,av,\,final} < I_{O,\,av,\,initial}$$

A lower current will develop a lower output voltage, which will be detected by the external voltage loop. In turn, it will try to increase the average (and peak) current. But the internal loop tries to keep the peak current constant. An oscillatory effect takes place and continues for some time.

Another subtle problem of the peak current mode is that the system is unstable for duty cycles greater than 0.5, which can be seen in Figure 72 and Figure 73.

FIGURE 72: PEAK CURRENT MODE CONTROL - D > 0.5

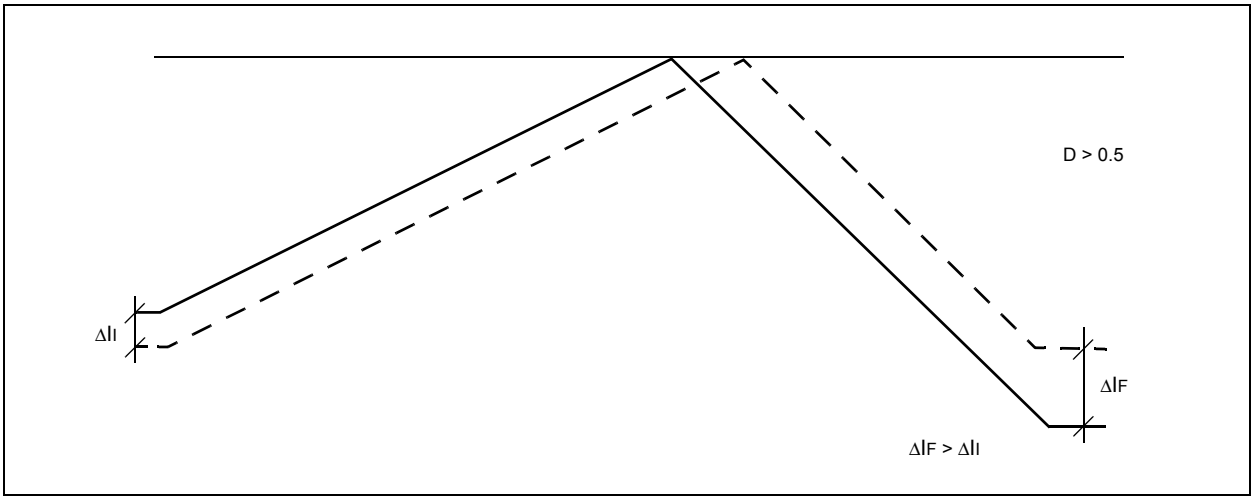
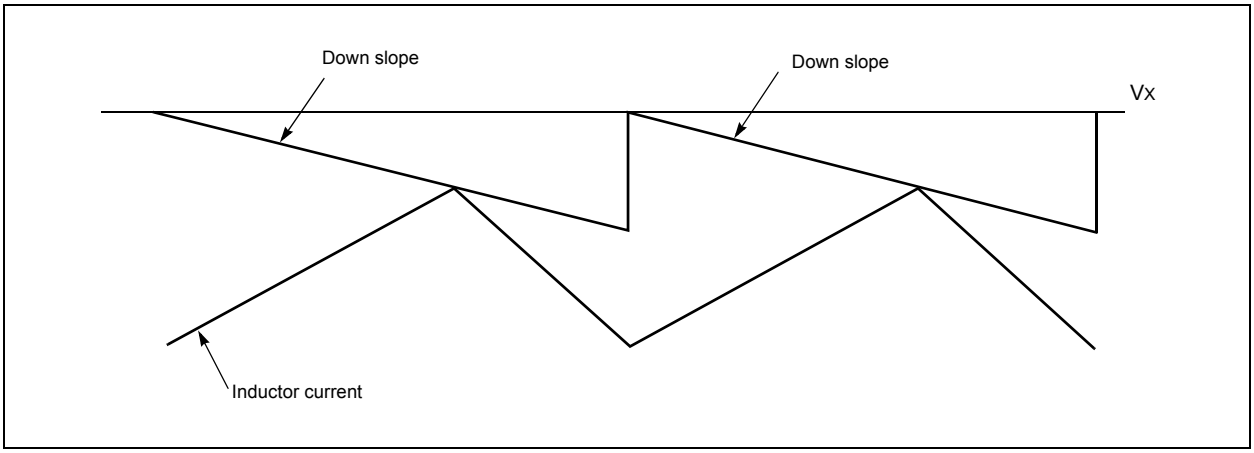


FIGURE 73: CURRENT MODE CONTROL - SLOPE COMPENSATION



As seen in Figure 72 when D < 0.5, at steady state, if for any reason there is a pertibation in the inductor current, at the end of the PWM period, the amplitude of the pertibation is reduced ($\Delta I_F < \Delta I_I$), so that after a number of PWM cycles, the system will be back at the initial condition. On the contrary, if the duty cycle is greater than 0.5 (Figure 73), the same current pertibation will be larger at the end of the period and will grow indefinitely, giving rise to an oscillatory behavior ($\Delta I_F > \Delta I_I$).

Without going into too many details, both problems can be easily corrected replacing the constant V_X peak current limit with a down slope signal that equals V_X at the beginning of each period, and which has a down slope proportional to half the current slope during T_{OFF} (Figure 73).

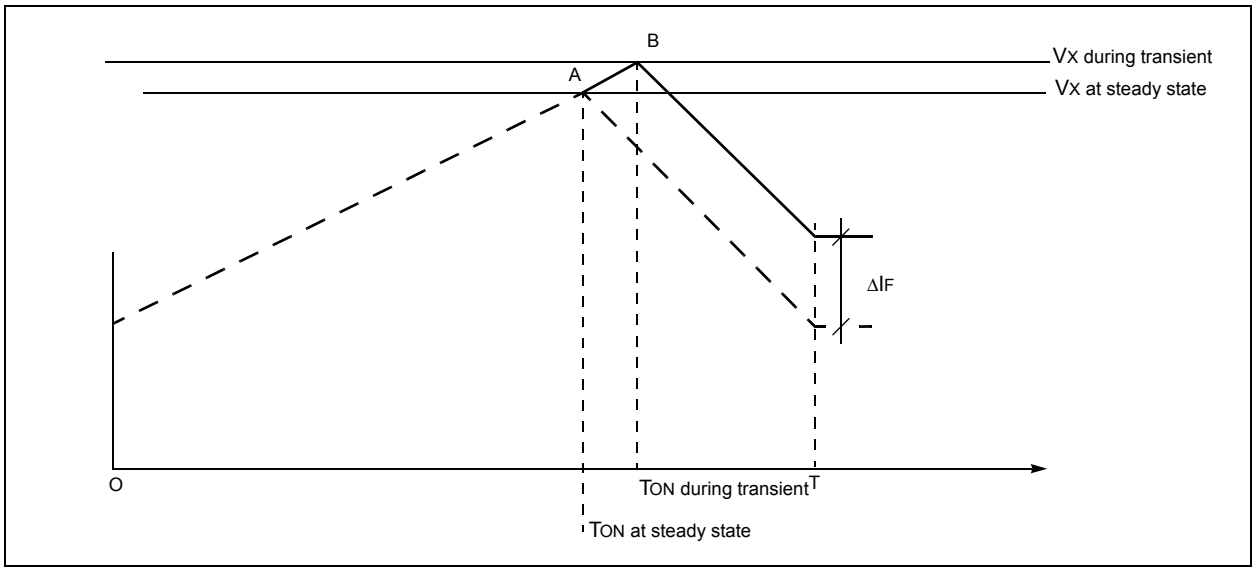
Load Compensation

What happens when the output load changes?

For example, if the output load changes by decreasing, the output voltage will momentarily decrease and consequently the V_X signal will be higher to compensate for it (see Figure 74).

The up slope signal will then last longer and will cross V_X at point B, instead of the original point A, and the duty cycle will correspondingly increase. This will cause the inductor current level to be higher at the end of the PWM period compared to its value at the beginning (ΔI_F, is extremely exaggerated in Figure 74 for clarity). This unbalance will remain while the average current increases to the new equilibrium value. At this point, the duty cycle is back to its initial value (no changes in input voltage V_{DC}) and the system has reached a new steady state.

FIGURE 74: PEAK CURRENT MODE CONTROL - LOAD COMPENSATION



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Other Current Mode Techniques

The current mode previously described with some detail is not the only one available. The most obvious technique is one where the loop keeps the average (not the peak) output current constant. This is good, since the output voltage is proportional to the average output current.

In analog, the circuitry is a bit more complex since some kind of low-pass filter must be added to the current loop error amplifier. On the contrary, from a digital point of view, the technique is very easy since the average value of the current can be directly sampled and converted by the ADC if the sampling trigger is at half the period of the duty cycle. A special register in the dsPIC DSC device allows the conversion to start operation exactly at this point (see Figure 75).

A second possibility is to implement the so-called hysteretic control, where the current value can change between two values, which can be either fixed or dynamically computed by the dsPIC DSC device itself. In this case, the internal comparators and their threshold set by DACs allow implement of the system without any intervention from the CPU (see Figure 76).

As seen in Figure 76, as soon as the decreasing inductor current reaches threshold one, the current limit event in the dsPIC DSC device takes place, and associated with it is the forcing high of the pin. As a consequence, current starts rising. As soon as it reaches the second threshold, the fault event takes place and the output pin is reset, current decreases, and so on. The frequency of the generated PWM is not constant, but it will change as a function of line and load (remember that the up slope is proportional to V_{IN} and the down slope is proportional to V_{OUT}).

FIGURE 75: ADC TRIGGER GENERATED BY PWM PERIPHERAL

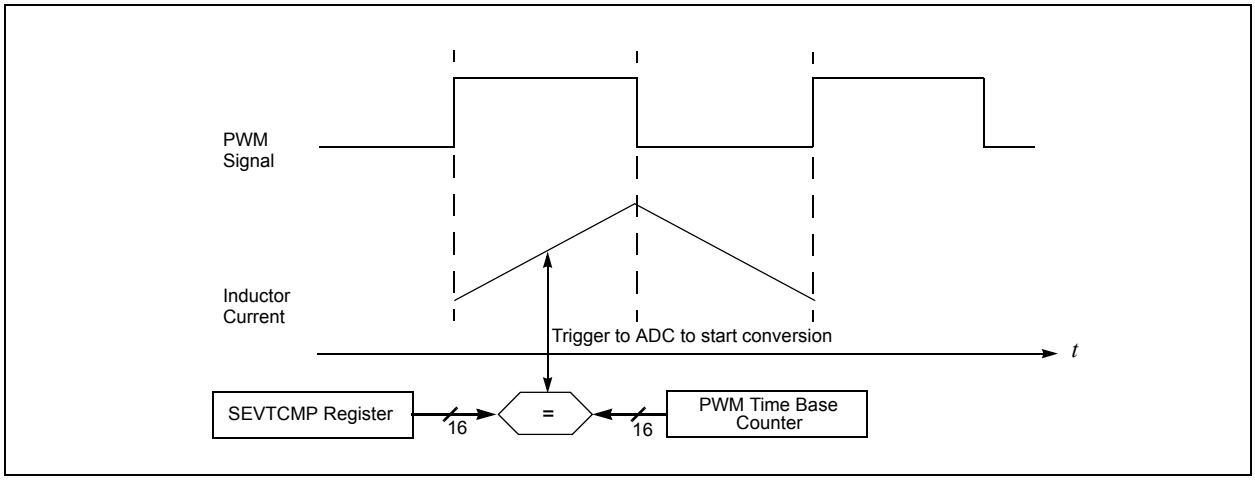
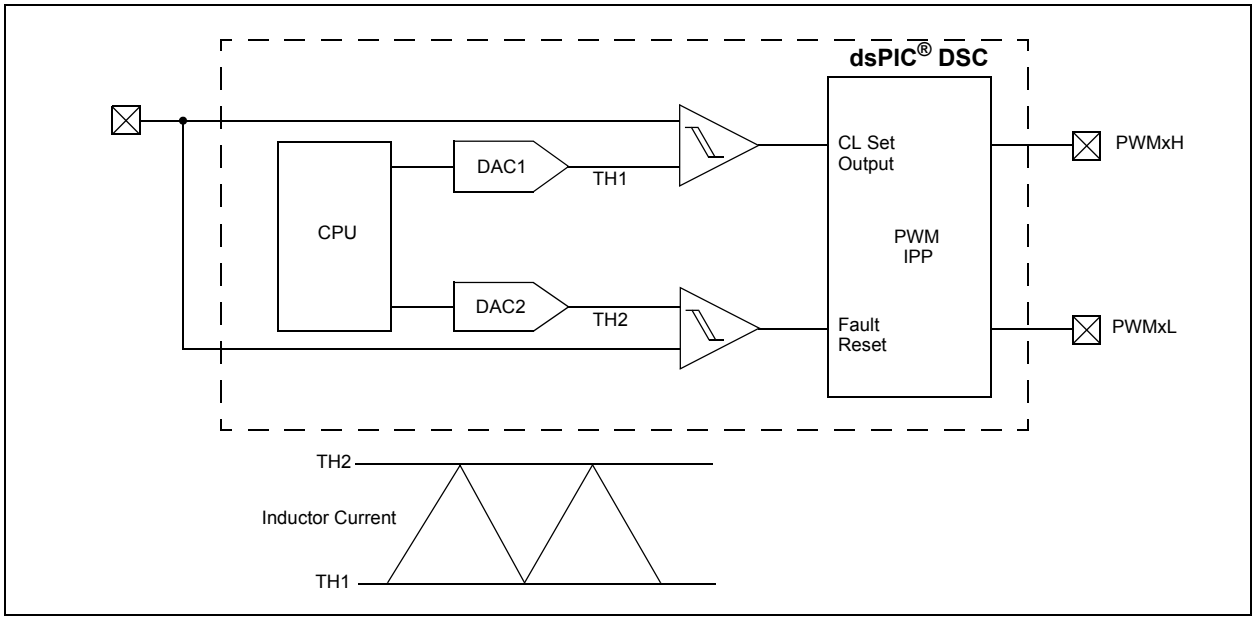


FIGURE 76: HYSTERETIC CONTROL IMPLEMENTATION WITH A dsPIC® DSC DEVICE



The internal comparators can also be used to implement a “constant on” time or a “constant off” time (see Figure 77 and Figure 78), where the match between the increasing inductor current and a preset threshold (DAC output) resets the PWM timer that controls the PWM period. The two control modes are essentially the same, the only difference being that the direct or inverted PWM output is considered.

FIGURE 77: “CONSTANT ON” TIME WAVEFORM

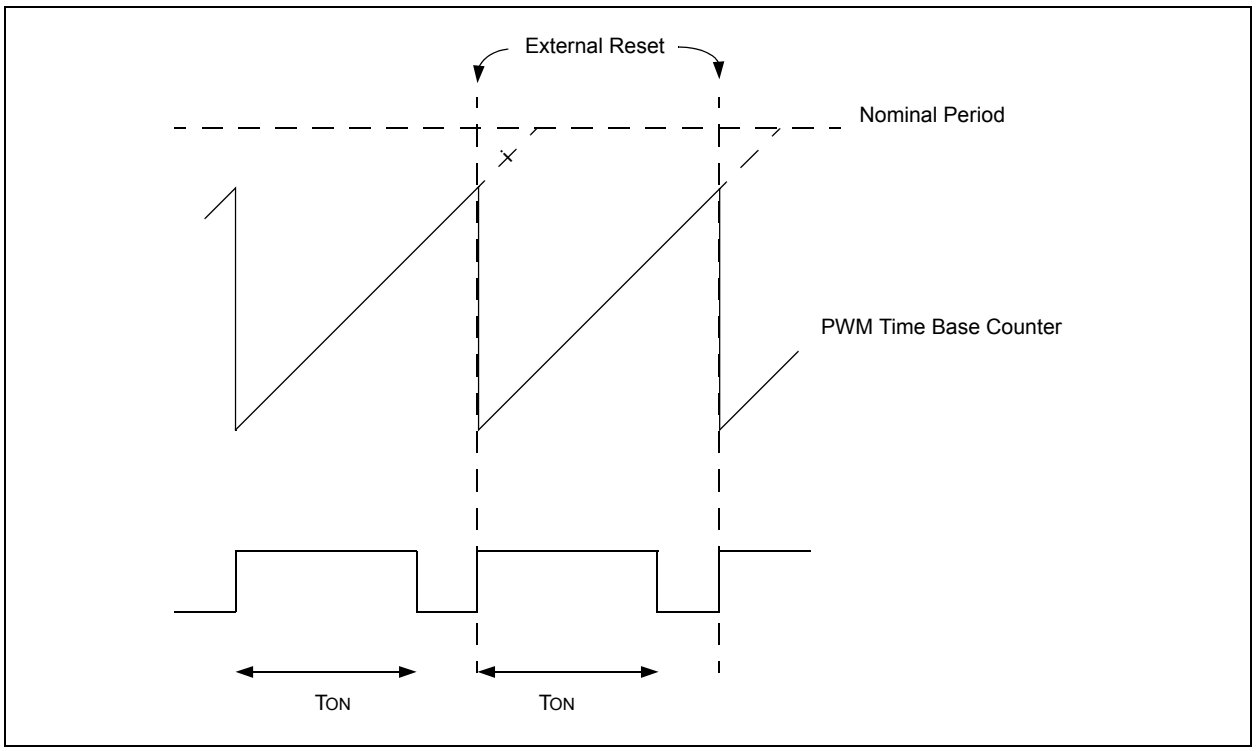
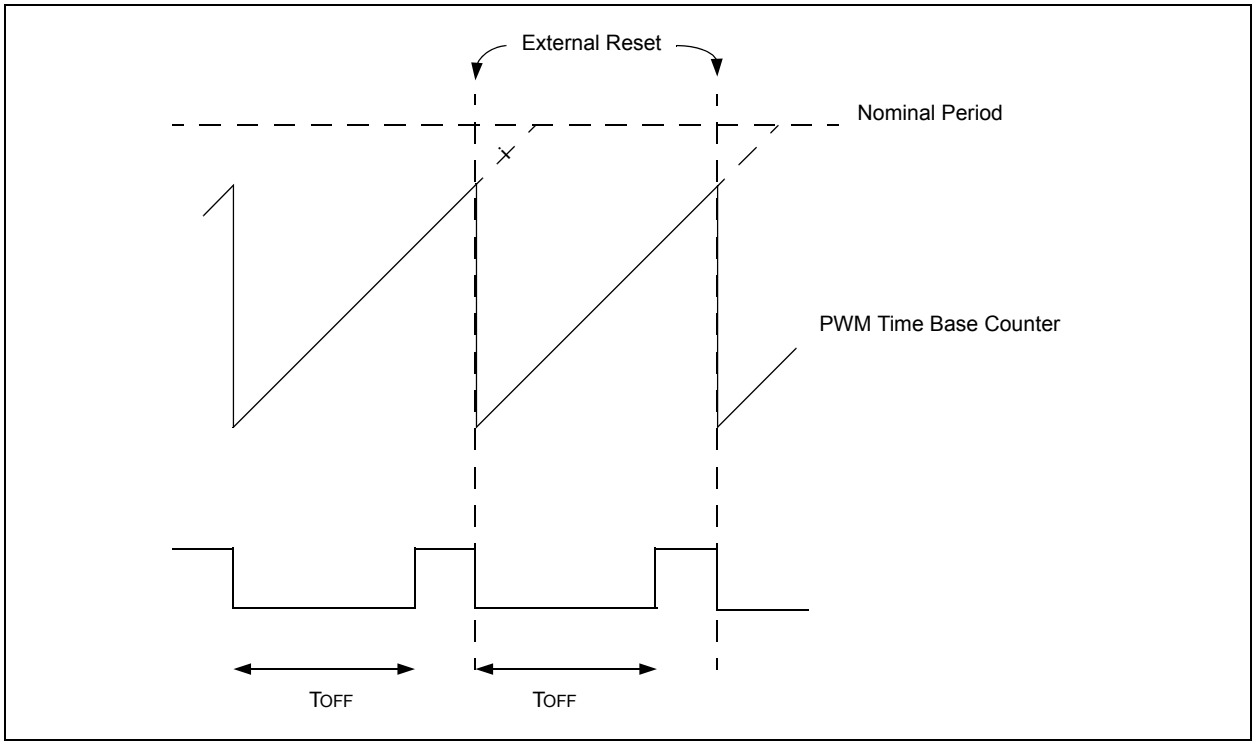


FIGURE 78: “CONSTANT OFF” TIME WAVEFORM



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Control Theory

Up to this point, feedback loops have been considered where the output VOUT is compared to a reference value, and the error signal is used to change some specific feature (i.e., the duty cycle) of the power modulator. This is a closed loop system and must be analyzed with control theory tools.

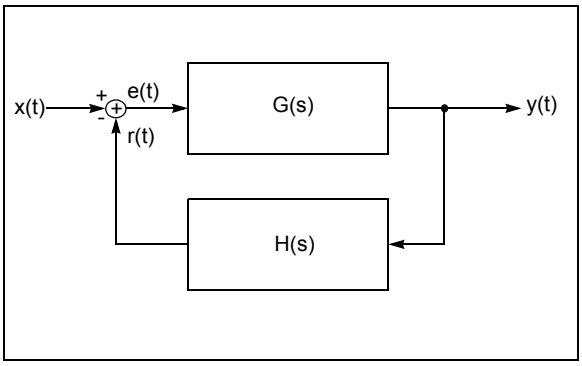
The problem here is that the system could become unstable if either the current or voltage loop is used. In the general circuit, like the one in Figure 63 and Figure 69, the behavior of any block, excluding EA and CA can be known or computed. The design challenge is then to select the EA (and CA) transfer function to be sure the system is stable.

Before analyzing the Buck Converter circuit from a control theory perspective, some basic relationships must be formulated.

FEEDBACK LOOPS

Figure 79 presents a general control loop where G(s) and H(s) are the transfer functions of the two blocks (Laplace transforms of the impulse responses). x(t) is the input signal to the system; y(t) is the output; y(t) is also fed back to the input through H(s) block, whose output, r(t) is subtracted from the input x(t) to form the error signal e(t).

FIGURE 79: CONTROL LOOP



With computation, as shown by Equation 274, the input/output relationship can be derived, which is called closed loop gain (GCL(s)).

EQUATION 274:

$$G_{CL}(s) = \frac{G(s)}{1 + G(s)H(s)}$$

GCL(s) can be simplified using Equation 275.

EQUATION 275:

$$G_{CL}(s) = \begin{cases} \frac{1}{H(s)} & if \ |G(s)| >> 1 \\ G(s) & if \ |G(s)| << 1 \end{cases}$$

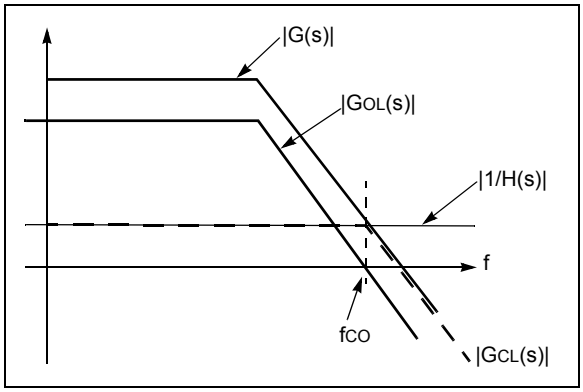
Equation 276 shows the product of the two terms, G(s) and H(s), which is called open loop gain (GOL(s)).

EQUATION 276:

$$G_{OL}(s) = G(s)H(s)$$

Figure 80 represents G(s), H(s), GOL(s) and GCL(s). Remember that the plot is in log scale, so that multiplications correspond to sums and divisions correspond to subtractions.

FIGURE 80: CONTROL LOOP FUNCTIONS



Some mathematics to understand the plot are provided in Equation 277.

EQUATION 277:

$$G_{OL}(s) = G(s)H(s) \Rightarrow$$

$$\left|G_{OL}(s)\right|_{dB} = \left|G(s)\right|_{dB} + \left|H(s)\right|_{dB} = \left|G(s)\right|_{dB} - \left|\frac{1}{H(s)}\right|_{dB}$$

Consequently in this case, where H(s) = const, the open loop gain is simply obtained moving the G(s) plot rigidly toward the y-axis an amount equal to |1/Hs)|.

The problem now is: how can it be determined whether a system represented by Equation 274 is stable? And, what are the conditions that make a system stable?

Both questions can be answered with an approximate analysis.

The key point in control theory is that determining if (and how well) a closed system, like the one in Figure 79 is stable, can be accomplished just by looking at the behavior of the open loop gain (GOL(s)).

In Equation 274, the denominator must be prevented from becoming zero; otherwise, GCL would be infinitely large as shown in Equation 278.

EQUATION 278:

$$1 + G(s)H(s) \neq 0$$

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Solving Equation 278 results in Equation 279.

EQUATION 279:

$$The\ phase\ of \lceil G(s)H(s) \rceil\ must\ be \neq 180° where |G(s)H(s)| = 1$$

Referring to Figure 80, it is recognized that the point where |GOL(s)| = |G(s)H(s)| = 1 is fCO (crossover frequency). The phase at this frequency must be different from 180°. To be on the safe side, a phase of about 130°-140° is requested, or correspondingly a phase margin = (180° - phase at fCO) ≥ 45°.

With some simplifications, the criteria of stability can be stated as:

- The slope of GOL(s) at fCO must be -20 dB/decade and,
- The phase margin at fCO must be at least 45°.

These are only sufficient conditions for the stability, but are widely used because of their simplicity.

The meaning of the second criteria should be clear from the previous discussion. The first criteria can be interpreted this way.

By looking at the GOL(s) transfer function, it is observed that it is a ratio of polynomials. With some effort (at this point it does not really matter how difficult it can be), the GOL(s) numerator and denominator can be transformed into the product of first order terms (eventually complex numbers), as shown in Equation 280.

EQUATION 280:

$$G_{OL}(s) = \frac{\prod_{k=1}^{N} (s - z_k)}{\prod_{l=1}^{M} (s - p_l)}$$

Each term of the numerator is a zero, each term at the denominator is a pole. In normal conditions, like those encountered in power supply units, each zero contributes to the open loop gain phase with a +π/2 phase contribution, while each pole contributes with a –π/2 phase contribution. From the point of view of the loop gain, each zero gives place to a change in the slope of the gain itself of +20 dB/decade, while a pole gives a -20 dB/decade slope change. Therefore, the slope the GOL(s) criteria previously mentioned can be interpreted as in the nearby of the crossover frequency (fCO), the total contribution to the loop gain is similar to what a single pole system would provide.

POWER CONVERTER AND CONTROL THEORY

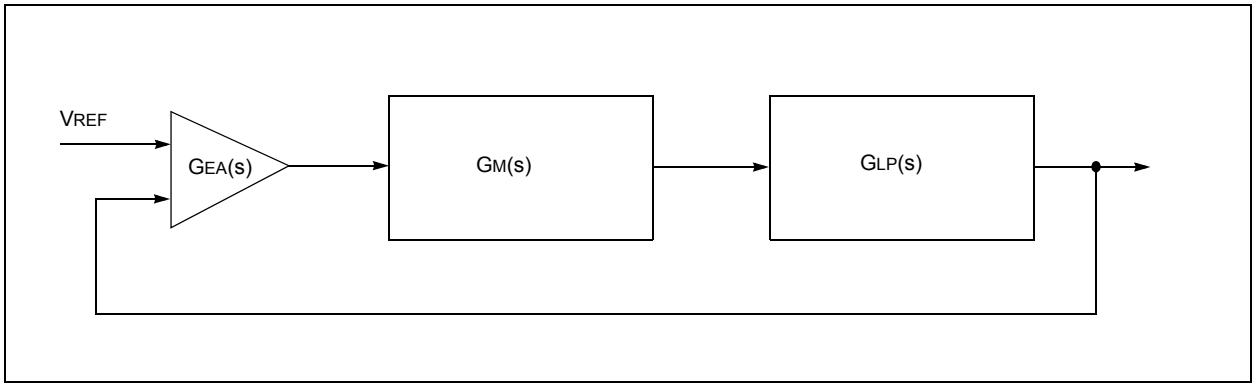
Now that you have a rough idea of the meaning of stability and the criteria to determine if a system is stable, refer back to the Buck Converter with a voltage mode control loop (Figure 63). It is imperative to match the converter functions to the general control theory block diagram and determine the transfer functions.

Therefore, Figure 63 can be redrawn as Figure 81, where G(s), the input to output transfer function, is made up of three blocks:

- GEA(s) is the error amplifier transfer function
- GM(s) is the transfer function of the PWM generator
- GLP(s) is the output low-pass filter transfer function.

H(s), the transfer function from the output to the input is absent, or better: H(s) = `1`.

FIGURE 81: BUCK CONVERTER VOLTAGE MODE LOOP



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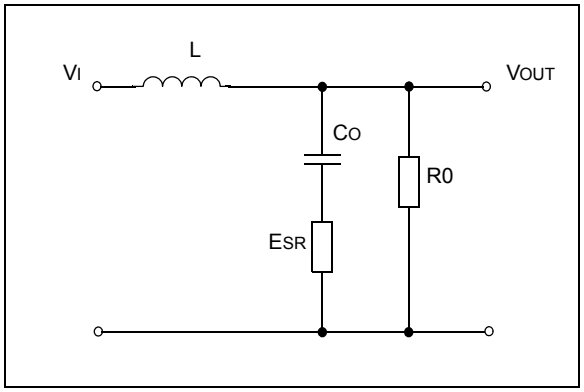
The GM(s) transfer function is probably not immediately intuitive. But think of it this way: if the input signal is a DC value with a small amplitude sinusoidal waveform ripple superimposed, the output will be a PWM signal whose duty cycle value follows the same sinusoidal law around the Steady state value. Simplistically, the input/output relationship is the ratio between the output duty cycle range and the input sinusoidal amplitude and the frequency is preserved. There are a few different techniques that can be used to mathematically determine the I/O relationship. Without going into such details the important thing is that as soon as the topology and the power system have been decided, GM(s) can be computed.

GLP(s) is somehow easier, and can be computed analytically, considering the low-pass filter in Figure 82, where the output capacitor ESR has also been taken into account.

FIGURE 82: BUCK CONVERTER OUTPUT STAGE



At this point, GM(s) and GLP(s) are known: the design effort consists in finding a function GEA(s) that makes the system stable according to the definition previously given. In an analog design, this translates into the computation of a few passive components in standard compensating networks, where an op amp is used. One such circuit is shown in Figure 83 and its transfer function is shown in Figure 84.

FIGURE 83: ERROR AMPLIFIER NETWORK

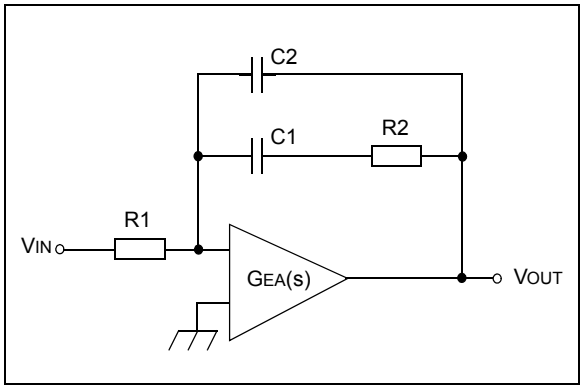
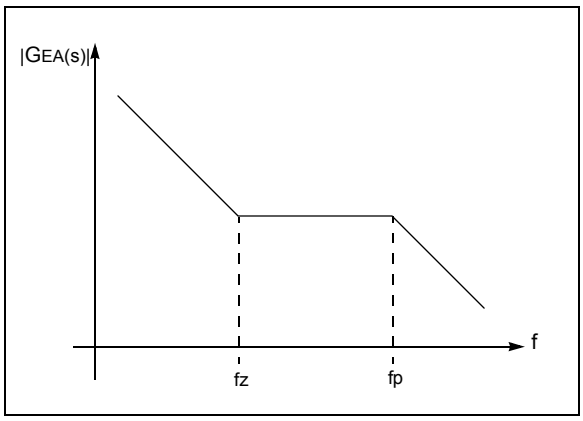


FIGURE 84: ERROR AMPLIFIER TRANSFER FUNCTION



Referring to the previous equations, GOL(s) = G(s)H(s) = GEA(s)GM(s)GLP(s), being H(s) = 1.

Working in dB, results in Equation 281.

EQUATION 281:

$$|G_{OL}(s)|_{dB} = |G_{EA}(s)|_{dB} + |G_M(s)|_{dB} + |G_{LP}(s)|_{dB}$$

known
known
unknown
unknown

The following details the preferred gain even if |GOL(s)| is not known:

- The lower the frequency, the higher the gain should be; this is because a very high gain at low frequencies gives place to small Steady state errors
- The higher the frequency, the smaller the gain should be to reduce the effects of high frequency noise
- In between frequencies it would be best to have a fairly constant gain

It can be concluded, the known and desired |GOL(s)| value can be stated, resulting in Equation 282.

EQUATION 282:

$$|G_{EA}(s)|_{dB} = |G_{OL}(s)|_{dB} - |G_M(s)|_{dB} - |G_{LP}(s)|_{dB}$$

In an analog implementation, a graphical solution can easily be found. In a less systematic approach, different capacitor values can be tested in the circuit of Figure 83 and Figure 84 until a satisfactory solution is found.

Digital Solutions

Until now, only the analog solutions (how the voltage and current mode loops can be implemented in analog) have been considered. This is because, for beginners, it is easier to understand the basic concepts in the analog domain first and then convert them to the digital world. On the contrary, many experienced converter designers have great experience in analog design and the presented material is the foundation upon which the digital approach is built on.

Of course, in a digital solution the passive power components will be used; what changes is the way the PWM is generated and how the feedback loop is implemented.

An overview of Microchip Switch Mode Power Supply devices follows, which provides an understanding of their architecture and the features they provide, which can be used to implement a Switch Mode Power Supply.

SWITCH MODE POWER SUPPLY (SMPS) dsPIC DSC DEVICES

Microchip's dsPIC DSC SMPS devices have been created specifically to aid designers with the implementation of digital switching systems. These devices are 16-bit processors based on the well established dsPIC30F and dsPIC33F family of devices, with three main building blocks:

- 16-bit MCU
- Digital Signal Processor core
- Intelligent Power Peripheral (IPP)

IPP is a superset of three peripherals: a PWM generator, a high-speed 10-bit analog-to-digital converter (ADC), and a high-speed comparator. Nothing new compared to many other processors? On the contrary, a lot of new features! The key points are:

- High performance of the peripherals
- High degree of interconnection between the three mentioned peripherals, that cooperate to the generation and control of the PWM output waveform without the direct intervention of the CPU

The PWM signals (up to four complimentary outputs) can have the same frequency, or each one can operate independently with a duty cycle resolution as low as 1.05 ns. The PWM can operate in nine different modes:

- Standard edge-aligned PWM
- Complementary PWM
- Push-pull PWM
- Multi-phase PWM
- Variable phase PWM
- Fixed off-time PWM
- Current reset PWM
- Current-limit PWM
- Independent time base PWM

The PWM can generate a set of triggers that will start the ADC operation, fault signals can stop the PWM operation, currents greater than a defined threshold in the internal comparators can inhibit the PWM outputs, and the PWM period counter can be reset by external signals to implement constant-off/-on outputs.

The high-speed 10-bit ADC can sample up to five signals at the same time and will always convert two input channels at a time (usually one current and one voltage). Multiple triggers can start the converter operation:

- Individual software trigger
- Global software trigger
- PWM Special Event Trigger
- PWM generators trigger
- Timer1 or Timer2 period match
- PWM generators current-limit ADC trigger
- PWM generators Fault ADC trigger

The comparators can be used to detect overcurrent, or as in some current mode loops, be used to detect when the inductor current has reached a preset value.

While the IPP takes care of the greater part of the generation and management of the PWM, ADC, and comparator signals, the CPU and its DSP engine have plenty of time to perform the computations required to close the control loop in a digital solution.

The 16-bit by 16-bit, high-speed multiplier and the 40-bit accumulators allow a very efficient implementation of even high-complexity control algorithms. The operations required to implement a digital loop are basically a sequence of multiply/accumulate instructions. The DSP core is capable of implementing such instructions in a very efficient way. The `MAC` instruction performs the following operations in one machine cycle (33 ns in dsPIC30F devices, 24 ns in dsPIC33F devices):

1. Multiply two values.
2. Accumulate the current multiply result to previous sums.
3. Update the registers containing the two factors with new values for the following `mac` operation.
4. Increment pointers so that they point to the values that will be used later.

Efficient usage of the memory allows implementation of fast accesses to locations in RAM (and in Flash) without reducing the overall speed of the processing unit. Specifically, one of the key problems in executing a `mac` operation is that while the multiply/accumulate computational part is performed, two new data must be fetched from the RAM to be ready for the next iteration. This means that it must be possible to make a read-access to RAM twice in one instruction cycle. Multiple solutions are available. Microchip's approach is to split (only for `mac` class instructions) RAM into two parts (X-RAM and Y-RAM) and duplicate the address and data

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bus and the address generating hardware. Two paths are thus available through which two new factors can be fetched simultaneously.

To complete a control loop implementation, some additional work is needed to set up initial conditions and usually, to check that the results are within a specified range; however, a full control loop computation is normally performed in 1 to 2 microseconds.

THE PID

In both the voltage and current mode control loops, in the analog solution, the objective was to design the transfer function of the error amplifier ($G_{EA}(s)$) to make the system stable. A similar design objective is to be reached in the digital design.

A very commonly used building block is the PID (proportional, integrative, derivative). It is normally used also in the analog domain, and is found to be a very easy and useful application in the digital domain also.

As it can be guessed from its name, a PID is made of three basic blocks whose outputs are:

- Proportional to the input
- The integral of the input
- The derivative of the input

Although there are a number of ways these blocks can be interconnected, the most traditional technique will be investigated, where the three blocks are connected in parallel, as shown in Figure 85.

Figure 85 also shows how the PID is inserted in the block diagram representing a system. The goal of the PID block is to generate an output u(t) that drives the system at hand (the “PLANT”) so that its output [y(t)] matches a reference signal [x(t)]. The input to the PID is the error between the reference signal (ideal or desired behavior of the PLANT) and the real output behavior. Obviously, the target is to operate such that an error that is as close to zero as possible results.

Comparing Figure 81 and Figure 85 it is recognized that G_{EA} transforms in the PID controller, while the PLANT is the product of $G_M(s)G_{LP}(s)$.

In the following, starting from the description of a PID in the analog domain, it will be transformed into the equivalent digital PID.

For Figure 85, the equation that describes the behavior in the continuous time domain is shown in Equation 283.

EQUATION 283:

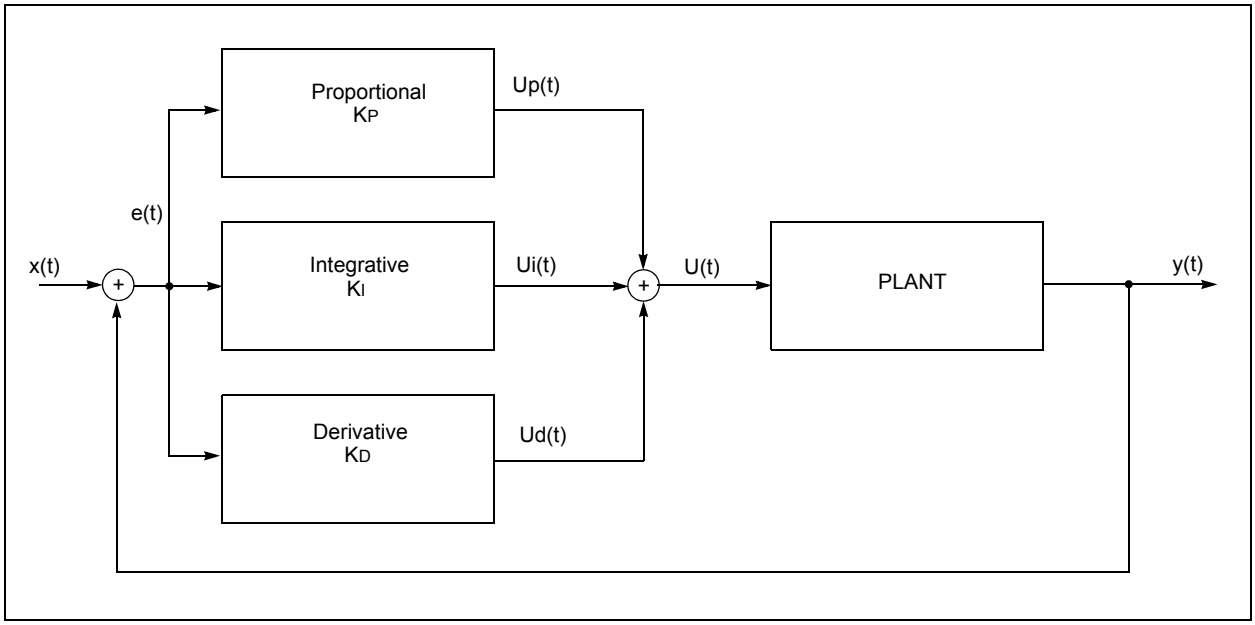
$$u(t) = K_P e(t) + K_I \int e(t)dt + K_D \frac{de(t)}{dt}$$

And its transfer function is (Laplace transform of the impulse response) shown in Equation 284.

EQUATION 284:

$$U(s) = K_P + \frac{K_I}{s} + K_D s = \frac{K_D s^2 + K_P s + K_I}{s}$$

FIGURE 85: GENERIC SYSTEM CONTROLLED BY A PID



As shown in Figure 86, there are two zeros and one pole at the origin. A high gain at low frequency is preferred to reduce DC errors, while a high gain at high frequency should be avoided (noise and spurious signals would be enhanced). This is why very often the transfer function is slightly changed to add a second pole (fp2, dashed transfer function).

The next step is to transform the analog PID and its equations in the discrete time version. To do that, a mapping from the s-domain to the z-domain must be performed using the Equation 285.

EQUATION 285:

$$s \rightarrow \frac{1 - z^{-1}}{T}$$

where T is the sampling period

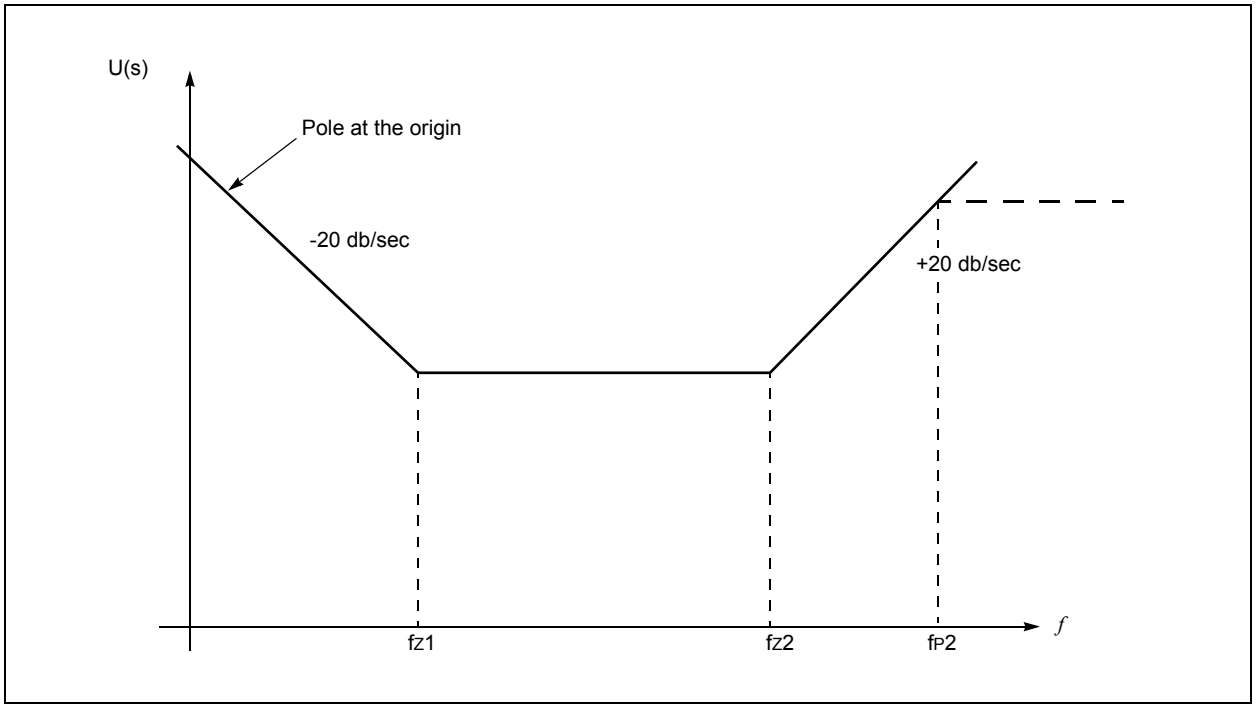
The z-domain is the most useful domain where sampled signals can be analyzed and systems synthesized. This is the discrete systems counterpart of the Laplace transform. It is easy to move from the time domain to the z-domain and vice versa through a transformation called Z-transform. One of the most notable features of the Z-transform is that a rational transfer function in s transforms in a rational transfer function in z^{-1}. This means that, starting from an analog transfer function like the one in Equation 280, a transfer function is obtained in the digital domain which strictly resembles it, as shown in Equation 286.

EQUATION 286:

$$H(z) = \frac{A \prod_{r=1}^{N} (1 - c_r z^{-1})}{\prod_{k=1}^{M} (1 - d_k z^{-1})}$$

There are a few possible variable transformations like the one in Equation 285 that maps the s-domain to the z-domain. Each transformation has different characteristics of how the two domains map to each other; however, the details are beyond the scope of this application note.

FIGURE 86: ANALOG PID TRANSFER FUNCTION



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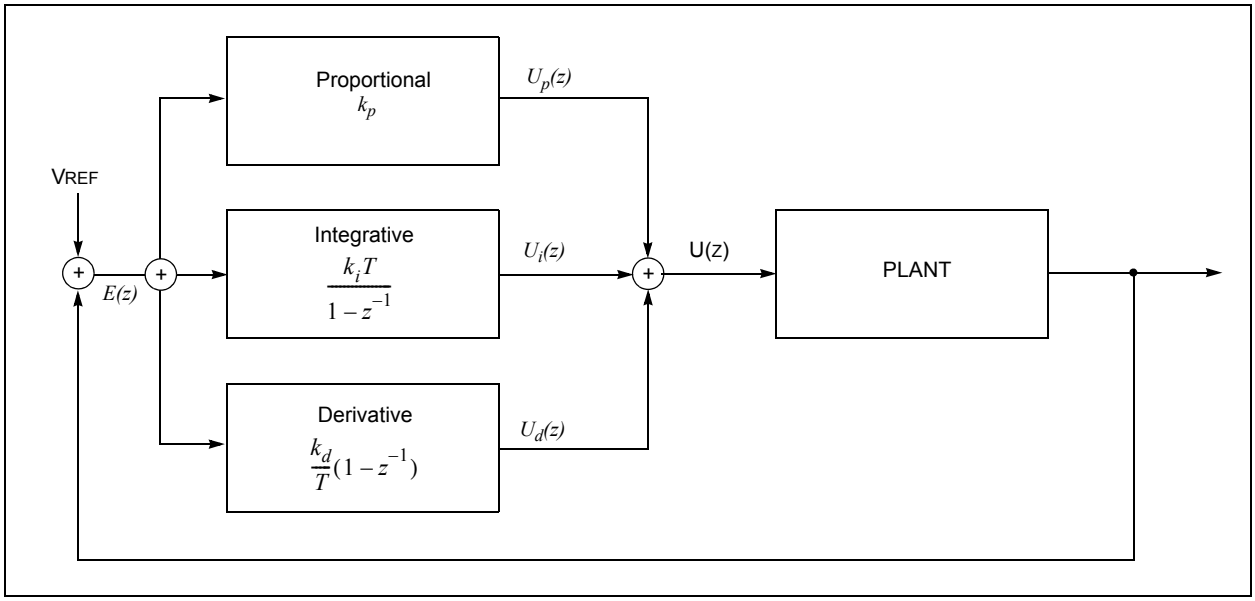
The block diagram now is as shown in Figure 87.

FIGURE 87: GENERIC SYSTEM CONTROLLED BY A DIGITAL PID



Using the mathematics shown in Equation 287, the transfer function in the z-domain can easily be obtained.

EQUATION 287:

$$U_P(z) = k_p E(z)$$

$$U_i(z) = \frac{k_i T}{1-z^{-1}} E(z)$$

$$U_d(z) = \frac{k_d}{T}(1-z^{-1})E(z) \Rightarrow$$

$$U(z) = \left[k_p + \frac{k_i T}{1-z^{-1}} + \frac{k_d}{T}(1-z^{-1})\right]E(z)$$

$$U(z) = \frac{(k_p T + k_i T^2 + k_d) - (k_p T + 2k_d)z^{-1} + k_d z^{-2}}{T(1-z^{-1})} E(z) \Rightarrow$$

$$U(z)(1-z^{-1}) = [K_A + K_B z^{-1} + K_C z^{-2}]E(z)$$

where

$$K_A = k_P + k_i T + \frac{k_d}{T}; K_B = -\left(k_p + 2\frac{k_d}{T}\right); K_C = \frac{k_d}{T}$$

The results are shown in Equation 288.

EQUATION 288:

$$U(z)(1-z^{-1}) = [K_A + K_B z^{-1} + K_C z^{-2}]E(z)$$

Going back to the time domain (performing the inverse Z-transform) is shown in Equation 289.

EQUATION 289:

$$u(n) = u(n-1) + K_A e(n) + K_B e(n-1) + K_C e(n-2) \Rightarrow$$

$$u(n) = u(n-1) + (k_p + k_i + k_d)e(n) + -(k_p + 2k_d)e(n-1) + k_d e(n-2)$$

The meaning of such an expression is that the current value of the output [u(n)] (in this case the duty cycle of the PWM) is computed from the value of the output at the previous instant in time [u(n - 1)], plus the current error times a coefficient (K_A), plus the error from previous step times another coefficient (K_B), plus the error from two steps ago, times a third coefficient (K_C).

This is the discrete time domain equation the dsPIC DSC device is requested to calculate. Note that this operation is performed at maximum, once per PWM period, T.

The terms in Equation 289 can be rearranged, as shown in Equation 290.

EQUATION 290:

$$\begin{aligned} u(n) &= \\ &+ u(n-1) + \\ &+ k_p[e(n) - e(n-1)] + \\ &+ k_i[e(n)] + \\ &+ k_d[e(n) - 2e(n-1) + e(n-2)] \end{aligned}$$

A few comments regarding Equation 290:

- The proportional contribution depends on the difference between the current error and the previous error.
- The integrative contribution depends on the current error.
- The derivative contribution depends on the increment of the error, which can be rewritten as Equation 291.

1. If all errors are '0', u(n) = u(n - 1).
2. If there is a constant error:
   a) The proportional contribution is '0'.
   b) The integrative part presents a non-zero contribution.
   c) The derivative part presents a zero contribution.
3. If only K_P is present (K_I and K_D = 0) when the current error is very close to the previous error, u(n) no longer changes. This explains the residual error received in this condition. This residual error then depends also on the resolution being used in the ADC and the computations.
4. If only K_I is present, there is always a contribution, even when the e(n) is constant. Again, the total residual error depends on the ADC and computations resolution.

EQUATION 291:

$$[e(n) - 2e(n-1) + e(n-2)] = [e(n) - e(n-1)] - [e(n-1) - e(n-2)] = \Delta e_{n-1,\,n} - \Delta e_{n-2,\,n-1}$$

If starting from Equation 292, and nulling two out of three coefficients ($K_B = K_C = 0$), results in Equation 293, which means that in reality, a contribution is coming from all three building blocks.

EQUATION 292:

$$u(n) = u(n-1) + K_A e(n) + K_B e(n-1) + K_C e(n-2)$$

EQUATION 293:

$$u(n) = u(n-1) + K_P e(n) + K_I e(n) + K_D e(n)$$

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Behavior of the PID

As can be assumed from Equation 284 and Equation 288, changing the values of K_P, K_I and K_D changes the behavior of the PID system, which changes its frequency response. It is not easy to see the relationship between the coefficients and the transfer function.

Referring to Equation 287 in the z-domain:

- If $K_P \neq 0$ and $K_I = K_D = 0$, the transfer function is a constant kp
- If $K_I \neq 0$ and $K_P = K_D = 0$, the transfer function has a zero in the origin and a pole in z = 1
- If $K_D \neq 0$, $K_P = K_I = 0$, the transfer function has one zero in z = 1 and one pole in the origin

The proportional term alone is capable of sensibly reducing the error, but it cannot nullify it, because (refer to Equation 290) when the error is almost constant (no matter its absolute value), but not zero, the output from the PID computation is constant. This means that the proportional term can sensibly reduce the error, but at the end a non-zero residual error always results, which cannot be completely eliminated by the proportional factor only.

To overcome this difficulty, the integral term representing the memory of the system, is capable of reducing the proportional residual error to zero. But the integral term should be used with caution, since it can bring the system to oscillation. The continuous accumulation of non-zero values can bring the system to saturate on one side, and then to the other side, and so on.

The derivative component helps the system to be reactive to sharp changes in the error value, since its contribution is proportional to the difference between current and previous errors.

Until now, nothing has been said about the values of the three coefficients, K_P, K_I and K_D. There are basically two methods that can be used to determine their values:

1. An empirical approach starting with $K_P \neq 0$, $K_I = K_D = 0$ and trimming the K_P value until a small residual error is received, and then incrementing K_I, until the system reaches an almost zero final error. And finally, the kd term is incremented to improve the performances of the system against step changes in the input error.

   Table 4 can be useful as a starting point to understand the relationship between the coefficients and the system behavior. It should be noted however, that this table is only a starting point since dissimilar systems behave differently.

TABLE 4: RELATIONSHIP BETWEEN COEFFICIENTS AND SYSTEM BEHAVIOR

Closed Loop Response	Rise Time	Overshoot	Settling Time	Steady State Error
K_P	Decrease	Increase	Small change	Decrease
K_I	Decrease	Increase	Increase	Eliminate
K_D	Small change	Decrease	Decrease	Small change

2. The second approach is more systematic and is known as the Ziegler/Nichols method. In this technique, start by incrementing the proportional gain (while the other coefficients are zero) until the system is at the edge of stability (step changes are applied to the reference value).

   In this condition the output is an oscillation with period T and the corresponding coefficient is K_P.

   The other coefficients are read from tables that can be found in Control Theory textbooks.

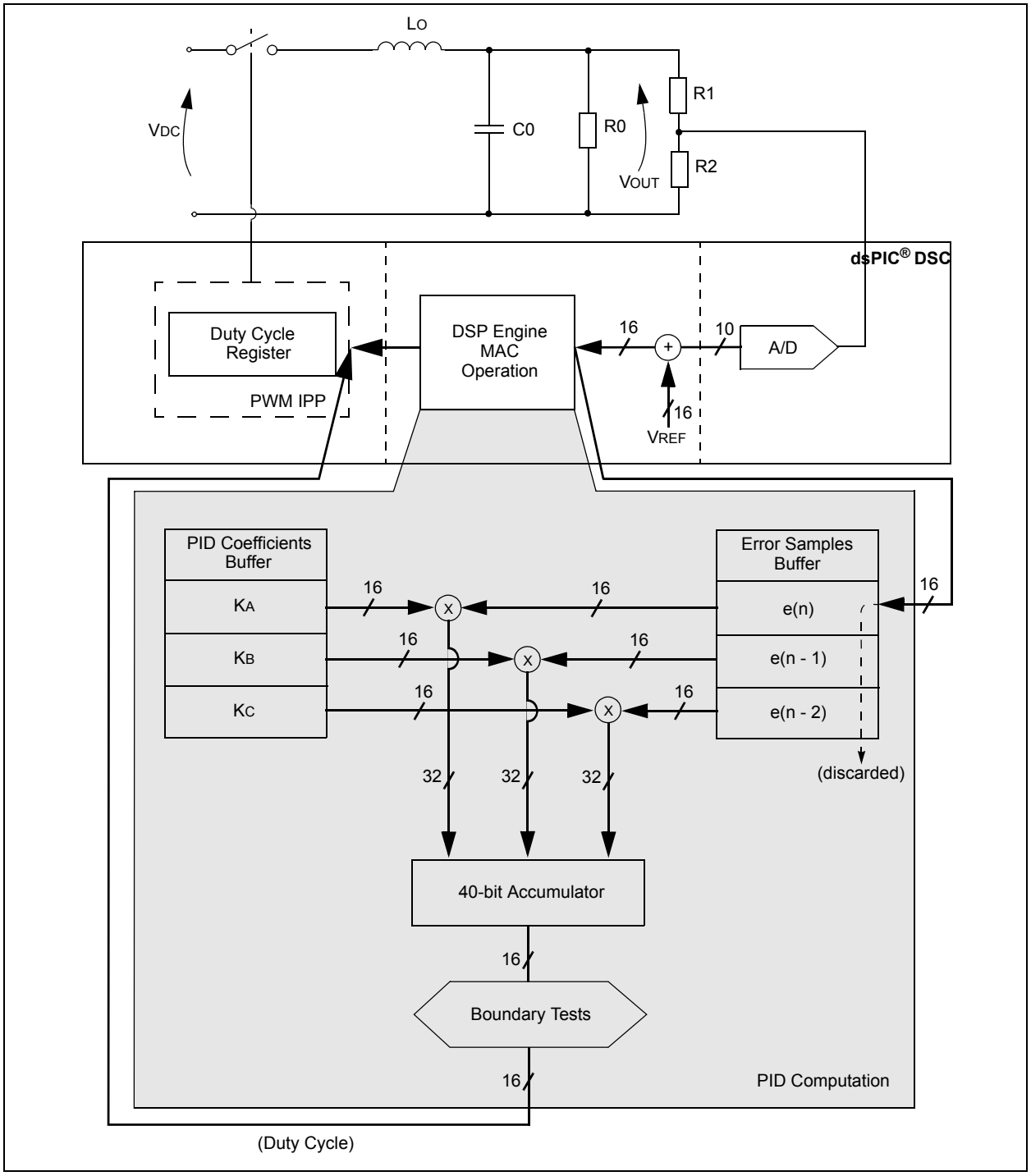
It should also be noted that the full PID equation is not often implemented. Often, only the proportional-integration part (P_I) is implemented. This depends on the system and system responses needed.

THE DIGITAL CONTROL LOOP WITH THE dsPIC DSC DEVICE

How does the PID fit into the DC-DC converter control loops? Thinking in “digital terms” Figure 63 is redrawn, as shown in Figure 87, where the sequence of operations is split between peripherals (hardware) of the SMPS parts and computations (firmware).

The feedback voltage is converted by the on-board ADC. In the dsPIC DSC device, a 10-bit value is returned; in reality it is known that the converter always converts two signals. This is intended to make available to the user, at the same time, a voltage and a current. In this implementation the current measurement is not used. Instead, a basic voltage control loop is implemented.

FIGURE 88: BUCK CONVERTER VOLTAGE MODE CONTROL LOOP IMPLEMENTED ON A dsPIC® DSC DEVICE



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The voltage from the ADC is subtracted from the reference signal and the resulting error is fed into the DSP engine to implement the PID.

The DSP engine implements Equation 289 exactly. The 40-bit accumulator in the DSP engine is used to accumulate the previous result values, which is value u(n) in Equation 294.

EQUATION 294:

$$u(n) = u(n-1) + K_A e(n) + K_B e(n-1) + K_C e(n-2)$$

The PID output (u(n)) is the current duty cycle value and is written into the IPP PWM duty cycle register.

This is almost all that is needed to implement a basic digital loop. In reality, some attention must be paid to the fact that, if the feedback voltage is very far from the reference voltage, large contributions to the duty cycle are accumulated. This results in the effect that the duty cycle can become too large, with a saturation effect. However, the PID can recover from this situation, but it is better to avoid it since the response time is greatly affected. A good practice is to clamp the duty cycle value to the PWM period (this is the meaning of "boundary tests" in Figure 87).

In the digital implementation of the control loop, there are some delays that must be taken into account:

- Analog-to-Digital sample/convert time
- PID computations time
- Some non-zero delay in the power component response
- Low-pass filter delay

All of these delays can be summed up as this time provides a boundary condition for the sampling frequency, in that it does not make any sense to sample the system faster that the reverse of this time. In other words, this is the required time for any change in the system to propagate along the loop.

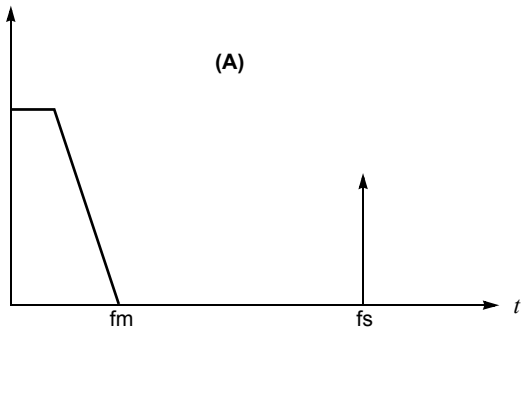
The reverse of this delay time determines the maximum sampling frequency that is reasonable to use in the system. Remembering the Nyquist sampling theorem, which states that to be able to reconstruct the original signal, the sampling frequency must be at least twice the maximum frequency of the signal of interest. This value of 2 is in fact only theoretical; in the real world it must be higher. Typical values can be from 6 to 10. Correspondingly, the maximum signal frequency that can be correctly operated upon is six to ten times smaller that the sampling frequency.

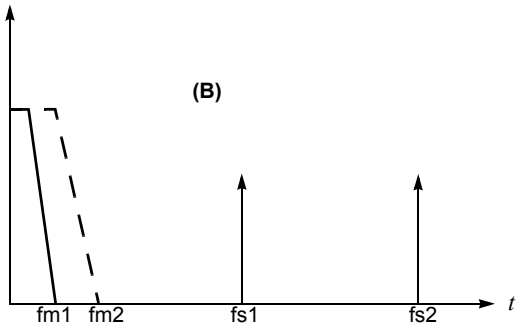
To clarify the concept, look at Figure 89(A), where fs is the sampling frequency, and fm is the maximum signal frequency value.

Optimally, trying to speed up as much as possible the operation of the digital loop to have the smallest possible delay in the loop, which is the maximum available sampling frequency. But why? The key point is that if there is a high sampling frequency, the maximum signal frequency is high; this means that the loop can easily respond to high frequency changes in the environmental conditions of the system. A graphical example is in Figure 89(B) for two different values of fs (fs1 < fs2). Keeping the same ratio between sampling frequency and maximum allowable signal frequency, results in a larger bandwidth with fs2 compared to fs1.

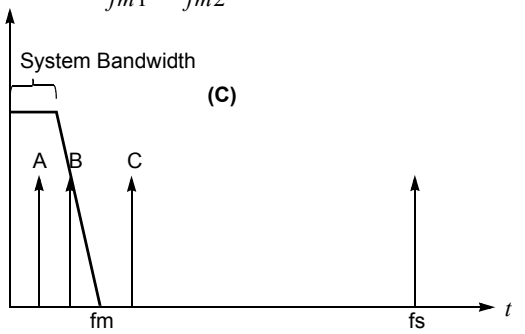
To further investigate the concept, suppose the input voltage V_{DC} has some ripple added, and this ripple is a sinusoid of frequency f_O. If the sinusoid frequency is small, the system can easily adapt the parameters of the converter to compensate for this sinusoidal change in the input and give a stable (without ripple) output. Now, continuously increment the sine wave frequency. Up to a certain value, the system will be able to follow it and compensate; but for some value of f the system will fail to correctly compensate up to a situation where the system delay will be longer than the period of the sinusoid and the loop will completely fail to control the output voltage (see Figure 89(C), with some simplifications).

FIGURE 89: SYSTEM LOOP BANDWIDTH AND SAMPLING FREQUENCY





$$\frac{fs1}{fm1} = \frac{fs2}{fm2} \Rightarrow fm2 > fm1$$



A, B and C represent the sinusoidal superimposed signal to the nominal duty cycle, where:

A = Signal is compensated by the system

B = Signal is only partially compensated

C = Signal is not compensated at all

One of the main differences between the analog and the digital loop, is that while in the former all values in time and amplitude are continuous, in the latter time and amplitude are both discretized. Time is discrete since, as seen above, samples of the signals have been taken with a fixed period repetition rate. Amplitude is discrete since the ADC maps input values into a finite set of output possible values. For example, in a 10-bit ADC, only 1024 output values are available, while the input has an infinitely continuous range.

So, what is the effect of such discretizations?

Both of them can be considered as noise that is added to the signals. However, the analysis of the effects of such additive noise if far beyond the scope of this application note. But, an important point regarding discretization can be introduced: how the ADC and the digital PWM resolution will impact the behavior of the system.

The minimum ADC resolution can be computed from the ratio of the desired output voltage amplitude and the required precision in volts of the output voltage, according to the relationship shown in Equation 295.

EQUATION 295:

$$res = \log_2 \frac{V_{OUT}}{\Delta V_{OUT,\,requested}}$$

A 5V nominal output when a 1% precision is required, results in Equation 296.

EQUATION 296:

$$res = \log_2 \frac{5}{0.05} \approx 7 \text{ bits}$$

As for the digital PWM peripheral, there are two different resolutions. The digital PWM frequency resolution depends on the number of bits used to generate the basic frequency. In SMPS devices the frequency of the PWM can be computed with Equation 297.

EQUATION 297:

$$F_{PWM} \approx \frac{14,55 \bullet 10^6 \bullet 64}{PTPER}$$

where *PTPER* is the register setting the PWM frequency

The minimum change in frequency corresponds to the minimum change in the value of the PTPER register. In dsPIC30F devices, since the three Least Significant bits (LSbs) in the register are not available, the minimum change is 8 (2^3 = 8), which corresponds to 8,4 ns. Table 5 provides the frequency resolution that can be received for various values of the nominal frequency. The resolution is plotted in Figure 90.

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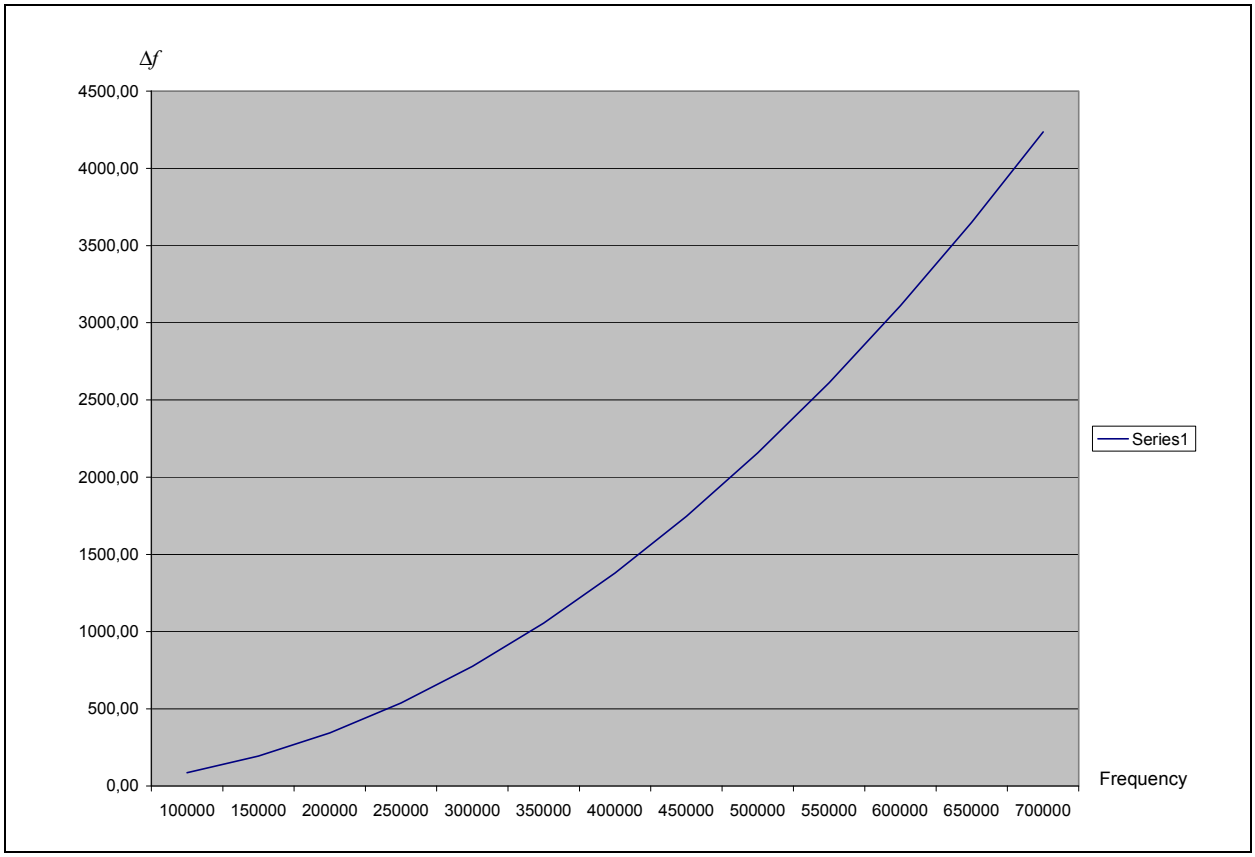
TABLE 5: FREQUENCY RESOLUTION

Frequency	Maximum Frequency	Minimum Frequency
100000	100085,98	99914,16
150000	150193,55	149806,95
200000	200344,23	199656,95
250000	250538,10	249464,21
300000	300775,19	299228,79
350000	351055,58	348950,75
400000	401379,31	398630,14
450000	451746,44	448267,01
500000	502157,03	497861,42
550000	552611,14	547413,42
600000	603108,81	596923,08
650000	653650,11	646390,43
700000	704235,09	695815,54

FIGURE 90:



The second resolution in PWM signals is the duty cycle resolution, which at 1.05 ns is very high.

A parameter that is worth computing, is the system output resolution, which is how much the output voltage will change in response to a minimum change in the PWM duty cycle. This is a measure of the minimum correction of the output voltage that can be generated (see Equation 298).

EQUATION 298:

$$\Delta V_{MIN} = V_{OUT,nom} \bullet 1.05ns \bullet F_{PWM}$$

For example, a 100 kHz PWM frequency and nominal 5V output voltage results in Equation 299.

EQUATION 299:

$$\Delta V_{MIN} = 5 \bullet 1.05ns \bullet 100^3 = 0.5mV$$

A final consideration is that the PWM resolution should be at least one bit higher that the ADC resolution; otherwise, the output value will cross the boundary between two ADC values and the system will continuously try to reach a stable condition, oscillating between these two values.

CODE EXAMPLE

The block diagram in (Figure 91) shows a real implementation of a voltage mode closed loop. The code used in this application note is available for download (see **Appendix A: "Source Code"**).

The main program is composed of two parts:

1. A set of initialization routines, where all the peripherals used (IPP PWM and IPP ADC) are programmed.
2. A main loop. In the example (Figure 91) it is empty. This is because all the relevant operations are performed in the ADC interrupt routine.

   The reason for this is that the computations (as previously seen) should be performed as fast as possible to increase the bandwidth of the system. The main loop will be periodically interrupted by the high-priority ADC Interrupt Service Routine (ISR), so that low priority tasks can be performed in this loop. For instance, the management of the user interface or communication to external units.

The ADC interrupt, as pointed out, is the real "core" of the firmware. The basic operations performed are:

1. Collect data from the ADC hardware.
2. Compute the difference between the currently read voltage value of the system (V_{FB}) and the reference voltage value.
3. Implement the PID, whose output is the duty cycle.
4. Clamp the computed value between a minimum and a maximum value.
5. Update the duty cycle with the currently generated (new) duty cycle.

The processor is run from its internal Fast RC (FRC) oscillator, with a nominal frequency of 14.55 MHz. An internal PLL (32x) raises the operating frequency of the core and peripherals. Taking advantage of the clock speed and high performance DSP engine, the ADC interrupt routine is executed in 1.4 µs, and the basic PID functionality is performed in 1.15 µs.

In general terms, it is not necessary to update the duty cycle at each PWM period. As seen before, the duty cycle update frequency is what determines the maximum loop bandwidth, which is the capability of the system to respond to fast changes in the input (line regulation) or output (load regulation). If for instance, the PWM frequency is 200 kHz, and the voltage/current is sampled and the duty cycle is updated every other period, this results in a 100 kHz update rate, which is 10 µs between two successive interactions with the system.

If the firmware requires 1.4 µs to execute the ADC routine, 8.6 µs (10 – 1.4 = 8.6) are still available to perform all necessary operations, such as, communication on the UART and/or the management of a human interface. The dsPIC DSC device is powerful enough to provide the capability to implement not only the raw control loop, but additional functionality as well!

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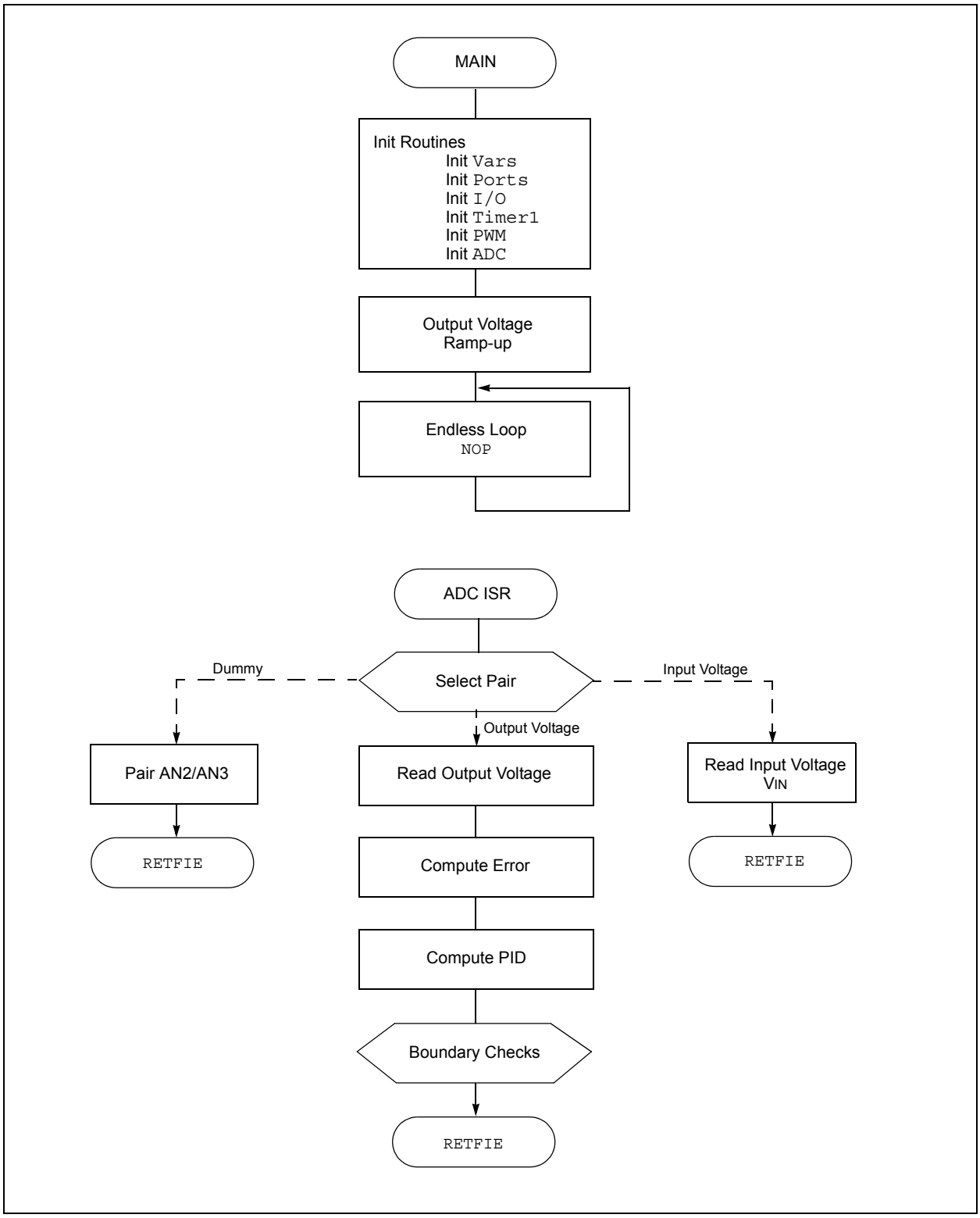
FIGURE 91: PROGRAM FLOW



DETAILED CODE DESCRIPTION

In the following section some details of the code that implements the basic PID functionality are analyzed.

In this design, the code has been designed and tested using Microchip's dsPICDEM™ Buck Development Board (part number DM300023).

Variables Definition

A buffer for the error values is allocated in X-RAM memory in the near area, as shown in Example 1.

EXAMPLE 1:

```
.section PidVars_Xmem, bss, near, xmemory
; Pid values
Error_n:        .space 2
Error_n_1:      .space 2
Error_n_2:      .space 2
```

Another buffer for the PID coefficients is allocated in Y-RAM, again in the near area, as shown in Example 2.

EXAMPLE 2:

```
.section PidVars_Ymem, bss, near, ymemory
;Pid gain values
K_A:            .space 2
K_B:            .space 2
K_C:            .space 2
```

Some additional service variables are also allocated in the near area, as shown in Example 3.

EXAMPLE 3:

```
MyFlag:         .space 2; bit flags
Vdesired:       .space 2
Vset:           .space 2
Vin:            .space 2
Vfb:            .space 2
SystemTimer:    .space 2
Vctrl:          .space 2
```

Code Description

The main code starts with some initialization routines:

- `InitVars`

  Clears the buffers and initializes the K_A, K_B and K_C parameters. It also initializes some core register bits to obtain the desired behavior of the DSP engine (signed mode enabled for DSP multiply operations, accumulator A saturation enabled, data space write saturation enabled, integer mode enabled for DSP multiply operations). Pointers are initialized at the beginning of the two buffers.

- `InitPorts`

  A few pins from port B are used as analog inputs so the configuration register must be consistently programmed. PORTE I/O pins are used by the PWM peripheral also and are initialized as output pins.

- `InitIO`

  A fixed low value is output on the PWM ports at start-up in order to discharge any cap that could be storing energy from previous runs.

- `InitTimer1`

  Initializes Timer1 and enables interrupts.

- `InitPWM`

  One PWM channel is enabled in the following configuration:

  a) Primary time base provides timing for this PWM generator.
  b) DCx register provides duty cycle information for this PWM generator.
  c) Positive dead time actively applied for all output modes.
  d) Dead time period (0x0190).
  e) Trigger output for every second trigger event.
  f) PWM module controls the PWMxH and PWMxL pins.
  g) Fault input is disabled.
  h) Compare value for PWM time base for trigger the ADC module (= 8).

- `ADC`

  The converter is enabled with a clock of 13.3 MHz; pairs 0 and 1 are configured so that IRQ is generated and the trigger is, in both cases, the PWM1 generator.

- `StartOps`

  Starts the timers and all operations of the system. The target output voltage is set (V_{SET}) and the initial output voltage is fixed to some small value ($V_{DESIRED}$ = 0x40).

After the initial phase, a ramp is generated to have a smooth path from the initial zero voltage to the final value. Timer1, with an interrupt rate of 1 µs, is used. At each timer interrupt, the desired voltage is incremented by a fixed delta until the final desired output voltage is reached.

Then the main code enters an endless loop, which during normal operation, is interrupted only by the ADC ISRs.

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ADC Interrupt Service Routine (ISR)

This is the real core of the code. The first thing to do is to determine which pair of input analog channels generated the interrupt. A computed GOTO is used to jump to the corresponding piece of code. Since a voltage control loop is implemented, only the output voltage value (label OutputValues) is of interest.

Then some housekeeping is performed (pointers to the buffer start address are initialized). Then the current voltage input value is read and adjusted as shown in Example 4. In this portion of code, W3 points to the ADC register containing the voltage value. A left shift (multiply by two) is required since the hardware circuit to read the output voltage is a one-half resistors voltage divider.

EXAMPLE 4:

```
; Calculate Voltage error
mov         [W3], W0
sl          W0, #1, W0
mov         W0, Vfb
```

The current value of the error can now be determined (see Example 5), remembering that the error is the difference between the desired voltage and the real voltage read through the ADC. In this portion of code, W0 contains at the beginning of the real output voltage value and at the end the newly computed error.

EXAMPLE 5:

```
; computation of proportional error
; ep = Vdesired - current output voltage
; ep [W1] = Vdesired - Vfb
mov         Vdesired, W1
sub         W1, W0, W0
```

The PID is computed using the movsac instruction first (to initialize the W6 and W7 registers and the buffers pointers), and then the mac instruction (three times), as shown in Example 6, which performs the multiply/accumulate instruction as described in Figure 81.

EXAMPLE 6:

```
movsac  A, [W8]+=2, W6, [W10]+=2, W7
mac     W6*W7, A, [W8]+=2, W6, [W10]+=2, W7
mac     W6*W7, A, [W8]+=2, W6, [W10]+=2, W7
mac     W6*W7, A
; save value rounded
sac.r   , -#8, [W2]
```

At the end, the result (stored in accumulator A) is also rounded and saved in a RAM location (VCTRL).

The duty cycle value, accumulated in subsequent steps, is stored continuously into accumulator A. Some checks on the content of accumulator A are performed to make sure that the accumulated duty cycle never becomes larger that the period or, vice versa, becomes too small.

Note that, to increase the resolution for the PID coefficients, an 8.8 format is used. This means that there is an implied comma (‘ , ’) between bit 7 and bit 8 of the 16-bit wide register. The nice thing of this representation is that it is also possible to use fractional numbers. In other words, a value ‘1’ in this format is represented by: 0000.0001.000.0000 = 0x0100.

CONCLUSION

The need for higher performance AC-to-DC and DC-to-DC converters is supported by the availability of processors such as Microchip's dsPIC DSC SMPS family of devices. These devices are able to perform computational intensive algorithms, while providing specialized peripherals.

Covering all aspects of converter design is beyond the scope of this application note. The intent is to provide at the very least the basic tools needed to understand and design a working converter.

A basic understanding of the main converter topologies, their requirements, and their performance is fundamental to implementing converters where maximum performance is achieved.

The first part of this application note deals with topologies (isolated and non-isolated), and behavioral details of the various systems are provided. In some instances, where appropriate, additional information is presented, such as power consumption and efficiency.

Design equations are provided for all topologies, which serve to fill in the gap between theory and practical implementation. Other design approaches can be used if desired.

Digital converters are closed loop systems, which come with advantages as well as issues. A fast review of basic control theory is presented, as well as an explanation on how to use the powerful tools that this theory provides toward designing a stable converter. Some effort has been taken to show how these results can be efficiently implemented using the Microchip dsPIC DSC SMPS family of devices. Implementation of a PID system is shown and the code is also available (see **Appendix A: "Source Code"**).

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APPENDIX A: SOURCE CODE

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APPENDIX B: REVISION HISTORY

Revision A (June 2008)

This is the initial released version of this document.

Revision B (September 2009)

This revision includes the following updates, which clarify the dsPIC DSC device families that can be used in conjunction with this application note.

- Updated the second sentence in the last paragraph on page 98 by adding a reference to the dsPIC30F family.
- Updated the device family reference to include the dsPIC33F part family in first paragraph of the Switch Mode Power Supply (SMPS) dsPIC DSC Devices section.
- Updated the machine cycle value device family references in the eight paragraph of the Switch Mode Power Supply (SMPS) dsPIC DSC Devices section.

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