things lab
Biomedical Engineeringe at Dankook University

Assignment 01
Make Logic Gates

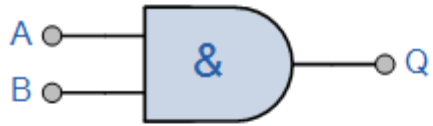
Content

1. AND
2. OR
3. NOT
4. NAND
5. NOR
6. XOR
7. XNOR

AND Gate

AND Gate

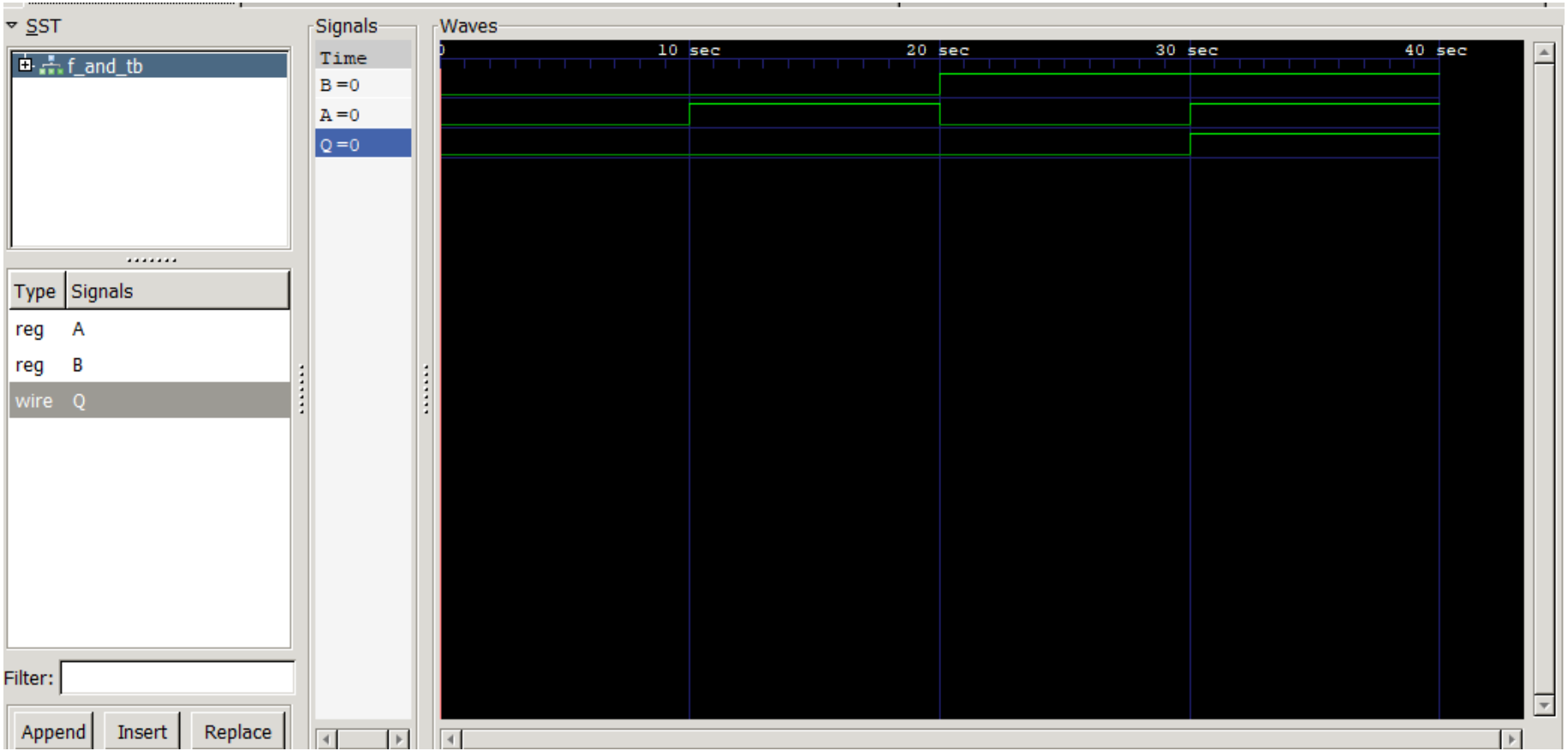
AND Gate

Symbol	Truth Table		
 2-input AND Gate	B	A	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1

AND Gate in Console

```
iverilog -o f_and.vvp f_and_tb.v f_and.v
iverilog -o f_and.vvp f_and_tb.v f_and.v
Process started (PID=136000) >>>
<<< Process finished (PID=136000). (Exit code 0)
================ READY ================
vvp f_and.vvp
vvp f_and.vvp
Process started (PID=135532) >>>
VCD info: dumpfile f_and.vcd opened for output.
time        B          A          Q
 0:         0          0          0
10:         0          1          0
20:         1          0          0
30:         1          1          1
<<< Process finished (PID=135532). (Exit code 0)
================ READY ================
```

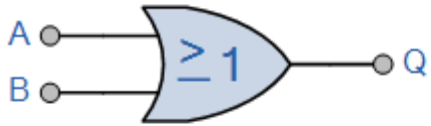
AND Gate in gtkwave



OR Gate

OR Gate

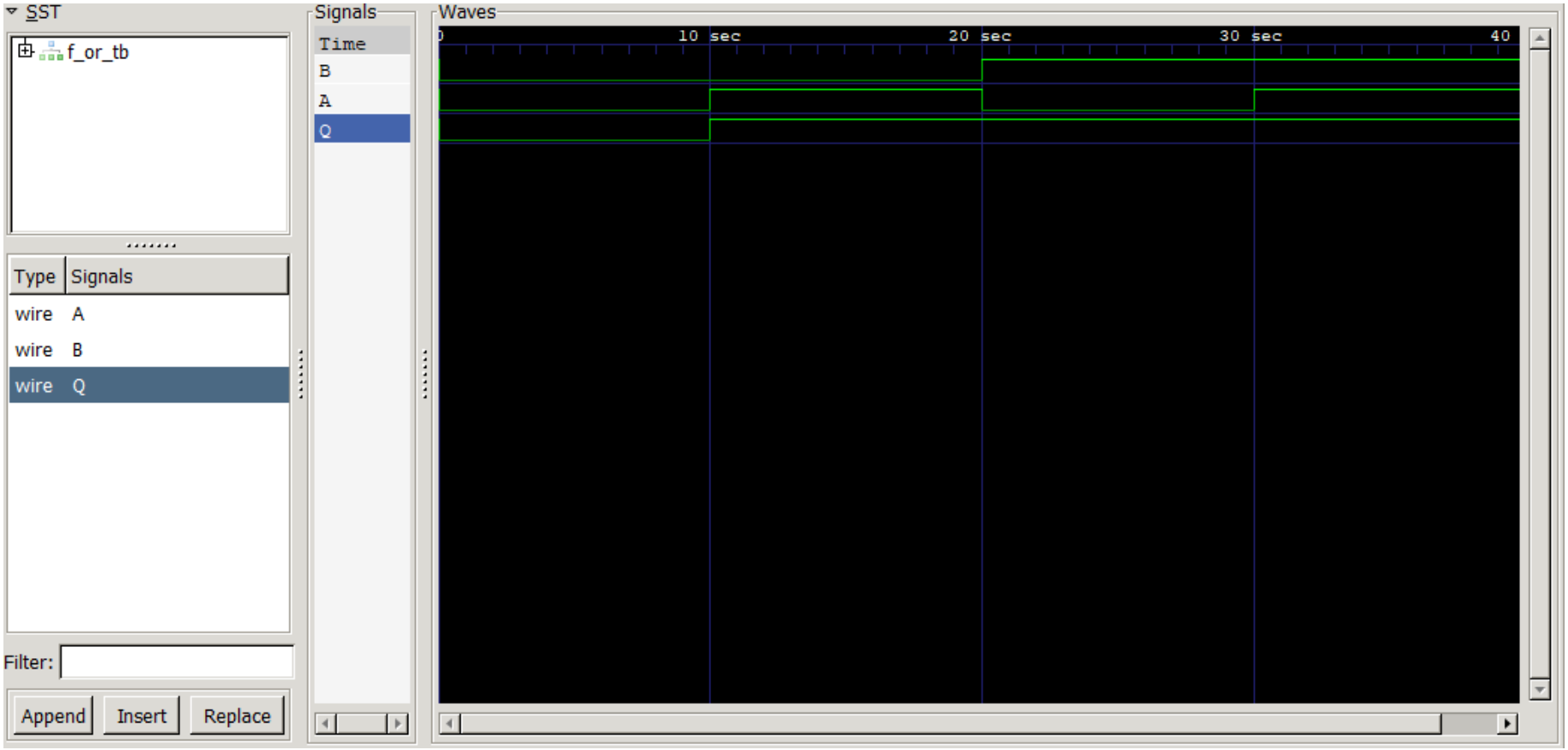
OR Gate

Symbol	Truth Table		
 2-input OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1

OR Gate in Console

```
iverilog -o f_or.vvp f_or_tb.v f_or.v
iverilog -o f_or.vvp f_or_tb.v f_or.v
Process started (PID=122176) >>>
<<< Process finished (PID=122176). (Exit code 0)
================ READY ================
vvp f_or.vvp
vvp f_or.vvp
Process started (PID=127876) >>>
VCD info: dumpfile f_or.vcd opened for output.
time        B          A          Q
 0:         0          0          0
10:         0          1          1
20:         1          0          1
30:         1          1          1
<<< Process finished (PID=127876). (Exit code 0)
================ READY ================
```

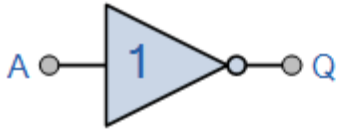
OR Gate in gtkwave



NOT Gate

NOT Gate

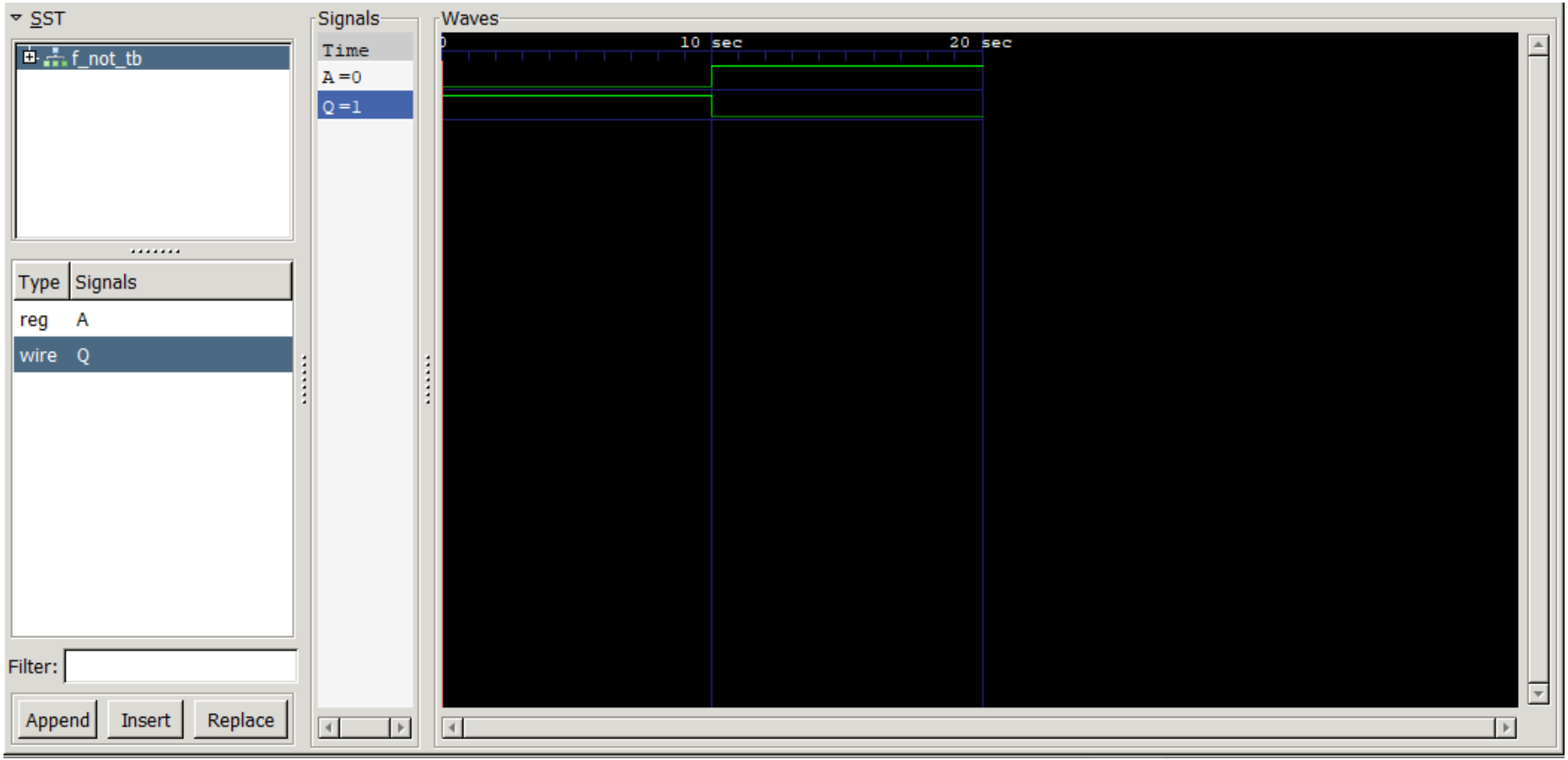
NOT Gate

Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0

NOT Gate in Console

```
iverilog -o f_not.vvp f_not_tb.v f_not.v
iverilog -o f_not.vvp f_not_tb.v f_not.v
Process started (PID=128984) >>>
<<< Process finished (PID=128984). (Exit code 0)
================ READY ================
vvp f_not.vvp
vvp f_not.vvp
Process started (PID=130320) >>>
VCD info: dumpfile f_not.vcd opened for output.
time        A          Q
 0:         0          1
10:         1          0
<<< Process finished (PID=130320). (Exit code 0)
================ READY ================
```

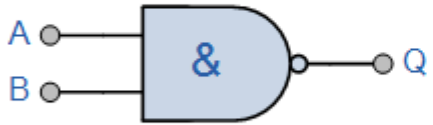
NOT Gate in gtkwave



NAND Gate

NAND Gate

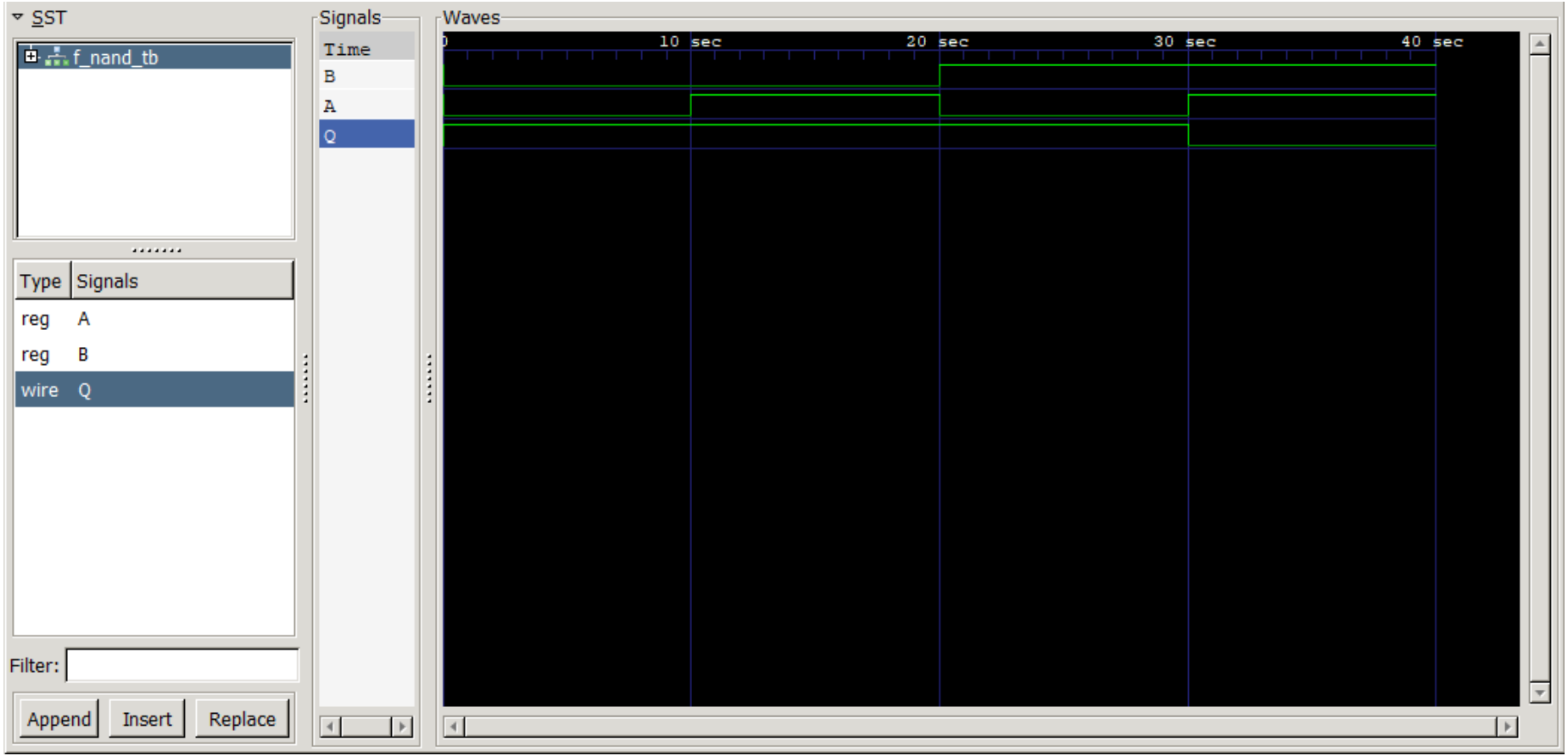
NAND Gate

Symbol	Truth Table		
 2-input NAND Gate	B	A	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0

NAND Gate in Console

```
iverilog -o f_nand.vvp f_nand_tb.v f_nand.v
iverilog -o f_nand.vvp f_nand_tb.v f_nand.v
Process started (PID=136712) >>>
<<< Process finished (PID=136712). (Exit code 0)
================ READY ================
vvp f_nand.vvp
vvp f_nand.vvp
Process started (PID=122148) >>>
VCD info: dumpfile f_nand.vcd opened for output.
time        B           A           Q
 0:         0           0           1
10:         0           1           1
20:         1           0           1
30:         1           1           0
<<< Process finished (PID=122148). (Exit code 0)
================ READY ================
```

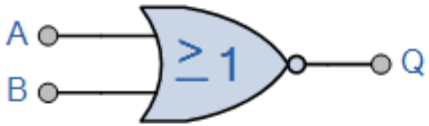
NAND Gate in gtkwave



NOR Gate

NOR Gate

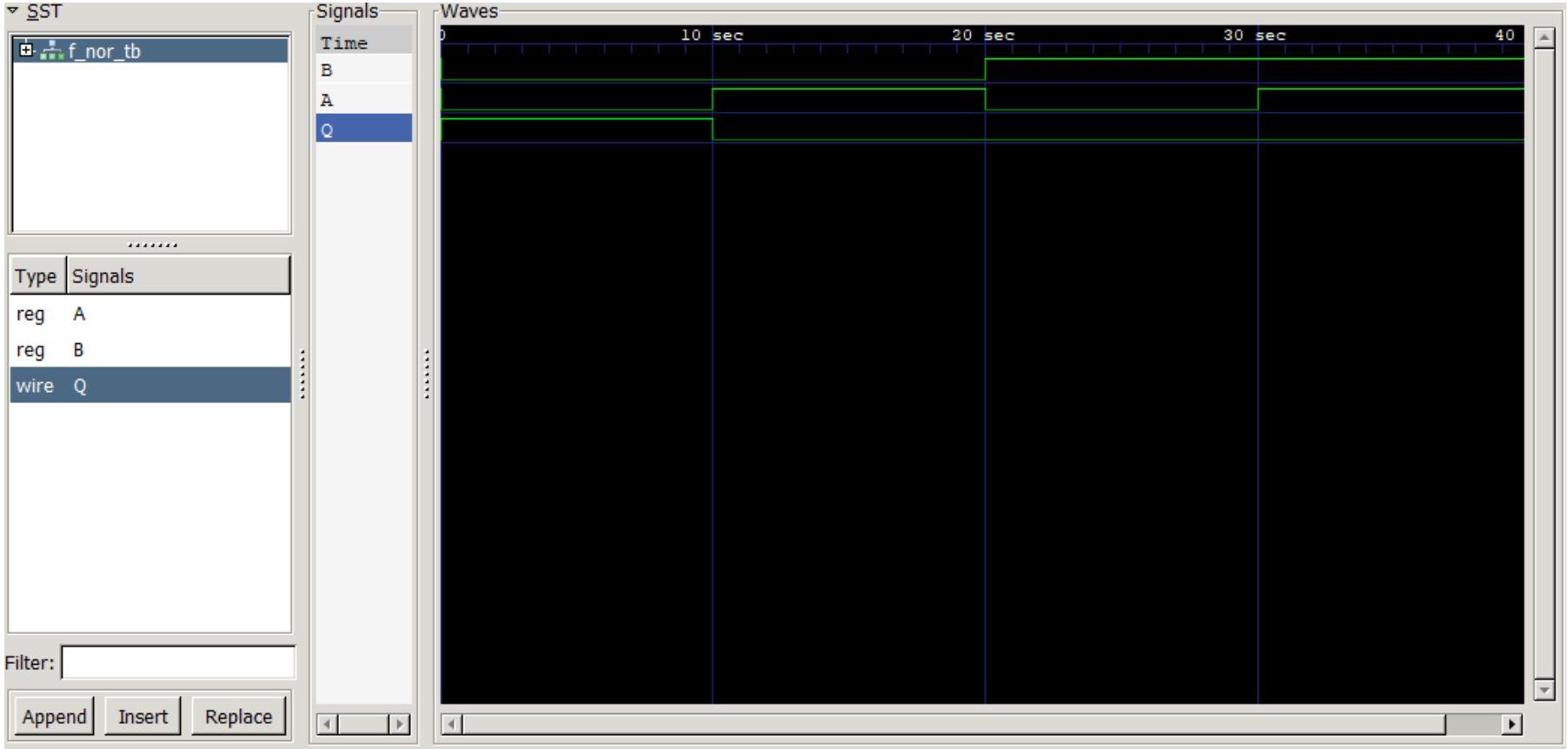
NOR Gate

Symbol	Truth Table		
	B	A	Q
 2-input NOR Gate	0	0	1
	0	1	0
	1	0	0
	1	1	0

NOR Gate in Console

```
iverilog -o f_nor.vvp f_nor_tb.v f_nor.v
iverilog -o f_nor.vvp f_nor_tb.v f_nor.v
Process started (PID=122984) >>>
<<< Process finished (PID=122984). (Exit code 0)
================ READY ================
vvp f_nor.vvp
vvp f_nor.vvp
Process started (PID=131152) >>>
VCD info: dumpfile f_nor.vcd opened for output.
time        B          A          Q
 0:         0          0          1
10:         0          1          0
20:         1          0          0
30:         1          1          0
<<< Process finished (PID=131152). (Exit code 0)
================ READY ================
```

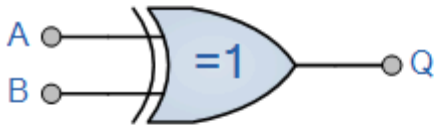
NOR Gate in gtkwave



XOR Gate

XOR Gate

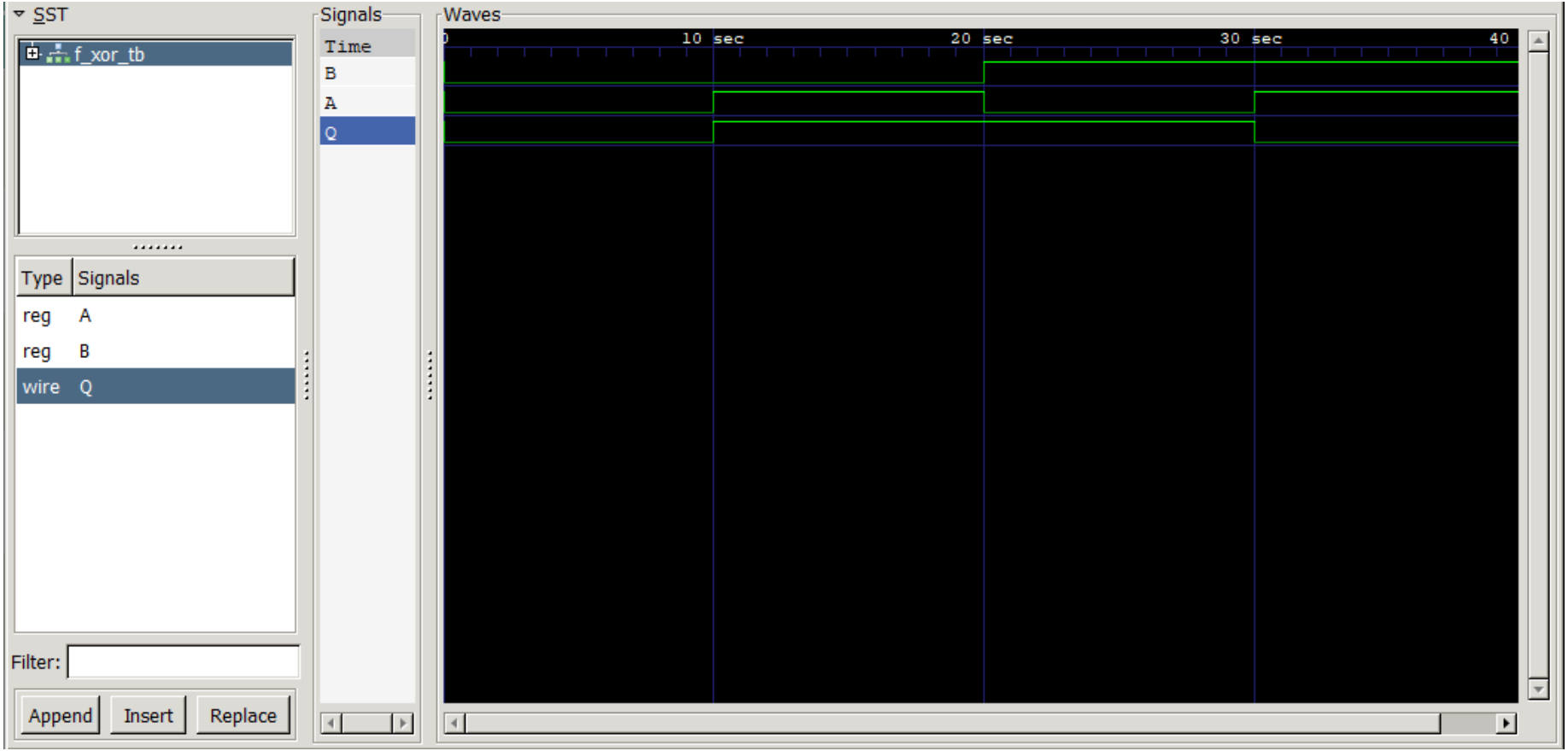
XOR Gate

Symbol	Truth Table		
 2-input Ex-OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0

XOR Gate in Console

```
iverilog -o f_xor.vvp f_xor_tb.v f_xor.v
iverilog -o f_xor.vvp f_xor_tb.v f_xor.v
Process started (PID=136356) >>>
<<< Process finished (PID=136356). (Exit code 0)
================ READY ================
vvp f_xor.vvp
vvp f_xor.vvp
Process started (PID=136936) >>>
VCD info: dumpfile f_xor.vcd opened for output.
time        B           A           Q
 0:         0           0           0
10:         0           1           1
20:         1           0           1
30:         1           1           0
<<< Process finished (PID=136936). (Exit code 0)
================ READY ================
```

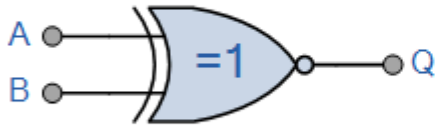
XOR Gate in gtkwave



XNOR Gate

XNOR Gate

XNOR Gate

Symbol	Truth Table		
 2-input Ex-NOR Gate	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1

XNOR Gate in Console

```
iverilog -o f_xnor.vvp f_xnor_tb.v f_xnor.v
iverilog -o f_xnor.vvp f_xnor_tb.v f_xnor.v
Process started (PID=128696) >>>
<<< Process finished (PID=128696). (Exit code 0)
================ READY ================
vvp f_xnor.vvp
vvp f_xnor.vvp
Process started (PID=133408) >>>
VCD info: dumpfile f_xnor.vcd opened for output.
time        B        A        Q
 0:         0        0        1
10:         0        1        0
20:         1        0        0
30:         1        1        1
<<< Process finished (PID=133408). (Exit code 0)
================ READY ================
```

XNOR Gate in gtkwave