01. Intro the Verilog

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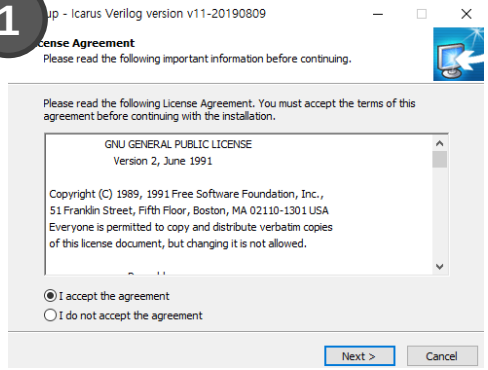
1. Install the Verilog

- Go to the http://bleyer.org/icarus/iverilog-v11-20190809-x64_setup.exe

1



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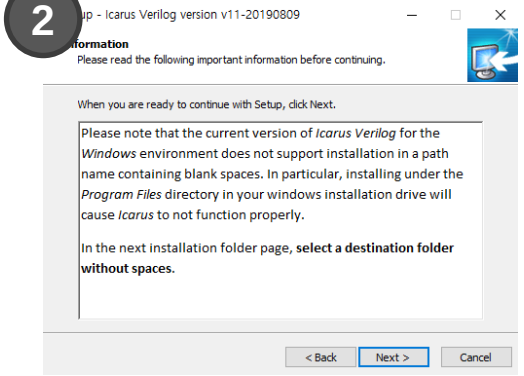

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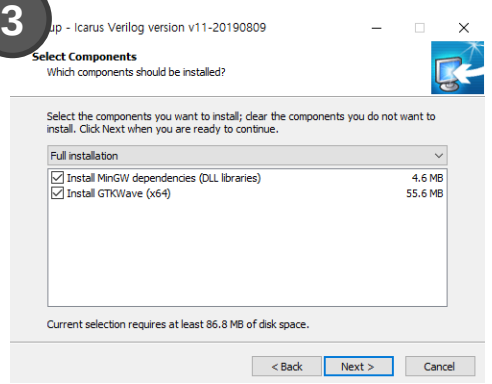

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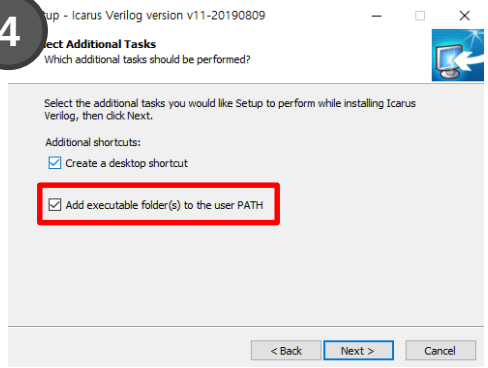

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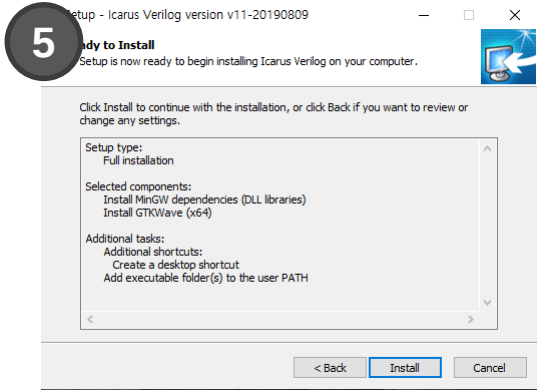

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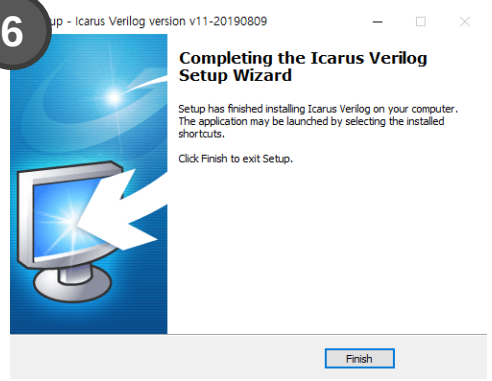
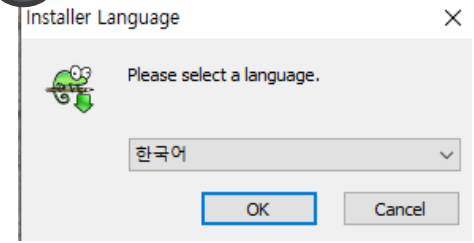


2. Install the Notepad++

- Go to https://github.com/notepad-plus-plus/notepad-plus-plus/releases/download/v7.8.5/npp.7.8.5.Installer.exe

1



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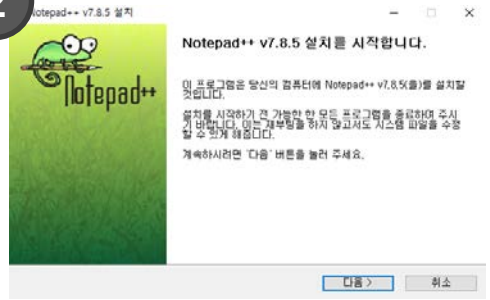
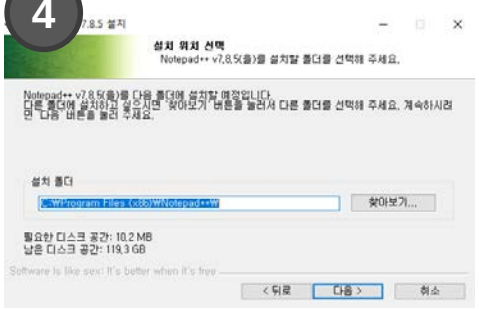


3

4



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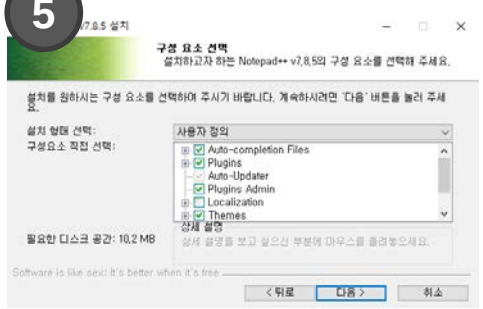

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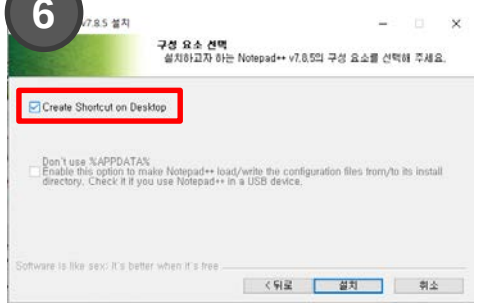

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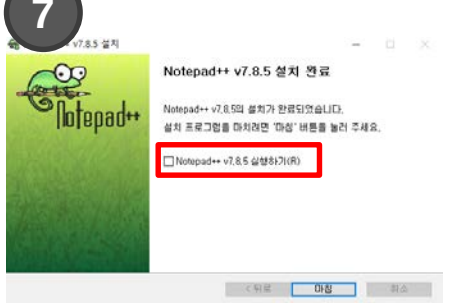
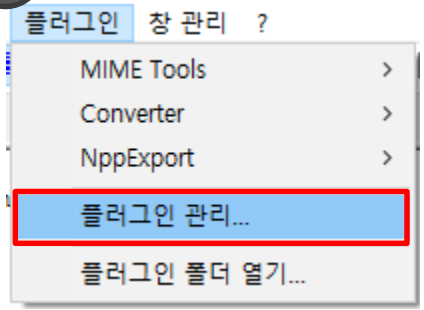
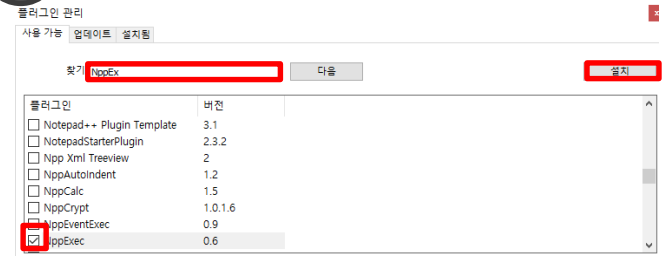


3. Install the plugin for Verilog

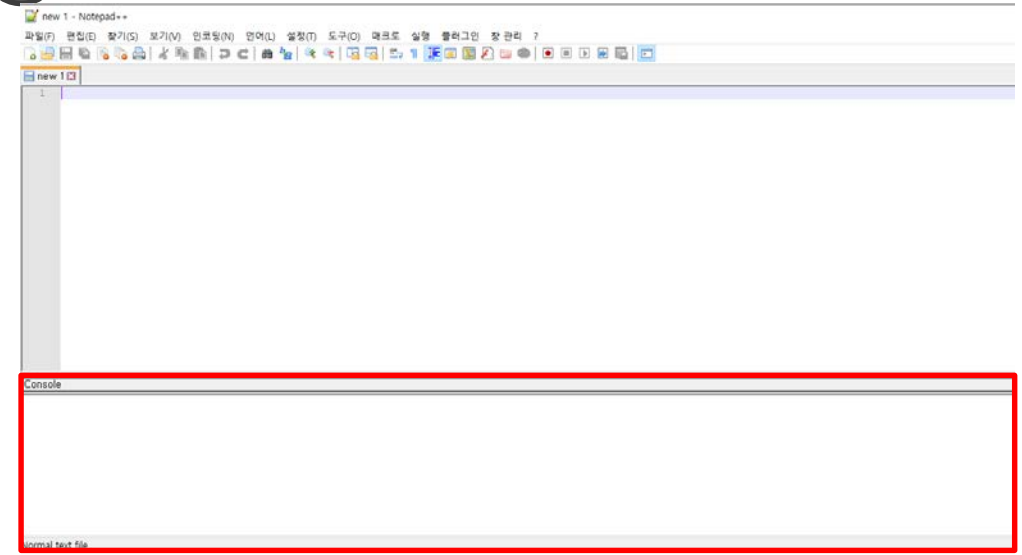
1 플러그인 – 플러그인 관리



2 NppEx 찾고 체크 한 후 설치버튼 클릭

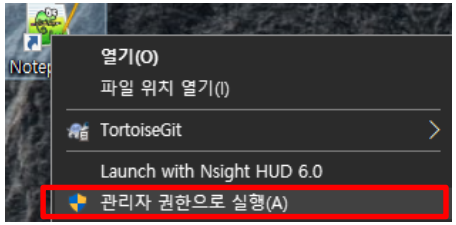


3 Code 입력부분 밑에 Console창 생긴것을 확인할 수 있다.

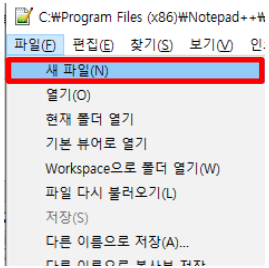


3. Example Verilog 01 – Hello World

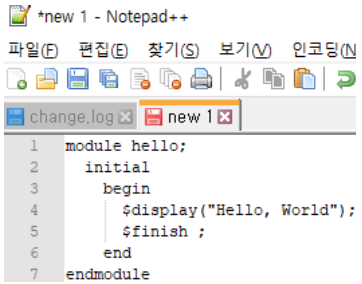
1 관리자 권한으로 실행



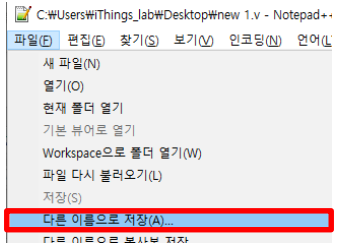
2 파일 – 새 파일



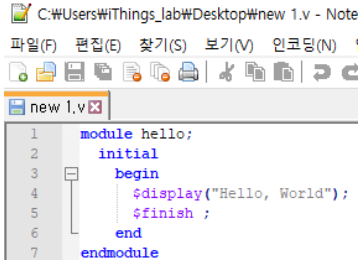
3 Type the code



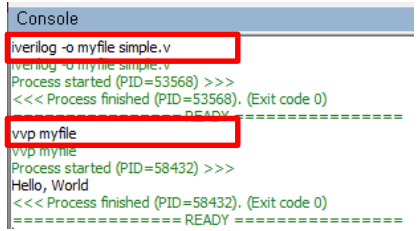
4 원하는 폴더에 *simple.v*로 저장



5 highlight된것을 확인



6 하단 Console창에 입력



3. Example Verilog 02 – Logic Gate

1 *functions.v* 파일 만들기

functions.v | functions_tb.v

```
1  module functions (a,b,f_and, f_or, f_not, f_nand, f_nor, fxor, f_xnor);
2      input a, b;
3      output f_and, f_or, f_not, f_nand, f_nor, fxor, f_xnor;
4      assign f_and    = a & b;
5      assign f_or     = a | b;
6      assign f_not    = ~a;
7      assign f_nand   = ~(a & b);
8      assign f_nor    = ~(a | b);
9      assign f_xor    = a ^ b;
10     assign f_xnor   = ~(a ^ b);
11
12 endmodule
```

2 *functions_tb.v* 파일 만들기

functions.v | functions_tb.v

```
1  `timescale 1ns/1ns
2  module functions_tb;
3      reg a,b;
4      wire f_and, f_or, f_not, f_nand, f_nor, fxor, f_xnor;
5      functions f (a,b,f_and, f_or, f_not, f_nand, f_nor, fxor, f_xnor);
6      initial begin
7      $display("time\ta\tb\tand\tor\tnot\tnand\tnor\txor\txnor");
8      a = 0;
9      b = 0;
10     # 5 $finish;
11 end
12 initial begin
13     $monitor ("%2d:\t%b\t%b\t%b\t%b\t%b\t%b\t%b\t%b\t%b",
14               $time, a, b, f_and, f_or, f_not, f_nand, f_nor, fxor, f_xnor);
15 end
16 always #1 a = !a;
17 always #2 b = !b;
18 endmodule
```

3 하단 Console창에 입력 후 결과 확인

Console

```
iverilog -o functions functions.v functions_tb.v
iverilog -o functions functions.v functions_tb.v
Process started (PID=62956) >>>
<<< Process finished (PID=62956). (Exit code 0)
================ READY ================
vvp functions
vvp functions
Process started (PID=61344) >>>
time    a    b    and    or    not    nand    nor    xor    xnor
 0:     0    0    0      0     1      1       1      z      1
 1:     1    0    0      1     0      1       0      z      0
 2:     0    1    0      1     1      1       0      z      0
 3:     1    1    1      1     0      0       0      z      1
 4:     0    0    0      0     1      1       1      z      1
 5:     1    0    0      1     0      1       0      z      0
<<< Process finished (PID=61344). (Exit code 0)
================ READY ================
```

3. Example Verilog 03 – gtkwave

1 *andOrNot.v* 파일

andOrNot.v | andOrNot_tb.v

```
1  module andOrNot(A, B, C, D, E);
2     output D, E;
3     input  A, B, C;
4     wire   w1;
5
6     and  G1(w1, A, B);
7     not  G2(E, C);
8     or   G3(D, w1, E);
9
10 endmodule
```

2 *andOrNot_tb.v* 파일

andOrNot.v | andOrNot_tb.v

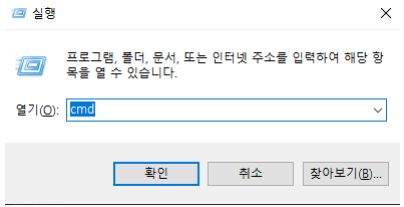
```
1  `timescale 1ns/100ps
2  `include "andOrNot.v"
3
4  module andOrNot_tb;
5
6     wire A, B, C, D, E;
7     integer k=0;
8
9     assign {A,B,C} = k;
10    andOrNot the_circuit(A, B, C, D, E);
11
12    initial begin
13       $dumpfile("andOrNot.vcd");
14       $dumpvars(0, andOrNot_tb);
15
16       for (k=0; k<8; k=k+1)
17         #10 $display("done testing case %d", k);
18
19       $finish;
20
21    end
22
23 endmodule
```

3 Console창을 통한 debug

Console

```
iverilog -o andOrNot.vvp andOrNot_tb.v
iverilog -o andOrNot.vvp andOrNot_tb.v
Process started (PID=57896) >>>
<<< Process finished (PID=57896). (Exit code 0)
================ READY ================
vvp andOrNot.vvp
vvp andOrNot.vvp
Process started (PID=48716) >>>
VCD info: dumpfile andOrNot.vcd opened for output.
done testing case       0
done testing case       1
done testing case       2
done testing case       3
done testing case       4
done testing case       5
done testing case       6
done testing case       7
<<< Process finished (PID=48716). (Exit code 0)
================ READY ================
```

4 실행 - cmd



5 Command창에 아래와 같이 기입

6 gtkwave 실행화면