UROP1000 Project Report

FPGA-controlled silicon photonic switches for datacenters

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ABSTRACT

The objective of this project is to improve response time and increase the efficiency of the real-time feedback control system for microring resonators in silicon photonics chips functional for transmission channel switching in datacenters regardless of temperature or external disturbances. This report investigates the correlation between resonance wavelength of resonators and the value shift due to applied electrical signals in Thermo-Optical or Electro-Optical tuners by analyzing the photocurrent. Referring to the data, refinement of hardware interface for signals transmittance was performed by revising utilized components for accuracy and precision in addition to prevention of short-circuit issues. Furthermore, the development of finite-state-machine (FSM) programmed in the Zedboard Field-Programmable-Gate-Array (FPGA) device would enhance the signals processing and hence the photonics switches stabilization.

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CHAPTER ONE INTRODUCTION

1.1 Project Introduction

1.1.1 Background Information

Cloud services including cloud storage and computing have been increasingly popular in the last decade. The datacenter requires more advanced technology to effectively handle this growing demand, with larger bandwidth, faster transmission rate, and lower power consumption. The idea of a silicon photonic chip as an optical interconnect has been introduced to meet the request of high-speed data switching and routing in datacenter. The aim is to integrate both electronics and photonics onto the silicon platform.

Multiple-input-ports multiple-output-ports (MIMO) interconnects on silicon photonics chip enables high-speed photonic switching by using the advantages of the features of a single light wavelength signal. Wavelength Division Multiplexing (WDM) also allows more channels for transferring information simultaneously, up to terabits per second with lower power consumption. This UROP 1000 project is focusing on implementing Field Programmable Gate Array (FPGA) to actively stabilize the silicon photonic chip.

1.1.2 Literature Review

In this following literature review, we will discuss silicon optical modulators and the methods used to create a feedback control system such as a microprocessor to stabilize the photonic switch.

In [1], the characteristics of electro-optical effects in silicon is discussed. Classical theoretical approach suggests Drude-Lorenz model characterize the electro-optical effect. However, the experimental result shows deviation from the theoretical model. Empirical equations of change of absorption and change of refractive index for silicon at 1.3μm and 1.55μm are introduced to characterize the electro-optical effect in silicon.

The thermo-optical effect in silicon is explored in [2]. The result concludes that thermos-optical effect exhibits high resolution, large dynamics, and no self-heating effect. Thermal design is also important to improve the performance in terms of speed of operation of TO tuner. In addition, [2] also suggests that SOI has been examined to have better optical confinement characteristics of the device.

A single ring stabilization method by using slope detector computed by a microprocessor is discussed in [3]. The microprocessor keeps track of the photocurrent variation and gives step voltage to Electro-optical (EO) tuner or Thermo-optical tuner (TO) to blueshift or redshift the resonance wavelength.

1.2 Project Details

The UROP1000 project is a continuation of Mr. Yeung Tung Hong's last year Final Year Project. This project is focusing on using Field Programmable Gate Array (FPGA) on actively controlling a single silicon micro-resonator chip. 2-by-2 and 1-by-4 photonic device is characterized and tested in this project. The primary objective of this UROP1000 project is to implement the feedback system algorithm to control on-chip EO and TO tuners.

1.2.1 Project Description

In this project, tuner laser from near 1550nm generates light signal into the silicon photonic chip which is wire bonded to the PCB and attached to the thermal electric cooler (TEC). After the setup is fine-tuned, an Optical Power Meter (OPM) is used to measure the light output intensity. To simulate thermal disturbance, a signal generator is used to apply sinusoidal wave to the TEC. The on-chip photodetector measures the intensity of light inside the micro ring and sends the signal to the FPGA. The signal from PD is amplified and converted prior to being sent to the FPGA. With the feedback system implemented to the FPGA, the control algorithm will measure the PD signal and decide to apply desirable voltage to the TO or EO tuners. Moreover, oscilloscope is used to record the voltage of PD, EO, and TO for monitoring purpose.

1.2.2 Components

Hardware:

- FPGA board with ZYNQ-7000 SoC by Xilinx
- Dual 1Msps 12-bit Analog to Digital Converter (Pmod AD1 module)
- 8-bit Digital to Analog Converter (DAC08080)
- General-Purpose Operational Amplifier (UA741)

Software:

- Xilinx Vivado version 2019.1
- Origin 8.5
- K-layout
- Microsoft Excel

1.2.3 System Block Diagram

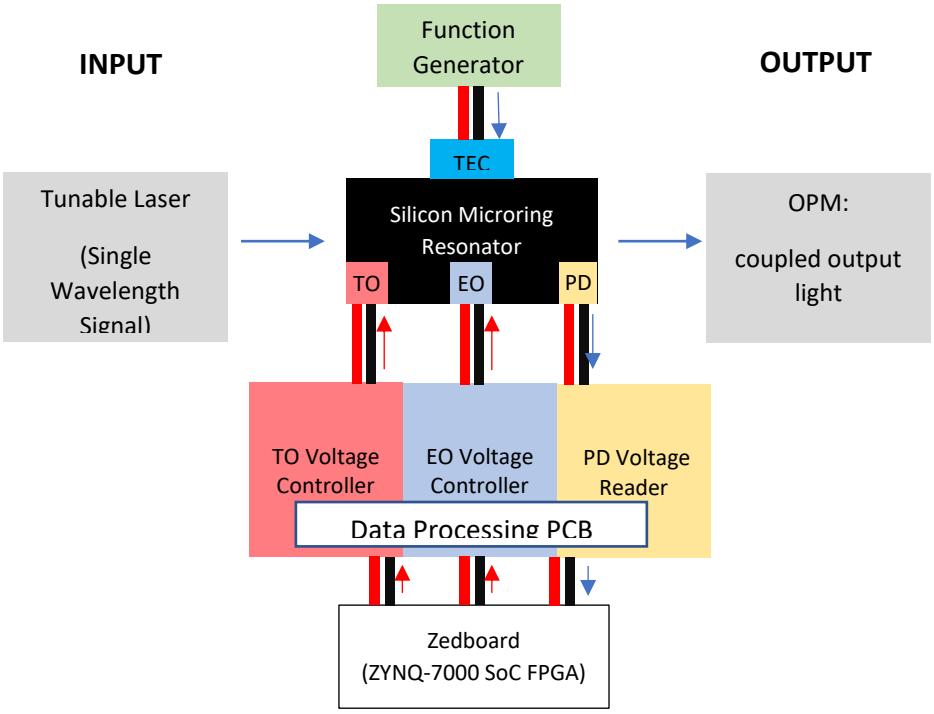

Figure 1.1 System Block Diagram

1.2.4 Project Tasks

The following is the list of tasks of this UROP 1000 project, listed in chronological order.

1. Study operation concepts and design structure of silicon photonic switch
2. Study and practice how to do the experiment and measurement
3. Study and modify Verilog code under Xilinx Vivado of control algorithm
4. Wire bond the silicon photonic chip and test the functionality of wire bonded chip
5. Data analysis for device characterization
6. Build a circuit for connecting the chip and the FPGA
7. Simulate and Test the feedback control program by Zedboard on single microring resonator
8. Connect the chip, the circuit, and the FPGA
9. Identify the problem of implementation process

1.2.5 Division of task

Table 1.1

Table 1.1 Division of task in UROP 1000 project

TASKS	Ferris	Gerry	Stefan
TASK 1			
TASK 2			
TASK 3			
TASK 4			
TASK 5			
TASK 6			
TASK 7			
TASK 8			
TASK 9			

1.2.6 Technical Challenges

There are numbers of technical challenges in this project. The first one is the fragileness of the chip, the fiber optics head, and the wire bond. In this project, numbers of microring are broken due to various reasons, such as damaged by fiber head (1 pieces), stretched by probe (1 piece), damaged by electrostatic discharge (3 pieces), broken by default (2 pieces). Accordingly, 5 wire bonding appointments have been made to connect different microring to the PCB. In addition, 1 fiber input head and 1 fiber output head are broken due to accident. Moreover, electrostatic discharge occurs few times, yet it can be solved by building the circuit to prevent this issue from happening after we refer to the previous paper of this project. [4]

1.2.7 Report Outline

This report is organized into seven parts. The device characterization of the microring resonator is provided in Chapter 2. The detail of the circuit and the FPGA programming will be presented in Chapter 3 and Chapter 4, respectively. Chapter 5 will be demonstrating the result after connecting the components. In Chapter 6, the future works for this project will be further discussed. Conclusion and afterword can be found in Chapter 7.

CHAPTER TWO DEVICE CHARACTERIZATION

This chapter will discuss the structure of the microring resonators which are used in this project. Further, the data collected from measurement will be presented and analyzed to determine the important characteristics of the photonic chip and its modulators. The characteristics are expected to improve the feedback system by predicting the appropriate voltage needed to be applied to the TO or EO tuners when it is on the off-resonance state.

2.1 Structure of Microring Resonator

Microring resonator is an optical device that is embedded with the on-chip modulators, which are a Photodetector (PD), a Thermo-Optical (TO) tuner, and Electro-Optical (EO) tuner. As shown in Figure 2.1(a), input light (monochromatic laser beam with wavelength ~1550nm to minimize attenuation) will be flowing in from the input port. The resonance wavelength will be coupled into the microring and then coupled out at the drop port. Conversely, the resonance non-resonance wavelength will leave at the throughput port. In our experiment, arrays of 2-by-2 (shared ground) and 4-by-1 (separated ground) microrings with multiple-input-port multiple-output-port (MIMO) interconnects are used, illustrated in Figure 2.1(b). Figure 2.1(c) shows the SEM image of the photonic chip and the microring. Figure 2.4(d) shows the circuit illustration for the modulators inside the microring with a shared ground.

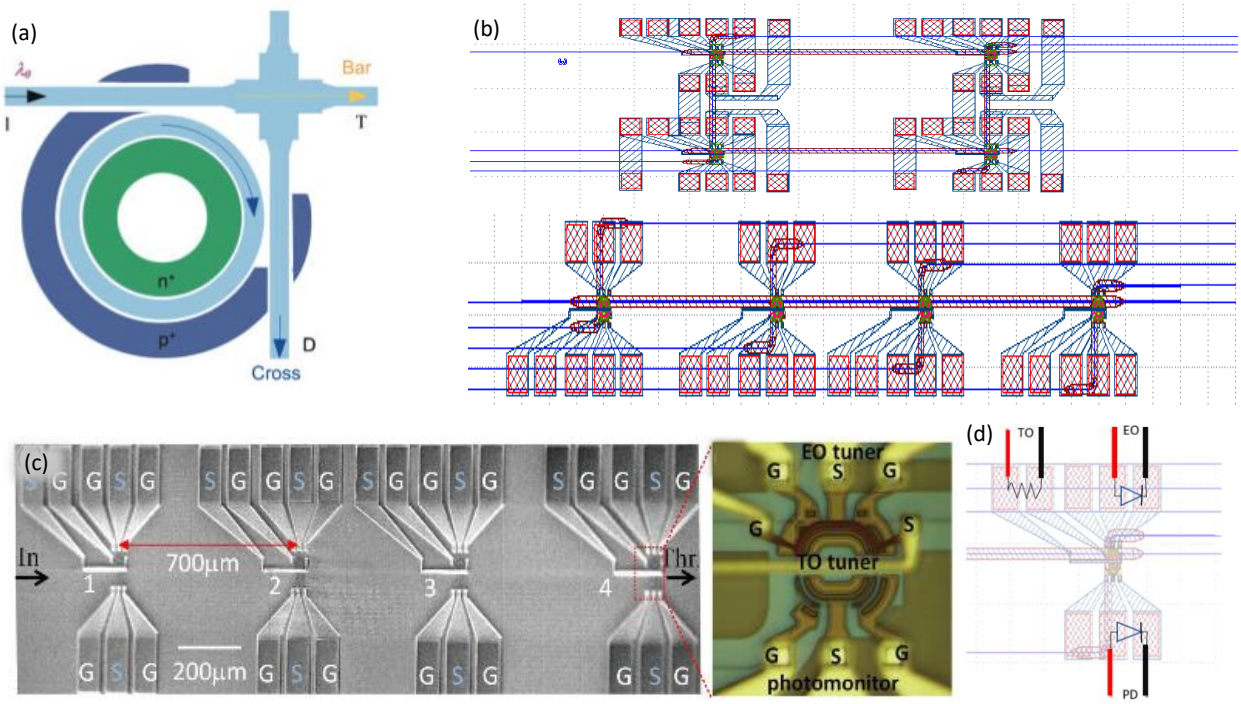

Figure 2.1 Structure of Microring
(a) port arrangement of microring (I=input, T=throughput, D=drop) [5]; (b) array of 2-by-2 and 4-by-4 microrings; (c) SEM image of currently used photonic chip [7]; (d) simplified electrical circuit illustration of optical modulators with shared ground [4]

2.2 Device Characterization

2.2.1 Resonance wavelength

While all devices are fabricated evenly, a small variation in the fabrication process can make each microring to have different resonance wavelength. By using the tunable laser generator as the light input and the OPM to measure the output intensity, the resonance wavelength can be determined by measuring the output intensity on either drop port or the throughput port.

On resonance wavelength, the phase-matching condition satisfies:

$$N_{eff}L = m\,\lambda_m \tag{2.1}$$

The FSR is defined as the periodic spectral separation of two successive resonance wavelengths, given by the equation:

$$FSR = \frac{\lambda_m^2}{n_g L} \tag{2.2}$$

Figure 2.2 shows the output intensity of the drop port, throughput port, and the combination port of 2-by-2 photonic chip array as a function of the input wavelength (1540nm-1560nm). The measured FSRs are 7.10nm and 7.11nm.

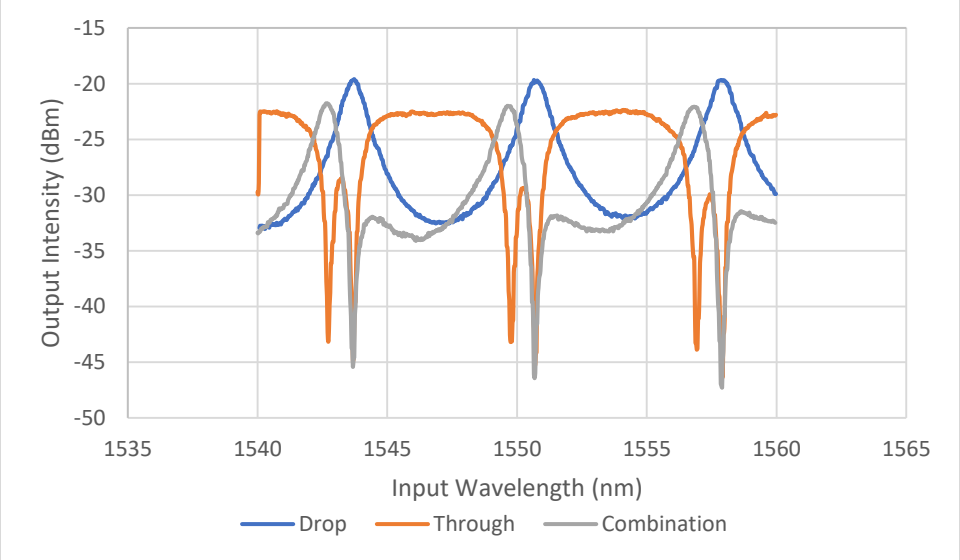

Figure 2.2 Scanning of ports of 2-by-2 chip
blue: drop port of chip 2; orange line: series of throughput port of chip 1 and chip 2;
grey: series of drop port of chip 1 and throughput port of chip 2.

2.2.2 PD, TO, and EO characteristics

As the feedback system requires input and output mechanism to stabilize the photonic chip, these on-chip modulators serve as the tool to connect the feedback system with the microring resonator. The PD is used to measure photocurrent, which corresponds to the energy level inside the microring. -2V is applied across the PD to measure the effect of different wavelength affect the PD. The photocurrent measurement is done by connecting 1MΩ resistor in series with the PD and measures the voltage across the resistor. In the experiment, the PD photocurrent measurement is done manually by collecting different data points while changing the input wavelength. An improved method for measurement is considered in future works and will be further explored in Chapter 6. Figure 2.3 shows the photocurrent as a function of input wavelength.

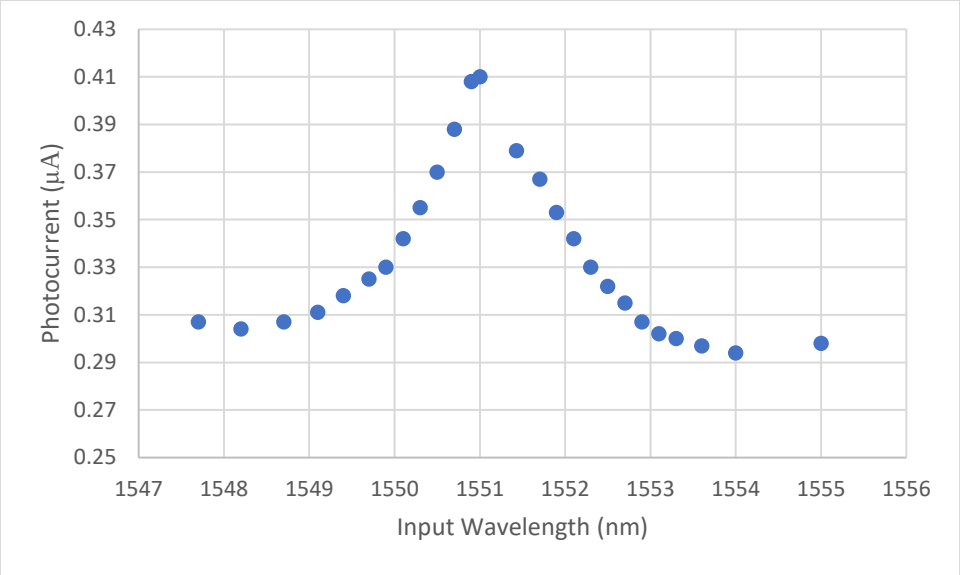

Figure 2.3 Photocurrent as a function of input wavelength

The TO and the EO are used to apply redshift and blueshift effect on the microring. Either EO or TO will be activated according to the condition determined by the feedback system. They work by the principle of Thermo-Optical effect and Electro-Optical effect, in which the refractive index of the silicon waveguide will be changed due to the effects. The voltage range of TO and EO are 0.00V-3.22V (to avoid overheating) and 0.85V to 1.51V (as saturation occurs in higher voltage). By using the Lorentzian peak analysis, the resonance frequency can be determined. Figure 2.4 and Figure 2.5 shows the TO and EO wavelength redshift and blueshift on drop port as a function of input wavelength with EO voltage as a parameter. Moreover, Feng [5] suggests that the response time for TO is ~7ns for rise time and ~14ns for fall time, while the response time for EO is ~1.2ns and ~1.3ns for fall time.

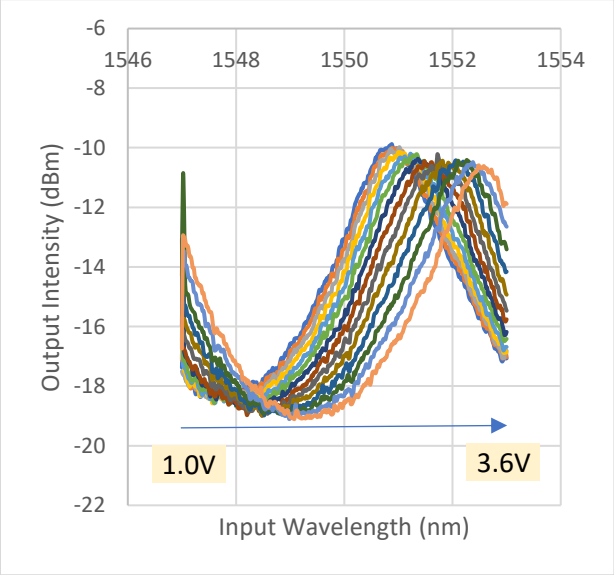

Figure 2.4 TO redshift effect with 0.2V step

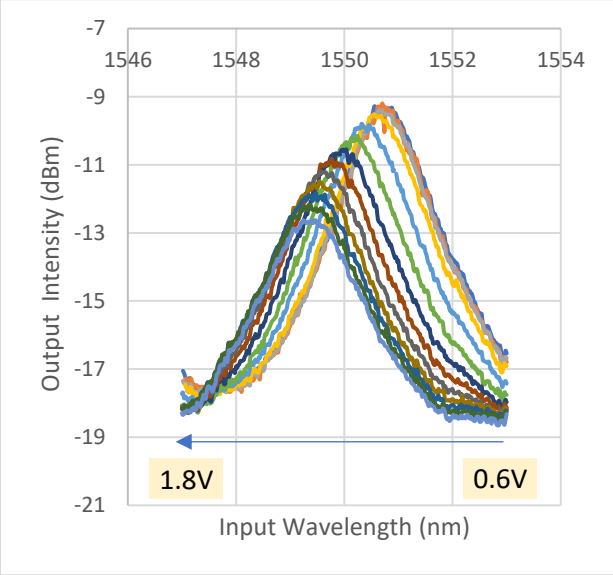

Figure 2.5 EO blueshift effect with 0.1V step

2.3 Data Analysis

In this part, data analysis is used to determine the TO and EO intrinsic characteristics. Since TO is a resistor, the important characteristics to be determined is just its resistance. For EO, because it is a semiconductor, further analysis is needed to determine its intrinsic characteristic.

2.3.1 Thermo-Optical Tuner

In TO tuner, the Thermo-Optical effect changes the resonance wavelength by changing the refractive index linearly proportional to the temperature. The analysis for TO is done as the following:

$$P = \frac{V^2}{R} = C\ \Delta T \tag{2.3}$$

where P is the heat power dissipation, V is TO voltage, R is the intrinsic resistance, C is the heat capacity, and ΔT is the temperature change.

In common, the effective distance which light travels inside a medium is the Optical Path Length (OPL), which is given by:

$$\mathrm{OPL} = \mathrm{n_{eff}\,L} \tag{2.4}$$

where n_{eff} is the effective refractive index of the silicon and L is the distance traveled by light. In this case, the standard value of n_{eff} for silicon for 1550nm is 3.48. The temperature change will be affecting the OPL either by changing the effective refractive index (Thermo-optical effect) or the length (Linear thermal expansion). The linear approximations of the effects are given by:

$$\Delta\mathrm{L} = \mathrm{L_0}\ \alpha\ \Delta\mathrm{T} \tag{2.5}$$

$$\Delta\mathrm{n_{eff}} = \mathrm{n_{eff,0}}\ \beta\ \Delta\mathrm{T} \tag{2.6}$$

The standard value of α is $2.56 \cdot 10^{-6}$, while the standard value of β is $1.86 \cdot 10^{-4}$. Since $\beta >> \alpha$, we can approximate the change of OPL with respect to the change of temperature as following:

$$\Delta\mathrm{OPL} \cong \mathrm{n_{eff}}\,\Delta\mathrm{L} + \Delta\mathrm{n_{eff}}\,\mathrm{L} \cong \Delta\mathrm{n_{eff}}\,\mathrm{L} = \mathrm{n_{eff}}\,\beta\,\mathrm{L}\,\Delta\mathrm{T} \tag{2.7}$$

Combining eq. (2.3) with (2.6),

$$\Delta\mathrm{OPL} = \frac{(\mathrm{n_{eff}}\,\beta\,\mathrm{L})}{\mathrm{R\,C}}\,\mathrm{V}^2 \tag{2.8}$$

Linear regression can be used to determine the value of the slope, which is the intrinsic value of each TO in each microring. Figure 2.6 shows the plot of resonance wavelength vs. the square of TO voltage. In principle, there is no limitation of how far TO can redshift the resonance wavelength, but applying too high voltage may damage the chip.

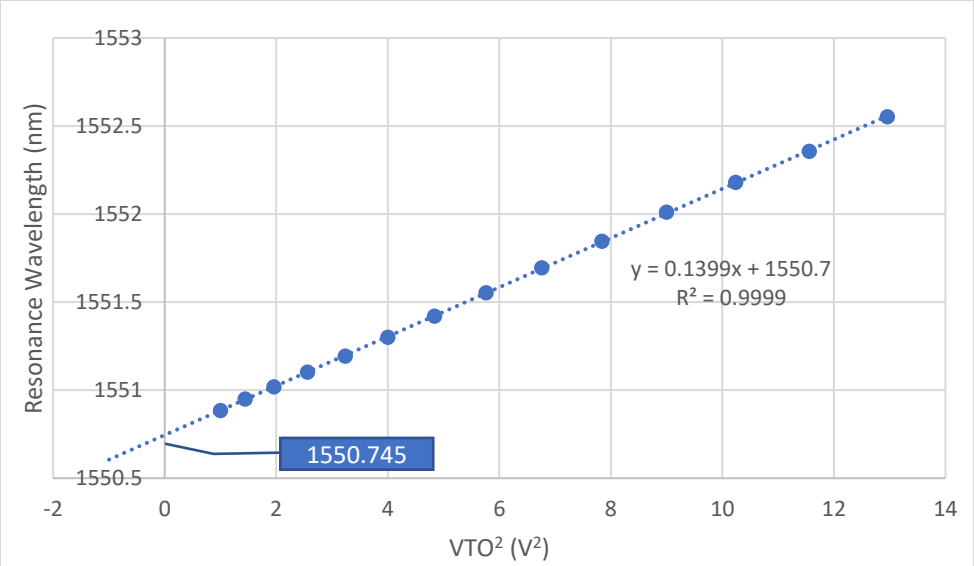

Figure 2.6 TO data analysis

2.3.2 Electro-Optical Tuner

In EO tuner, there are 2 effects which change the resonance wavelength. In addition to the Electro-Optical effect, the Thermo-Optical Effect also affects this tuner. Since both effects shift the wavelength in the opposite direction, a saturation voltage can be measured, in which the blueshift is maximum. Figure 2.7 shows the graph of the resonance wavelength and resonance intensity as a function of the voltage applied across EO.

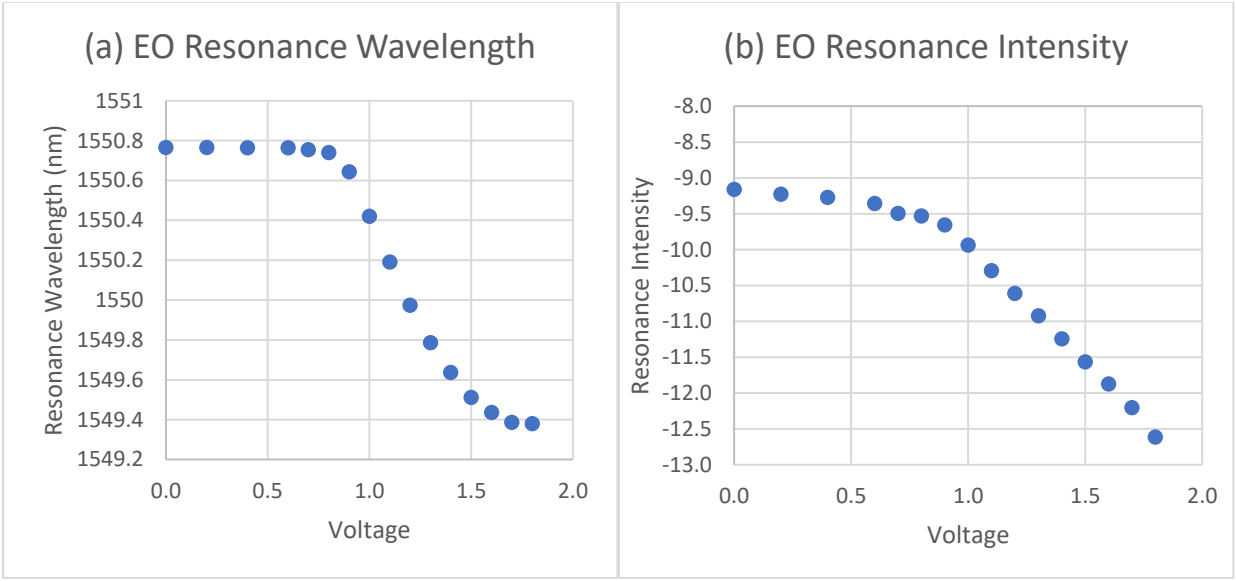

Figure 2.7 EO blueshift
(a) Resonance wavelength shift vs EO voltage; (b) Resonance intensity shift vs EO voltage

A more comprehensive analysis is done on another photonic chip, but using throughput port. The issue from using throughput port is that the output intensity vs. input wavelength curve does not follow

the Lorentzian curve as the drop port did. Therefore, the resonance intensity cannot be further analyzed because of software limitation. In this photonic chip, the maximum wavelength shift is 1.04nm.

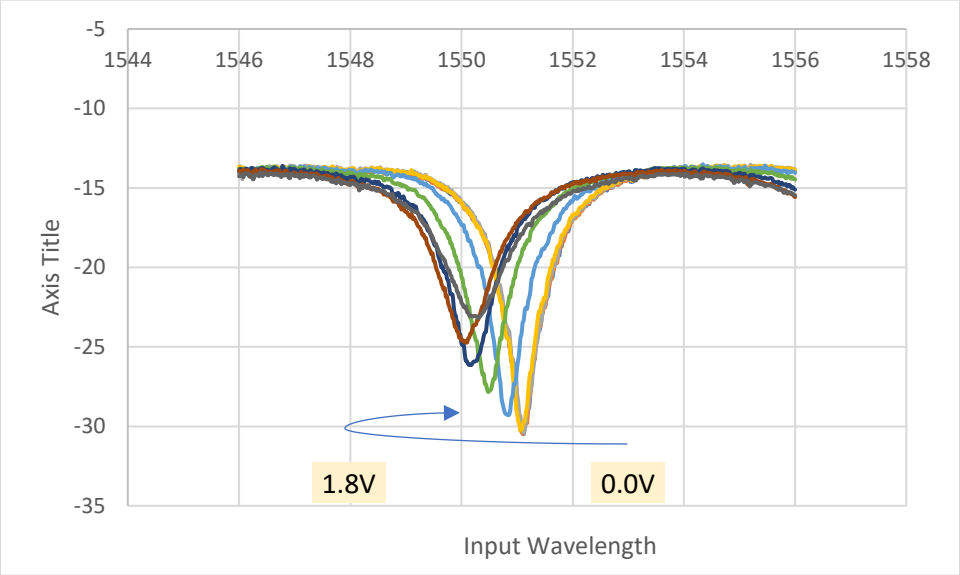

Figure 2.8 EO Throughput blueshift effect with 0.2V step

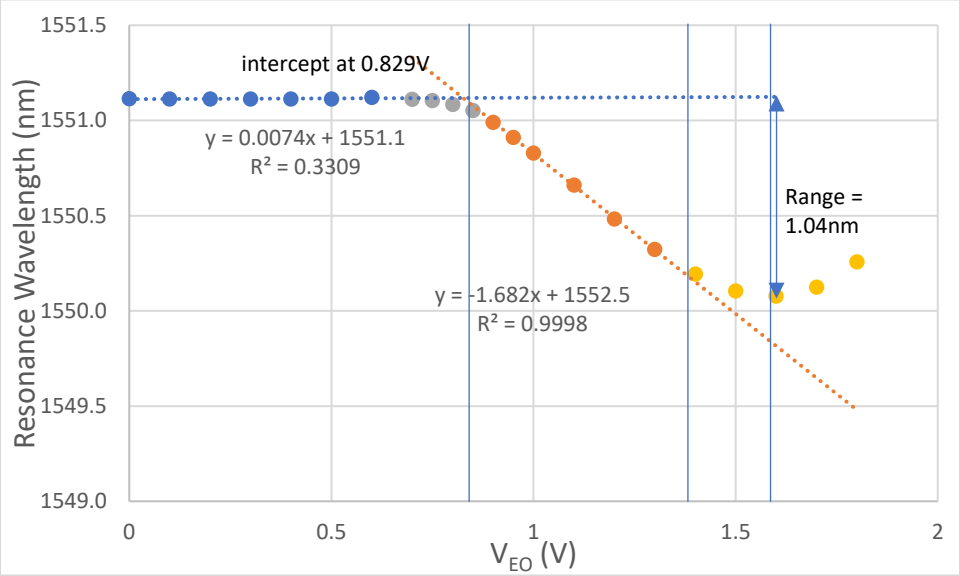

Figure 2.9 Throughput Analysis of EO
blue: below cutoff region, no change in resonance wavelength; orange: linear region, only Electro-Optical effect occurs; yellow: saturated region, where Thermo-Optical effect occurs

There are various types of Electro-Optical effect in general, but the prominent effect in this silicon microring is only due to Plasma Dispersion Effect [6], which changes the imaginary and real part of the refractive index. The change of imaginary part of refractive index ($\Delta\alpha$) is accountable to the change of absorption, while the real part of refractive index (Δn) affects the wavelength shift. The Drude-Lorenz classical model is given by:

$$\Delta\alpha = \frac{e^3\lambda_0^2}{4\pi^2c^3\epsilon_0 n}\left(\frac{\Delta N_e}{\mu_e(m_{ce}^*)^2} + \frac{\Delta N_h}{\mu_h(m_{ch}^*)^2}\right) = a_1\Delta N_e + a_2\Delta N_h \quad (2.8)$$

$$\Delta n = -\frac{e^2\lambda_0^2}{8\pi^2c^2\epsilon_0 n}\left(\frac{\Delta N_e}{m_{ce}^*} + \frac{\Delta N_h}{m_{ch}^*}\right) = b_1\Delta N_e + b_2\Delta N_h \quad (2.9)$$

Where λ_0 is the input wavelength, m_{ce}^* and m_{ch}^* are the conductivity effective mass of electron and hole, and μ_e and μ_h are the electron and hole mobility. The classical model shows that both $\Delta\alpha$ and Δn have a linear dependency to the ΔN_e and ΔN_h. However, the experimental result in [1] demonstrated discrepancy from the classical Drude-Lorenz model. The more accurate model must include a quantum mechanical approach. An empirical model is built to simplify this issue. The empirical model for silicon micro-resonator at 1550nm, introduced by Soref-Bennet [1] is given by:

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8\cdot 10^{-22}\Delta N_e + 8.5\cdot 10^{-18}(\Delta N_h)^{0.8}] \quad (2.10)$$

$$\Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = 8.5\cdot 10^{-22}\Delta N_e + 6.0\cdot 10^{-18}\Delta N_h \quad (2.11)$$

In our experiment, we have not demonstrated the method to measure the ΔN_e and ΔN_h independently. Therefore, our data analysis is still cannot conclude any intrinsic characteristic of the EO. This data analysis will be considered in future works and will be discussed in Chapter six.

CHAPTER THREE HARDWARE INTERFACE AND CIRCUITAL DESIGN

This chapter will elaborate on the details of the hardware interface in the feedback control system. The circuit system consists of wire-bonding between silicon photonics chip with connection PCB, PD Voltage Reader, and Voltage Controller for TO & EO including Electrostatic Discharge Protection and assembly to FPGA.

3.1 Wire-bonding

Wire-bonding holds an important role in uniting the silicon photonics chip with the data processing PCB and eventually to the FPGA. As described in Figure 2.1(d), the microring resonators are surrounded by Thermo-Optical (TO) Tuner, Electro-Optical (EO) Tuner, and the Photodiode (PD) which could be represented as an analogy of resistor and diodes. The terminals of these components were then extended by conductive pads to provide pathways for wire-bonding. With the wire-bonder in the Sensor and Instrumentation Laboratory, these pads could be connected to the connection PCB as shown in Figure 3.1b.

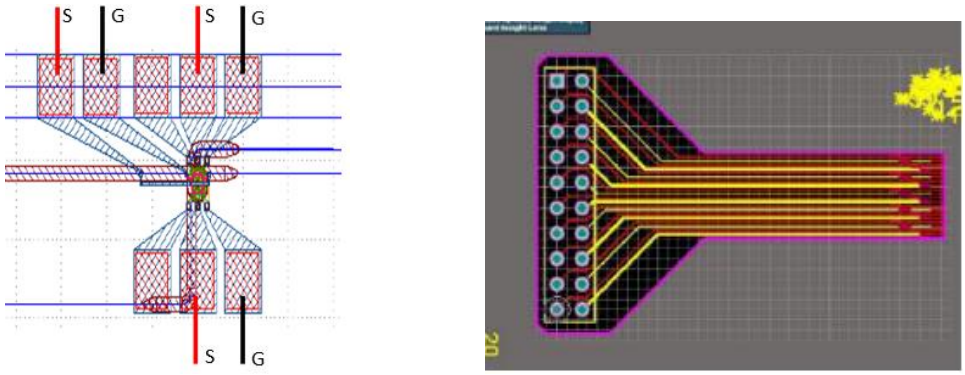

Figure 3.1 Preparation for Wire-bonding
(a) Terminals of each component for signals or ground; (b) Connection PCB with 20 pins at its end

The connection PCB provides several advantages which could increase the successful yield rate of wire-bonding. Provided with 20 pins, each connection PCB allows more terminals of optical modulators in each microring resonators to be wire-bonded. The pins would then be plugged to the data processing circuit via jump wires matching the suitable terminals for electrical signals or ground as illustrated in Figure 3.1a. Furthermore, the neck-shaped structure shortened the distance of pins to the silicon photonics chip and hence, decreases the required length of bonding wires. This is important to reduce the chance of wire entanglements or the unwanted inductance which may affect or interrupt our measurements.

3.2 Data Processing PCB

3.2.1 Photodiode Voltage Reader

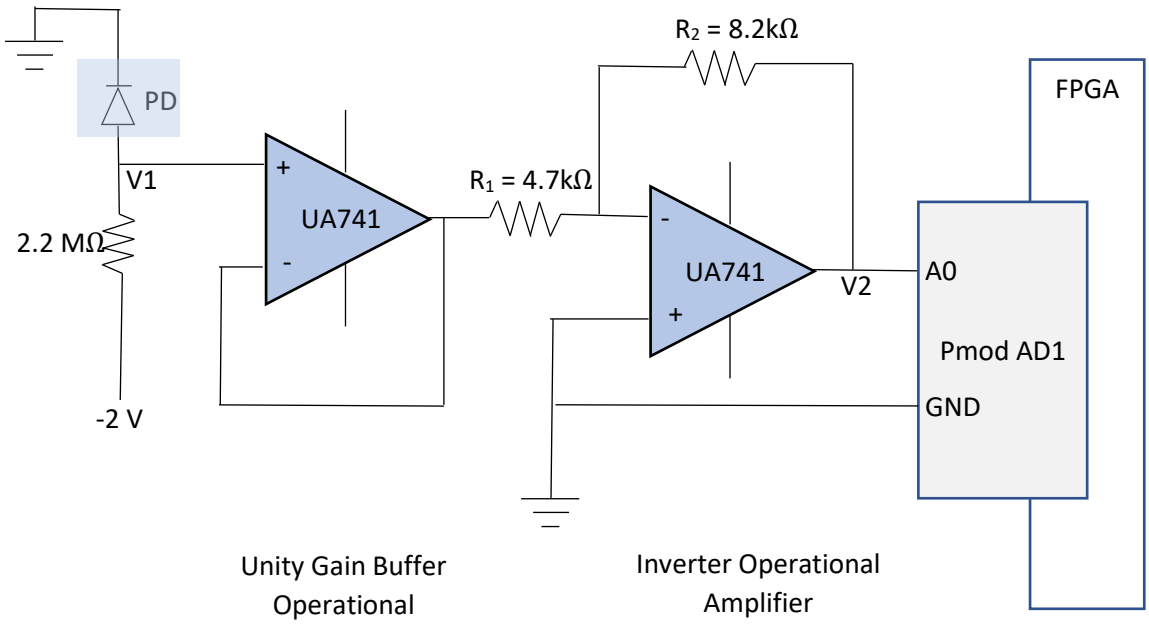

Figure 3.2 Schematics for photodiode voltage reader consisting of buffer and inverter UA741 operational amplifiers with Digilent Pmod AD1 Analog-to-Digital Converter

The Photodiode Voltage Reader circuit consists of buffer and inverter op-amps channeling the output from PD to Digilent Pmod AD1 Analog-to-Digital Converter which is connected to the FPGA as illustrated in Figure 3.3. Since the value of PD voltage V1 is negative, reverse-bias is performed to the PD which would then be connected to 2.2MΩ resistor in series. Unity gain buffer op-amp has an output which mirrors V1 but provides high input impedance and low output impedance. This feature is useful to chain the PD circuit from the inverter op-amp and the Pmod AD1 without worrying of impedance problems. On the other hand, the inverter op-amp inverts the output voltage from the buffer which satisfies the following equation.

$$\frac{V_2}{V_1} = -\frac{R_2}{R_1} \tag{3.1}$$

The minus sign indicates a phase shift of 180^0 to the output voltage, V2. The resistor value of R2 and R1 could be varied to change the gain factor of the voltage. Larger R2/R1 would give a larger magnitude of V2 which would then increase the sensitivity to change in PD voltage for the feedback input.

Pmod AD1 as a 12-bit Analog-to-Digital Converter would then convert the signal into 12-bits data which is readable by the Zedboard. It can read an input voltage ranging from 0 to 3.3V and interact with Zedboard through the Serial Peripheral Interface which is modelled with equation 3.2.

$$V_{in} = 3.3\ V * \frac{V_{read}}{2^{12}} \tag{3.2}$$

Where Vin is the input voltage and Vread is the 12-bit unsigned decimal value read by the Zedboard.

3.2.2 TO and EO Voltage Controller

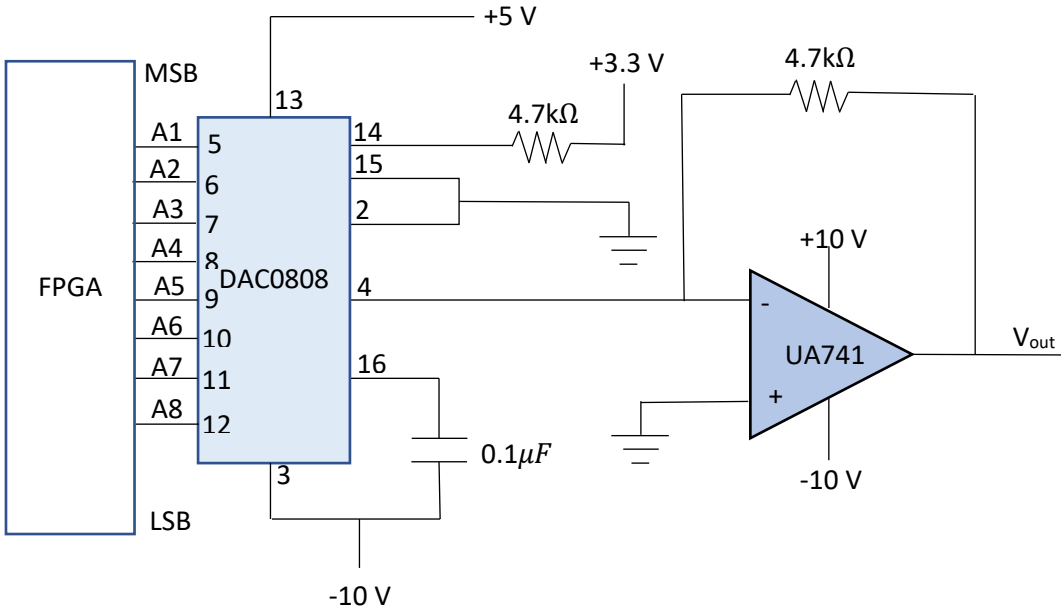

Figure 3.3 Schematics for TO and EO voltage reader consisting of operational amplifier and DAC0808 Digital-to-Analog Converter

After processing input signal from PD Voltage Reader, Zedboard FPGA would then emit digital 8-bit control voltage data to TO and EO tuners through each of their own Voltage Controller. This data would be processed by DAC0808 8-bit Digital-to-Analog Converter and enter the transimpedance amplifier (TIA) circuit via UA741 operational amplifier. The output control voltage (Vout) could be obtained by equation 3.3, where A1 is the Most Significant Bit (MSB) and A8 is the Least Significant Bit (LSB) of the FPGA 8-bit voltage data. Vres is adjustable depending on provided conditions. With this circuit, wavelength shift tuning is expected to be performed more precisely.

$$V_{out} = V_{res} * \sum_{i=1}^{8} \frac{A_i}{2^i} \tag{3.3}$$

3.2.3 Electrostatic Discharge Protection

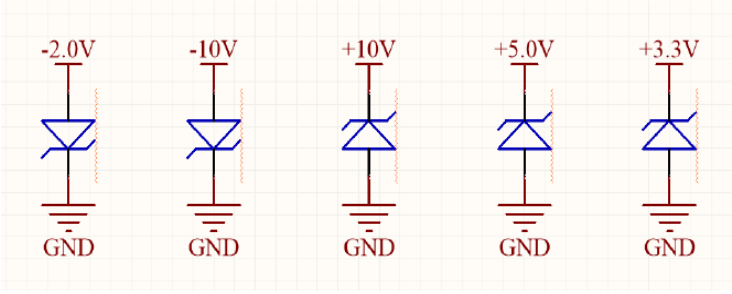

Figure 3.4 TVS diodes for electrostatic discharge protection

Electrostatic Discharge (ESD) might happen to silicon photonics chip during transient phases, e.g. switching on/off power supplies or connecting/disconnecting to data processing circuit, which could

possibly damage the optical modulators surrounding the resonators. To ensure quality and safety, Transient-Voltage-Suppression (TVS) diodes could be installed for all voltage sources to prevent drastic changes in electric current or discharge to the components. The polarity of the diodes should be adjusted depending on the polarity of the voltage sources. Excessive electric current should be able to flow to the ground after surpassing breakdown voltage of the diodes.

3.3 PCB Assembly to FPGA

Table 3.1 Assigned pins in Data Processing PCB, Pmod AD1, and Zedboard to be connected.

Data Processing PCB	Digilent Pmod AD1	Zedboard (FPGA Board)
-	CS	JB1
-	D0	JB2
-	D1	JB3
-	CLK	JB4
3.3 V	Vcc (=3.3 V)	VCC3V3
GND	GND	GND
V2 (PD Voltage)	A0	-
VE0[0] (MSB, A1 in EO Voltage Controller)	-	JA1
VE0[1]	-	JA2
VE0[2]	-	JA3
VE0[3]	-	JA4
VE0[4]	-	JA7
VE0[5]	-	JA8
VE0[6]	-	JA9
VE0[7] (LSB, A8 in EO Voltage Controller)	-	JA10
VTO[0] (MSB, A1 in TO Voltage Controller)	-	JC1 N
VTO[1]	-	JC1 P
VTO[2]	-	JC2 N
VTO[3]	-	JC2 P
VTO[4]	-	JC3 N
VTO[5]	-	JC3 P
VTO[6]	-	JC4 N
VTO[7] (LSB, A8 in TO Voltage Controller)	-	JC4 P

The hardware interface would then be completed by assembly and connection of pins from data processing PCB, silicon photonics chip, and Zedboard as shown in Table 3.1. It should be noticed that Zedboard through Pmod AD1 provides 3.3V of Vcc to the remaining circuits. Pmod AD1 translates the analog data from PD Voltage Reader into digital data to Zedboard through JB pins. In addition, responses from Zedboard to TO and EO tuners would be transferred through JC pins and JA pins respectively [8].

CHAPTER FOUR FPGA STABILIZATION

4.1 Finite State Machine

The first FSM utilized slope detection algorithm for stabilization of microring resonator. The microprocessor tracked the previous value and the current value of the photodetector voltage and compare them to increment the voltage of the EO or TO such that the stable on-resonance state is achievable. In addition, the temperature of the chip is also included in the previous FSM design to decide whether the microprocessor should change the voltage of TO or EO. In this UROP, however, the revised version of the algorithm can be made by removing temperature variable because it is speculated that the temperature is not the only external factors that affect the resonance state of the microring, rather there are several of them such as the humidity of the chip.

The proposed FSM can be generally depicted in the following figure. Instead of using temperature as a decision-maker, the perturbation state is utilized by applying a large amount of EO voltage. After that, the microprocessor will read the value of the current Photodetector voltage and compare it to the previous value. This will allow the microprocessor to know which one of the voltages should be applied. The rest of the FSM structure is the same as the previous FSM with some slight changes in the parameter values.

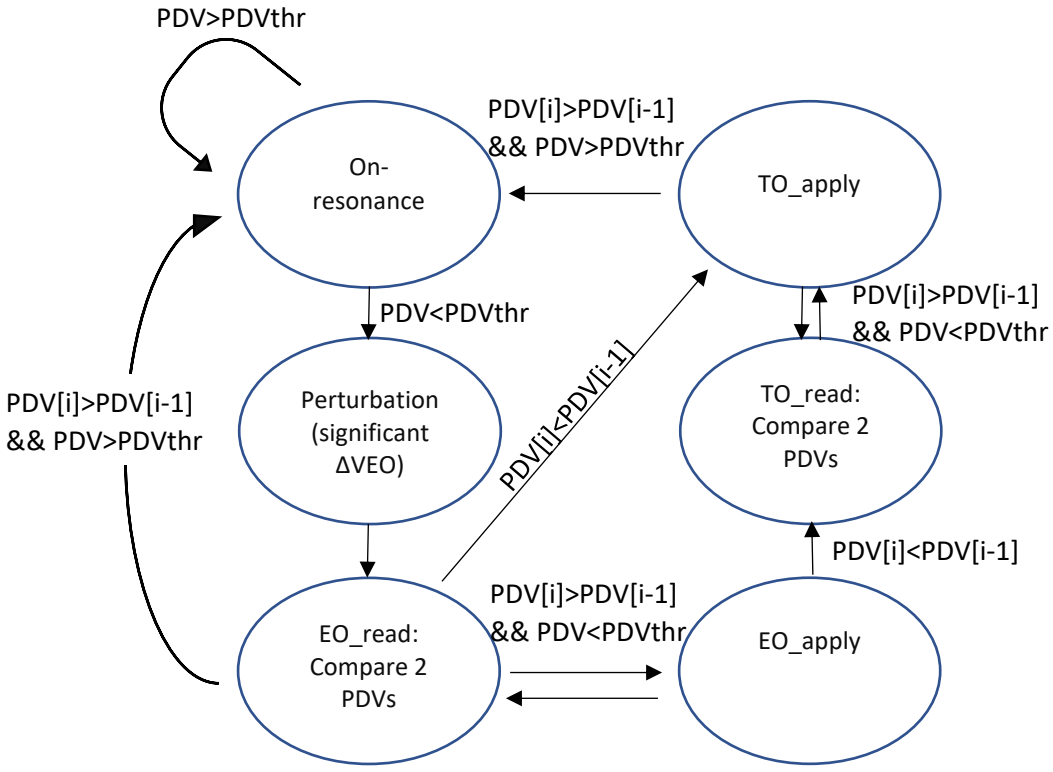

Figure 4.1 Revised FSM

4.2 Simulation of the control algorithm

To verify the correctness of the proposed algorithm, it is necessary to simulate it under ideal circumstances. The test bench of the simulation consists of two parts, namely EO test and TO test. The simulation results are shown in the following figures. In these figures, *rst* represents the binary value of reset button, *clk* represents clock, *Vread* is the read voltage from photodetector, *VTO* and *VEO* indicate the voltage of TO and EO respectively. Also, the values shown in the simulation are not physical values (the relation between those is shown in the conversion relations).

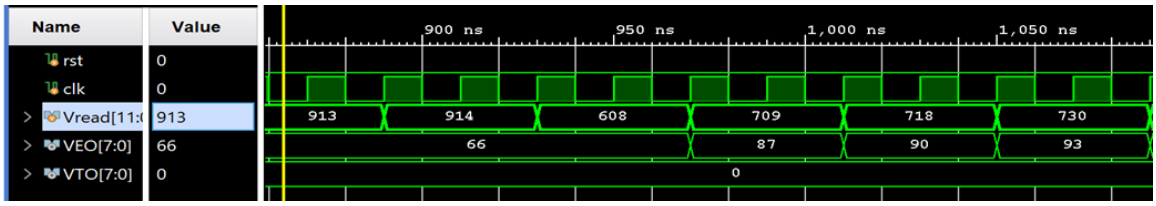

Figure 4.2 EO test during sudden change in Vread

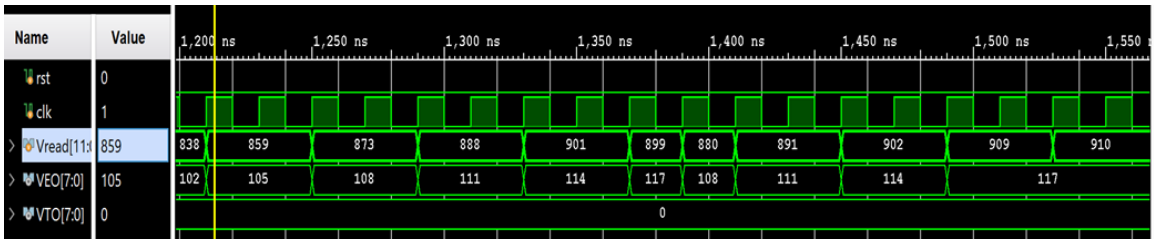

Figure 4.3 EO test after reaching the threshold voltage

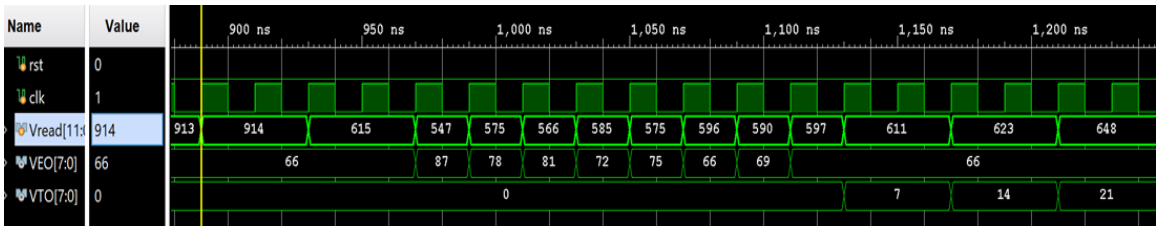

Figure 4.4 TO test during sudden change in Vread

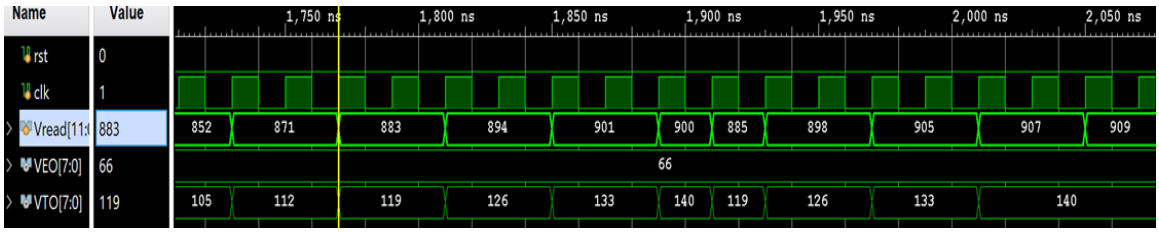

Figure 4.5 TO test after reaching the threshold voltage

CHAPTER FIVE RESULT AND EVALUATION

5.1 Experimental Setup

Figure 5.1 illustrates the experimental setup that we are currently using. Thermo Electric Cooler (TEC) is used to simulate temperature variation. Positive/negative temperature change can be produced by applying forward/reverse bias to the TEC. Silver paste is used to increase thermal conductivity between the photonic chip and the TEC. By simulating temperature change, the photocurrent will change and detected as the input to the FPGA. By control algorithm, FPGA will determine whether to apply voltage to the TO or EO to stabilize the resonance state of the photonic chip. The OPM is also used to observe the resonance status of the microring resonator.

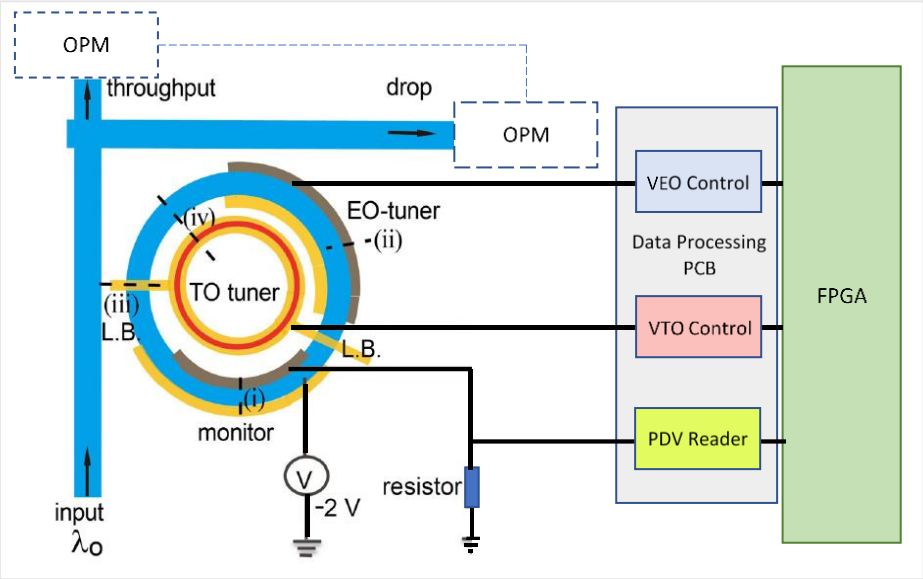

Figure 5.1 Experimental Setup

5.2 Result

Signal generator is used to generate signal to the TEC. Figure 5.2 shows our testing result by reading the OPM on throughput port while applying -1V to 1V (10 °C), 200mHz sinusoidal waveform to the TEC.

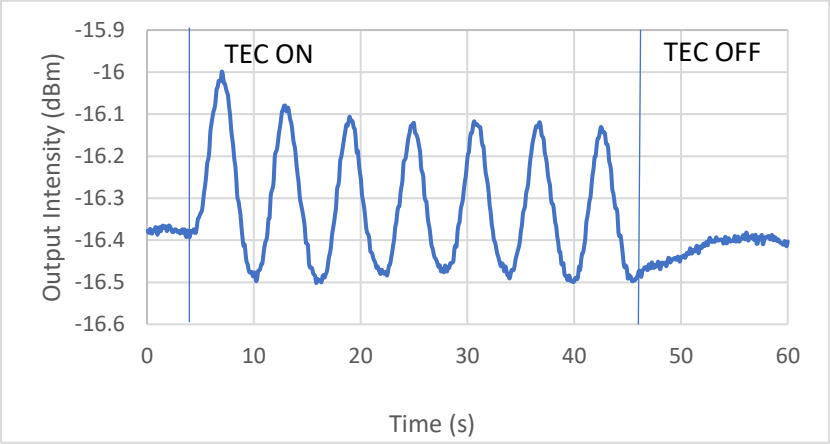

Figure 5.2 Testing result, -1V to 1V sinusoidal TEC perturbation, without active stabilization

4-channel oscilloscope is also used to measure the signal generator voltage, PD reading, TO voltage, and EO voltage. In our experiment, due to some issues, active stabilization has not been established yet. Evaluation regarding the issue will be done on the following part.

5.3 Evaluation

Since we have not successfully demonstrated the active stabilization in this project, evaluation is done to identify potential problems and how to address them in future part of this project.

5.3.1 Amplifying the PD voltage

As described in device characterization, photocurrent is used as the input to the feedback control algorithm. By shifting the wavelength from off-resonance to on-resonance, we observed that the photocurrent increases by ~30%. However, when we applied temperature variation to shift the resonance wavelength by applying voltage to the TEC, we observed that the photocurrent only drops by ~0.2% from its on-resonance value. This value is in the same order with the resolution of the FPGA input. Therefore, voltage amplification is necessary to get the feedback control system working.

5.3.2 Improving and debugging the FPGA code

After further analysis of our currently used setup, we also consider that the FPGA code might be the source of the failure. Since the response time of TO suggested by [5] is ~10μs and the clock cycle of our FPGA is 40ns, problem may occur because of this large difference. When the resonator is in off-resonance state and enters TO state, the algorithm will try to increase the TO voltage until the chip returns to in-resonance state. However, the algorithm will re-iterate this step in every clock cycle, while the TO tuner still does not have enough time to respond to the voltage change. The aftermath is resulting TO voltage stuck on the maximum value whenever the algorithm enters TO state. To solve this issue, we suggest two feasible solutions to be conducted, which are:

- Increasing the clock cycle to 10μs, however, the time to the active stabilization response time should be longer.
- Only using EO tuner with default voltage, however, the temperature range of active stabilization should be smaller.

CHAPTER SIX FUTURE WORKS

This chapter will discuss future works that can be done to resolve the issues and improve the overall quality of the feedback system.

6.1 Improved method for data measurement

Data measurement, in particular for EO and PD are incomplete due to technical limitation. In the experiment, we did not have a mechanism to continuously and precisely record the voltage and current data. Therefore, the data of photocurrent and EO tuner cannot be further analyzed. To overcome this technical limitation, we suggest equipment capable of measuring and recording multiple quantities (e.g. voltage and current) continuously, such as ones listed in the following.

- Pasco 550 Universal Interface + voltage/current sensor + Pasco Capstone (need quote)
- LabQuest Mini (US$203) + (Differential) Voltage/current probe (US$16-54 each) + Graphical Analysis (free)

Moreover, a semiconductor analyzer may be useful in future work on this project. Since both EO and PD are semiconductor, measuring the number of electrons and holes is needed for more accurate data analysis.

6.2 PCB design for the data processing circuit

After the final design of data processing circuit is established, we consider designing and printing PCB for future work. Printing PCB may serve several benefits, in terms of avoiding connection problem and better durability, replicability, and portability.

For the previous experiments, we used breadboards with few jump wires to connect all electrical components, e.g. resistors, ICs, TVS diodes, etc. Breadboards may be easier to create circuits with only few components because of its solderless connections and flexibility; however, it may not be the case for a more complex circuit. As more and more components and wires are added, it becomes more difficult to follow, recreate, and debug. Some holes or metal plates vary in firmness or depth, which might be a bug to test.

By designing the circuit into PCB, we may assemble and replicate more easily with software, e.g by Altium Designer. More compact design and soldering would connect components more firmly and prevent any unnecessary bugs from happening.

6.3 Extending the project to multiple switch

Should all the issues can be addressed successfully, this project should continue by actively stabilizing multiple microring resonators simultaneously. Zedboard FPGA has a limited number of I/O pins, therefore it could not control multiple switches simultaneously. Hence, a new processing circuit should be made and possibly in the form of PCB as described in part 6.2. With this new PCB, we could manipulate and control more tuners at once, which is more important in structures such as our 4-by-1 microring resonators. By simplifying and unifying the necessary I/O ports or pins, Zedboard could measure all 4 photocurrents at once which means it could also control tuners for each of the resonators.

CHAPTER SEVEN CONCLUSION

7.1 Summary

To summarize, in this UROP 1000 FPGA-controlled silicon photonic switches for datacenters project, we used Photodetector (PD) to measure the resonance state of the microring resonator, and Thermo-Optical (TO) tuner and Electro-Optical (EO) tuner to redshift and blueshift the resonance wavelength of the microring resonator. In this project, we have characterized the optical modulators (PD, TO, and EO), build the data processing circuit, and implemented the FPGA code. However, some problems are encountered during the testing of feedback control system. Therefore, active stabilization of silicon photonic chip has not been demonstrated yet. Evaluation is also done to identify potential problems and solve them in the future work of this project.

7.2 Afterword

We are pleased to be able to run this UROP 1000 project under the supervision of Prof. Andrew W. Poon and the PDL lab members. During this two-month summer period, we have had this exciting and challenging opportunity to explore and study a lot about photonics and its current state-of-art. We would also like to thank Kaiyi and Jiayang for guiding us for the experiments. We would like to apologize for any mistakes or disturbance during the project. Hopefully we could cooperate with this team in other wonderful opportunities ahead.

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