YUAN LI

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RESEARCH INTERESTS

My research focuses on delivering efficient and flexible communication support in heterogeneous manycores, specialized accelerators, and chiplet-based systems by incorporating network architectural innovation and emerging interconnection technologies such as silicon photonics.

EDUCATION

George Washington University — Washington, D.C.
Ph.D. in Computer Engineering — August 2017 – Present
Department of Electrical and Computer Engineering

University of Newcastle upon Tyne — Newcastle upon Tyne, U.K.
M.S. in Microelectronics — September 2010 – December 2011
School of Electrical, Electronic and Computer Engineering

University of Science and Technology of China (USTC) — Hefei, China
B.S. in Physics — September 2006 – June 2010
Department of Physics

PUBLICATIONS

[1] **Yuan Li**, Ahmed Louri, and Avinash Karanth. "SPACX: Silicon Photonics-based Chiplet Accelerator for DNN Inference." in *Proceedings of the 28th IEEE International Symposium on High-Performance Computer Architecture* ***(HPCA)***, 2022.

[2] **Yuan Li**, Ahmed Louri, and Avinash Karanth. "Scaling Deep Learning Inference with Chiplet-based Architecture and Photonic Interconnects." in *Proceedings of the 58th ACM/IEEE Design Automation Conference* ***(DAC)***, 2021.

[3] **Yuan Li**, Ke Wang, Hao Zheng, Ahmed Louri, and Avinash Karanth. "ASCEND: A Scalable and Energy-Efficient Deep Neural Network Accelerator with Photonic Interconnects." in *IEEE Transactions on Circuits and Systems I* ***(TCAS-I)***, 2022.

[4] **Yuan Li**, Ahmed Louri, and Avinash Karanth. "SPRINT: A High-Performance, Energy-Efficient, and Scalable Chiplet-based Accelerator with Photonic Interconnects for CNN Inference." in *IEEE Transactions on Parallel and Distributed Systems* ***(TPDS)***, 2021.

[5] **Yuan Li** and Ahmed Louri. "ALPHA: A Learning-Enabled High-Performance Network-on-Chip Router Design for Heterogeneous Manycore Architectures." in *IEEE Transactions on Sustainable Computing* ***(TSUSC)***, 2020.

[6] Ke Wang, Hao Zheng, **Yuan Li**, Jiajun Li, and Ahmed Louri. "AGAPE: Anomaly Detection with Generative Adversarial Network for Improved Performance, Energy, and Security in Manycore Systems." in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition* ***(DATE)***, 2022.

[7] Ke Wang, Hao Zheng, **Yuan Li**, and Ahmed Louri. "SecureNoC: A Learning-Enabled, High-Performance, and Secure On-Chip Communication Framework Design." in *IEEE Transactions on Sustainable Computing* ***(TSUSC)***, 2021.

HONORS AND AWARDS

- Lin Wen Graduate Scholarship, George Washington University — 2021
- NSF I-Corps Site Grant Award, George Washington University — 2019
- EECE Postgraduate Scholarship, University of Newcastle upon Tyne — 2010
- Outstanding Freshman Scholarship, University of Science and Technology of China — 2006

TEACHING EXPERIENCE

Teaching Assistant 2021
- Data Structures and Algorithms (ECE 1125.30)
- Computer Architecture and Design (ECE 4535.81 / 6005.81)

Teaching Assistant 2020
- Data Structures and Algorithms (ECE 1125.30)
- Computer Architecture and Design (ECE 4535.81 / 6005.81)

RESEARCH EXPERIENCE

Silicon Photonics and Chiplet based Deep Neural Network (DNN) Hardware Accelerators 2020 – present
- Explored the use of silicon photonics technology to overcome the communication challenges in DNN hardware accelerators
- Designed and simulated photonic interconnection networks that adapt to various general and tailored dataflows for high-performance and energy-efficient communication in DNN hardware accelerators, with a collection of simulators and tools including *Timploop*, *MAESTRO*, *DRAMSim*, *CACTI*, *DSENT*, and *Synopsys Design Compiler*
- Delivered two conference papers (HPCA' 22 and DAC' 21) and two journal papers (TCAS-I and TPDS)

DRAM and Non-Volatile Memory (NVM) Integration and Management in Chiplet based Systems 2019 – 2020
- Explored integration of DRAM and NVM stacks in 2.5D systems with heterogeneous chiplets
- Developed a data exchange mechanism between DRAM and NVM stacks and corresponding hardware modifications targeting actively moving memory pages with high access count yet short access time frame to DRAM stacks
- Simulated the data exchange mechanism and hardware architecture with *Gem5-GPU*, *DRAMSim*, *CACTI*, and *DSENT*

Efficient Network-on-Chip for Accelerator-Rich Heterogeneous Manycore Systems 2018 – 2019
- Developed a Network-on-Chip router microarchitecture and an artificial neural network (ANN) based mechanism to alleviate local and global contention for high-throughput and low-latency communication
- Simulated the router microarchitecture and ANN mechanism with *Gem5*, *Gem5-GPU*, *DSENT*, and *Synopsys Design Compiler*
- Delivered one journal paper (TSUSC)

Intelligent Hardware Trojan (HT) Detection in Secure Network-on-Chip Architectures 2021 – present
- Participated in developing runtime accurate HT detection modules in Network-on-Chip architectures using multilayer perceptron (MLP) and generative adversarial network (GAN) models
- Participated in power and area evaluation of HT detection modules with *DSENT* and *Synopsys Design Compiler*
- Delivered one conference paper (DATE' 22) and one journal paper (TSUSC)

RELEVANT TECHNICAL COURSEWORK

Computer Architecture Modeling
- Processor microarchitecture and memory hierarchy modeling with *WinMIPS64*, *Dinero*, *SimpleScalar*, and *Gem5*
- Network-on-Chip modeling with *BookSim*, *Gem5*, and *DSENT*

Embedded System Design
- Data acquisition and motion control system design with *NI LabVIEW* and *NI PXI & CompactRIO*
- Data acquisition system design with *Microchip PIC18 controllers* and *MPLAB X IDE*

Printed Circuit Board (PCB) Design
- Signal processing, thermal control, and fiber-optic communication PCBs design with *NI Multisim* and *Altium Designer*

Design for Testability (DFT)
- Multi-cycle MIPS processor scan flops synthesis and ATPG with *Synopsys Design Vision* and *Synopsys TetraMAX*

HDL Programming and Synthesis
- Digital filter implementation with *VHDL* and *FLEX EPF10K70 FPGA*
- Single-cycle MIPS processor design and implementation with *Verilog* and *Cyclone IV EP4CE115 FPGA*
- Multi-cycle MIPS processor design and synthesis with *Verilog*, *Cadence SimVision*, and *Synopsys Design Vision*
- Virtual channel Network-on-Chip router design and synthesis with *Verilog*, *Cadence SimVision*, and *Synopsys Design Vision*

Integrated Circuit Layout Design
- D flip-flop layout design with *Cadence Virtuoso*
- Multi-cycle MIPS processor layout design and routing with *Cadence Virtuoso* and *Cadence Encounter*

Device Simulation and Fabrication
- MOS transistor scaling and simulation with *Synopsys TSUPREM-4*
- Device fabrication training with 0.16 μm process technology at INEX Microtechnology Ltd.

PRESENTATIONS

[1] "SPACX: Silicon Photonics-based Chiplet Accelerator for DNN Inference", 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Virtual Conference, April 2022.

[2] "Scaling Deep Learning Inference with Chiplet-based Architecture and Photonic Interconnects", 58th ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, December 2021.

SERVICE AND TECHNICAL REVIEWING

Conference Reviewer/Sub-Reviewer

- ACM/IEEE International Symposium on Computer Architecture (ISCA) 2019, 2022
- IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2020, 2021
- IEEE/ACM International Symposium on Networks-on-Chip (NOCS) 2018, 2019
- IEEE International Conference on Computer Design (ICCD) 2018

Journal Reviewer

- IEEE Transactions on Emerging Topics in Computing 2018

PROGRAMMING LANGUAGES AND DESIGN TOOLS EXPERIENCE

Programming Language
C/C++, *Python*, *Visual Basic*, *MATLAB*, *HTML*, *LaTeX*, *Bash*, *Assembly*, *Verilog/VHDL*

Design Tool
Gem5, *Gem5-GPU*, *SimpleScalar*, *Timeloop*, *MAESTRO*, *DRAMSim*, *Dinero*, *BookSim*, *WinMIPS64*, *CACTI*, *DSENT*
LabVIEW, *MPLAB X IDE*, *NI Multisim*, *Altium Designer*
Synopsys TetraMAX, *Altera Quartus II*, *Cadence SimVision*, *Cadence Virtuoso/Encounter*, *Synopsys Design Vision*, *Synopsys TSUPREM-4*