

ΑΣΚΗΣΗ 1

ΟΙ 4 ΕΙΣΟΔΟΙ A,B,C,D

ΟΙ 4 ΕΞΟΔΟΙ X,Y,Z,W

a	b	c	d	Μετατροπή		x	y	z	w
				δυαδικό σε Gray					
0	0	0	0			0	0	0	0
0	0	0	1			0	0	0	1
0	0	1	0			0	0	1	1
0	0	1	1			0	0	1	0
0	1	0	0			0	1	1	0
0	1	0	1			0	1	1	1
0	1	1	0			0	1	0	1
0	1	1	1			0	1	0	0
1	0	0	0			1	1	0	0
1	0	0	1			1	1	0	1
1	0	1	0			1	1	1	1
1	0	1	1			1	1	1	0
1	1	0	0			1	0	1	0
1	1	0	1			1	0	1	1
1	1	1	0			1	0	0	1
1	1	1	1			1	0	0	0

Όπως δείχνουν οι πίνακες κρατάμε το α συνεχώς ίδιο δηλαδή $a=x$ στην μετατροπή μας.

Απλοποιώ την λύση στο μυαλό μου χρησιμοποιώ μόνο δυο εισόδους και δυο εξόδους

a,b

x,y

Παρατηρώ έτσι ότι μας ενδιαφέρει μόνο η γ εξόδους

Χρησιμοποιώ Karnaugh για να απλοποιήσω την λύση

a\b	0	1
0	0	1
1	1	0

a	b	x	y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

$ab' + a'b = a \oplus b$ με πύλη xor

Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3ask1/ask1 - ask1

File Edit View Project Assignments Processing Tools Window Help

The screenshot shows the Quartus II IDE with a logic design in the center and a compilation report on the right. The logic design is a simple circuit with four inputs (a, b, c, d) and four outputs (X, Y, W, Z). Each input is connected to a buffer (BUF) and then to an AND gate (AND). The outputs of the AND gates are connected to the outputs X, Y, W, and Z. The compilation report on the right shows the following tasks and their durations:

Task	Time
Compile Design	00:00:12
Analysis & Synthesis	00:00:02
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:02
TimeQuest Timing Analysis	00:00:02
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

The Messages window at the bottom shows the following messages:

```
'vnt' TD Message
> Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
> 293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```

Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3ask1/ask1 - ask1

File Edit View Project Assignments Processing Tools Window Help

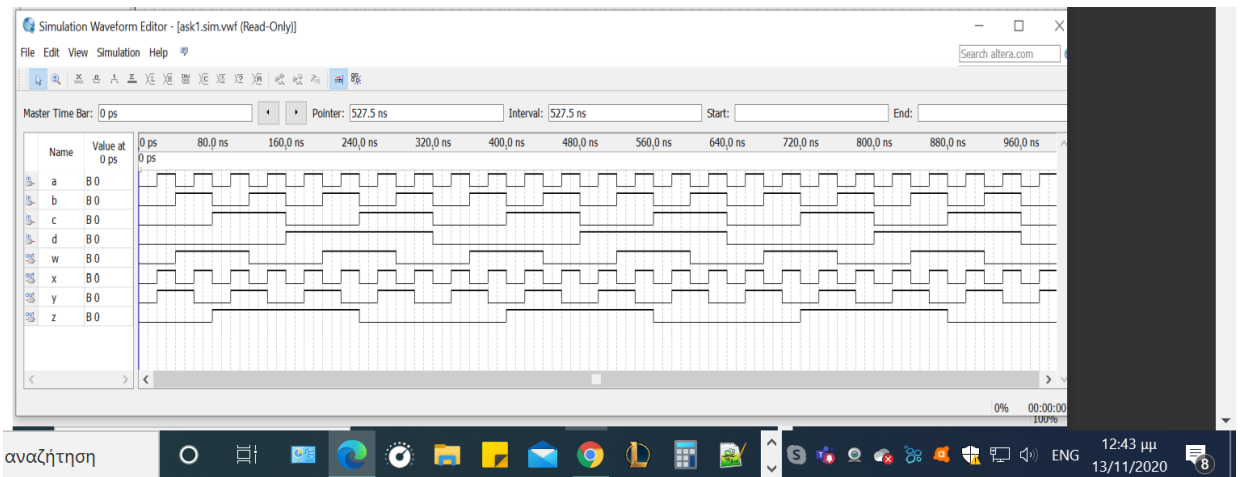
The screenshot shows the Quartus II IDE with a logic design in the center and a flow summary table on the right. The logic design is a simple circuit with four inputs (a, b, c, d) and four outputs (X, Y, W, Z). Each input is connected to a buffer (BUF) and then to an AND gate (AND). The outputs of the AND gates are connected to the outputs X, Y, W, and Z. The flow summary table on the right shows the following information:

Table	Flow Summary
Flow Status	Successful - Fri Nov 06 21:30:38 2020
Flow Set	Quartus II 64-Bit Version
Revision Name	ask1
Top-level Entity Name	ask1
Family	Cyclone II
Device	EP2K35F672C6
Timing Models	Final
Total logic elements	3 / 33,216 (< 1 %)
Total combinational functions	3 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	8 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

A dialog box titled "Quartus II" is displayed, showing the message: "Full Compilation was successful (12 warnings)".

The Messages window at the bottom shows the following messages:

```
'vnt' TD Message
> Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
> 293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```



Ασκηση 3:

a	b	c	d	Συμπληρωμα συμπληρωμα ως προς 9=1010 wxyz=(abcd)'+9	w	x	y	z
0	0	0	0		1	0	0	1
0	0	0	1		1	0	0	0
0	0	1	0		0	1	1	1
0	0	1	1		0	1	1	0
0	1	0	0		0	1	0	1
0	1	0	1		0	1	0	0
0	1	1	0		0	0	1	1
0	1	1	1		0	0	1	1
1	0	0	0		0	0	0	1
1	0	0	1		0	0	0	0

Για απλοποίηση του w χρησιμοποιώ Karnaugh

ab\cd	0	1	11	10
0	1	1	0	0
1	0	0	0	0
11	0	0	0	0
10	0	0	0	0

$$W = a'b'c'd' + a'b'cd = a'b'c'(d+d') = a'b'c'$$

Για το x χρησιμοποιω karnagh για απλοποιηση :

ab\cd	0	1	11	10
0	0	0	1	1
1	1	1	0	0
11	0	0	0	0
10	0	0	0	0

$X = b \oplus c$ διοτι,

$$X = a'b'c'd' + a'bc'd + a'b'cd + a'b'cd' =$$

$$= a'b'c'(d+d') + a'b'c(d=d') = a'b'c' + a'b'c = bc' + b'c$$

Για το y:

ab\cd	0	1	11	10
0	0	0	1	1
1	0	0	1	1
11	0	0	0	0
10	0	0	0	0

$$Y = cdb' + cd'b' + cdb + cd'b = cb'(d'+d) + cb(d+d') = cb' + cb = c(b+b)$$

$$Y = c;$$

Ωστοσο για την τελευταια εξοδο z δεν χρειαζομαι karnaugh

Αφου παρατηρω από την πινακα αληθειας $z = d'$

~για να ανιχνευσουμε το λαθος στον πινακα αληθειας σε ποια περιπτωση

ο πινακας bcd είναι μεγαλυτερος του 1001. Αρκει οι τιμες του b/c να είναι ταυτοχρονα 1

$$\text{Αρα fault} = a + (bc)$$

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ergasthrio3_ask2

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
- ergasthrio3_ask2

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	00:00:11
Analysis & Synthesis	00:00:01
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:03
TimeQuest Timing Analysis	00:00:01
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

ergasthrio3_ask2.bdf

Compilation Report - ergasthrio3_ask2

Logic diagram showing inputs a, b, c, d connected to inverters, AND gates, and OR gates, resulting in outputs w, x, y, z, and faul.

Messages

System (2) Processing (100)

Message

Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings

Project Navigator

Entity

- Cyclone II: EP2C35F672C6
- ergasthrio3_ask2

Flow Summary

Flow Status	Successful - Fri Nov 06 23:51:20 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ergasthrio3_ask2
Top-level Entity Name	ergasthrio3_ask2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	3 / 33,216 (< 1 %)
Total combinational functions	3 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	9 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Tasks

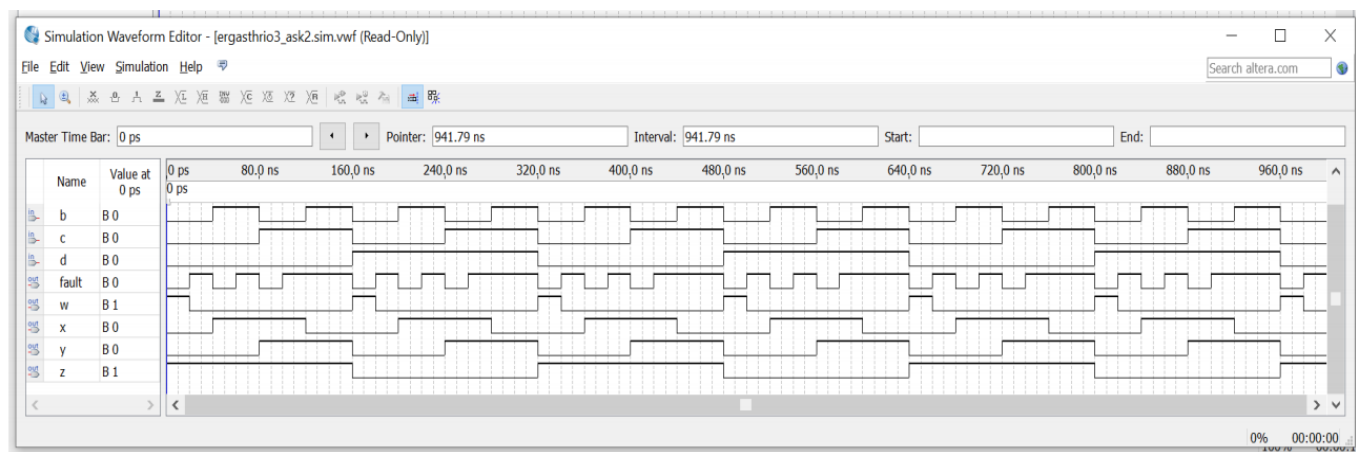
Flow: Compilation Customize...

Task	Time
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Analysis & Synthesis	00:00:01
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:03
TimeQuest Timing Analysis	00:00:01
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

Messages

System (2) / Processing (100)

402, 62 100%



ΑΣΚΗΣΗ 3:

Αφου η εκφωνηση μας λειει 3 εισοδους .επομενως φτανει μεχρι το 3

x	-4	-3	-2	-1	0	1	2	3
y	10	3	-2	-5	-6	-5	-2	-3

Αρα χρειαζομαστε 4 εξοδους και 1 για το προσημο :

Στον πινακα θα βαλω για μεγαλυτερη ευκολια αντι για x1,x2,x3 a,b,c

a	b	c	ΜΕΤΑΤΡΟΠΗ			y1	y2	y3	y4	y5
			Συμπληρωμα ως προς 2							
1	0	0				0	1	0	1	0
1	0	1				0	0	0	1	1
1	1	0				1	1	1	1	0
1	1	1				1	1	0	1	1
0	0	0				1	1	0	1	0
0	0	1				1	1	0	1	1
0	1	0				1	1	1	1	0
0	1	1				0	0	0	1	1

Για την y1 θα κανουμε karnagh

a\bc	0	1	11	10
0	1	1	0	1
1	0	0	1	1

$$Y1=a'b'+ab+a'c'$$

Για την y2 κανουμε Karnaugh:

a\bc	0	1	11	10
0	1	1	0	1
1	1	0	1	1

$$Y2=a'b'+c'+ab$$

Για την y3 κανουμε Karnaugh:

a\bc	0	1	11	10
0	0	0	0	1
1	0	0	0	1

$$Y3=a'b$$

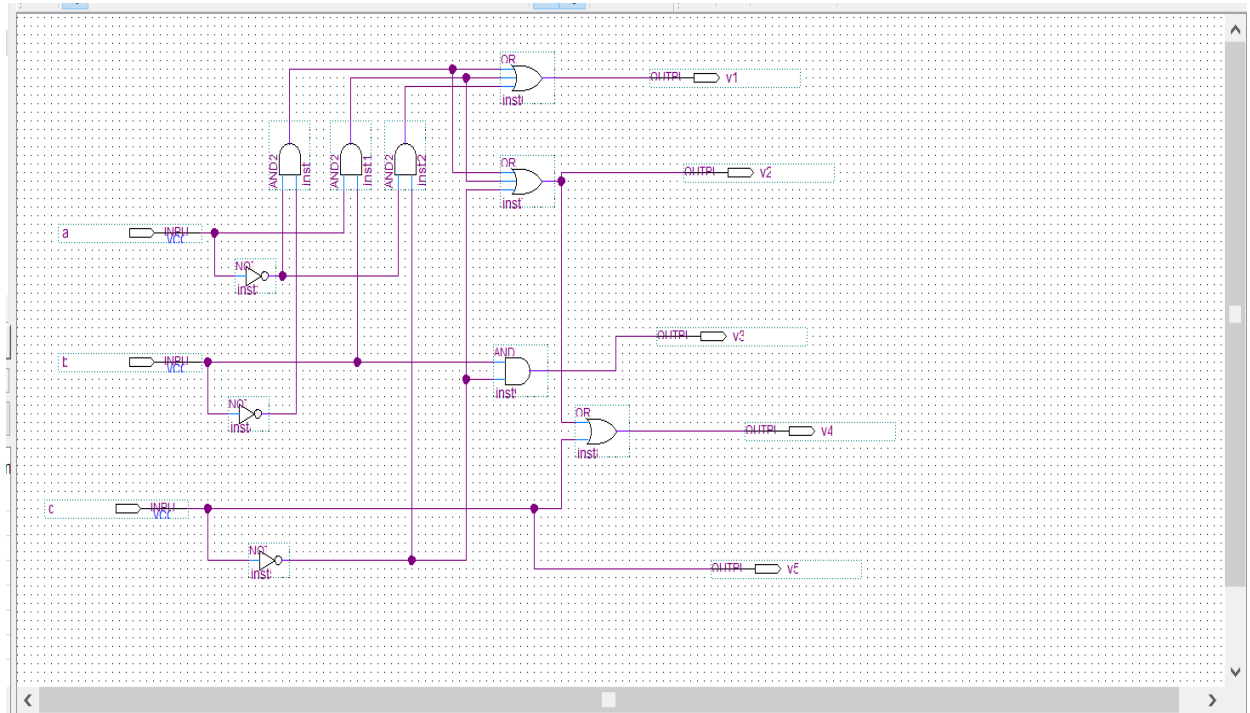
Για την y4 παρατηρω ότι είναι συνεχεια 1

$$\text{Οποτε } y4=1$$

Για την γ5 χρησιμοποιω Karnaugh:

a\bc	0	1	11	10
0	0	1	1	0
1	0	1	1	0

$Y5=c$



Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3ask3/ergasthrio3ask3 - ergasthrio3ask3

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Project Navigator

Entity	Logic Cells	Dedicated Logic F
Cyclone II: EP2C35F672C6	3 (3)	0 (0)
ergasthrio3ask3		

Flow Summary

Flow Status: Successful - Fri Nov 13 15:52:24 2020

Quartus II 64-Bit Version: 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition

Revision Name: ergasthrio3ask3

Top-level Entity Name: ergasthrio3ask3

Family: Cyclone II

Device: EP2C35F672C6

Timing Models: Final

Total logic elements: 3 / 33,216 (< 1 %)

Total combinational functions: 3 / 33,216 (< 1 %)

Dedicated logic registers: 0 / 33,216 (0 %)

Total registers: 0

Total pins: 0

Total virtual pins: 0

Total memory bits: 0

Embedded Multiplier 9

Total PLLs: 0

Quartus II

Full Compilation was successful (14 warnings)

OK

Tasks

Flow: Compilation

Task

Task	Time
Compile Design	00:00:13
Analysis & Synthesis	00:00:03
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:02
TimeQuest Timing Analysis	00:00:02
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

Messages

System / Processing (101)

457, -19 100% 00:00:13

Πληκτρολογήστε εδώ για αναζήτηση

W X

ENG 3:52 μμ 13/11/2020

