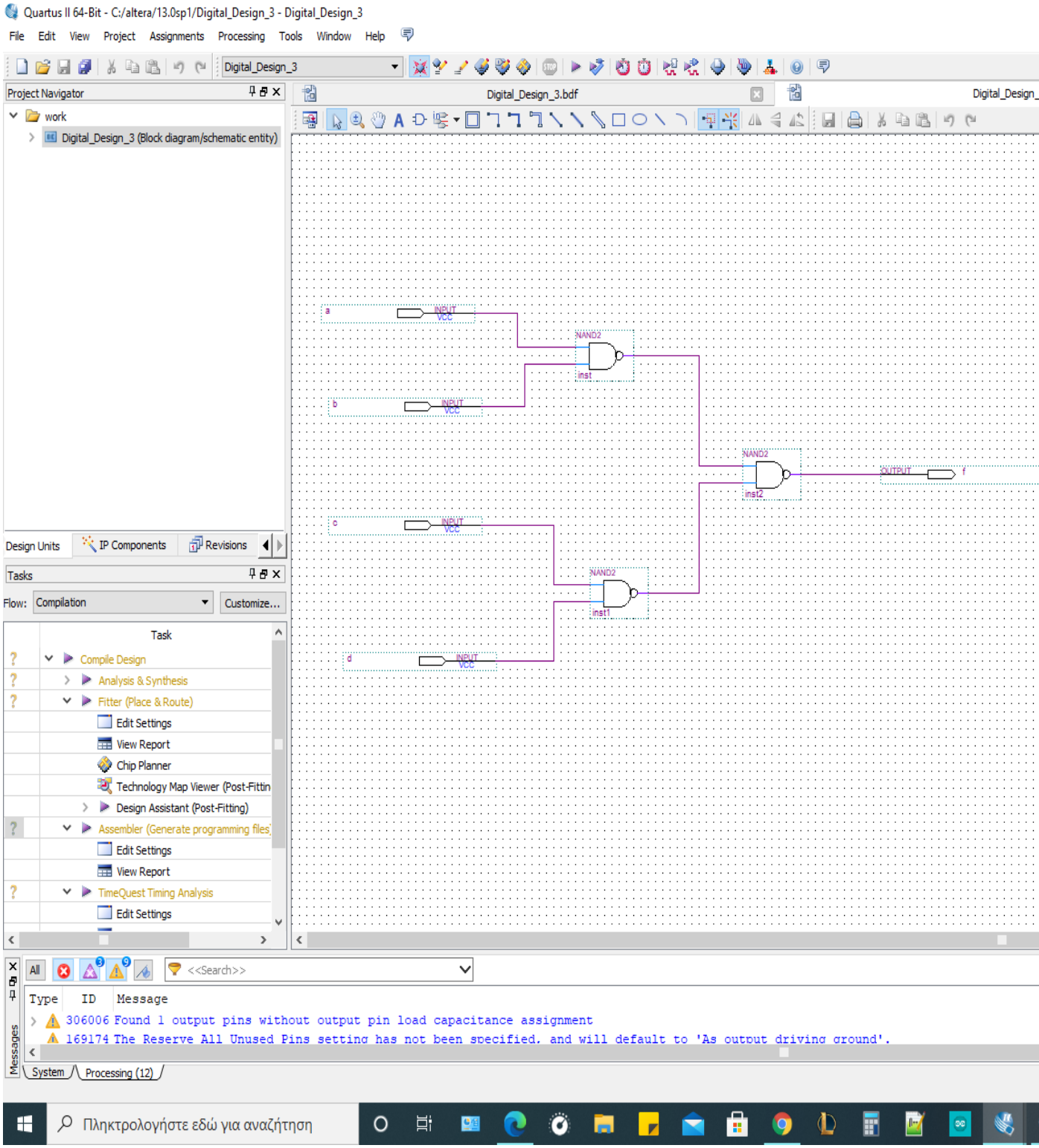
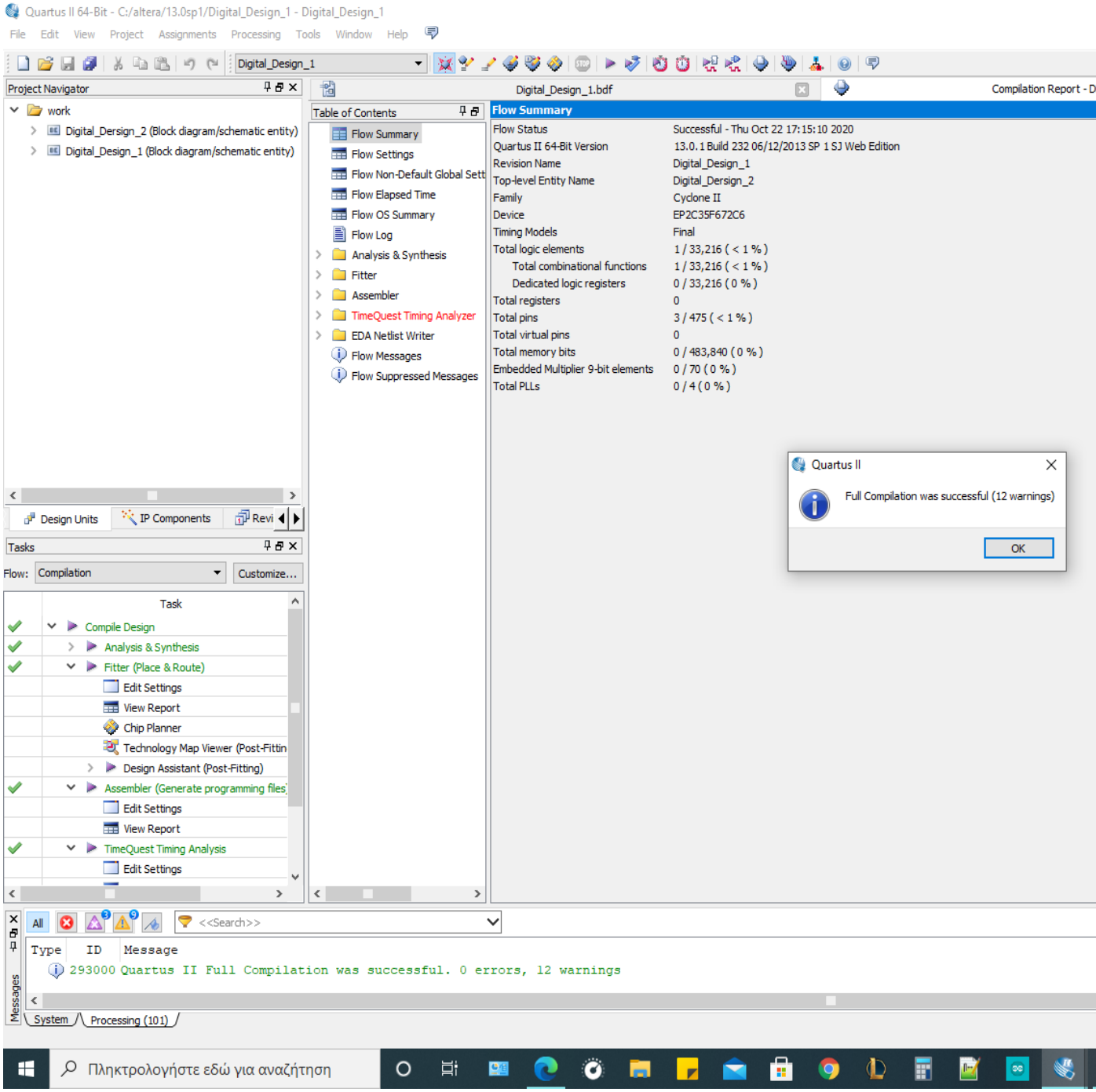
ΓΙΩΡΓΟΣ ΧΑΤΖΗΛΙΓΟΣ ΑΜ4835

ΕΡΩΤΗΜΑ 1




Quartus II 64-Bit - C:/altera/13.0sp1/Digital_Design_1 - Digital_Design_1
File Edit View Project Assignments Processing Tools Window Help
Digital_Design_1
Project Navigator
work
Digital_Dersign_2 (Block diagram/schematic entity)
Digital_Design_1 (Block diagram/schematic entity)
Design Units
IP Components
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Edit Settings
View Report
Chip Planner
Technology Map Viewer (Post-Fittin
Design Assistant (Post-Fitting)
Assembler (Generate programming files
Edit Settings
View Report
TimeQuest Timing Analysis
Edit Settings
Digital_Design_1.bdf
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Flow Summary
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Flow Non-Default Global Sett
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Compilation Report - D
Flow Summary
Flow Status Successful - Thu Oct 22 17:15:10 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name Digital_Design_1
Top-level Entity Name Digital_Dersign_2
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 1 / 33,216 (< 1 %)
Total combinational functions 1 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 3 / 475 (< 1 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
Quartus II
Full Compilation was successful (12 warnings)
OK
All
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (101)
Πληκτρολογήστε εδώ για αναζήτηση

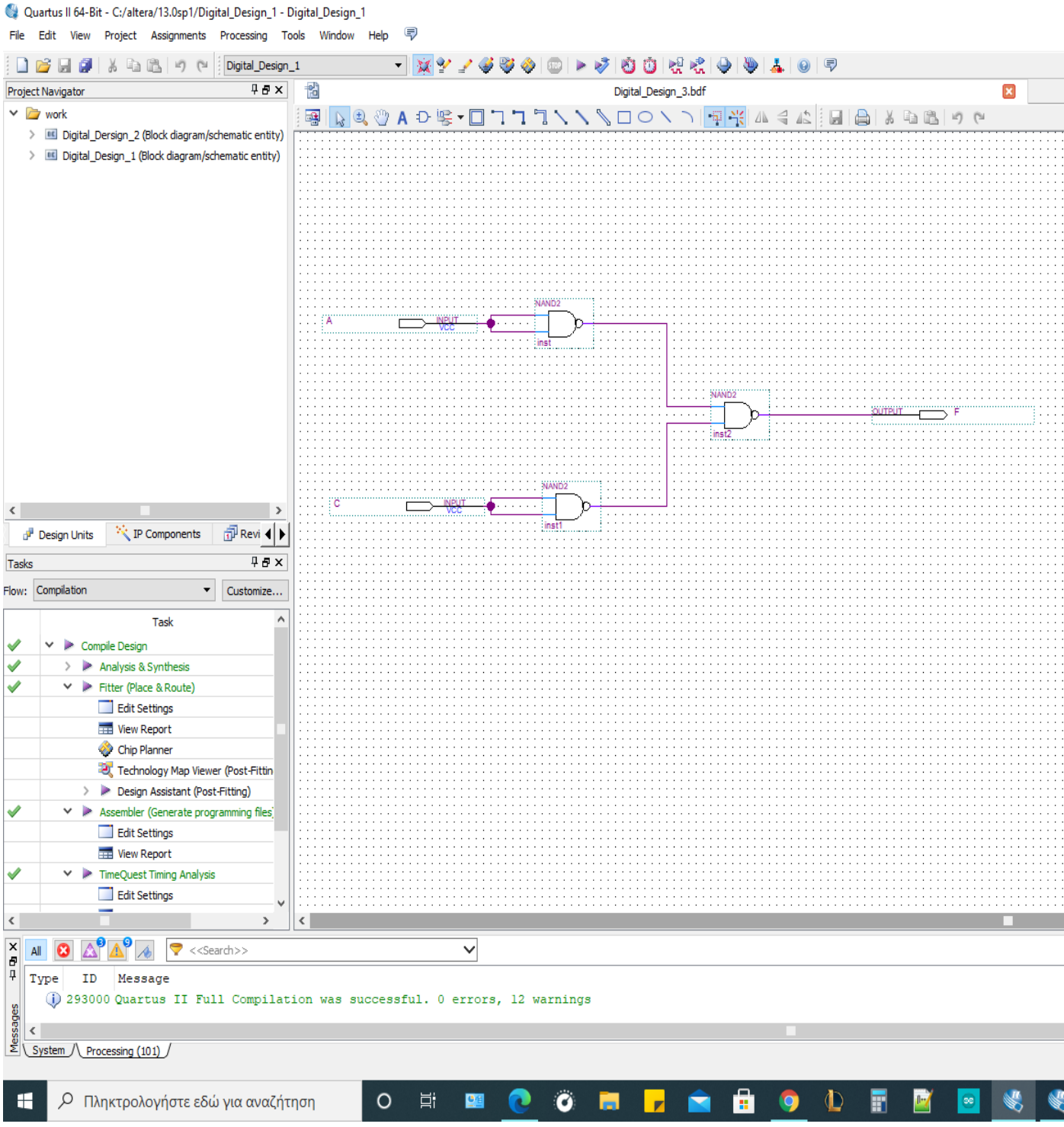
Εργαστηριακή Άσκηση (1) ΑΜ4835

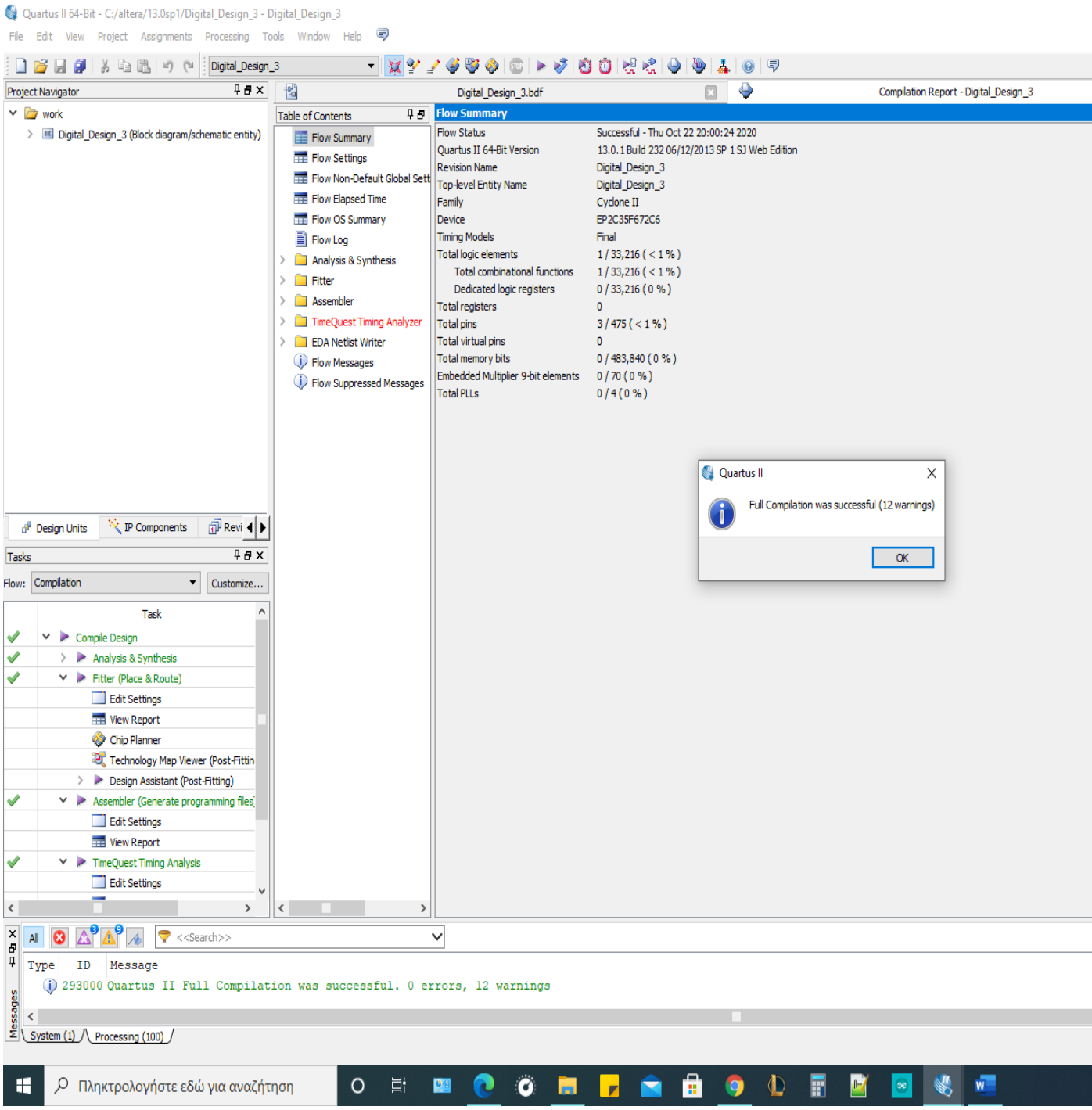
Πίνακας αλήθειας για την Συνάρτηση

$f(a,b,c,d) = (a \cdot b)'(c \cdot d)'$

a	b	c	d	a·b	cd	(ab)'	(cd)'	(ab)'(cd)'
0	0	0	0	0	0	1	1	1
0	0	0	1	0	0	1	1	1
1	0	0	0	0	0	1	1	1
0	0	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1
0	0	1	1	0	1	1	0	0
0	1	0	1	0	0	1	1	1
1	1	0	0	1	0	0	1	0
1	1	1	0	1	0	0	1	0
1	0	1	1	0	1	1	0	0
0	1	1	1	0	1	1	0	0
1	1	0	1	1	0	0	1	0
1	1	1	1	1	1	0	0	0
1	0	0	1	0	0	1	1	1

Ερωτημα2


Quartus II 64-Bit - C:/altera/13.0sp1/Digital_Design_1 - Digital_Design_1
File Edit View Project Assignments Processing Tools Window Help
Digital_Design_1
Project Navigator
work
Digital_Dersign_2 (Block diagram/schematic entity)
Digital_Design_1 (Block diagram/schematic entity)
Design Units
IP Components
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Edit Settings
View Report
Chip Planner
Technology Map Viewer (Post-Fittin
Design Assistant (Post-Fitting)
Assembler (Generate programming files
Edit Settings
View Report
TimeQuest Timing Analysis
Edit Settings
Digital_Design_3.bdf
A
INPUT
VCC
NAND2
inst
C
INPUT
VCC
NAND2
inst1
NAND2
inst2
OUTPUT
F
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (101)
Πληκτρολογήστε εδώ για αναζήτηση


Quartus II 64-Bit - C:/altera/13.0sp1/Digital_Design_3 - Digital_Design_3
File Edit View Project Assignments Processing Tools Window Help
Digital_Design_3
Project Navigator
work
Digital_Design_3 (Block diagram/schematic entity)
Design Units
IP Components
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Edit Settings
View Report
Chip Planner
Technology Map Viewer (Post-Fittin
Design Assistant (Post-Fitting)
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View Report
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Edit Settings
Digital_Design_3.bdf
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Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Compilation Report - Digital_Design_3
Flow Summary
Flow Status Successful - Thu Oct 22 20:00:24 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name Digital_Design_3
Top-level Entity Name Digital_Design_3
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 1 / 33,216 (< 1 %)
Total combinational functions 1 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
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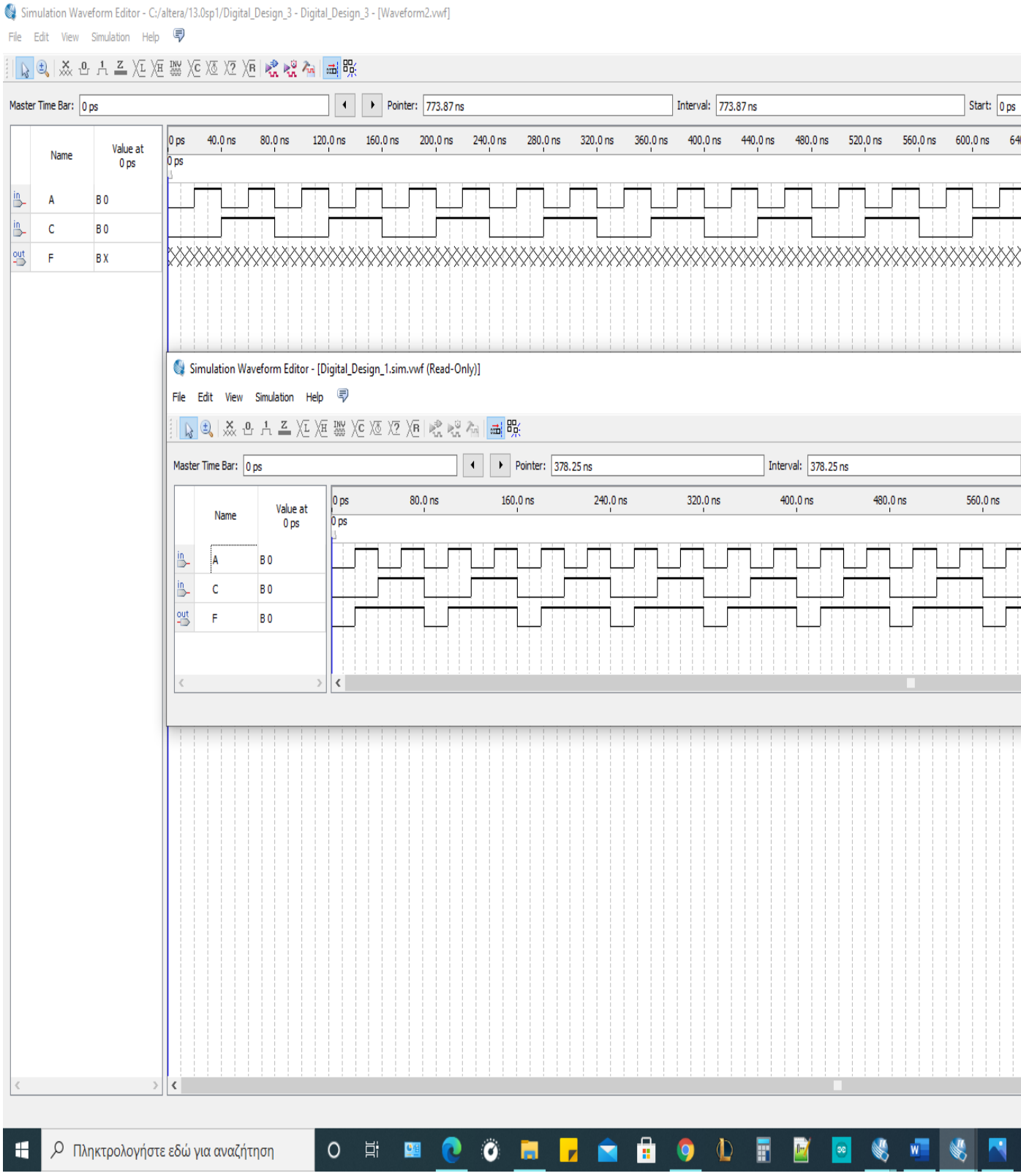
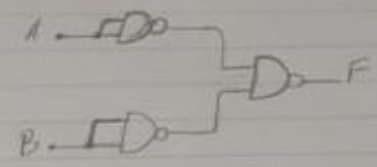
Quartus II
Full Compilation was successful (12 warnings)
OK
All
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System (1)
Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση


Simulation Waveform Editor - C:/altera/13.0sp1/Digital_Design_3 - Digital_Design_3 - [Waveform2.vwf]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 773.87 ns
Interval: 773.87 ns
Start: 0 ps
Name
Value at 0 ps
A B 0
C B 0
F B X
0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns
Simulation Waveform Editor - [Digital_Design_1.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 378.25 ns
Interval: 378.25 ns
Name
Value at 0 ps
A B 0
C B 0
F B 0
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns
Πληκτρολογήστε εδώ για αναζήτηση

Άσκηση ②

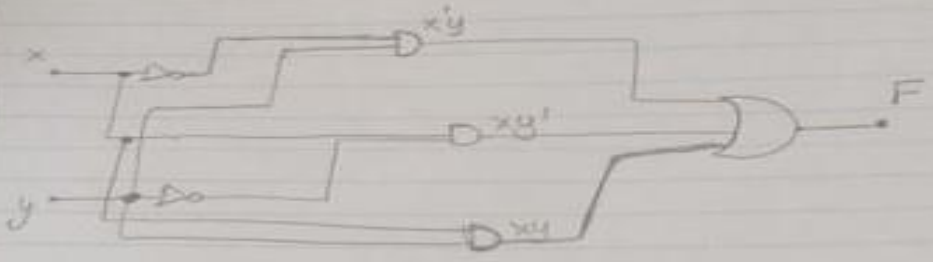


Σύμφωνα με την αλγεβρα Boole

$F=((AA)'\cdot(CC)')'=(A+A')\cdot(C'+C')'=(A'\cdot C')'=A+C$

ΕΡΩΤΗΜΑ 3

$F=xy+x'y+y'x$



Η απλοποίηση γίνεται:

$F=xy+x'y+xy'=y(x+x')+y'x$

Ή

$F=xy+xy+xy'=xy+x(y+y')=xy+x$

• Είναι φτηνότερη η απλοποίηση διότι χρησιμοποιούμε λιγότερα καλώδια, σύνδεσμους, διακόπτες