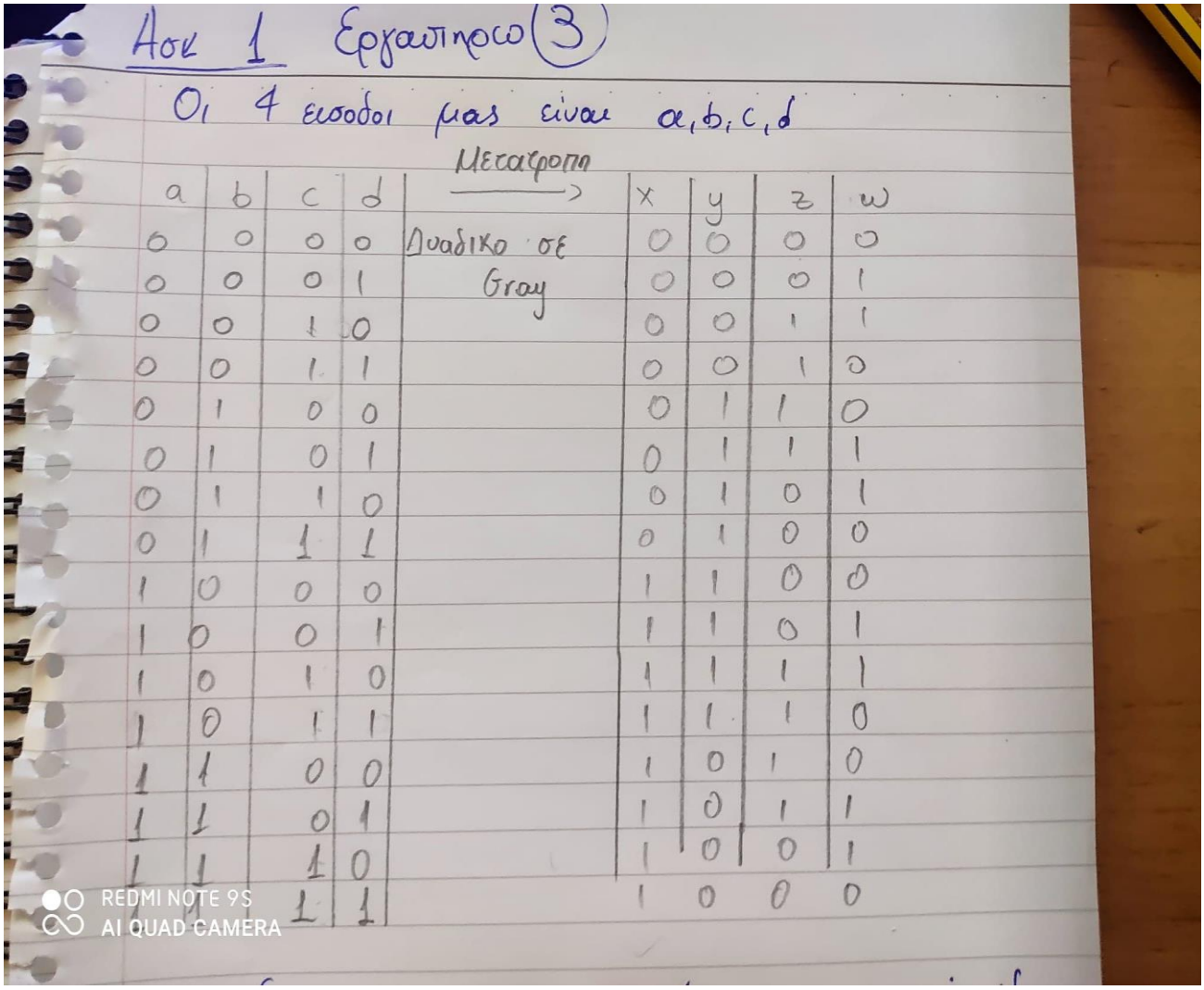
ΓΙΩΡΓΟΣ ΧΑΤΖΗΛΙΓΟΣ ΑΜ4835

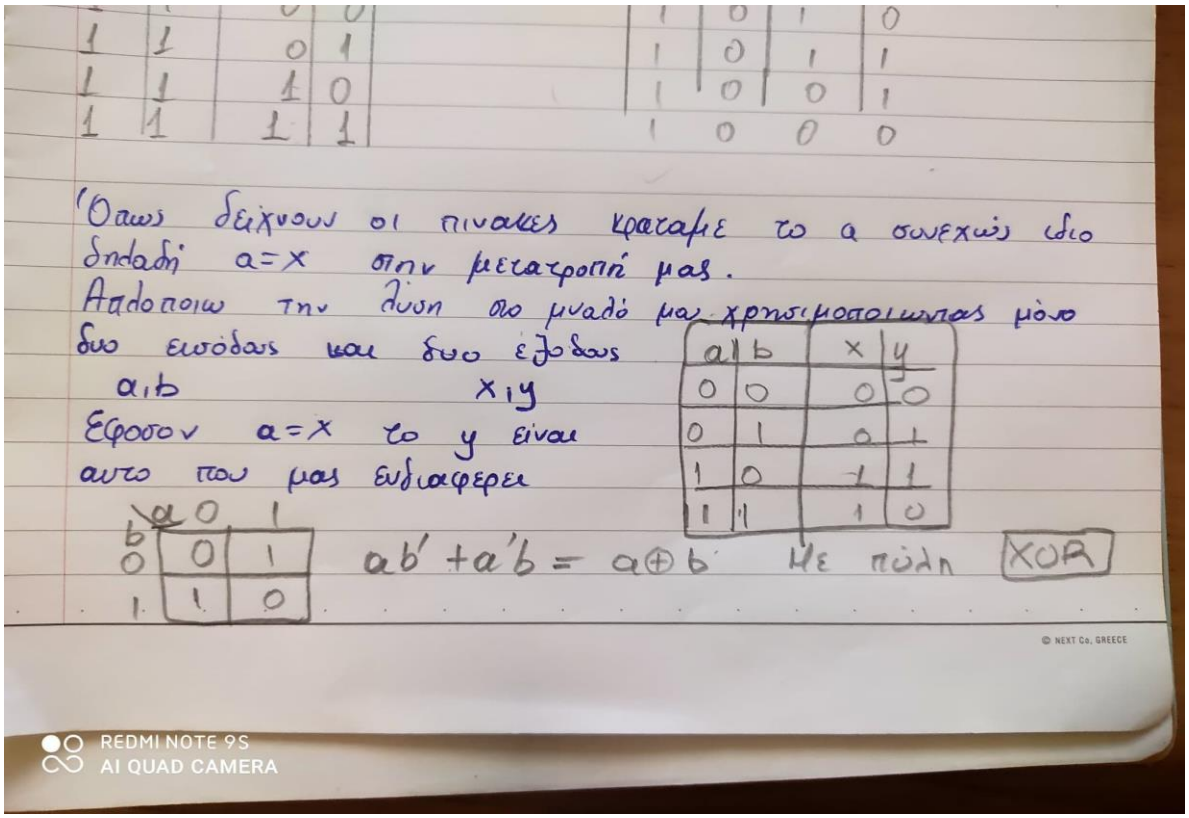


Ασκ 1 Εργαστηριο (3)

Οι 4 εισοδοι μας είναι a, b, c, d

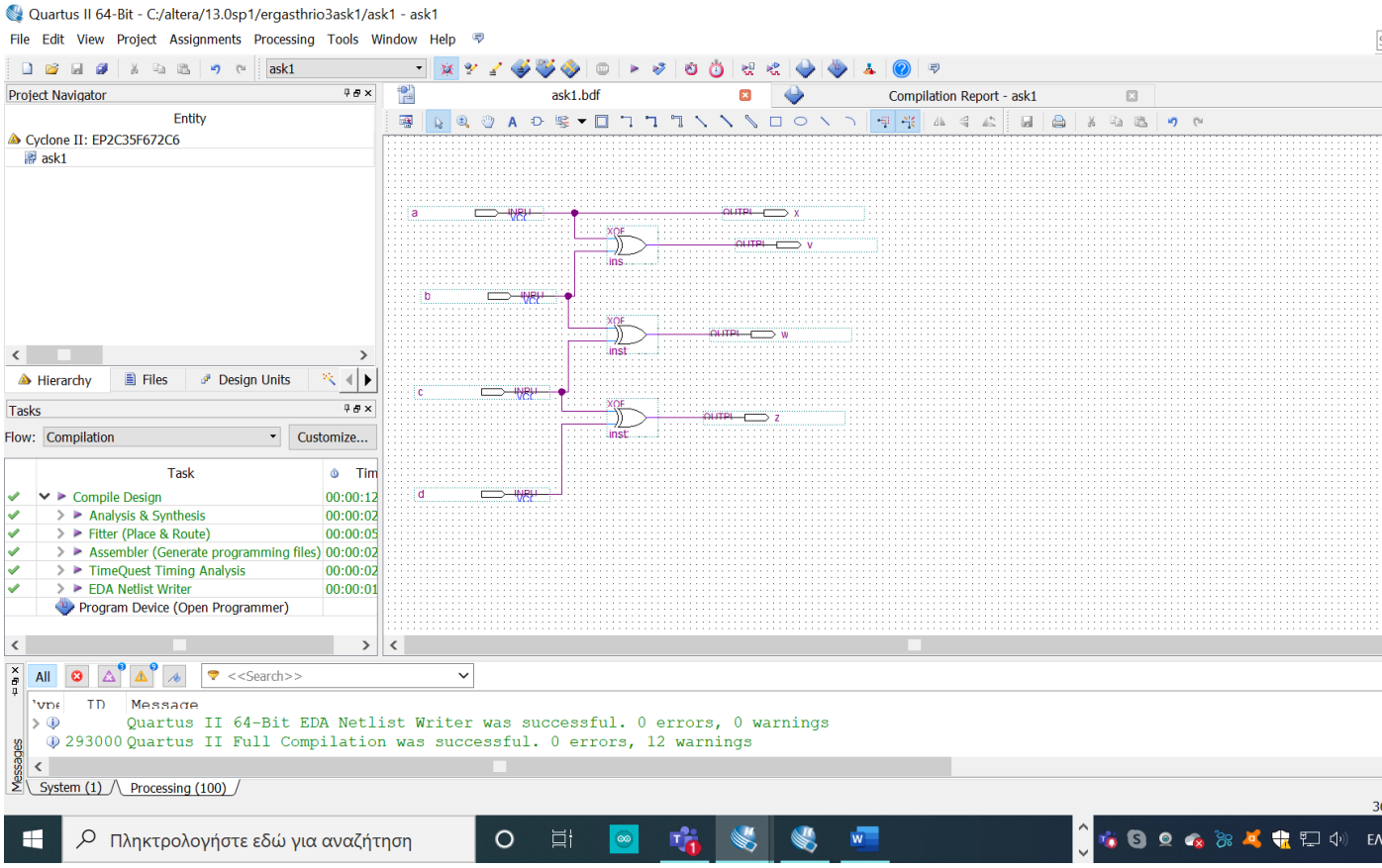
Μετατροπη ⟶ Δυαδικο σε Gray

a	b	c	d	x	y	z	w
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

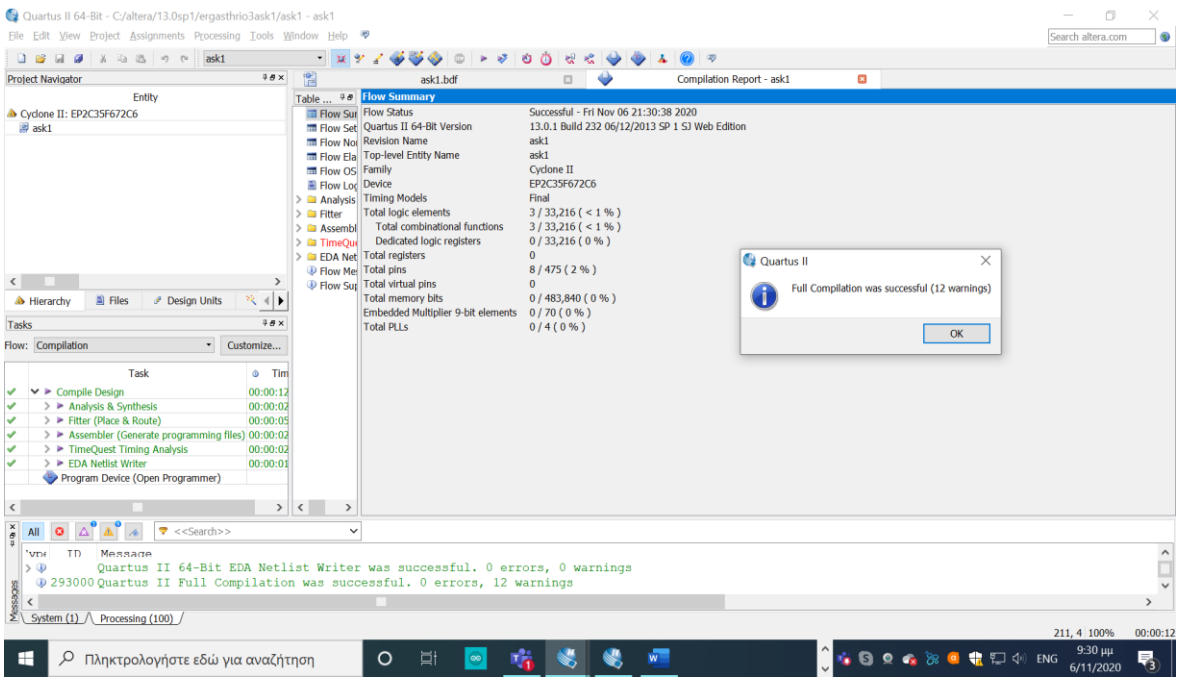


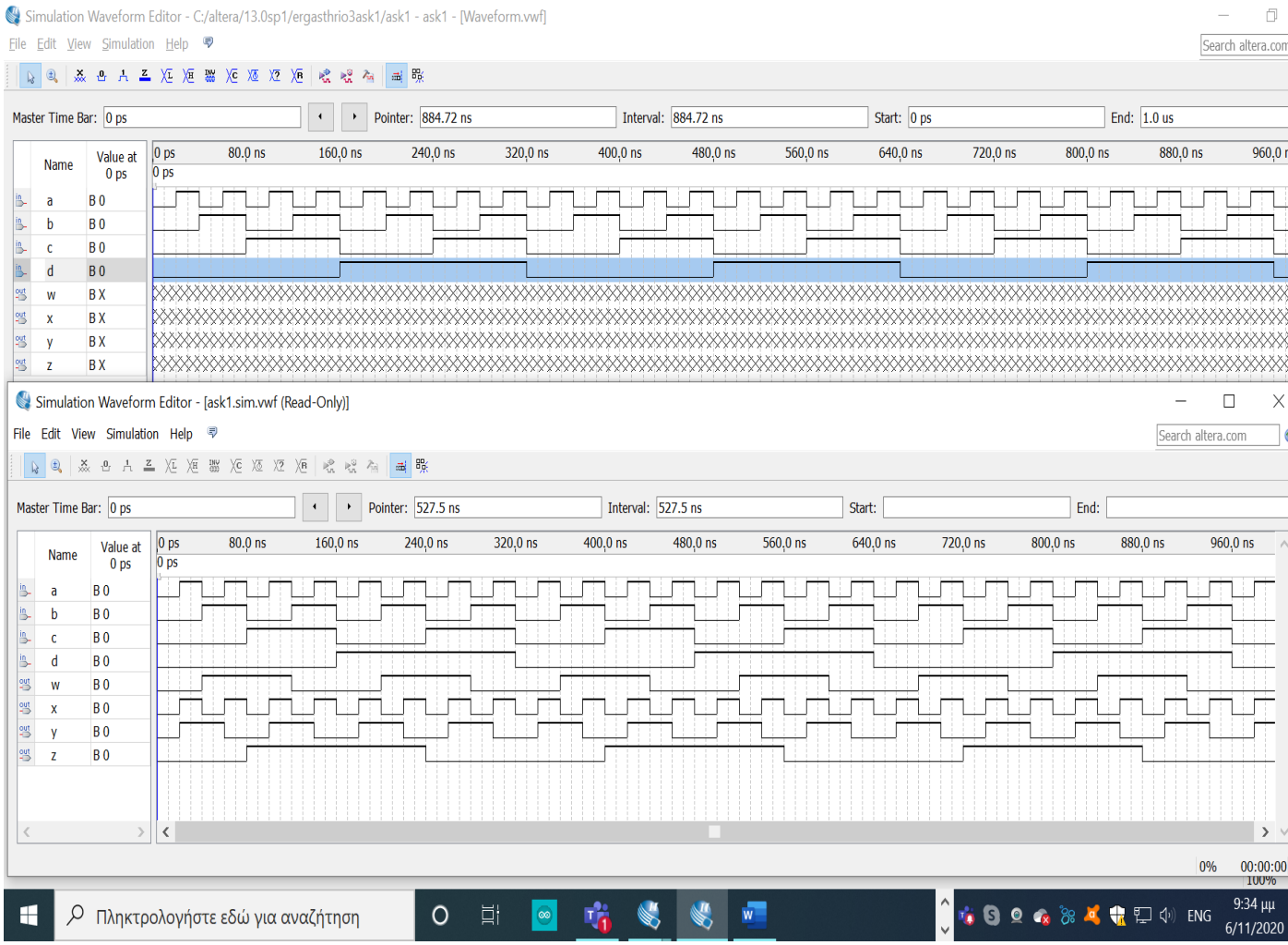
Θα δουλεψω το κυκλωμα μου μονο με πυλες xor:

Ακολουθει το κυκλωμα :



To compailation:





Ακολουθει Ασκηση2:

Άσκηση (2) Εφαρμογή (3)

a	b	c	d	Περιγραφή	w	x	y	z
0	0	0	0	Συμπληρώμα	1	0	0	1
0	0	0	1	ως προς 9	1	0	0	0
0	0	1	0	9 = 1010	0	1	1	1
0	0	1	1	wxyz=(abcd)'+9	0	1	1	0
0	1	0	0		0	1	0	1
0	1	0	1		0	1	0	0
0	1	1	0		0	0	1	1
0	1	1	1		0	0	1	0
1	0	0	0		0	0	0	1
1	0	0	1		0	0	0	0

Για το w κάνε να το απλοποιήσω χρησιμοποιώντας Karnaugh

ab \ cd	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

(a: 00, 01, 11 — b)

$W = a'b'c'd' + a'b'cd = a'b'c'(d'+d) = a'b'c'$

Για το x

ab \ cd	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	0	0	0	0
01	0	0	0	0

(a: 01, 11, 01 — b)

$X = b \oplus c$

Διότι,

$X = a'bc'd' + a'bc'd + a'b'cd + a'b'cd' =$

$= a'bc'(d'+d) + a'b'c(d+d') = a'bc' + a'b'c = bc' + b'c$

$= b \oplus c$

Για τον y

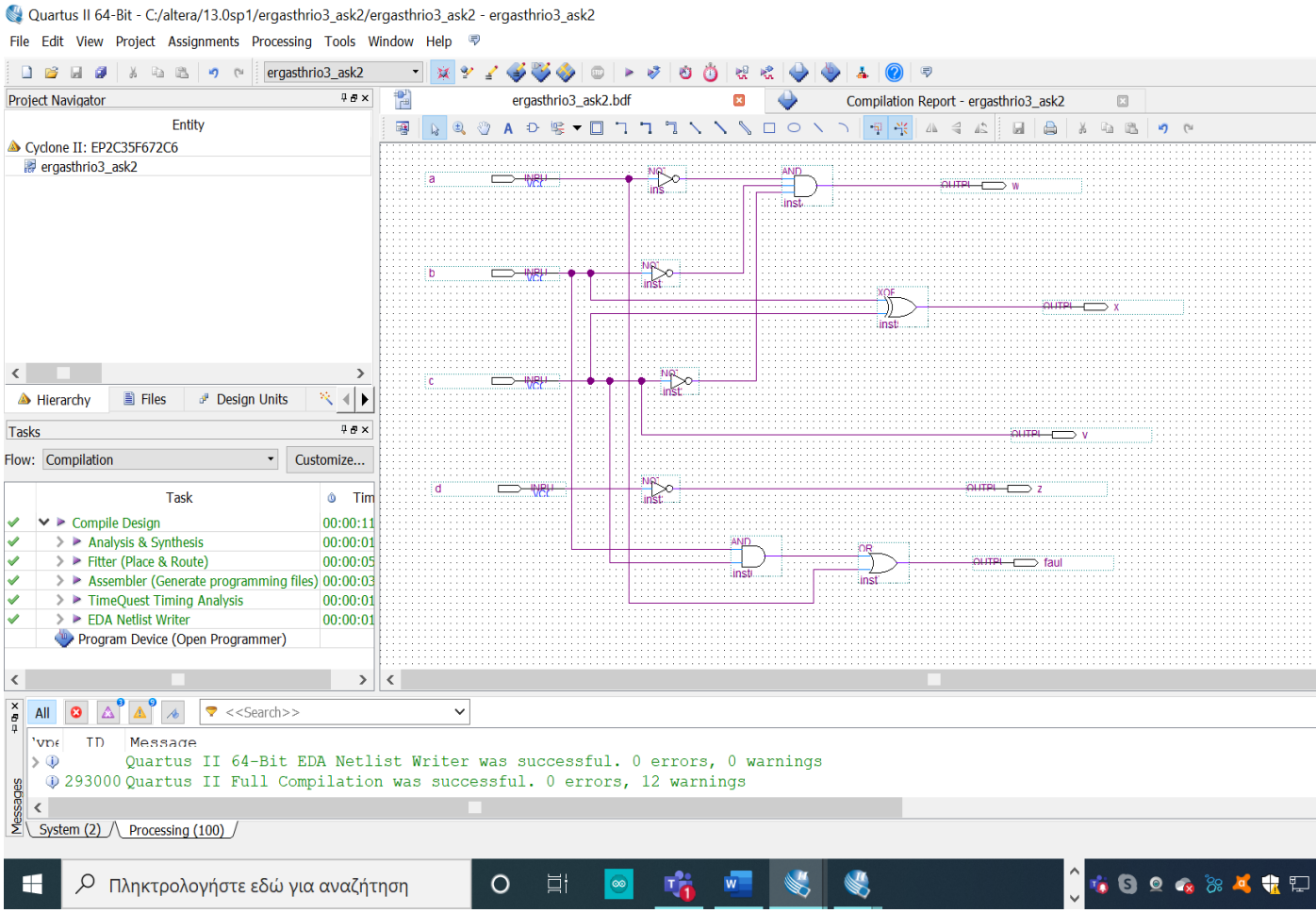
ab \ cd	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	0	0

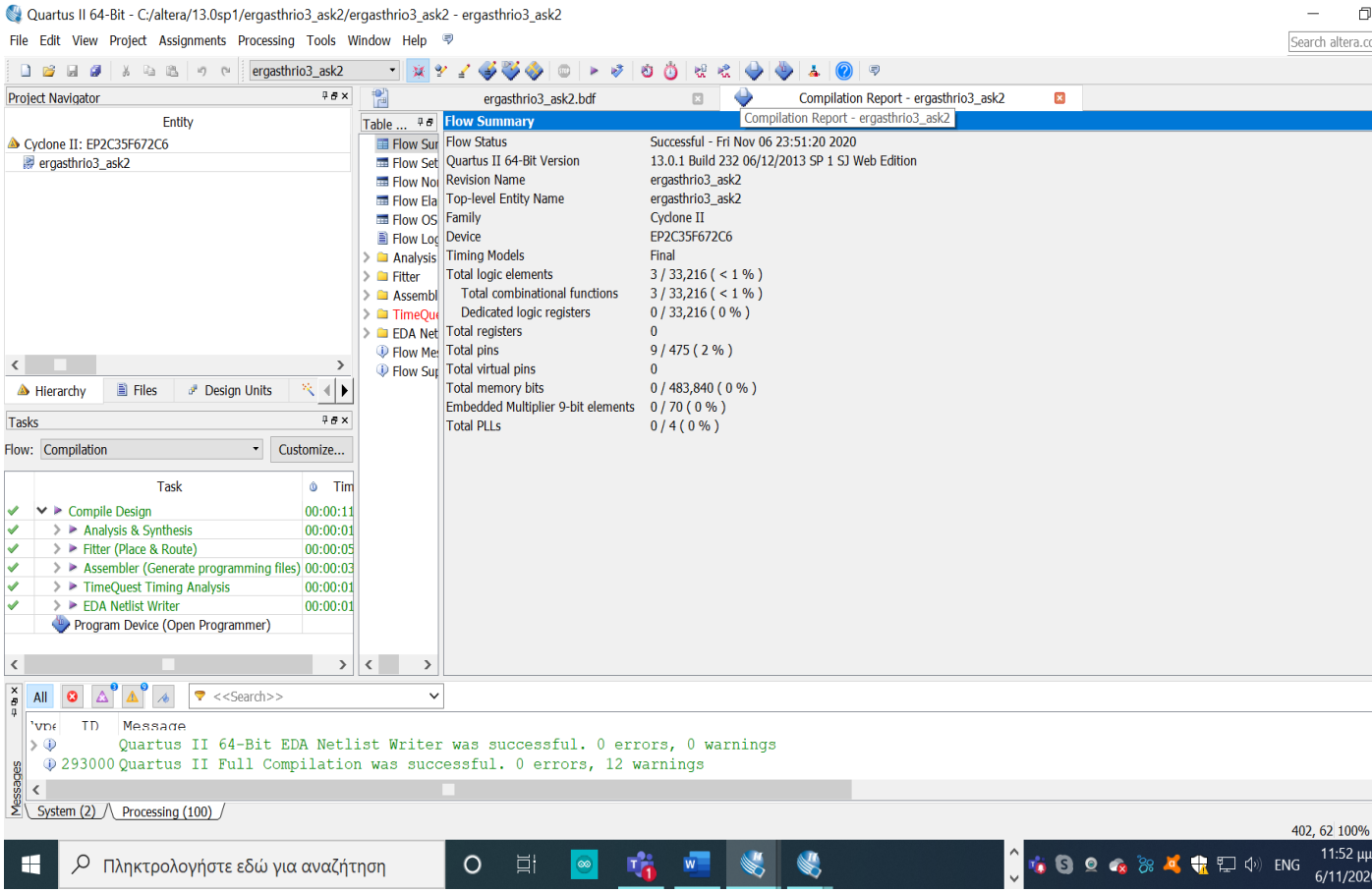
$$y = cdb' + cd'b' + cdb + cd'b =$$
$$= cb'(d'+d) + cb(d+d') = cb' + cb = c(b+b') = c$$

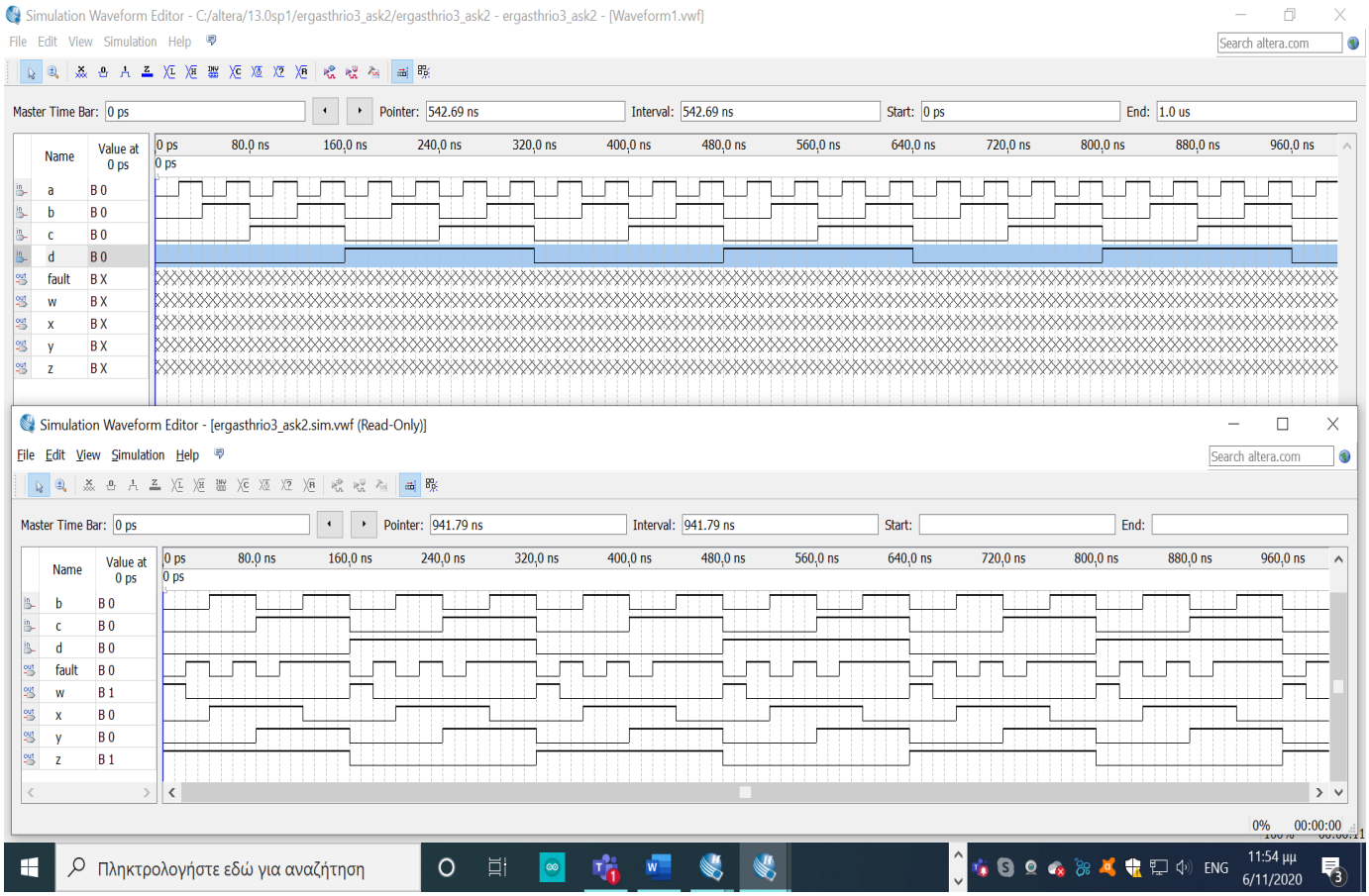
$$\boxed{y = c}$$

Όσσο, για το τελευταίο z δεν χρειαζόμαι Karnaugh αφού παρατηρώ από τον πίνακα αληθείας το εξής οτι $\boxed{z = d'}$

- Για να αντιχνευσουμε το λάθος στον πίνακα αληθείας θα πρέπει να δούμε σε ποια περιπτωση ο πίνακας BCD είναι μεγαλύτερος του 1001. Αρκεί να κάνουμε ένα κύκλωμα Αν οι τιμές του a και b/c είναι ταυτόχρονα 1
Αρα, Fault = $a + (b \cdot c)$


Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3_ask2/ergasthrio3_ask2 - ergasthrio3_ask2
File Edit View Project Assignments Processing Tools Window Help
ergasthrio3_ask2
Project Navigator
Entity
Cyclone II: EP2C35F672C6
ergasthrio3_ask2
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design 00:00:11
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:03
TimeQuest Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
ergasthrio3_ask2.bdf
Compilation Report - ergasthrio3_ask2
a
b
c
d
INPUT
VCC
NOT
AND
XOR
OR
OUTPUT
w
x
v
z
faul
inst
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System (2)
Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση


Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3_ask2/ergasthrio3_ask2 - ergasthrio3_ask2
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F672C6
ergasthrio3_ask2
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
Compile Design 00:00:11
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:03
TimeQuest Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
ergasthrio3_ask2.bdf
Compilation Report - ergasthrio3_ask2
Flow Summary
Flow Status Successful - Fri Nov 06 23:51:20 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name ergasthrio3_ask2
Top-level Entity Name ergasthrio3_ask2
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 3 / 33,216 (< 1 %)
Total combinational functions 3 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 9 / 475 (2 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
System (2) Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση
ENG



Ακολουθει ασκηση 3:

Ερώτημα 3ο

Αφού το X έχει 3 εισόδους
Επομένως φτάνει μέχρι το 3

x	-4	-3	-2	-1	0	1	2	3
y	10	3	-2	-5	-6	-5	-2	-3

Άρα χρειαζόμαστε 4 εξόδους για αριθμούς
1 για πρόσημο

c	b	a	⟶	Y_5	Y_4	Y_3	Y_2	Y_1
1	0	0	Συμπλήρωμα	0	1	0	1	0
1	0	1	ως προς 2	0	0	0	1	1
1	1	0		1	1	1	1	0
1	1	1		1	1	0	1	1
0	0	0		1	1	0	1	0
0	0	1		1	1	0	1	1
0	1	0		1	1	1	1	0
0	1	1		0	0	0	1	1

Για y_1

a \ b	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$y_1 = a$

Για y_0

a \ b	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$y_2 = 1$

Fig y_3

	00	01	11	10
0	0	0	0	1
1	0	0	0	1

$y_3 = c'b$

Fig y_4

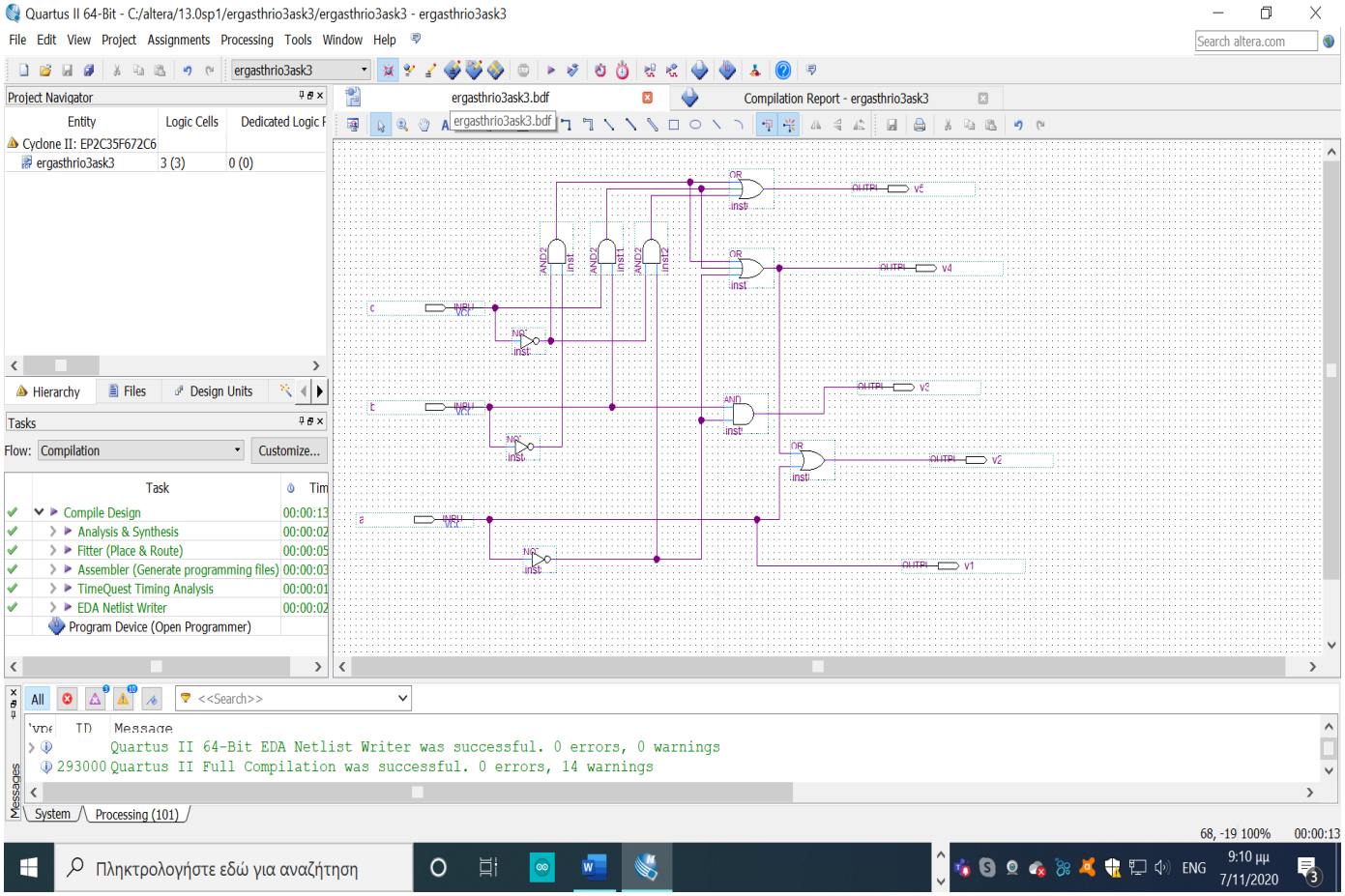
	00	01	11	10
0	1	1	0	1
1	1	0	1	1

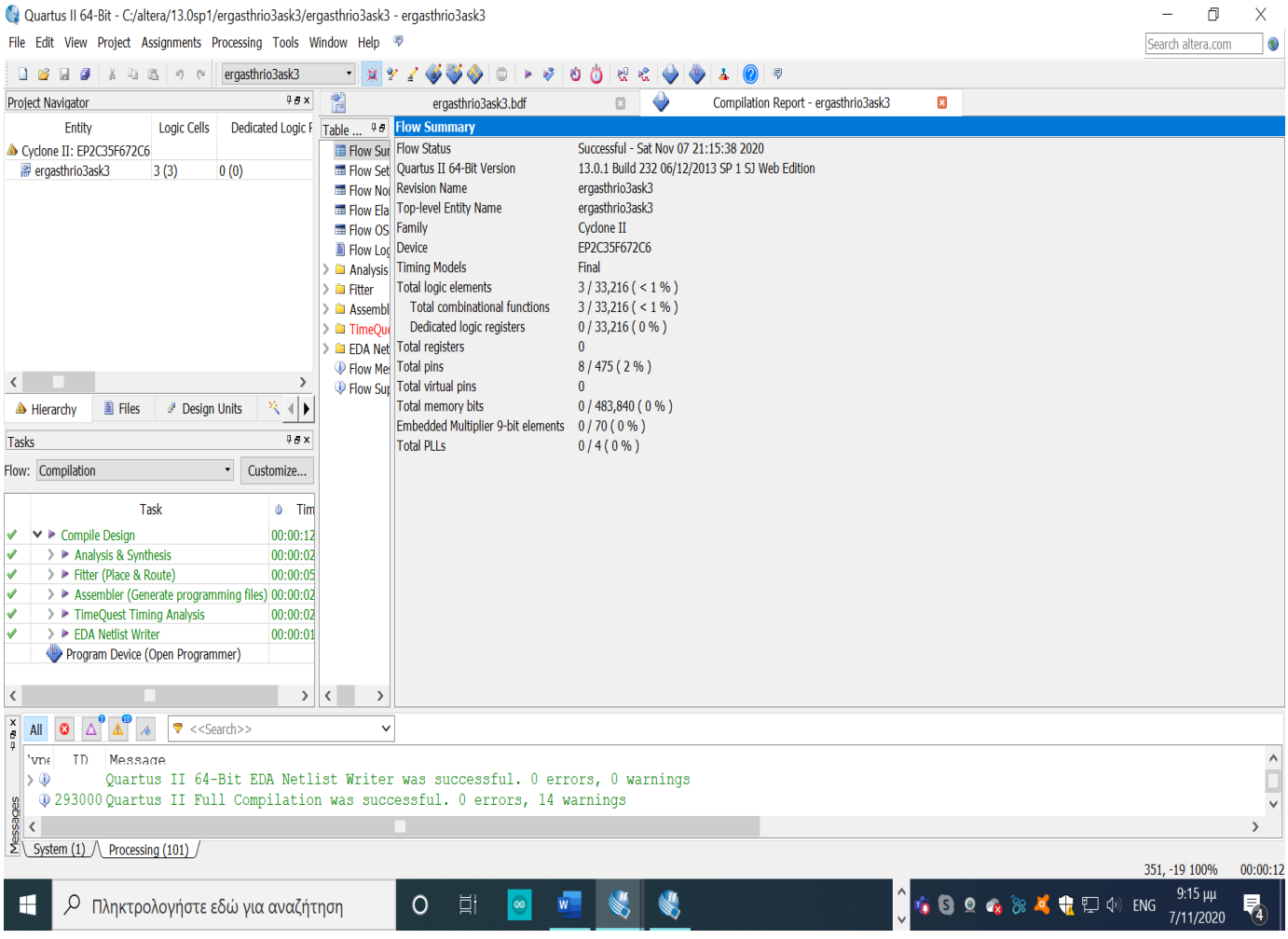
$y_4 = c'b' + a' + cb$

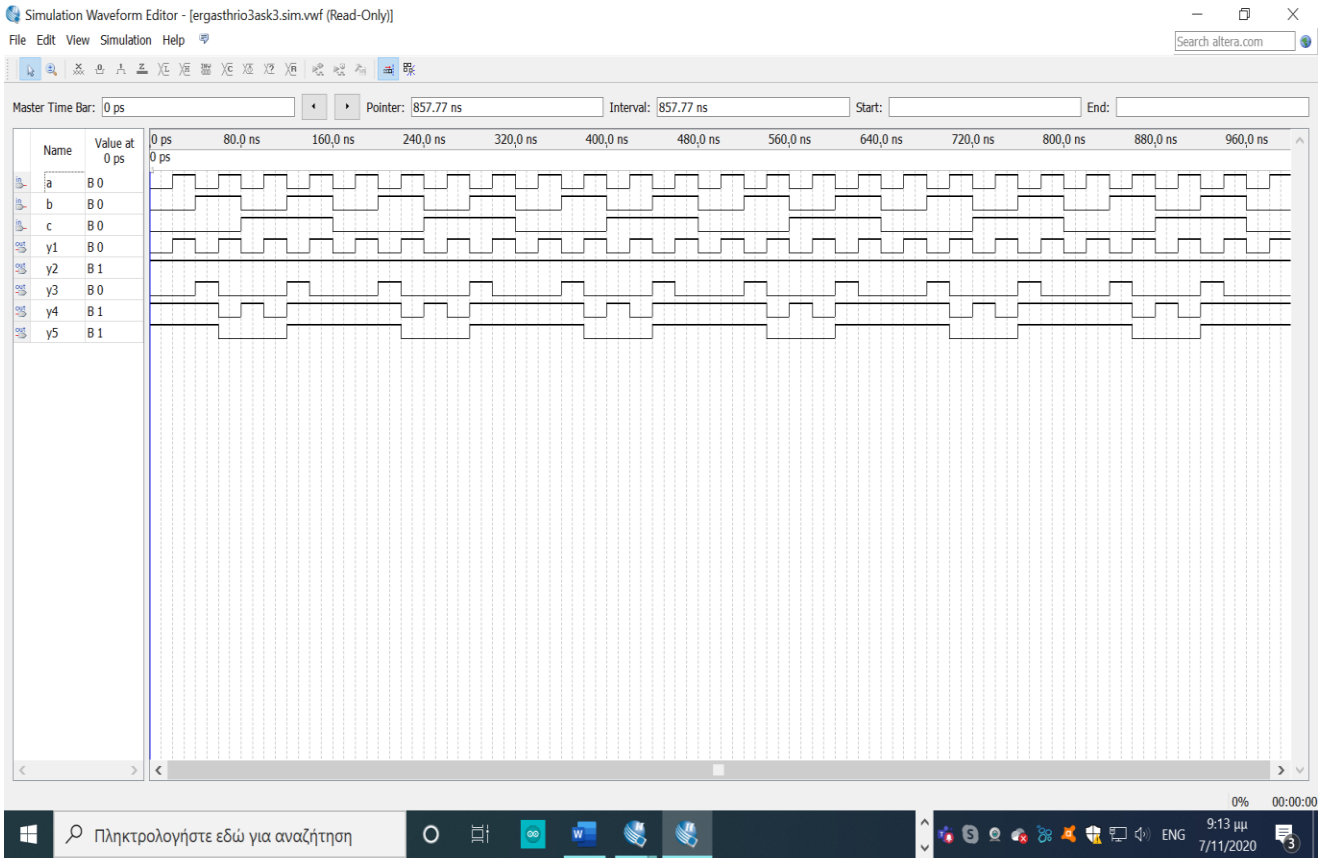
Fig y_5 ,

	00	01	11	10
0	1	1	0	1
1	1	0	0	1	1

$y_5 = c'b' + cb + c'a'$


Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3ask3/ergasthrio3ask3 - ergasthrio3ask3
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Entity
Logic Cells
Cyclone II: EP2C35F672C6
ergasthrio3ask3
3 (3)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
ergasthrio3ask3.bdf
Compilation Report - ergasthrio3ask3
OR
AND2
AND
NOT
INPUT
OUTPUT
v5
v4
v3
v2
v1
c
b
a
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 14 warnings
Messages
System
Processing (101)
68, -19 100%
00:00:13
Πληκτρολογήστε εδώ για αναζήτηση
ENG
9:10 μμ
7/11/2020


Quartus II 64-Bit - C:/altera/13.0sp1/ergasthrio3ask3/ergasthrio3ask3 - ergasthrio3ask3
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
ergasthrio3ask3
Project Navigator
Entity
Logic Cells
Dedicated Logic F
Cyclone II: EP2C35F672C6
ergasthrio3ask3
3 (3)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design 00:00:12
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:02
TimeQuest Timing Analysis 00:00:02
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
ergasthrio3ask3.bdf
Compilation Report - ergasthrio3ask3
Table ...
Flow Summary
Flow Status Successful - Sat Nov 07 21:15:38 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name ergasthrio3ask3
Top-level Entity Name ergasthrio3ask3
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 3 / 33,216 (< 1 %)
Total combinational functions 3 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 8 / 475 (2 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
Messages
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 14 warnings
System (1)
Processing (101)
351, -19 100%
00:00:12
Πληκτρολογήστε εδώ για αναζήτηση
ENG
9:15 μμ
7/11/2020


Simulation Waveform Editor - [ergasthrio3ask3.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 857.77 ns
Interval: 857.77 ns
Start:
End:
Name
Value at 0 ps
a B 0
b B 0
c B 0
y1 B 0
y2 B 1
y3 B 0
y4 B 1
y5 B 1
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns
0%
00:00:00
Πληκτρολογήστε εδώ για αναζήτηση
ENG
9:13 μμ
7/11/2020