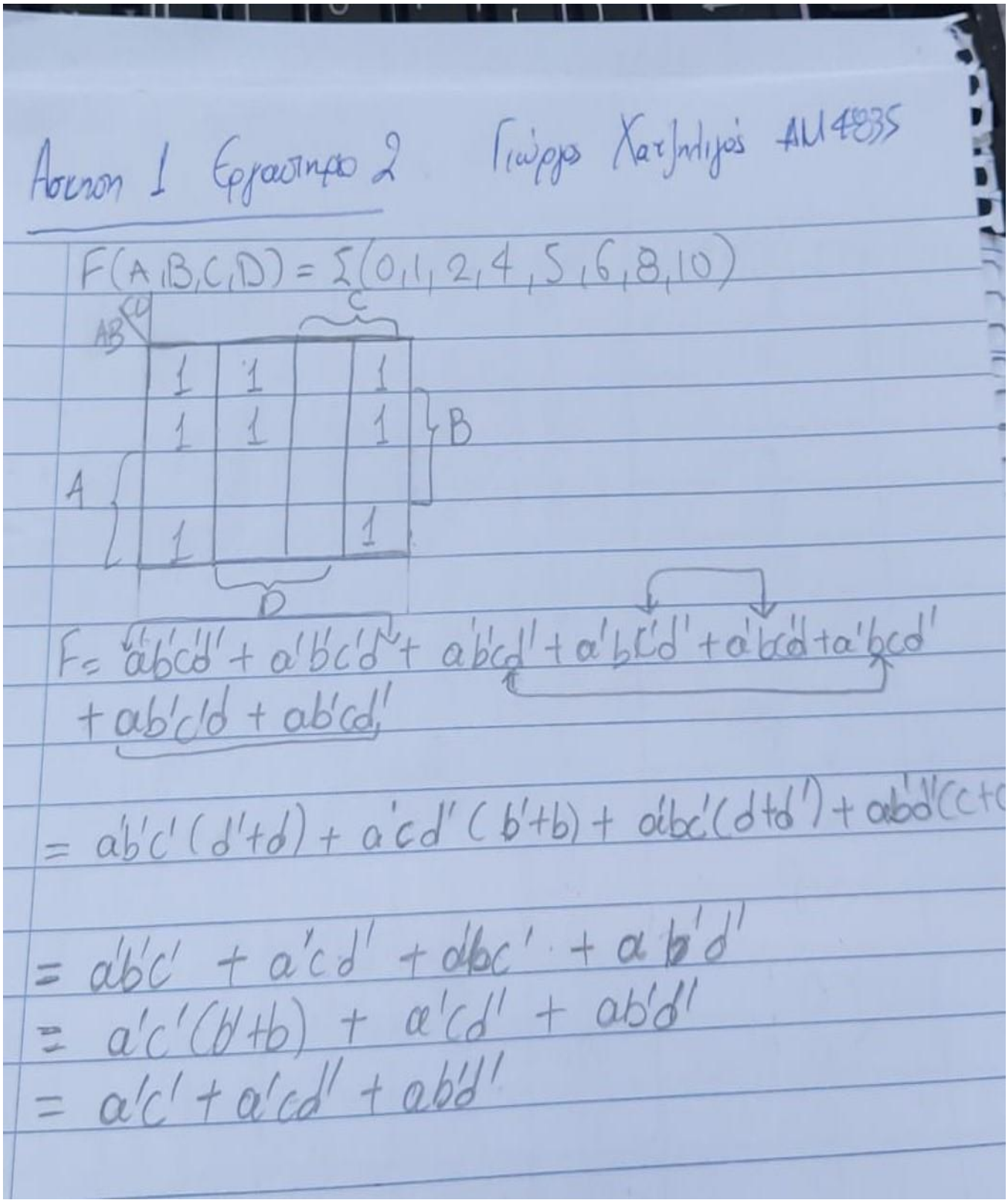
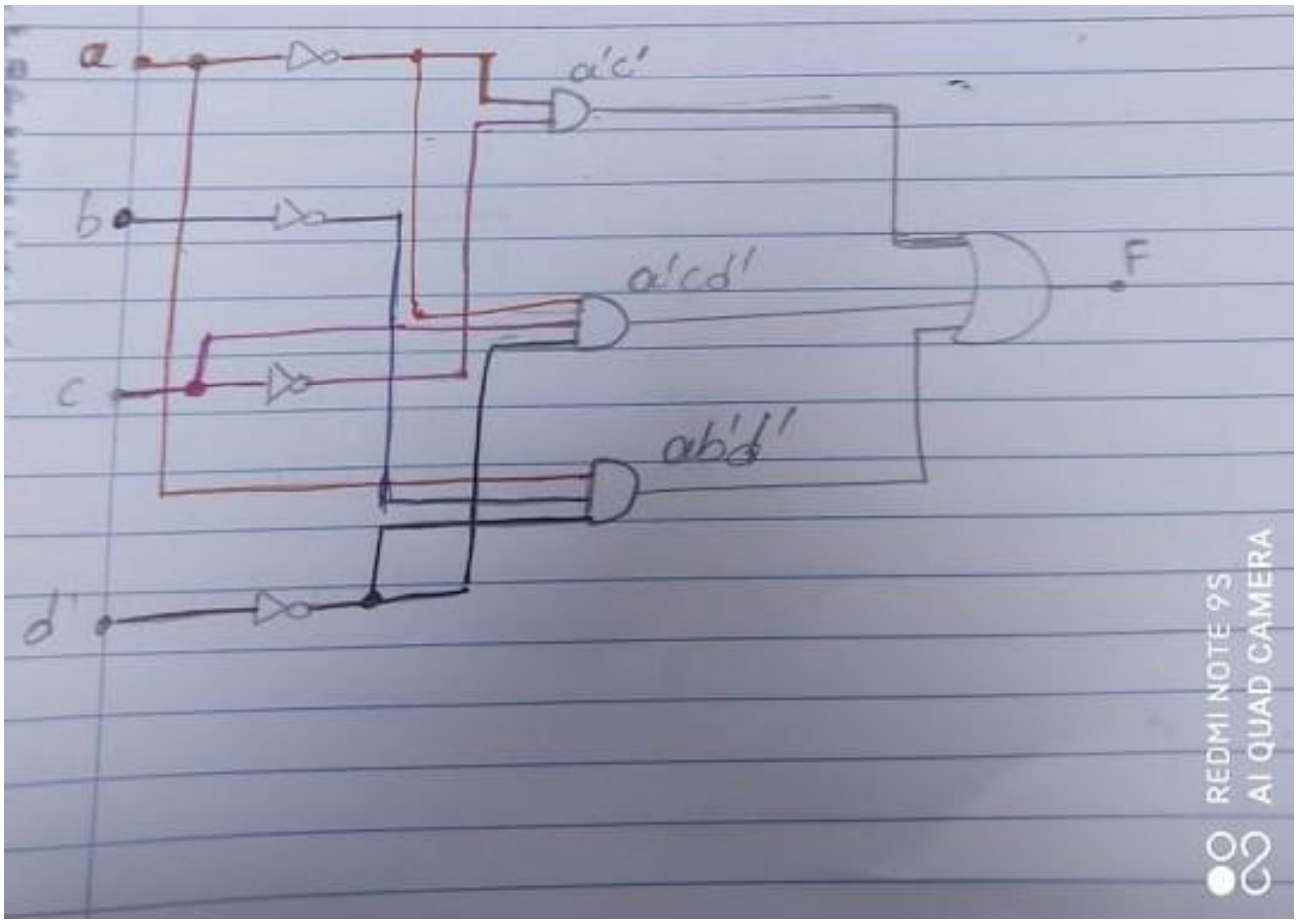
Γιωργος Χατζηλιγος ΑΜ4835

ΕΡΓΑΣΤΗΡΙΑΚΕΣ ΑΣΚΗΣΕΙΣ ΣΕΙΡΑ 2

ΑΣΚΣΗΣΗ

1


Ασκηση 1 Εργαστηριο 2 Γιώργος Χατζηλιγός ΑΜ4835
F(A,B,C,D) = Σ(0,1,2,4,5,6,8,10)
AB
CD
A
B
C
D
F= a'b'c'd' + a'b'c'd + a'b'cd' + a'bc'd' + a'bcd + a'bcd'
+ ab'c'd + ab'cd'
= a'b'c'(d'+d) + a'cd'(b'+b) + a'bc'(d+d') + ab'd'(c+c
= a'b'c' + a'cd' + a'bc' + ab'd'
= a'c'(b'+b) + a'cd' + ab'd'
= a'c' + a'cd' + ab'd'

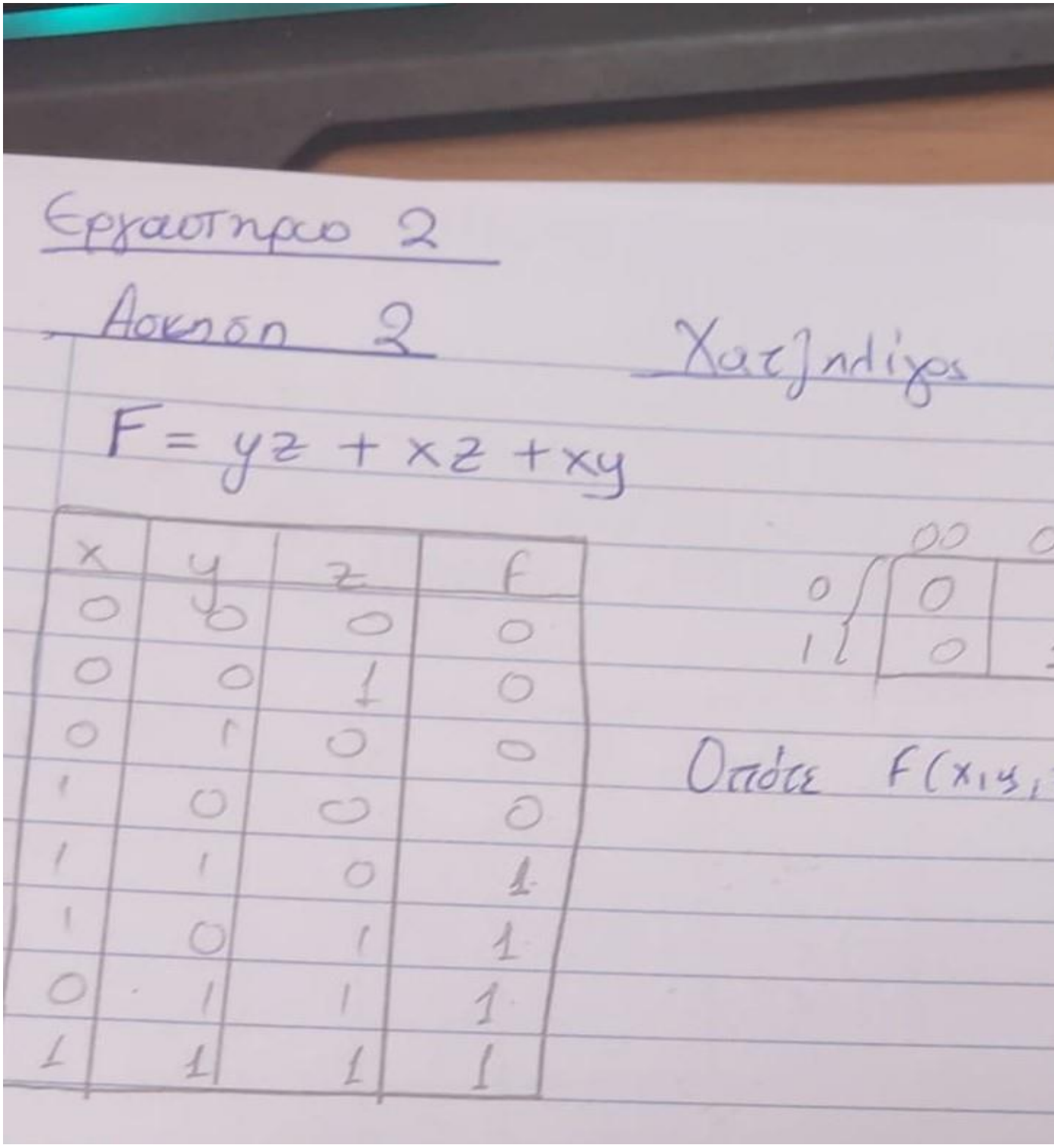

a
b
c
d'
a'c'
a'cd'
ab'd'
F
REDMI NOTE 9S
AI QUAD CAMERA

Άσκηση 1 Εργαστήριο 2

Γιώργος Χατζηλίγος ΑΜ4835

a	b	c	d	a'c'	a'cd'	ab'd'	a'c'+a'cd'+ab'd'
0	0	0	0	1	0	0	1
1	0	0	0	0	0	1	1
0	1	0	0	1	0	0	1
0	0	1	0	1	1	0	1
0	0	0	1	1	0	0	1
1	1	0	0	0	0	0	0
1	0	1	0	0	0	1	1
1	0	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	0	1	1	0	0	1
0	0	1	1	0	0	0	0
1	1	1	0	0	0	0	0
1	0	1	1	0	0	0	0
0	1	1	1	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	1	0	0	0	0

ΑΣΚΗΣΗ2



Εργαστηριο 2

Ασκηση 2

Χατζηνδίγος

$F = yz + xz + xy$

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

Οπότε F(x,y,

Εργαστηριο 2

Ασκηση 2

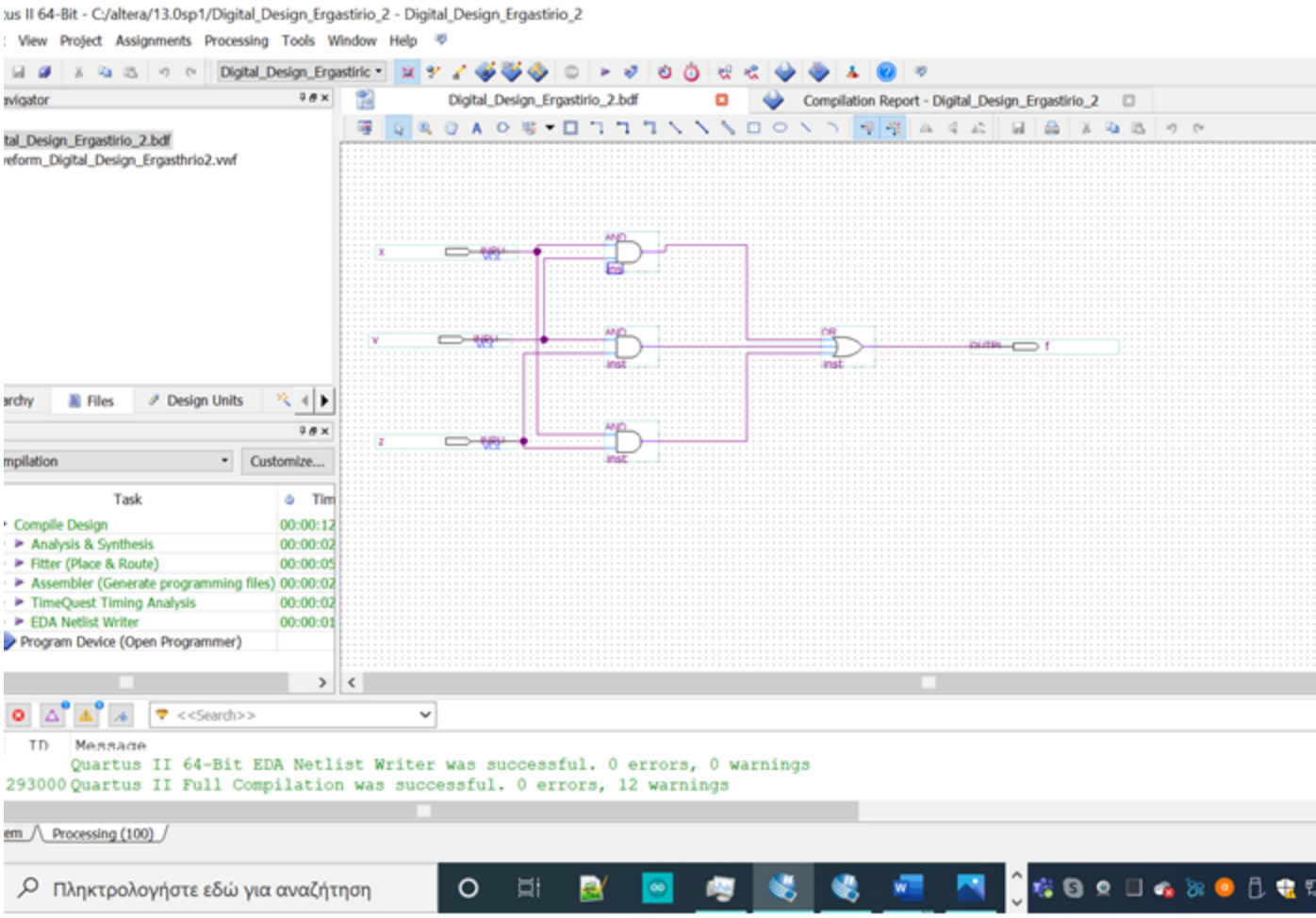
Χατζηδιγκος Γιωργος ΑΜ4835

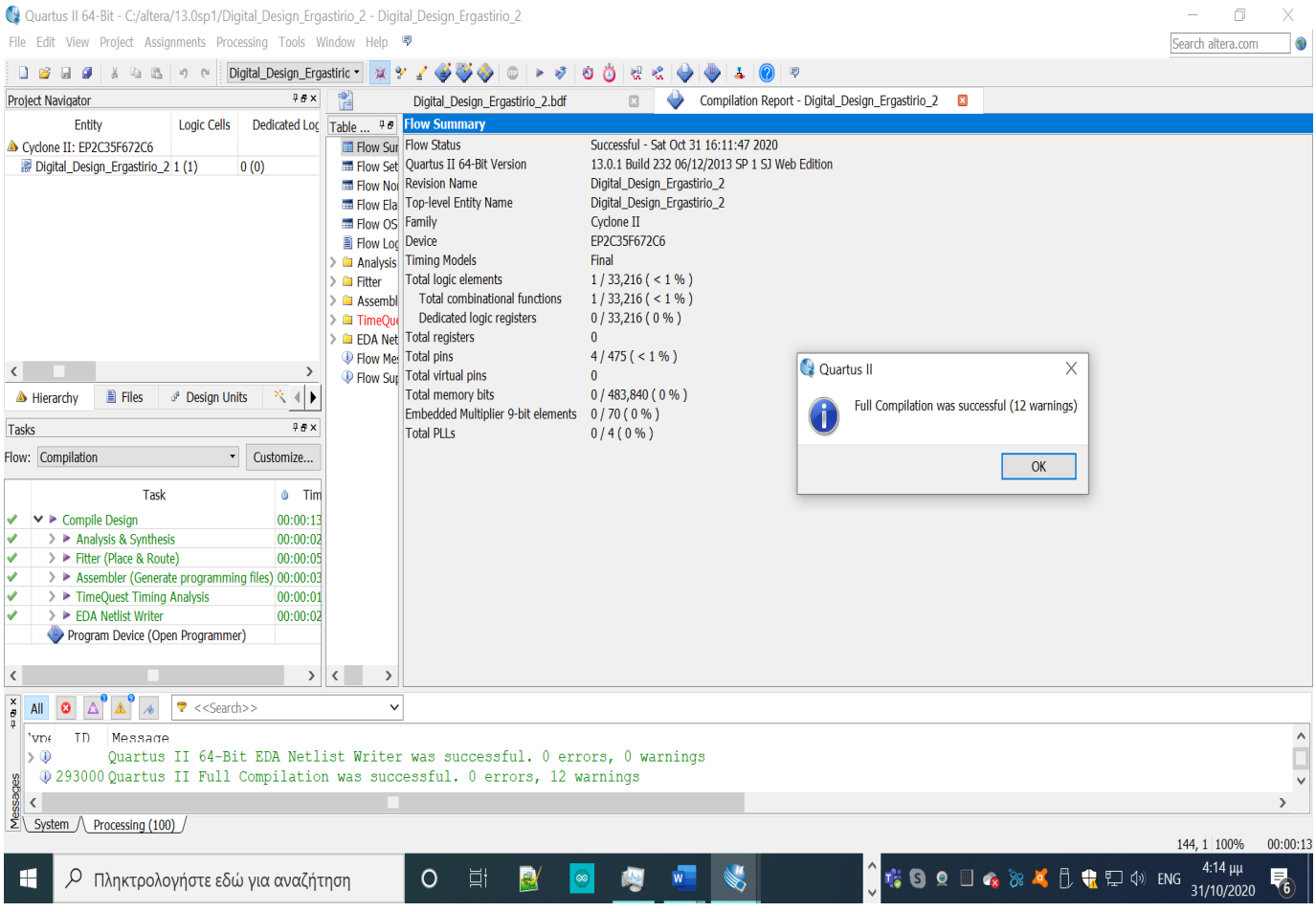
$F = yz + xz + xy$

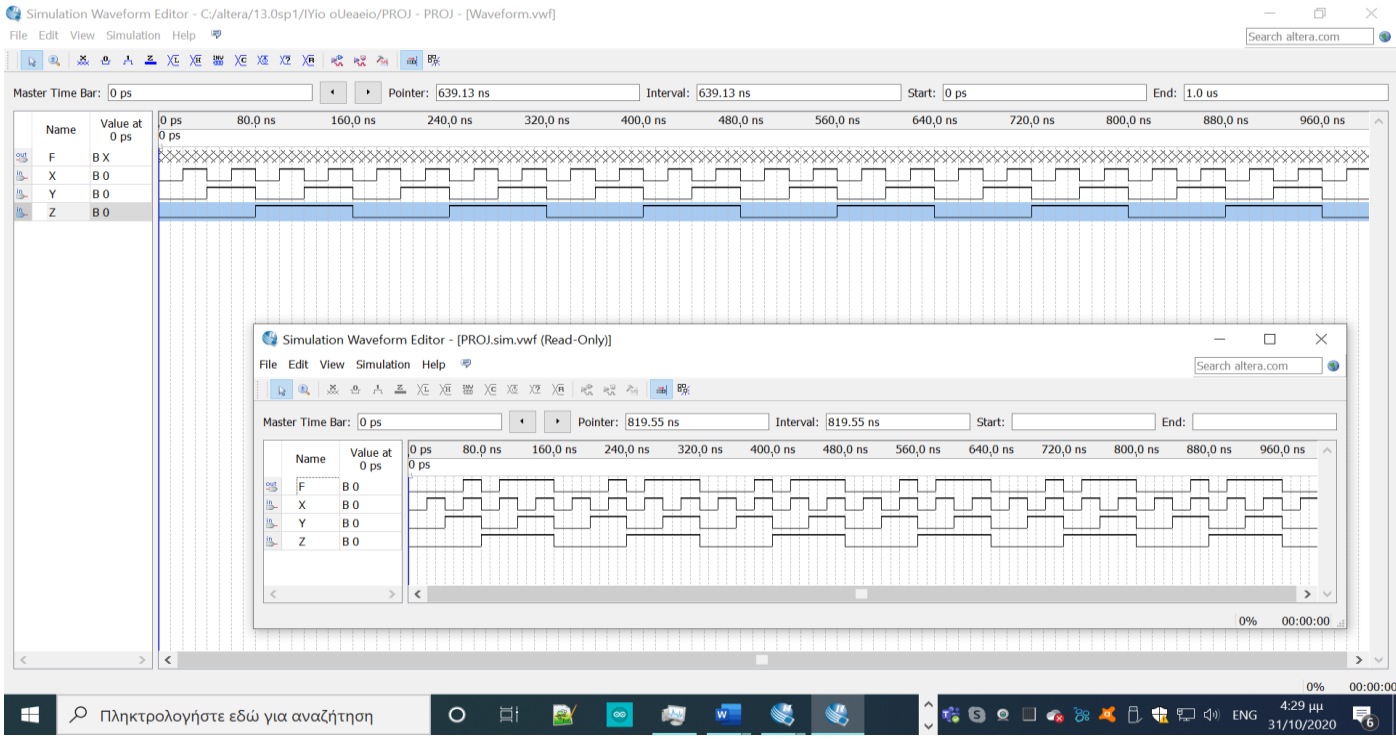
x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

	00	01	11	10
0	0	0	1	0
1	0	1	1	1

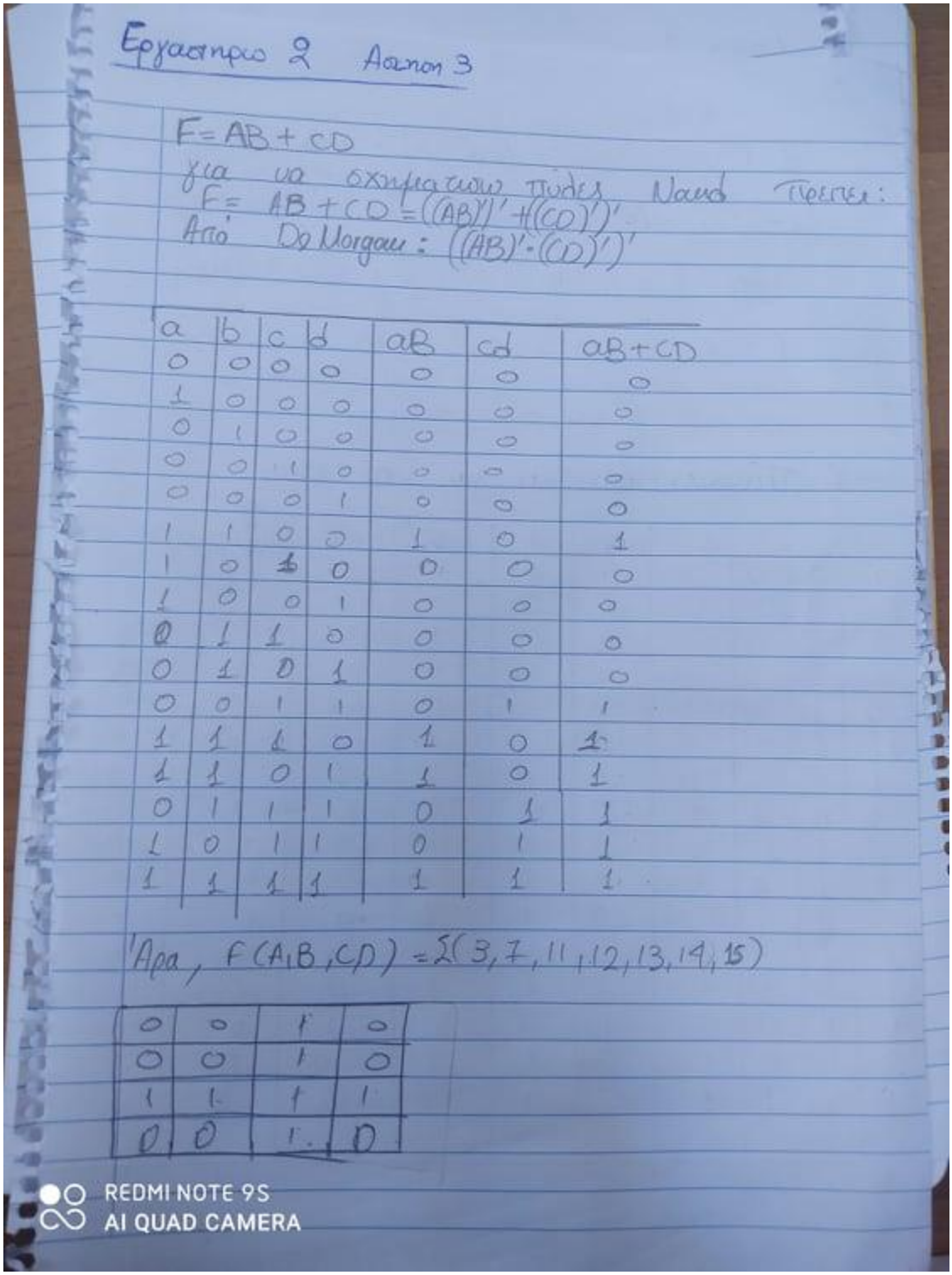
Οπότε $F(x,y,z) = \Sigma(3,5,6,7)$


us II 64-Bit - C:/altera/13.0sp1/Digital_Design_Ergastirio_2 - Digital_Design_Ergastirio_2
View Project Assignments Processing Tools Window Help
Digital_Design_Ergastirio_2.bdf
Compilation Report - Digital_Design_Ergastirio_2
Files
Design Units
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Quartus II Full Compilation was successful. 0 errors, 12 warnings
Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση


Quartus II 64-Bit - C:/altera/13.0sp1/Digital_Design_Ergastirio_2 - Digital_Design_Ergastirio_2
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Digital_Design_Ergastirio_2.bdf
Compilation Report - Digital_Design_Ergastirio_2
Project Navigator
Entity
Logic Cells
Cyclone II: EP2C35F672C6
Digital_Design_Ergastirio_2 1 (1)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design 00:00:13
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:03
TimeQuest Timing Analysis 00:00:01
EDA Netlist Writer 00:00:02
Program Device (Open Programmer)
Flow Summary
Flow Status Successful - Sat Oct 31 16:11:47 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name Digital_Design_Ergastirio_2
Top-level Entity Name Digital_Design_Ergastirio_2
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 1 / 33,216 (< 1 %)
Total combinational functions 1 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 4 / 475 (< 1 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
Quartus II
Full Compilation was successful (12 warnings)
OK
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
System
Processing (100)
144, 1 100% 00:00:13
Πληκτρολογήστε εδώ για αναζήτηση
ENG
4:14 μμ
31/10/2020


Simulation Waveform Editor - C:/altera/13.0sp1/IYio oUeaeio/PROJ - PROJ - [Waveform.vwf]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 639.13 ns
Interval: 639.13 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
F B X
X B 0
Y B 0
Z B 0
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Simulation Waveform Editor - [PROJ.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 819.55 ns
Interval: 819.55 ns
Start:
End:
Name
Value at 0 ps
F B 0
X B 0
Y B 0
Z B 0
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
0%
00:00:00
0%
Πληκτρολογήστε εδώ για αναζήτηση
ENG
4:29 μμ
31/10/2020

ΑΣΚΗΣΗ 3



Εργασηριο 2 Ασκηση 3

F = AB + CD

για να σχεδιασουμε πυλες Nand τοτε:

F = AB + CD = ((AB)' + (CD)')'

Από De Morgan: ((AB)' · (CD)')'

a	b	c	d	aB	cd	aB+CD
0	0	0	0	0	0	0
1	0	0	0	0	0	0
0	1	0	0	0	0	0
0	0	1	0	0	0	0
0	0	0	1	0	0	0
1	1	0	0	1	0	1
1	0	1	0	0	0	0
1	0	0	1	0	0	0
0	1	1	0	0	0	0
0	1	0	1	0	0	0
0	0	1	1	0	1	1
1	1	1	0	1	0	1
1	1	0	1	1	0	1
0	1	1	1	0	1	1
1	0	1	1	0	1	1
1	1	1	1	1	1	1

Άρα, F(A,B,C,D) = Σ(3,7,11,12,13,14,15)

0	0	1	0
0	0	1	0
1	1	1	1
0	0	1	0

Η $F' = (ab+cd)' = (ab)'\cdot(cd)' = (d+b)\cdot(cd') =$

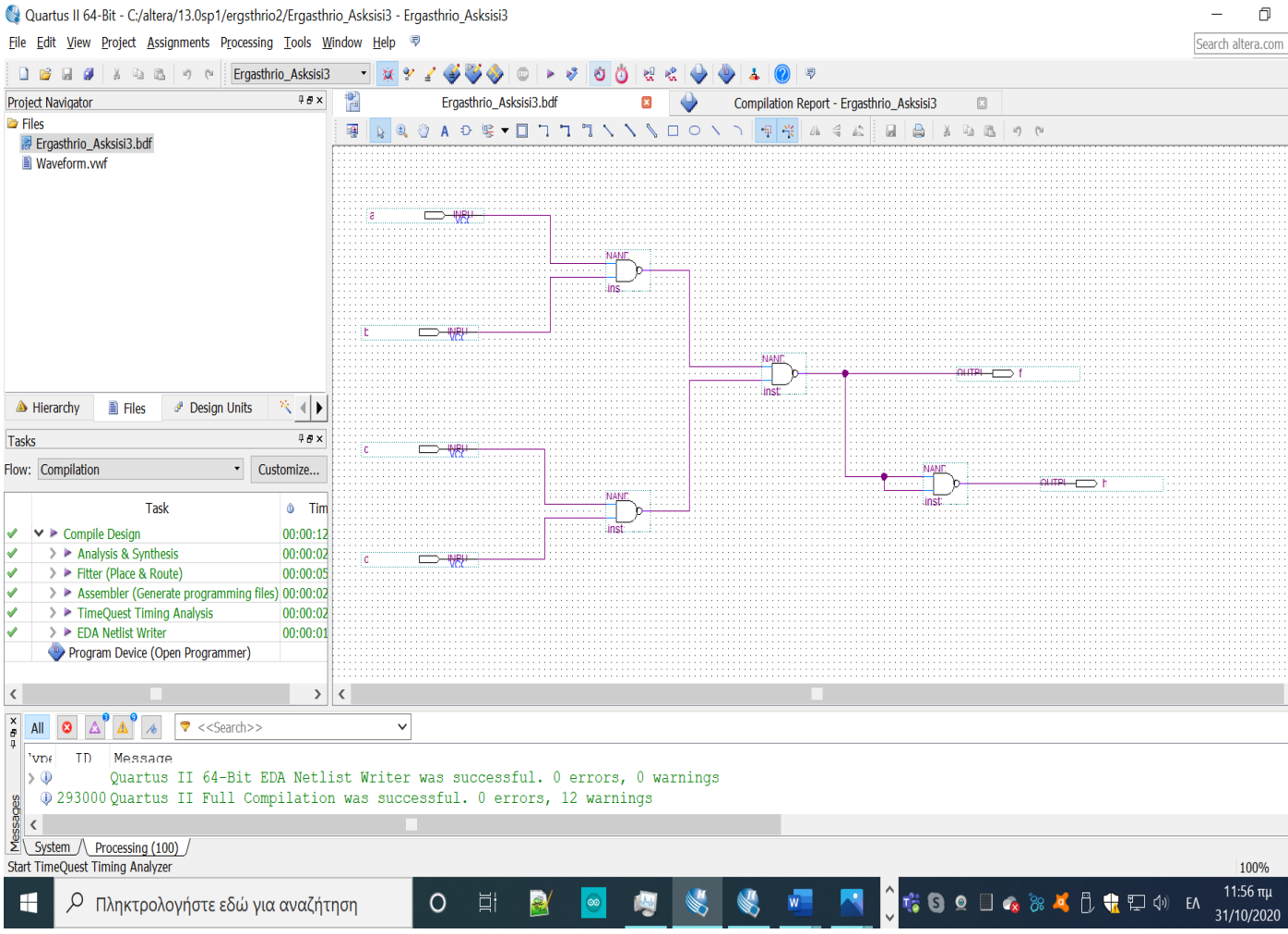
$(a'\cdot b')'\cdot(c'\cdot d')'$ ← Δυστυχώς δεν μας ταιριάζει

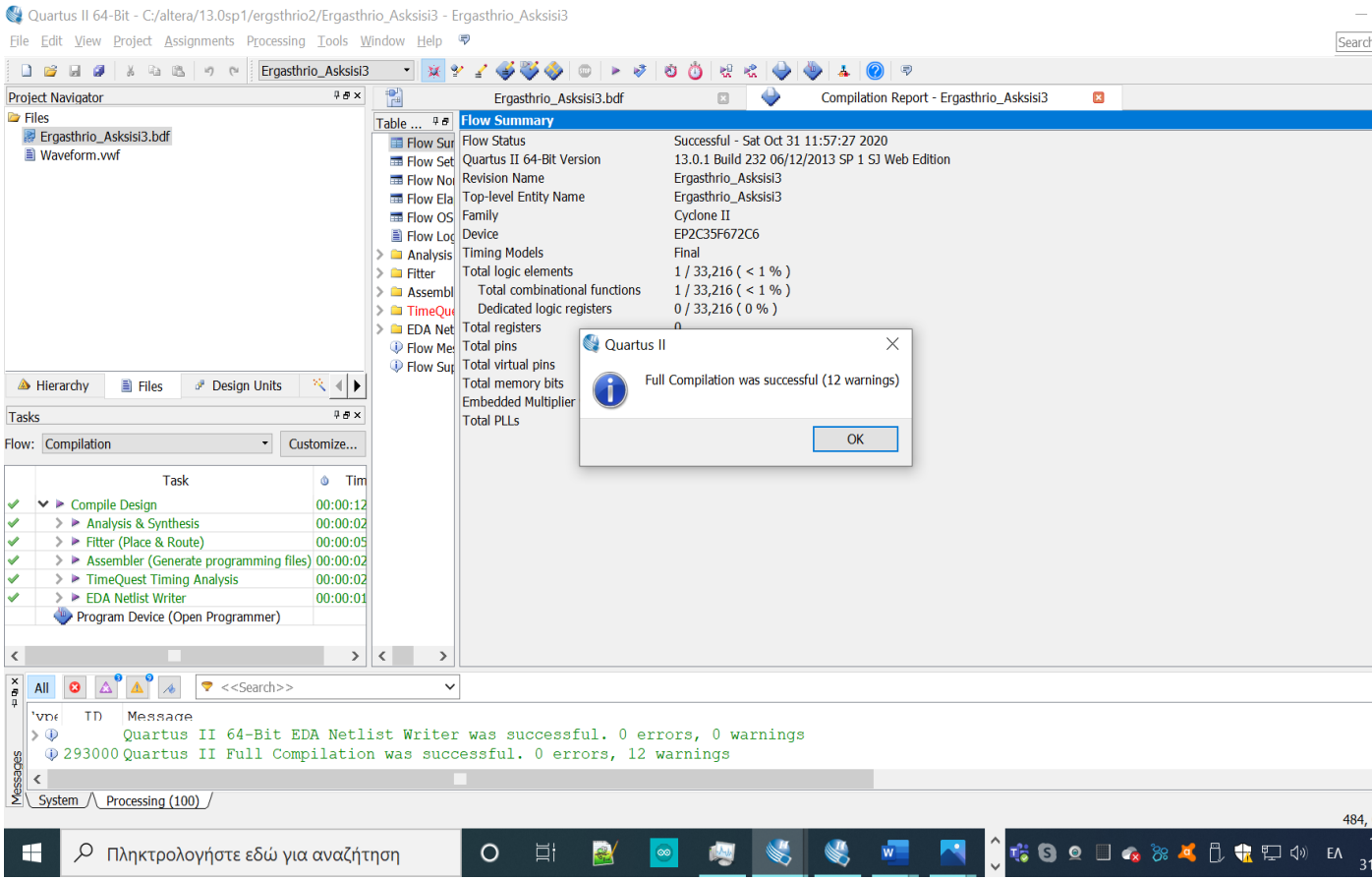
Οπότε $F' = [((AB)'(CD)')']' = (AB)'(CD)'$

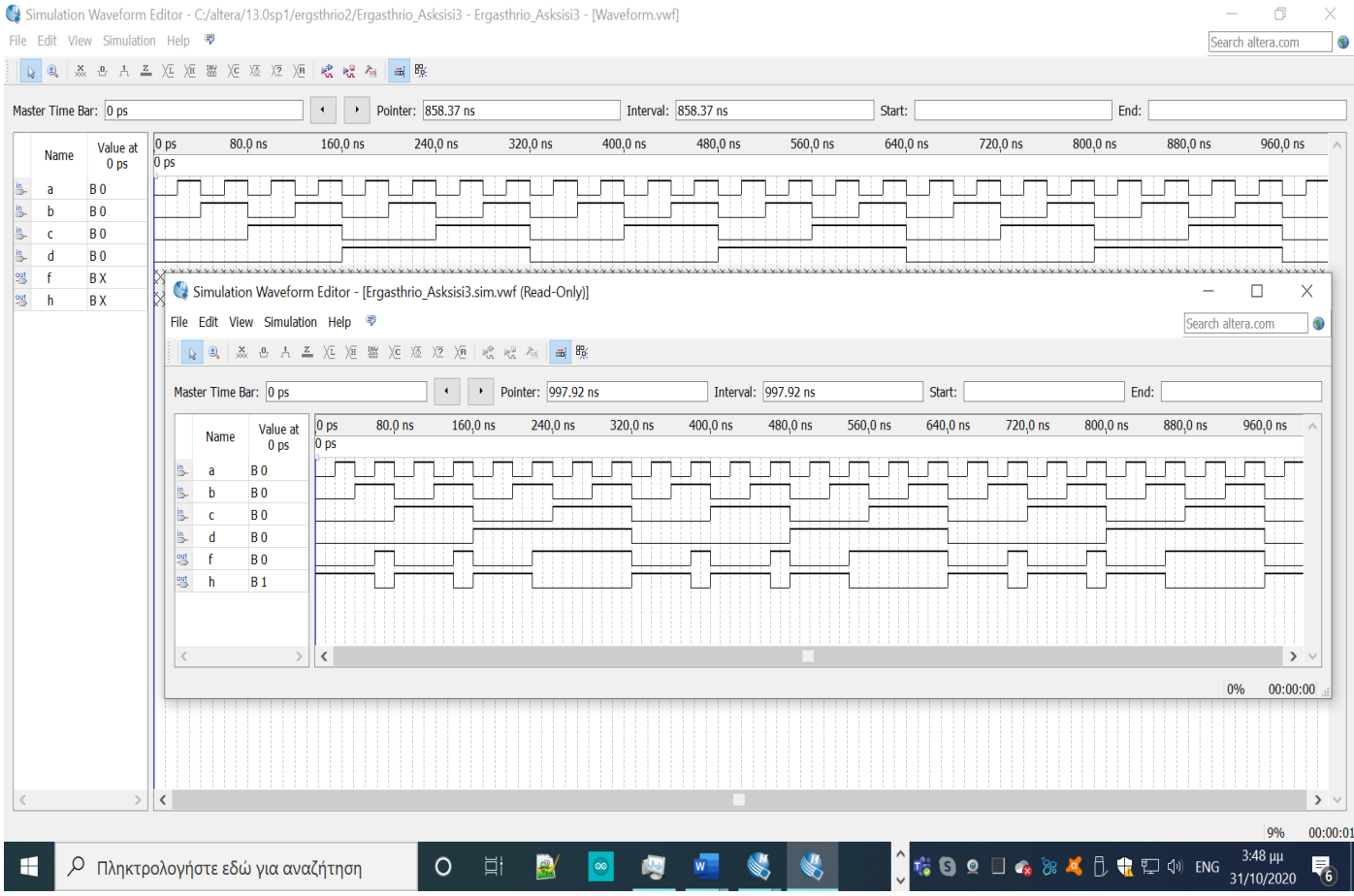
$F'(A,B,C,D) = \Sigma(0,1,2,4,5,6,8,9,10,16)$
Έχουν αντίθετες τιμές στο χάρτη
για αυτό έβαλα αυτές τιμές.

→ <u>Πίνακας αληθείας για τις Nand</u>

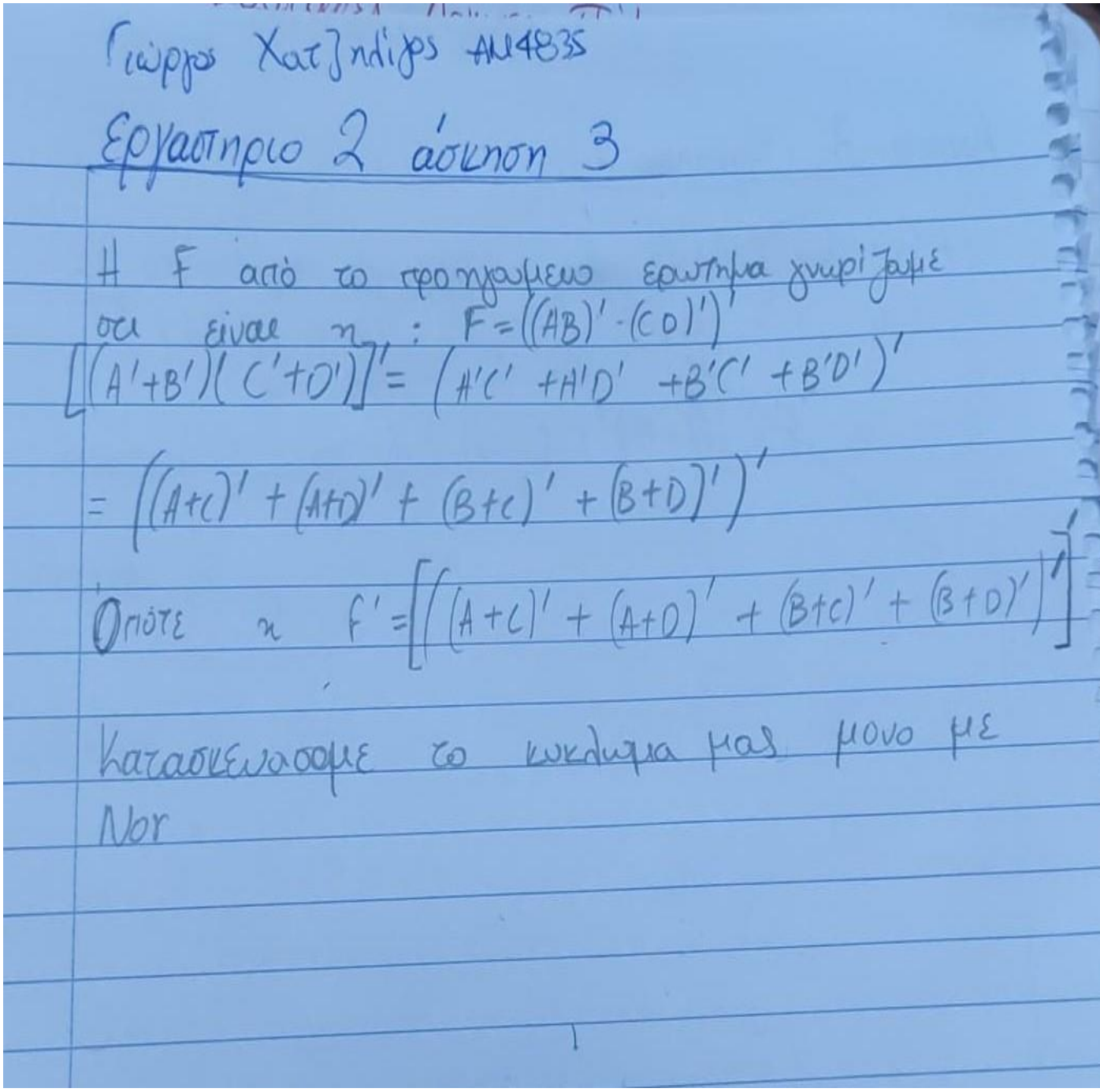
a	b	c	d	aB	cd	(aB)'	(cd)'	(ab)'(cd)'	F [(ab)'(cd)']'
0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	1	1	1	0
0	1	0	0	0	0	1	1	1	0
0	0	1	0	0	0	1	1	1	0
0	0	0	1	0	0	1	1	1	0
1	1	0	0	1	0	0	1	0	1
1	0	1	0	0	0	1	1	1	0
1	0	0	1	0	0	1	1	1	0
0	1	1	0	0	0	1	1	1	0
0	1	0	1	0	0	1	1	1	0
0	0	1	1	0	1	1	0	0	1
1	1	1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0	0	1
1	1	0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	0	0	0	1

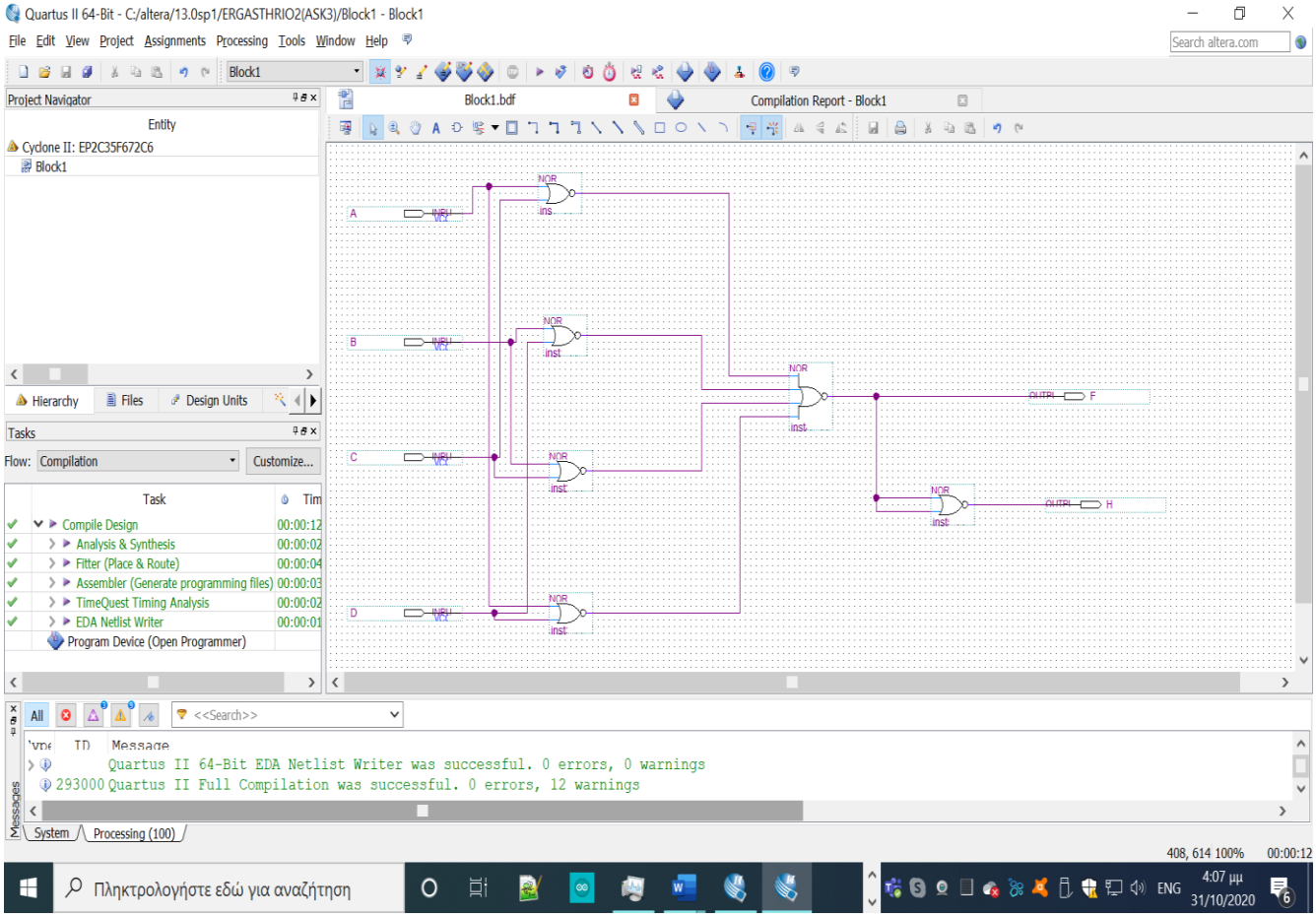

Quartus II 64-Bit - C:/altera/13.0sp1/ergsthrio2/Ergasthrio_Asksisi3 - Ergasthrio_Asksisi3
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Ergasthrio_Asksisi3
Project Navigator
Files
Ergasthrio_Asksisi3.bdf
Waveform.vwf
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Tim
Compile Design 00:00:12
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:02
TimeQuest Timing Analysis 00:00:02
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
Ergasthrio_Asksisi3.bdf
Compilation Report - Ergasthrio_Asksisi3
a
b
c
c
INPUT
VCC
NAND
inst
inst1
inst2
inst3
OUTPUT
f
h
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (100)
Start TimeQuest Timing Analyzer
100%
Πληκτρολογήστε εδώ για αναζήτηση
ΕΛ
11:56 πμ
31/10/2020

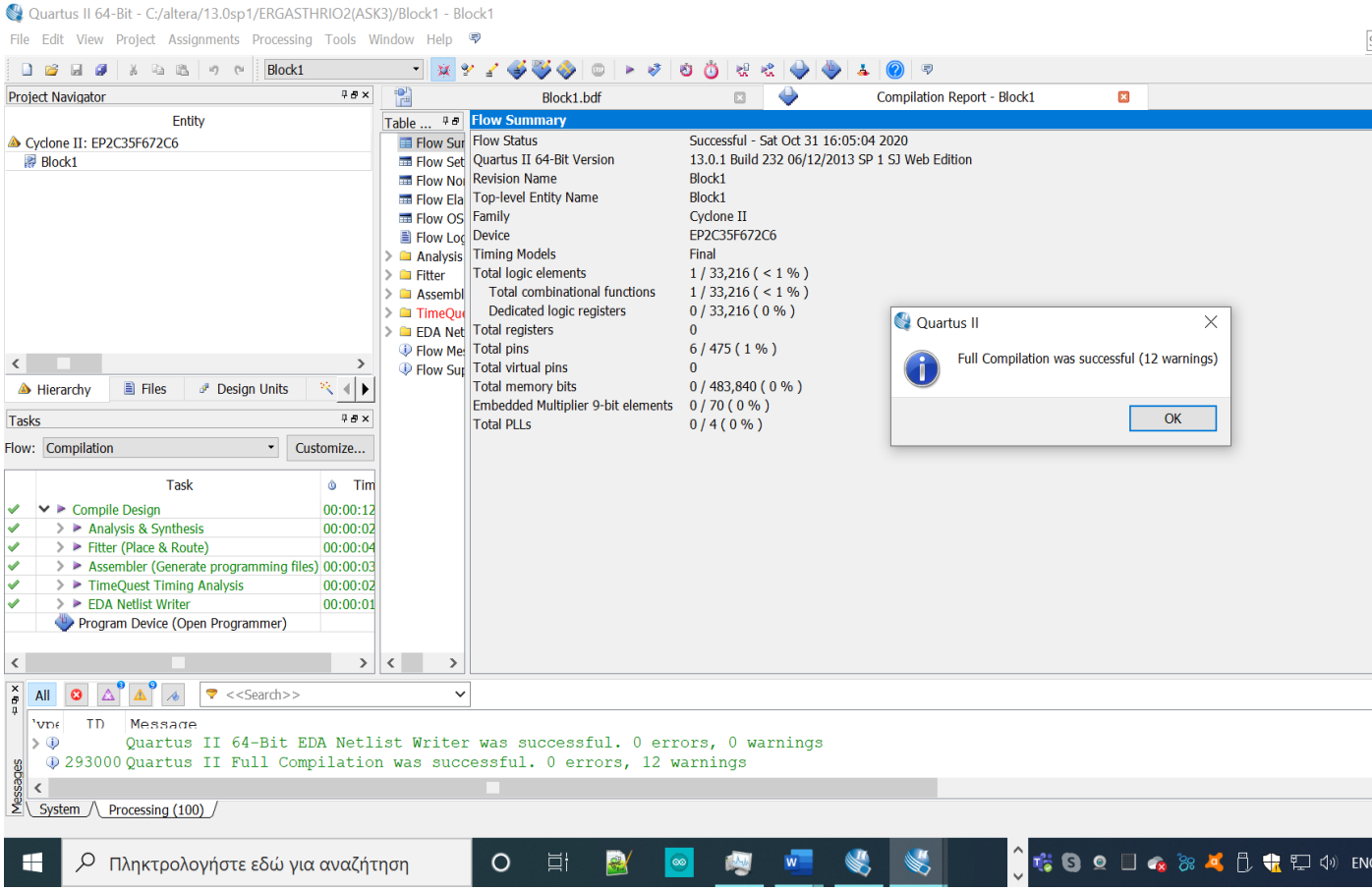

Quartus II 64-Bit - C:/altera/13.0sp1/ergsthrio2/Ergasthrio_Asksisi3 - Ergasthrio_Asksisi3
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
Ergasthrio_Asksisi3.bdf
Waveform.vwf
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design 00:00:12
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:05
Assembler (Generate programming files) 00:00:02
TimeQuest Timing Analysis 00:00:02
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
Ergasthrio_Asksisi3.bdf
Compilation Report - Ergasthrio_Asksisi3
Flow Summary
Flow Status Successful - Sat Oct 31 11:57:27 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name Ergasthrio_Asksisi3
Top-level Entity Name Ergasthrio_Asksisi3
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 1 / 33,216 (< 1 %)
Total combinational functions 1 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier
Total PLLs
Quartus II
Full Compilation was successful (12 warnings)
OK
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
System Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση


Simulation Waveform Editor - C:/altera/13.0sp1/ergsthrio2/Ergasthrio_Asksisi3 - Ergasthrio_Asksisi3 - [Waveform.vwf]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 858.37 ns
Interval: 858.37 ns
Start:
End:
Name
Value at 0 ps
a B 0
b B 0
c B 0
d B 0
f B X
h B X
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Simulation Waveform Editor - [Ergasthrio_Asksisi3.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 997.92 ns
Interval: 997.92 ns
Start:
End:
Name
Value at 0 ps
a B 0
b B 0
c B 0
d B 0
f B 0
h B 1
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
0%
00:00:00
9%
00:00:01
Πληκτρολογήστε εδώ για αναζήτηση
ENG
3:48 μμ
31/10/2020

ΤΟ ΑΝΤΙΣΤΟΙΧΟ ΔΙΑΓΡΑΜΜΑ ΜΕ ΠΥΛΕΣ NOR:




Quartus II 64-Bit - C:/altera/13.0sp1/ERGASTHRIO2(ASK3)/Block1 - Block1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Block1
Project Navigator
Entity
Cyclone II: EP2C35F672C6
Block1
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design 00:00:12
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:04
Assembler (Generate programming files) 00:00:03
TimeQuest Timing Analysis 00:00:02
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
Block1.bdf
Compilation Report - Block1
A
B
C
D
NOR
inst
OUTPUT
F
H
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (100)
408, 614 100%
00:00:12
Πληκτρολογήστε εδώ για αναζήτηση
ENG
4:07 μμ
31/10/2020


Quartus II 64-Bit - C:/altera/13.0sp1/ERGASTHRIO2(ASK3)/Block1 - Block1
File Edit View Project Assignments Processing Tools Window Help
Block1
Project Navigator
Entity
Cyclone II: EP2C35F672C6
Block1
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
Compile Design 00:00:12
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:04
Assembler (Generate programming files) 00:00:03
TimeQuest Timing Analysis 00:00:02
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
Block1.bdf
Compilation Report - Block1
Table ...
Flow Summary
Flow Status Successful - Sat Oct 31 16:05:04 2020
Quartus II 64-Bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name Block1
Top-level Entity Name Block1
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 1 / 33,216 (< 1 %)
Total combinational functions 1 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 6 / 475 (1 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
Quartus II
Full Compilation was successful (12 warnings)
OK
All
<<Search>>
Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
Messages
System Processing (100)
Πληκτρολογήστε εδώ για αναζήτηση