a module solution provider

WG7311-0A
WG7311-EA

WLAN/BT/FM Module

TI WL1271L IEEE 802.11b/g/n

BT 4.0 & FM solution

Datasheet

Revision 0.3

Index

1. OVERVIEW

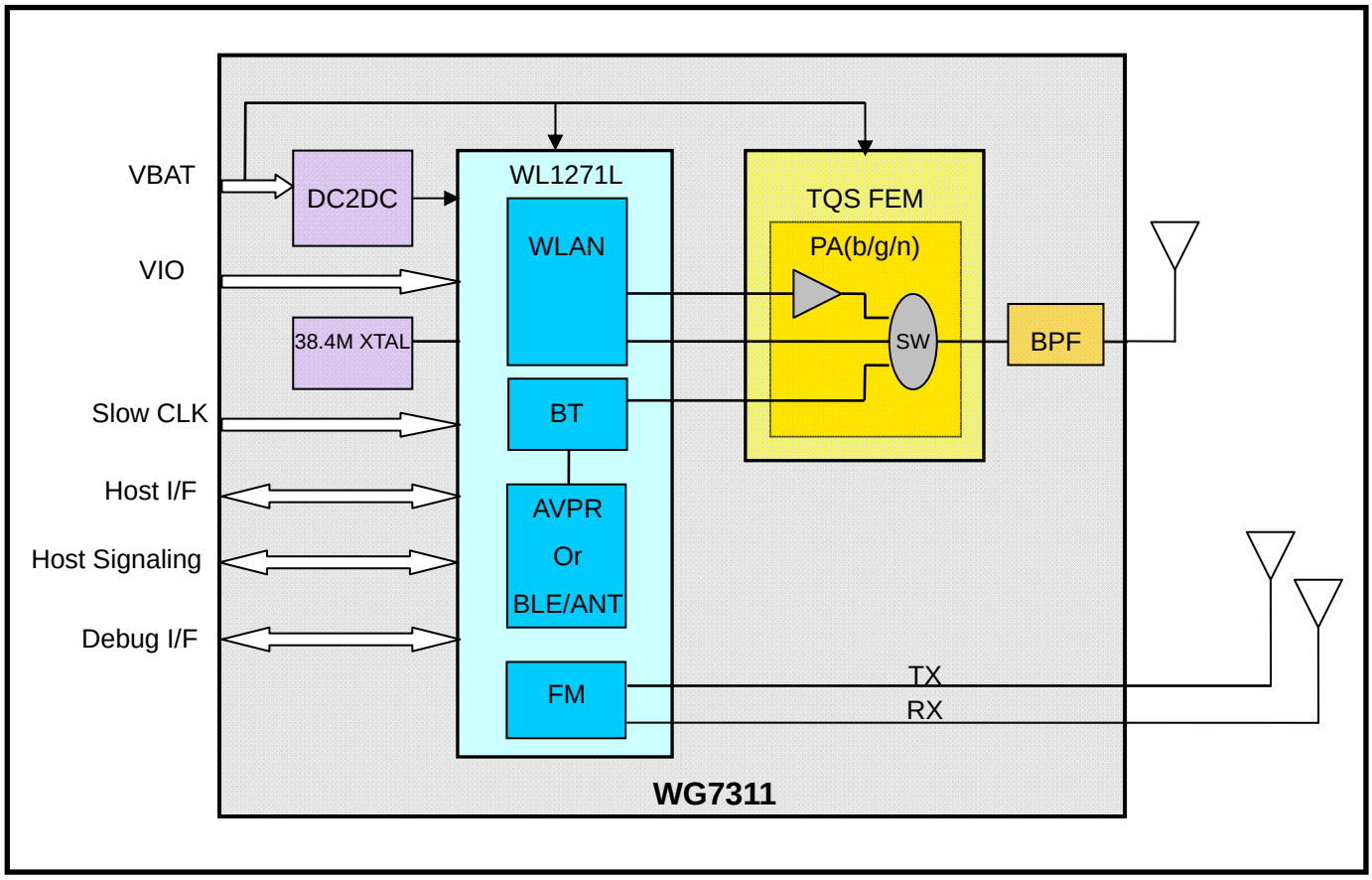
WG7311, a WiFi , Bluetooth and FM SiP (system in package) module, is the most demanded design for all handset and portable devices with TI WL1271L IEEE 802.11b/g/n and BT solutions to provide the best WiFi and BT coexistence interoperability and power saving technologies from TI.

1.1. General Features

- WLAN, Bluetooth and FM radio on a SiP module
- LGA96 pin package
- Dimension 10mm(L) x 10mm(W) x 1.4mm(H)
- Based on TI WL1271L 65-nm CMOS technology packaged in WSP for module
- Seamless integration with TI OMAP application processor and GSM-GPRS-UMTS chipset
- Internal support for WLAN and Bluetooth Co-existence (bandwidth sharing, antenna sharing)
- Direct connection to battery using external switching mode power supply supporting 5.5V to 2.3V operation
- VIO in the 1.8V domain
- Wide temperature range:
  Normal : -20˚C to 70˚C (WG7311-0A)
  Extended : -40˚C to 85˚C (WG7311-EA)

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram



2.2. Block Functional Feature

2.2.1. WLAN Features

- Support 802.11 2.4GHz b/g/n mode
- Optimized for ultra low current consumption in all operating modes including extremely low power modes
- IEEE Std 802.11d, e, h, I, k, r, s PICS compliant
- Supports Cisco Client eXtensions (CCX) standard
- Support Secure Digital Input/Output (SDIO) Interfaces

- Medium-Access Controller (MAC)
  - Embedded ARM Central Processing Unit (CPU)
  - 292kByte (Used for Program code, data and packet data) Embedded Random-Access Memory (RAM)
  - Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys
  - Supports Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
  - Designed to Work with IEEE Std 802.1x for Virtual Private Network (VPN) Solutions
- Baseband Processor
  - All IEEE Std 802.11b/g and 802.11n Data Rates up to 72.2Mbps
- 2.4 GHz Radio
  - Digital Radio Processor (DRP) implementation
  - Internal LNA
  - Supports: IEEE Std 802.11b, 802.11g, 802.11b/g, and 802.11n

2.2.2. Bluetooth Features

- Bluetooth 1.1, 1.2, 2.0+EDR and 2.1+EDR, 3.0 and 4.0 specification compliant – up to HCI level
- BT Enhanced Data Rate (2 and 3 Mbps)
- Enhanced host Interfaces (UART)
- Very low power consumption
- On-chip Embedded radio
- Embedded ARM Microprocessor System
- Temperature detection and compensation mechanism ensure minimal variation in the RF performance over the entire temperature range
- A2DP support
- Wide-Band Speech support
- Full support for the Ultra Low Power (ULP) Bluetooth standard (previously known as Wibree)

2.2.3. BLE Features

Fully compliant with BT4.0 Low Energy (BLE) dual mode standard:

- TI BLE solution optimized for the proximity/sports use-case
- Supports large number of multiple connections (up to 10)
- Multiple sniff instance are tightly coupled to achieve minimum power consumption
- Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN

Notes: Advanced audio and voice processing (AVPR) capabilities, and ANT are not available when BLE is enabled.

2.2.4. ANT Features

Fully compliant with all ANT Protocols:

- ANT solution optimized for the fitness, health and consumers use-case
- Supports large number of multiple connections (up to 8)
- Simple to complex network topologies
- Support high-resolution proximity pairing
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN
- ANT provides immediate access to the millions of ANT+ sensors already in the market and an ongoing option for cost and power optimized sensors

The ANT protocol has been designed to very power-efficient, yet is flexible enough to support various network topologies (point-to-point, star, 1-to-N, N-to-1) and data transfer modes (broadcast, broadcast with acknowledge, mass data transfer). Each logical ANT channel can be independently configured for 1-way or 2-way operation.

Notes: Advanced audio and voice processing (AVPR) capabilities, and BLE are not available when ANT is enabled.

2.2.5. FM Radio (RX/TX) Features

- On-Chip FM Receive
- On-Chip 0dBm output FM Transmitter
- Operation through BT host interface (UART) or separate I^2C interface for control and RDS data transfer
- Up to 48k Samples/sec audio sampling for stereo headsets
- Frequency resolution: 50-kHz step tuner
- Compatibility with Europe/US (87.5-108MHz) and Japan (76-90 MHz) FM Bands
- Full digital implementation
- Digital MPX signal, thus eliminating need for noise blanking circuits
- Integrated RDS/RDBS features
- Soft Mute
- Stereo/Mono blend based on signal condition for RX
- Selectable 50/75-us de-emphasis filter
- I^2S format for stereo/mono digital audio data
- Analog stereo audio inputs/outputs
- Software selectable level for soft mute and stereo/mono blend level for RX
- Fast independent up/down tuning function
- Supports a dedicated enable pin for the FM IP

3. MODULE SPECIFICATION

3.1. Absolute Maximum Ratings

Over operating free-air temperature range

Characteristics		Value	Unit
Supply Voltage Range	VBAT	-0.5 to 5.5	V
	VIO	-0.5 to 2.1	V
Input Voltage to Analog Pins		-0.5 to 2.1	V
Input Voltage to all Other Pins		-0.5 to VIO + 0.5V	V
Operating Ambient Temperature Range	WG7310-0A	-20 to 70	˚C
	WG7310-EA	-40 to 85	˚C
Storage Temperature Range	WG7310-0A	-40 to 85	˚C
	WG7310-EA	-50 to 105	˚C

3.2. Recommended Operating Conditions

The WG7311 requires two supplies: VBAT and VIO.

Power Supply	Voltage		
	Min.	Typ.	Max.
VBAT	2.3V	3.3V	4.8V
VIO	1.62V	1.8V	1.92V

3.3. WLAN RF

3.3.1. 2.4G Receiver

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP(1)	MAX	UNIT
Operation frequency range			2412		2484	MHz

Sensitivity(2)(3)	1 Mbps DSSS		-92.5	-96.0		dBm
	2 Mbps DSSS		-90.0	-92.5		
	5.5 Mbps CCK		-87.5	-90.5		
	11 Mbps CCK		-85.5	-88.0		
	6 Mbps OFDM		-88.0	-90.5		
	9 Mbps OFDM		-87.5	-89.5		
	12 Mbps OFDM		-86.0	-88.0		
	18 Mbps OFDM		-84.0	-86.0		
	24 Mbps OFDM		-81.5	-83.5		
	36 Mbps OFDM		-77.5	-80.0		
	48 Mbps OFDM		-73.5	-76.0		
	54 Mbps OFDM		-71.5	-74.0		
	MCS0(4)(5)		-87.5	-89.0		
	MCS1(4)(5)		-86.0	-88.0		
	MCS2(4)(5)		-84.0	-86.0		
	MCS3(4)(5)		-81.0	-85.0		
	MCS4(4)(5)		-77.5	-78.5		
	MCS5(4)(5)		-73.5	-75.5		
	MCS6(4)(5)		-71.5	-73.5		
	MCS7(4)(5)		-69.5	-71.5		
Max Iput Level(6)	OFDM(11g or 11n)				-15	dBm
	CCK				-8	
	1/2 DSSS				-4	
Adjacent Channel Rejection	54OFDM	ADJCI	30			dB
	11CCK		46.5			
Alternate Channel Rejection	54OFDM		-53			dBm
LO Leakage					-70	dBm

(1) Typical values are nominal room temperature

(2) For channel 13, sensitivity is degraded up to 2 dB in 802.11g/n.

(3) For channel 14, sensitivity is degraded up to 2 dB in 802.11b/g/n.

(4) Measurements without STBC with 1024 bytes.

(5) Greenfield mode : degrade 1 dB for mixed mode

(6) At < 10% PER limit

3.3.2. 2.4G Transmitter

CHARACTERISTICS	CONDITION	SYMBOL	MIN	MAX	UNIT
Maximum RMS output power	1 Mbps,2 Mbps(1)		17.5		dBm
	5.5 Mbps,11 Mbps(1)		17.5		
	6 Mbps,9 Mbps(2)		17.0		
	12 Mbps,1 8Mbps		16.5		
	24 Mbps,36 Mbps		13.5		
	48 Mbps,54 Mbps		13.0		
	MCS0(1)		16.0		
	MCS1,2		15.5		
	MCS3,4		13.5		
	MCS5,6		12.5		
	MCS7(Greenfield)(3)(4)		11.0		
Special mask margin	Each frequency region detailed in(5)		2		dB
EVM	24 Mbps and 36 Mbps at +14.5dBm		-21		dB
	48 Mbps and 54 Mbps at +13.0dBm)		-25		
	MCS7 at + 12.0dBm		-28		

(1) Customers are advised to look at filter insertion loss and board trace losses when assessing the maximum number to be calibrated during the production line testing

(2) At V_{BAT} = 2.7 V , performance degrades up to 0.5 dB , At-30℃ performance degraded up to additional 0.5 dB

(3) At V_{BAT} = 2.7 V , performance degrades up to 0.5 dB

(4) Mixed mode degrades 1.0dB;channel 10 at 75℃ degrades 0.5 dB more(total up to 1.5 dB).

(5) At V_{BAT} = 2.7 V , performance degrades up to 1.5 dB

(6) Spectral mask regions are defined according to the IEEE802.11 specifications (Regions A through C for 802.11b;Regions D through F for 802.11g):

Region A:f∈[Fc-22MHz,Fc -11 MHz] ∪[Fc+11 MHz, Fc +22 MHz]

Region B:f∉ [Fc-22MHz,Fc +22 MHz]

Region C:f∈[Fc-11MHz,Fc -9 MHz]∪[Fc+9 MHz, Fc +11 MHz]

Region D:f∈[Fc-20MHz,Fc -11 MHz]∪[Fc+11 MHz, Fc +20 MHz]

Region E:f∈[Fc-30MHz,Fc -20 MHz]∪[Fc+20 MHz, Fc +30 MHz]

Region F:f∉ [Fc-30MHz,Fc +30 MHz]

3.4. Bluetooth RF

BT Transmitter, GFSK, Class 2 & Class 1.5					
Characteristics		**Min**	**Typ**	**Max**	**Unit**
RF output power	CLASS1P5 = VBAT	7	9	---	dBm
Power variation over BT band		-1		1	dB
Gain control range			30		dB
Power control step		2	5	8	dB

BT Receiver Characteristics, In-Band Signals					
Characteristics		**Min**	**Typ**	**Max**	**Unit**
Sensitivity	GFSK, BER = 0.1%	-86	-90	---	dBm
	Pi/4-DQPSK, BER = 0.01%	-86	-90	---	
	8DPSK, BER = 0.01%	-80	-84	---	
Max. useable input power	GFSK, BER = 0.1%	-5	---	---	dBm
	Pi/4-DQPSK, BER = 0.1%	-10	---	---	
	8DPSK, BER = 0.1%	-10	---	---	

3.5. BLE RF

BT Transmitter						
Characteristics		**Min**	**Typ**	**Max**	**BLE SPEC**	**Unit**
RF output power	CLASS1P5 = VBAT	7	9	---	<= 10	dBm
Power variation over BLE band		-1		1		dB

BT Receiver Characteristics, In-Band Signals						
Characteristics		**Min**	**Typ**	**Max**	**BLE SPEC**	**Unit**
Sensitivity	PER=30.8%	-89	-92	---	<= -70	dBm

Max. useable input power	GFSK, PER = 30.8%	-5	---	---	>= -10	dBm

3.6. FM Radio Electrical Characteristics

Characteristics	Condition		Min	Typ	Max	Unit
Audio output impedance	FM function enabled and during auto-search				50	Ω
	FM function disabled and when muted		50			KΩ
Audio input impedance			30			KΩ
Selectable RF Rx input impedance	With external matching circuitry – Default = 50 Ω			50	500	Ω
RF input return loss	With external matching circuitry		-10			dB
Receiver current consumption	FM Rx at sensitivity level, BT in deep sleep			12	15	mA
Transmitter current consumption	FM TX on, BT in deep sleep	Digital audio		13	16	mA
		Analog audio				
FM off current				1	2	uA

3.7. External Slow Clock Input (SLEEP_CLK)

The external slow clock input SLEEP_CLK must be present at all times. The slow clock is used to maintain timers that synchronize the device to the access point (AP) beacons.

Table 1. External Slow Clock Input Requirements

Characteristics (1)	Condition	Min.	Typ.	Max.	Unit
Frequency			32.768		KHz
Reference Frequency	WLAN, BT,			+/-150	ppm

Accuracy	FM_RX				
	FM_TX (2)			+/- 40	
Input Transmit Time	10% ~ 90%			100	ns
Frequency Duty Cycle		30	50	70	%
Fail Safe Maximum Value				2.0	V
Input Voltage Limits	V_{IH}	0.65xVIO		VIO	V_{peak}
(Square Wave)	V_{IL}	0		0.35xVIO	
Input Impedance		1			MΩ
Input Capacitance				5	pF
Rise and fall time				100	ns
Phase noise	1kHz		-125		dBc/Hz
Jitter (3)	Integrated over 300Hz ~ 15000Hz			1	Hz

(1) Slow clock is a fail safe input

(2) If the available slow clock source does not meet the +/-40ppm requirement, there are two options;

- Use the fast clock for the FM_TX functionality. This is configured using a vendor-specific command to switch to Fref operation after enabling the FM core with the slow clock source.
- Enable clock error calibration in the FM core to compensate for the clock source error. The calibration can be done using a known vendor-input clock error or intrinsically to the core (self-calibration).

(3) Not required if fast clock is used for FM TX and RX

4. POWER CONSUMPTION

4.1. Device Shutdown Current

The SDIO/CLK_REQ lines should be driven by the host to prevent leakage in sleep/shutdown modes.

Mode Description	Power Supply	Typ.	Max.	Unit
Shutdown mode (BT, WLAN and FM sections in shutdown mode) Values are over process and at room temperature	1.8V (VIO)	3	5	uA
	Total V_{BAT} at 3.6V	14	35	

4.2. WLAN Power Consumption

WLAN supply current was measured using the HDK and the TrioScope tool, over process and temperature at F_{ref} 38.4MHz unless otherwise specified.

4.2.1. Active Mode

- During Listen Mode operation, the radio is in a low power mode optimized to receive only 11b beacons. The DC2DC, FEM and WL1271 devices are active but consume less current.
- In STBY mode, no RF operation required. The DC2DC, FEM and WL1271 device are active but consume lower current.
- In TX and RX modes, all devices are active and consume maximum currents.

Mode Description		Power Supply	11Mbps IEEE802.11b		54/65Mbps IEEE802.11g/n		Unit
			Typ (1)	Max (2)	Typ (1)	Max (2)	
Transmit	11b/g: Packet size	1.8V (VIO)	0.25	0.3	0.25	0.3	mA

Data	=2048 bytes 11n: Packet size =1024 bytes 11b delay=0.004ms 11g/n delay=0.002ms	Total V_{BAT} =3.6V	FEM current only	190	220	110	137	
			System current	260	275	189	207	
Receive Data (3)		1.8V (VIO)		0.25	0.3	0.25	0.3	mA
		Total V_{BAT} =3.6V		92	103	92	103	
Listen (3)		1.8V (VIO)		0.25	0.3	n/a	n/a	mA
		Total V_{BAT} =3.6V		69	75	n/a	n/a	
STBY		1.8V (VIO)		0.25	0.3	0.25	0.3	mA
		Total V_{BAT} =3.6V		6	9	6	9	

(1) Nominal process at 25℃

(2) Over process and temperature

(3) CH14 values add up to 2mA

4.2.2. Inactive and Dynamic Modes

Mode Description	Power Supply	Typ	Max	Unit
Sleep mode (BT and FM in reset) (1) (2)	1.8V (VIO)	12	15	uA
	Total V_{BAT} at 3.6V	85	107	

(1) Values indicate current between beacons

(2) Room temp over process

Mode Description (1)	Power Supply	Max	Unit
Dynamic mode Beacon (DTIM =1 : TBTT = 100ms) Beacon duration~1.6ms : Rate= 1Mbps Beacon in Listen mode	Total V_{BAT} at 3.6V to TPS62611	0.75	mA

(1) This mode reflects results with software drivers and not the Triscope tool.

4.3. BT Power Consumption

BT supply current was measured using the HDK and HCI Tester tool at F_{ref} 38.4MHz.

4.3.1. Static State

Characteristics		Typ	Max	Unit
Supply current in deep sleep mode	VIO	12	15	uA
	V_{BAT}	62	80	

4.3.2. Dynamic State

Transmit power at 4dBm, nominal, room temperature, V_{BAT}=3.6V, F_{ref} at 38.4MHz.

Use Case	Mode Description	Full V_{BAT} Source	Mixed Mode		Unit
			1.8V (1)	V_{BAT} (2)	
Idle current (ARM off) (3)	Master/Slave	1.8	2.9	0	mA
SCO link HV3	Master/Slave	8	11.4	1.2	
eSCO link EV3 64Kbps, no retransmission	Master/Slave	8.2	11.5	1.3	
eSCO link 2-EV3 64Kbps, no retransmission	Master/Slave	5.6	8.5	0.6	
GFSK full throughput: Tx=DH1, RX=DH5	Master/Slave	23.5	37.5	1.2	
EDR full throughput: Tx=2-DH1, RX=2-DH5	Master/Slave	24.3	38.6	1.1	
EDR full throughput: Tx=3-DH1, RX=3-DH5	Master/Slave	24.9	38.5	1.1	
Sniff, 1 attempt, 1.28sec	Master/Slave	100/110	90/115	<10	uA
Page or Inquiry Scan 1.28s, 11.25ms	Master/Slave	230	315	0	
Page scan 1.28s, 11.25msec and Inquiry Scan 2.56s, 11.25ms	Master/Slave	320	435	0	
Low power scan, 1.28 interval	Master/Slave	145	150	0	

(1) Voltage Input at INPUT_VBAT_SUPPLY

(2) Voltage input at BT_CLASS_1P5

(3) IDLE is a state in which the BT is awake and communicates with the host, but there is no RF activity.

4.4. BLE Power Consumption

BLE supply current was measured using the HDK and HCI Tester tool at Fref = 38.4 MHz.

Operational Mode	Description	Full V_{BAT} Source	Unit
Advertising (non-connectable)	AdvInterval = 1.28 s Adv Data = 15 Octets TX output power = +10 dBm Advertising on 3 adv channels	1124	uA
Advertising (discoverable)	AdvInterval = 1.28 s Adv Data = 15 Octets TX output power = +10 dBm Advertising on 3 adv channels	135	
Scanning	scanInterval = 1.28 s scanWindow = 11.25 ms Listens on single frequency per window	245	
Link Layer connection (master)	Master role connInterval = 500 ms connSlaveLatency = 0 Empty TX/RX LL packets TX output power = +10 dBm	160	

5. Module Outline

5.1. Signal Layout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	1	A1 GND	A2 N.C.	A3 VBAT	A4 VIO	A5 PM_DC_REQ	A6 GND	A7 CM_XTALM	A8 GND	A9 FA_AUD_IN_L	A10 GND	A11 FA_AUD_IN_R
B	2	B1 BD_WU	B2 GND	B3 CLASS1P5	B4 1V8	B5 N.C.	B6 N.C.	B7 GND	B8 CM_XTALP	B9 GND	B10 FA_AUD_OUT_L	B11 GND
C	3	C1 N.C.	C2 BD_TX_DBG								C10 GND	C11 FA_RX_ANT
D	4	D1 N.C.	D2 GND			D4 BD_AUD_CLK	D5 BD_AUD_FSYNC	D6 BD_HCI_CTS	D7 BD_HCI_RTS	D8 N.C.	D10 FA_AUD_OUT_R	D11 GND
E	5	E1 GND	E2 N.C.			E4 BD_AUD_IN	E5 BD_AUD_OUT	E6 GND	E7 GND	E8 BD_HCI_TX	E10 GND	E11 FA_TX_ANT
F	6	F1 N.C.	F2 GND			F4 GND	F5 GND		F7 GND	F8 BD_HCI_RX	F10 MD_SLOWCLK	F11 GND
G	7	G1 GND	G2 N.C.			G4 N.C.	G5 GND	G6 GND	G7 GND	G8 WD_IRQ	G10 GND	G11 FD_I2S_DO
H	8	H1 N.C.	H2 GND			H4 GND	H5 N.C.	H6 N.C.	H7 WD_UART_DBG	H8 MD_CLK_REQ_OUT	H10 FD_I2S_DI	H11 FD_I2S_CLK
J	9	J1 N.C.	J2 N.C.								J10 FD_IRQ	J11 FD_SCL
K	10	K1 GND	K2 N.C.	K3 N.C.	K4 BD_EN	K5 GND	K6 WD_RS232_RX	K7 WD_RS232_TX	K8 DS_SPI_CSX	K9 DS_SPI_DOUT	K10 FD_I2S_FSYNC	K11 FD_SDA
L	11	L1 N.C.	L2 GND	L3 FD_EN	L4 GND	L5 WB_RF_ANT	L6 GND	L7 DS_SDIO_D1	L8 DS_SDIO_D2	L9 DS_SPI_DIN	L10 DS_SPI_CLK	L11 WD_EN

WG7311 Pin Assignment Top View

5.2. Pin Description

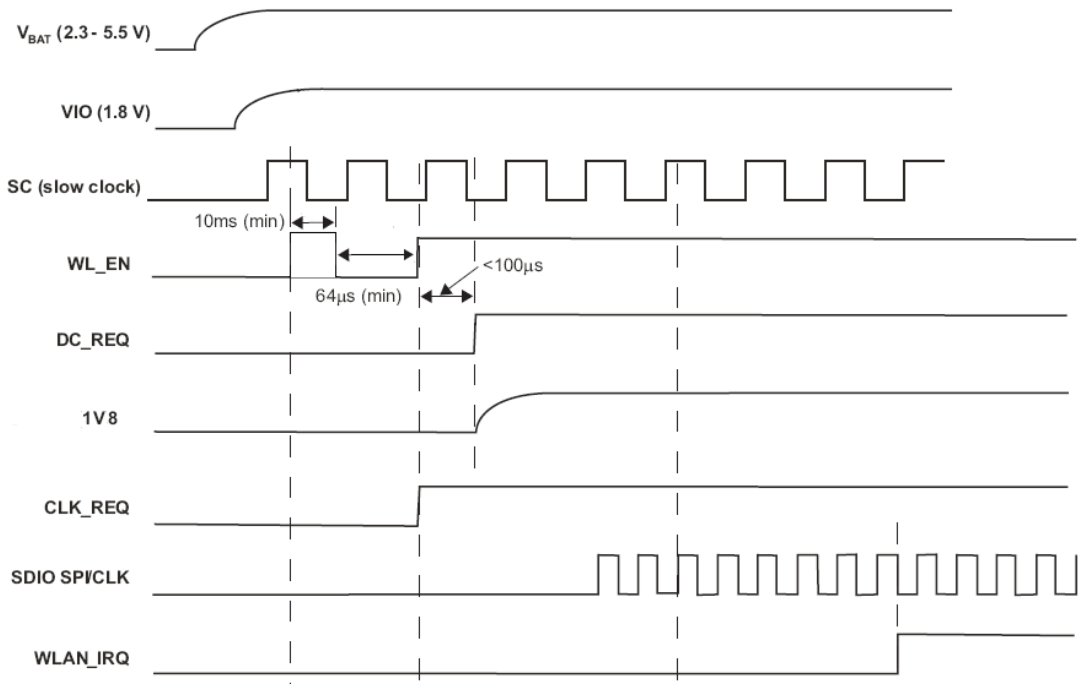
No.	Index	Name	Type	Description
1	A1	GND	GND	GROUND
2	A2	N.C.	-	Not connected
3	B1	BT_FUNC2: BT_WU/ DC2DC	O	BT WU (default) or BT DC2DC
4	B2	GND	GND	GROUND
5	C1	N.C.	-	Not connected
6	C2	BT_FUNC4: BT_TX_DBG	O	BT UARTD (reserved for debug)
7	D1	N.C.	-	Not connected
8	D2	GND	GND	GROUND
9	E1	GND	GND	GROUND
10	E2	N.C.	-	Not connected
11	F1	N.C.	-	Not connected
12	F2	GND	GND	GROUND
13	G1	GND	GND	GROUND
14	G2	N.C.	-	Not connected
15	H1	N.C.	-	Not connected
16	H2	GND	GND	GROUND
17	J1	N.C.	-	Not connected
18	J2	N.C.	-	Not connected
19	K1	GND	GND	GROUND
20	K2	N.C.	-	Not connected
21	L1	N.C.	-	Not connected
22	L2	GND	GND	GROUND
23	L3	FM_EN	I	FM RST
24	K3	N.C.	-	Not connected
25	L4	GND	GND	GROUND
26	K4	BT_EN	I	BT RST
27	L5	WB_RF_ANT	I/O	WL/BT RF ANT
28	K5	GND	GND	GROUND
29	L6	GND	GND	GROUND
30	K6	WL_RS232_RX/ I2S_M_SCL	I	RS232_RX (default) or I2C_M_SCL (reserved for debug)
31	L7	SDIO_D1	I/O	SDIO IF

No.	Index	Name	Type	Description
32	K7	WL_RS232_TX/ I2S_M_SDA	O	RS232_TX (default) or I2C_M_SDA (reserved for debug)
33	L8	SDIO_D2	I/O	SDIO IF
34	K8	SDIO_D3	I/O	SDIO IF
35	L9	SDIO_CMD	I/O	SDIO IF
36	K9	SDIO_D0	I/O	SDIO IF
37	L10	SDIO_CLK	I	SDIO IF
38	K10	FM_I2S_FSYNC	I/O	FM I2S IF
39	L11	WL_EN	I	WL RST
40	K11	FM_SDA	I/O	FM I2C IF
41	J11	FM_SCL	I/O	FM I2C IF
42	J10	FM_IRQ	O	FM I2C IF
43	H11	FM_I2S_CLK	I/O	FM I2S IF
44	H10	FM_I2S_DI	I	FM I2S IF
45	G11	FM_I2S_DO	O	FM I2S IF
46	G10	GND	GND	GROUND
47	F11	GND	GND	GROUND
48	F10	SLOWCLK	I	SLEEP CLK
49	E11	FM_TX_ANT	O	FM TX ANT
50	E10	GND	GND	GROUND
51	D11	GND	GND	GROUND
52	D10	FMAUDROUT	O	FM AUD OUT
53	C11	FM_RX_ANT	I	FM RX ANT
54	C10	GND	GND	GROUND
55	B11	GND	GND	GROUND
56	B10	FMAUDLOUT	O	FM AUD OUT
57	A11	FMAUDRIN	I	FM AUD IN
58	A10	GND	GND	GROUND
59	A9	FMAUDLIN	I	FM AUD IN
60	B9	GND	GND	GROUND
61	A8	GND	GND	GROUND
62	B8	XTALP	O	FREF INPUT (internal use only)
63	A7	XTALM	O	FREF INPUT (internal use only)
64	B7	GND	GND	GROUND

No.	Index	Name	Type	Description
65	A6	GND	GND	GROUND
66	B6	DC2DC_MODE	-	Connect to B5
67	A5	DC_REQ	O	DC_REQ to INTERNAL DC2DC
68	B5	DC2DC_MODE	-	Connect to B6
69	A4	VIO	I	1.62~1.92V POWER SUPPLY, 1.8V TYP
70	B4	1V8	O	1.8V DC2DC POWER SUPPLY
71	A3	VBAT	I	2.3~4.8V POWER SUPPLY, 3.3V TYP
72	B3	VDD_LDO_IN_CLASS1P5	I	BT CLASS2/CLASS1.5 POWER SUPPLY
73	D4	PCM_AUD_CLK	I/O	PCM I/F
74	E4	PCM_AUD_IN	I/O	PCM I/F
75	F4	GND	GND	GROUND
76	G4	N.C.	-	Not connected
77	H4	GND	GND	GROUND
78	H5	N.C.	-	Not connected
79	H6	N.C.	-	Not connected
80	H7	WL_UART_DBG	O	WL_UART_DBG (reserved for debug)
81	H8	CLK_REQ_OUT	O	CLK_REQ positive polarity
82	G8	WLAN_IRQ	O	WLAN interrupt request
83	F8	HCI_RX	I	BT UART I/F
84	E8	HCI_TX	O	BT UART I/F
85	D8	N.C.	-	Not connected
86	D7	HCI_RTS	I/O	BT UART I/F
87	D6	HCI_CTS	I/O	BT UART I/F
88	D5	PCM_AUD_FSYNC	I/O	PCM I/F
89	E5	PCM_AUD_OUT	O	PCM I/F
90	F5	GND	GND	GROUND
91	G5	GND	GND	GROUND
92	G6	GND	GND	GROUND
93	G7	GND	GND	GROUND
94	F7	GND	GND	GROUND
95	E7	GND	GND	GROUND
96	E6	GND	GND	GROUND

6. Power Sequence

6.1. WLAN Power on Sequence



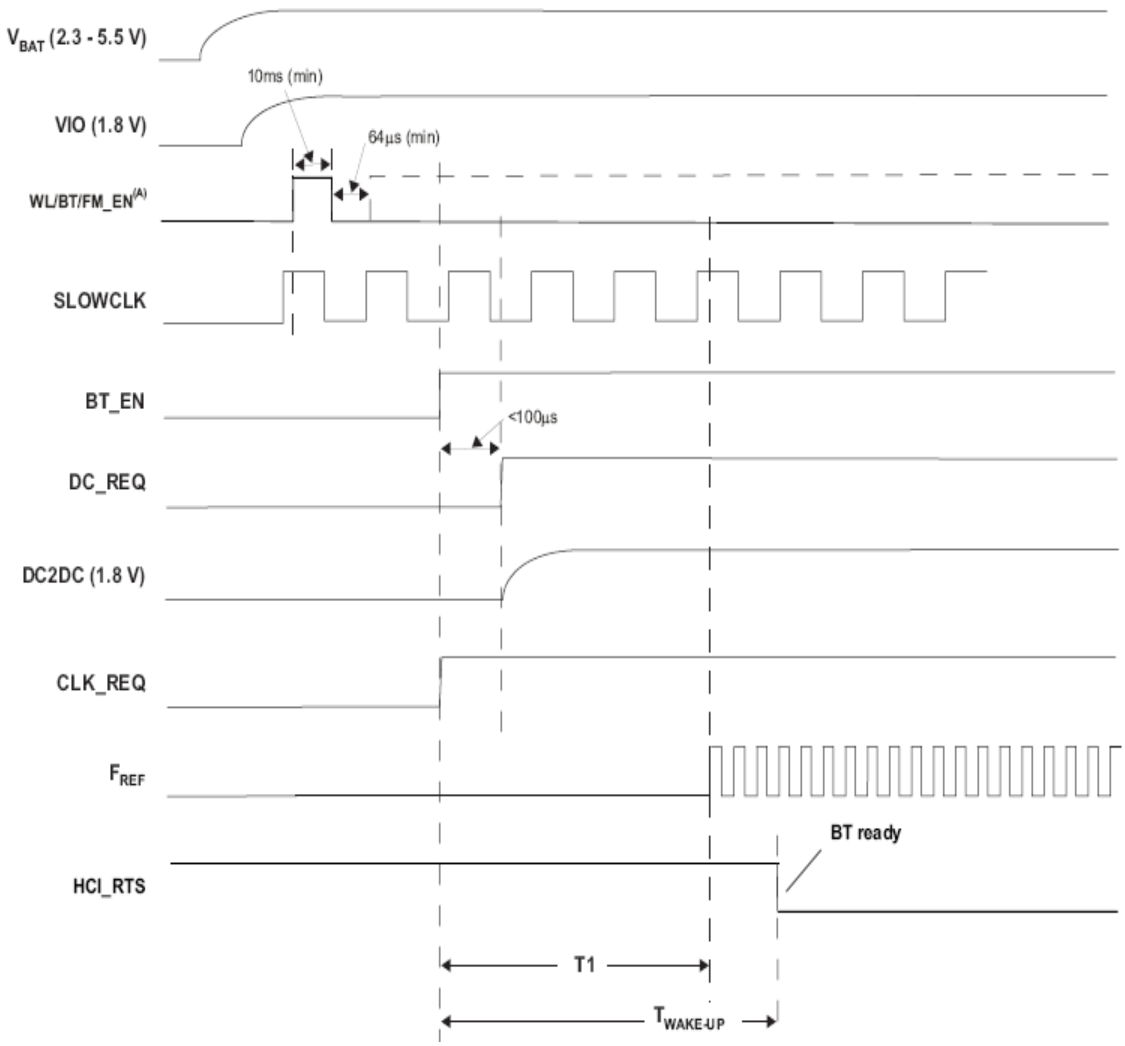
WLAN Power on sequence

The sequence describes device power up from shutdown.

6.2. Bluetooth Power Up Sequence

Power up requirements:

1. BT_EN must be low
2. VIO must be stable before releasing BT_EN.
3. Slow clock must be stable within 2 ms of BT_EN high.



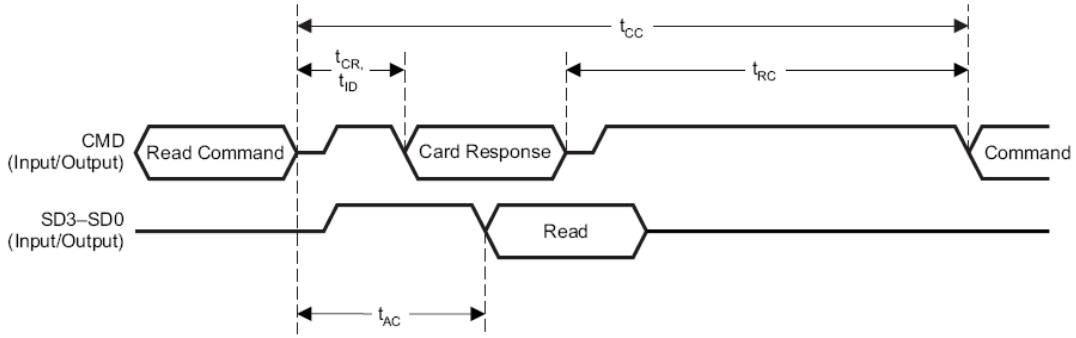
Bluetooth Power Up sequence

WG7311 indicates completion of power up sequence by asserting RTS low. This occurs up to 100ms after BT_EN goes high.

7. Interface Characteristics

7.1. WLAN SDIO Characteristic

7.1.1. SDIO Read Timing



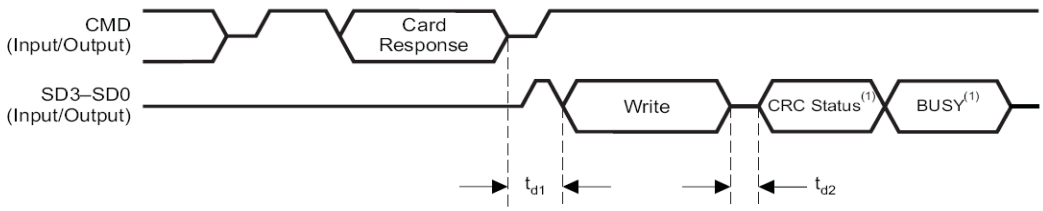
SDIO Single Block Read

Table 2. SDIO Read Switching characteristics

Table 3.

PARAMETER			MIN	MAX	UNIT
t_{CR}	Delay time, assign relative address or data transfer mode	Read-command CMD valid to card-response CMD valid	2	64	Clock cycles
t_{CC}	Delay time, CMD command valid to CMD command valid		58		Clock cycles
t_{RC}	Delay time, CMD response valid to CMD command valid		8		Clock cycles
t_{AC}	Access time, CMD command valid to SD3–SD0 read data valid		2		Clock cycles

7.1.2. SDIO Interface Write Timing



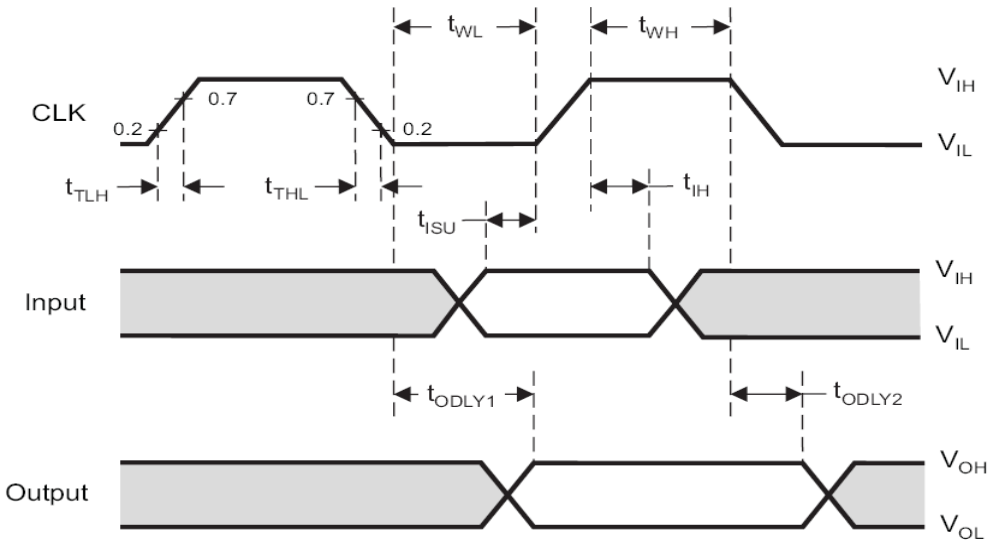
(1) CRC status and busy waveforms are only for data line 0. Data lines 1-3 are N/A. The busy waveform is optional and may not be present.

SDIO Single Block Write

Table 4. SDIO Write Switching characteristics

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, CMD card response invalid to SD3–SD0 write data valid	2		Clock cycles
t_{d2}	Delay time, SD3–SD0 write data invalid end to CRC status valid	2	2	Clock cycles

7.1.3. SDIO Clock Timing

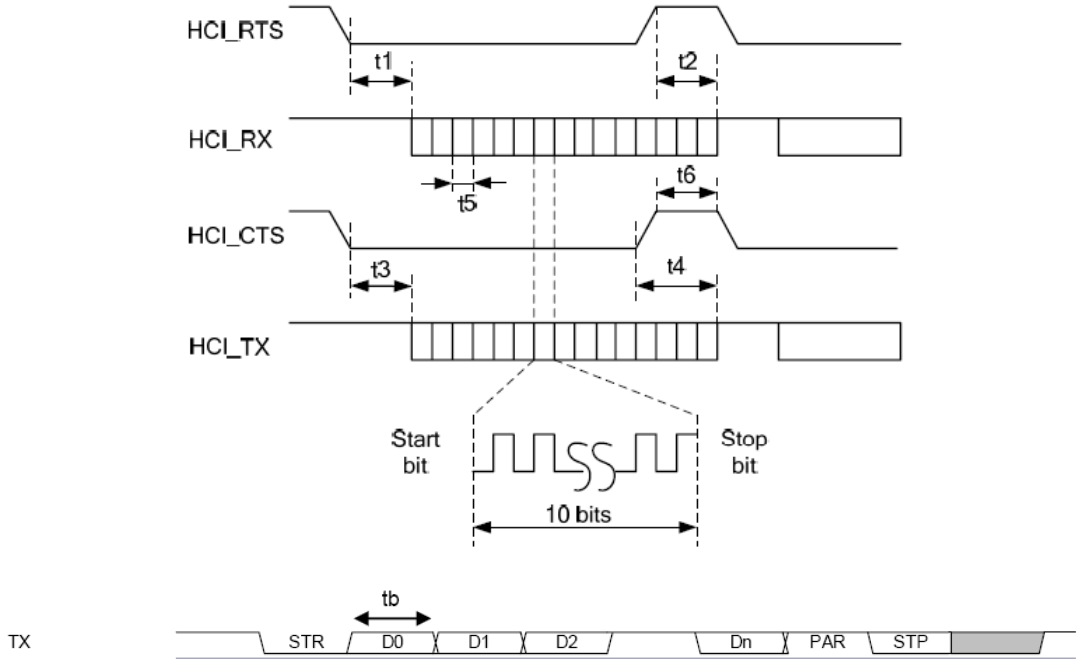


SDIO Clock Timing

Table 5. SDIO Timing requirement

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	$C_L \leq 30$ pF	0	26	MHz
DC	Low/high duty cycle	$C_L \leq 30$ pF	40	60	%
t_{TLH}	Rise time, CLK	$C_L \leq 30$ pF		4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 30$ pF		3.5	ns
t_{ISU}	Setup time, input valid before CLK ↑	$C_L \leq 30$ pF	4		ns
t_{IH}	Hold time, input valid after CLK ↑	$C_L \leq 30$ pF	5		ns
t_{ODLY}	Delay time, CLK↓ to output valid	$C_L \leq 30$ pF	2	12	ns

7.2. Bluetooth HCI Interface



* STR: Start bit; D0…Dn: Data bits (LSB first); PAR: Parity bit (if parity is used); STP: Stop bit

Table 6. BT HCI Timing characteristics

Characteristics	Condition	Symbol	Min	Typ.	Max	Unit
Baud rate	Any rate (1)		37.5	115.2	4000	kbps
Baud rate accuracy	Receive,Transmit	t5, t7			-2.5to+1.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS high pulse width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes

Exception for 19.2MHz: Maximum baud rate = 3.84Mbps.

7.3. Bluetooth PCM Interface

Bluetooth can be setting as master or slave mode. For more stable voice performance, slave mode is recommended.

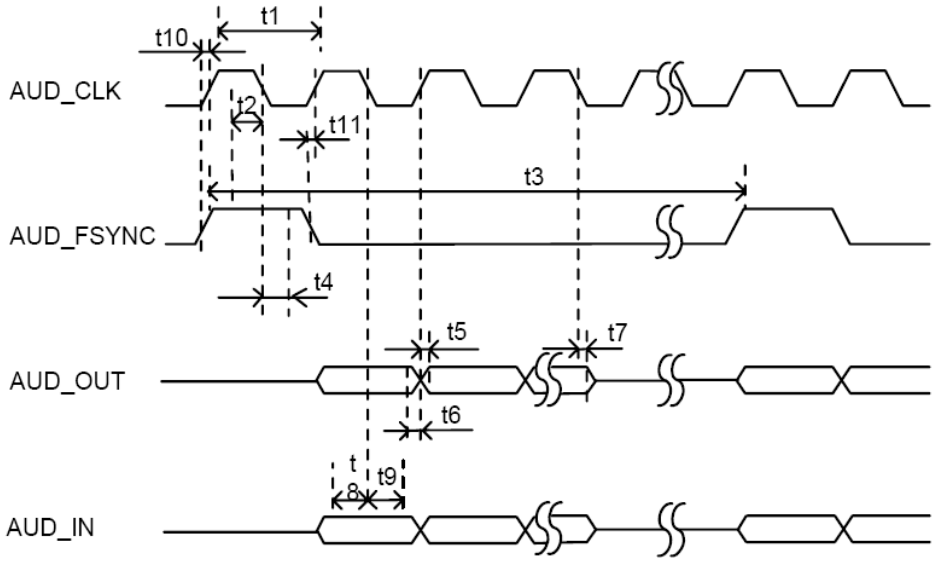


Table 7. BT PCM Slave mode Timing characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit
Master clock frequency	1/t1	64		16000	KHz
Clock duty cycle		40	50	60	%
Synchronization clock frequency	1/t3	1/(8xt1)		1/(65535xt1)	KHz
Synchronization signal width		t1		165545xt1	
Setup time for AUD_FSYNC high to AUD_CLK low	t2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t7			20	ns

8. Debug Interface

The debug interface helps customers to evaluate the HW/SW features for their application. It also helps to debug during the development stage. The WG7311 module support RS232 signals and UART signals for debug purpose. Connect RS232 and UART signals to the test points for future debug support.

8.1. WLAN RS232 Testing Port

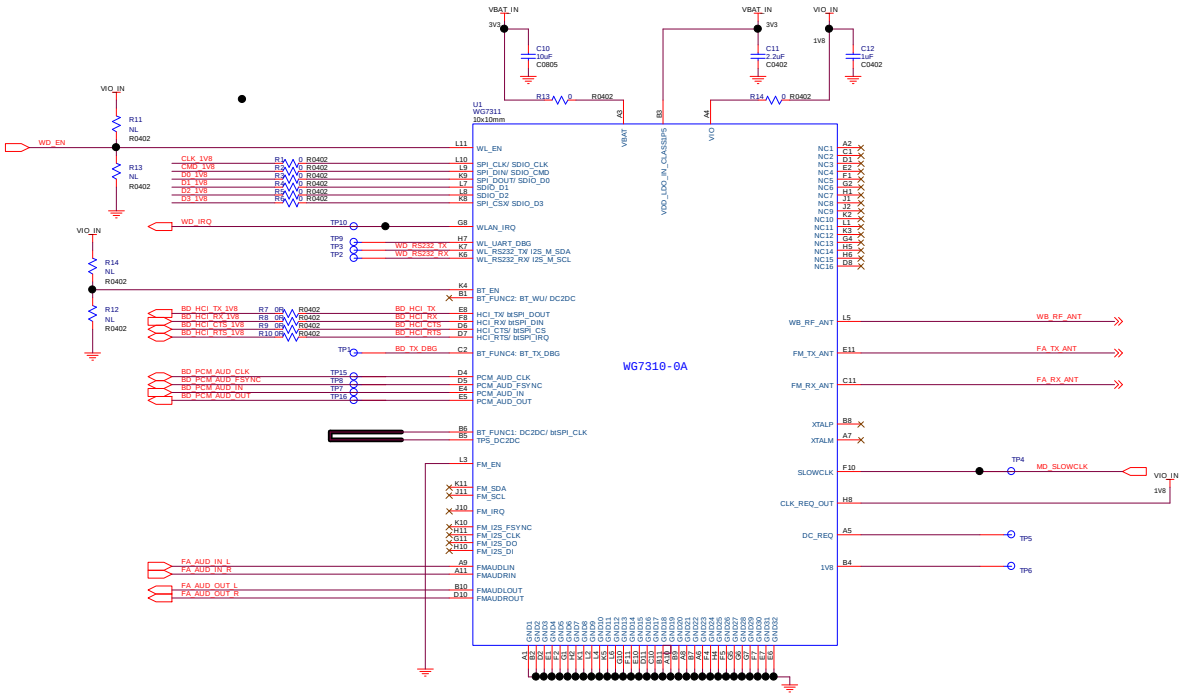
"Direct" serial interface (RS232_TX, RS232_RX) used by WLAN TrioScope software package for WLAN RF performance test, debug and manufacturing application.

8.2. Bluetooth HCI Testing Port

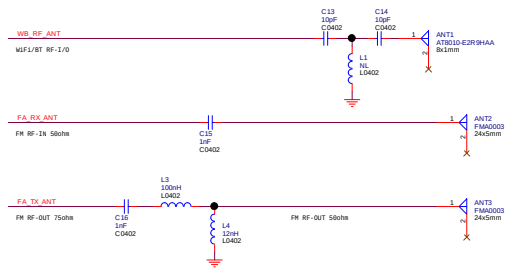
HCI_TX and HCI_RX are used by Bluetooth "HCI Tester" software package for Bluetooth RF performance test, debug and manufacturing application.

9. Reference Schematic

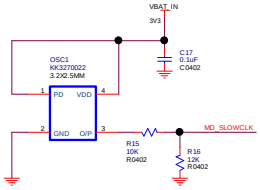
WG7311 MODULE



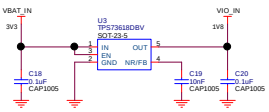
ANTENNA CIRCUITS

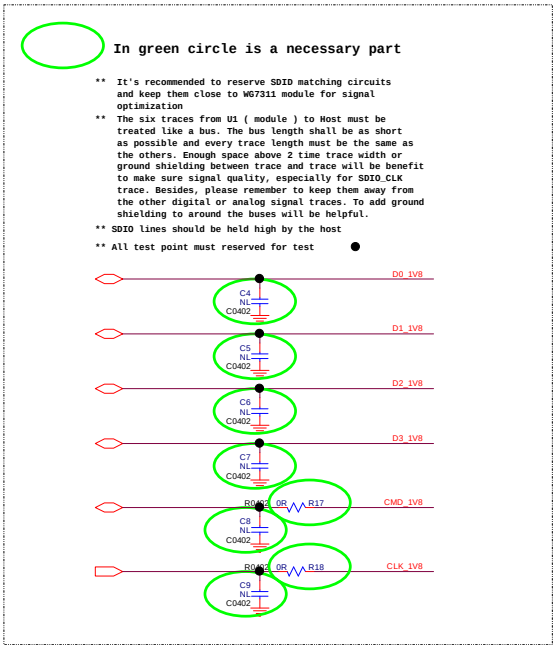


32.768K XOSC



1.8V LDO





Scheme Brief

WiFi Interface: SDIO

BT Interface: UART, PCM

FM Interface: UART (with BT together), Audio IN/OUT

Fast Clock: 38.4MHz built-inside

Slow Clock: 32.768KHz from outside

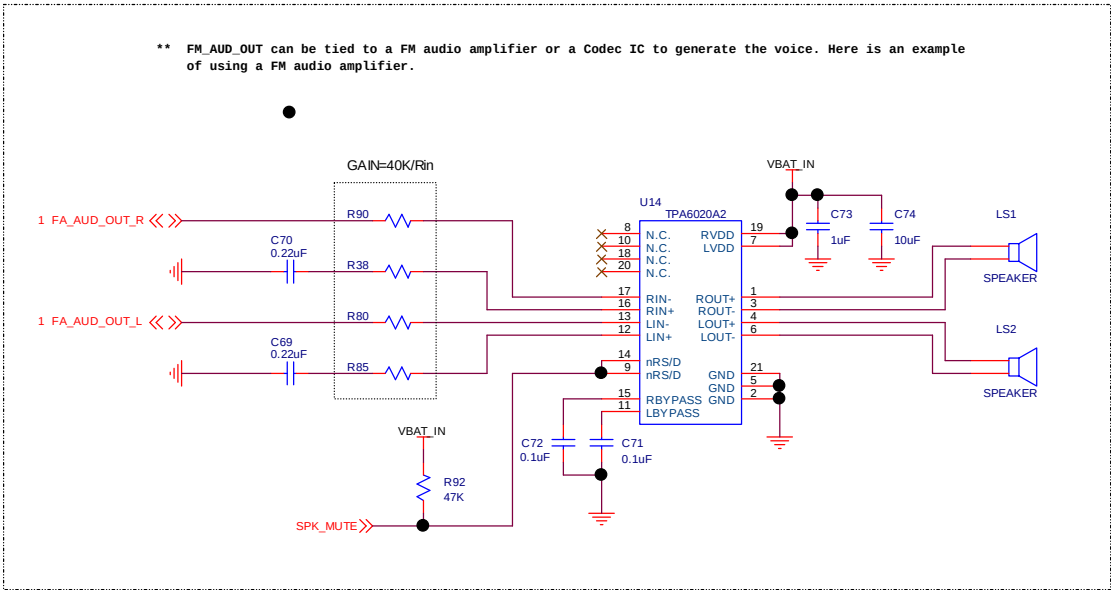
** Boot Conditions

VBAT_IN: 2.7~4.8V => 3.3V TYP

VIO_IN: 1.62~1.92V => 1.8V TYP

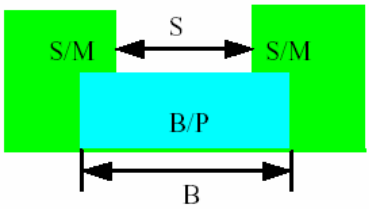
Slow Clock: 32.768KHz for module boot and deep sleep

1V8 FM AUDIO Output (Option)



10. Layout Recommendation

10.1. Recommended Bump Pad Design



Item	Recommend	Unit
"B" Bump pad diameter on SMD PCB	600	um
"S" Solder Mask Opening	400	um

Recommended Bump Pad Design for WG7311

COMMENT:

SMD = Solder Mask Define

S/M= Solder Mask

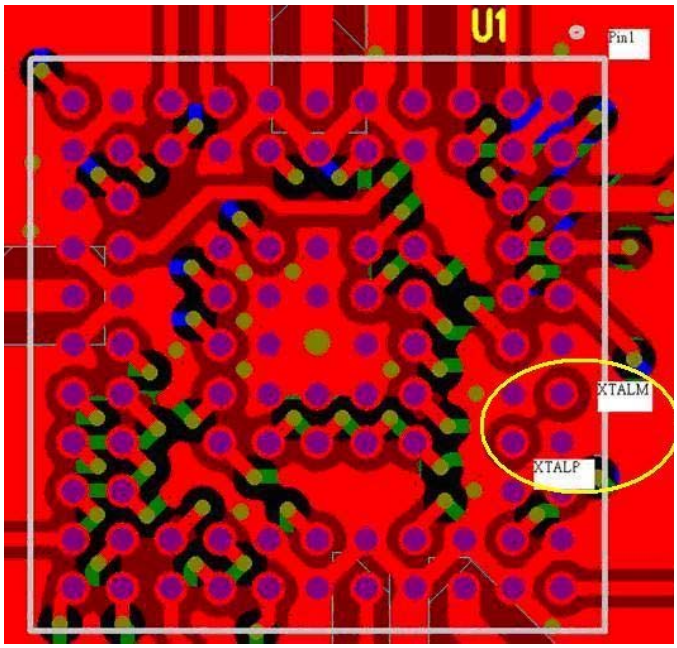
B/P= Bump Pad

10.2. Recommended Stencil Design

The bump pad size, it's solder mask opening and the relevant stencil Via diameter described in **Section 10.1** and **Section 10.2** shall be followed completely otherwise the module mounting yield rate couldn't be insured. The recommended stencil via diameter is 570um.

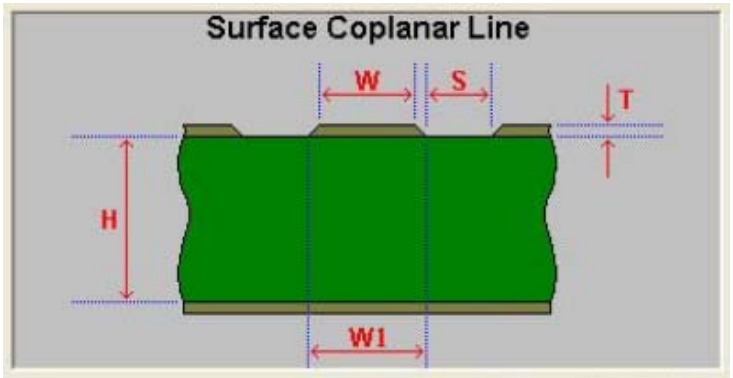
10.3. Recommended Trace Layout

- **XTALP and XTALM**
  - Having ground plane in Layer2 under the two floating pins to avoid unwanted central frequency offset



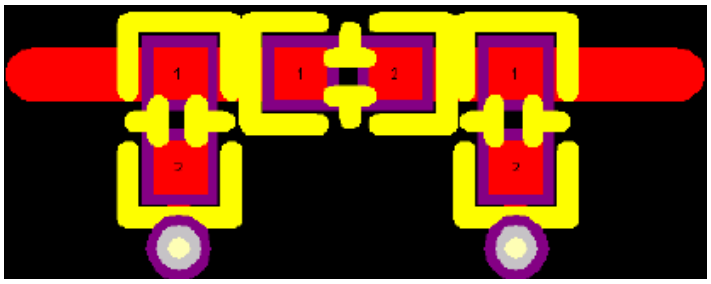
- **Digital Signals Layout**
  - SDIO signals traces (CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible.
  - SDIO Clock, Audio Clock (PCM_AUD_CLK), FM I2S Clock (FM_I2S_CLK), FM I2C Clock (FM_SCL), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.

- **RF Trace & Antenna**
  - 50 ohm trace impedance match on the trace to the antenna.
  - Recommended 50ohm trace design for PCB layout



Height Between L1 and L2 **(H):**	10.0 mil
Trace **(W):**	14.3 mil
(W1):	14.3 mil
Thickness **(T):**	2.1 mil
Separation **(S):**	10.0 mil
Dielectric **(Er):**	4.3

- Move all the high-speed traces and components far away from the antenna.
- Check ANT vendor for the layout guideline and clearance.
- Matching circuit layout should be as following figure.

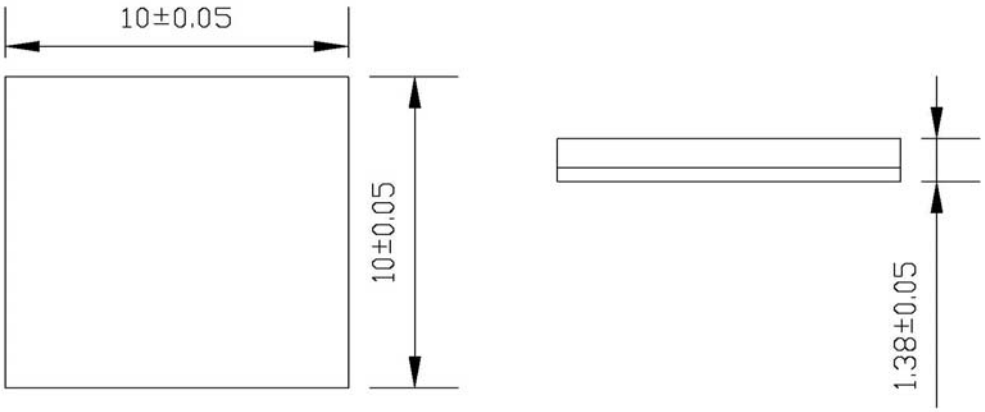


- **Power Trace**
  - Power trace for VBAT should be 40mil wide. 1.8V trace should be 18mil wide.
- **Ground**
  - Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation as following figure.
  - Have a complete Ground pour in layer 2 for thermal dissipation.
  - Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
  - Move GND vias close to the pad.

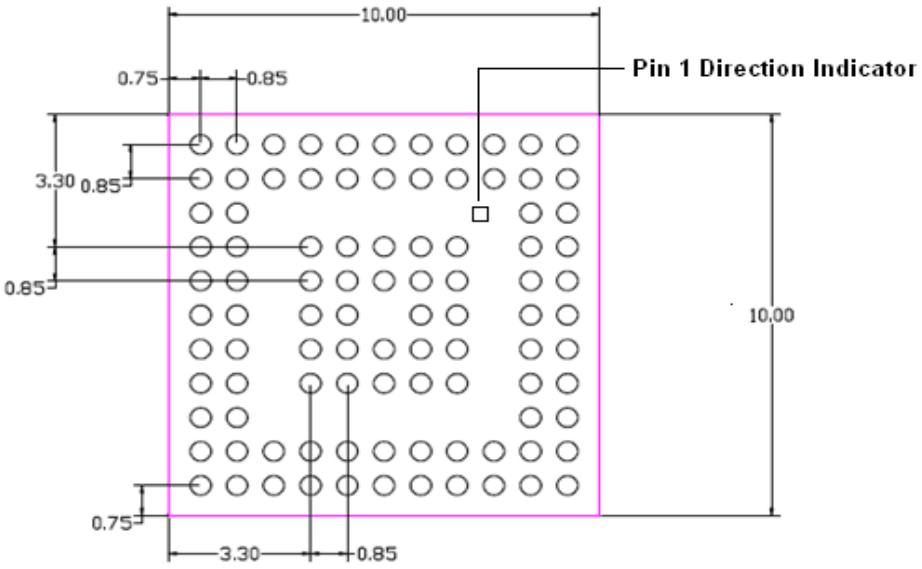
- **Slow Clock**
  - FM RF module uses the 32-kHz clock, it is extremely important that the slow-clock trace not be routed next to any digital signals.
  - The slow clock trace should not be routed above or below digital signals on other layers.

11. PACKAGE INFORMATION

11.1. Module Mechanical Outline



Top and Side View



unit: mm

Bottom View

- **Pin array = 11x11**
- **Pin number = 96 pins**
- **Bump pitch = 0.85mm**
- **Bump diameter = 0.5mm**
- **Dimension tolerance±0.05mm**

11.2. Ordering Information

Part number:	WG7311-0A	Normal temperature device
Part number:	WG7311-EA	Extended temperature device

11.3. Package Marking

Part Number : WG7311-**X**A

X = 0: WG7311-0A

X = E: WG7311-EA

Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2008=08

WW = Week (01~53)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = Reserve for internal use

12. SMT and Baking Recommendation

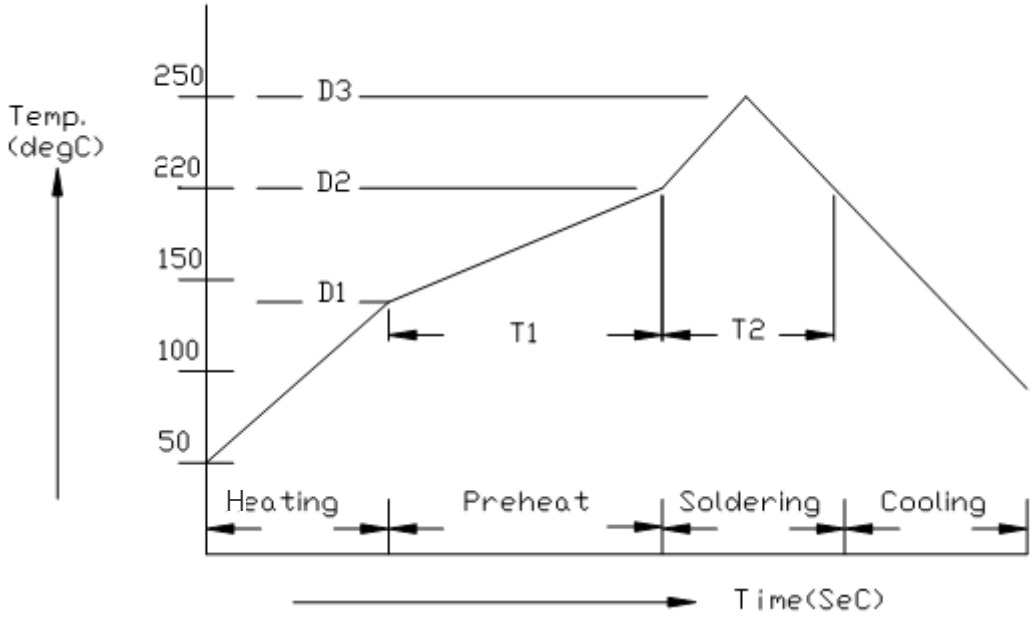
12.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs at 125 °C.

12.2. SMT Recommendation

- **Recommended Reflow profile：**



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

- **Stencil thickness**： 0.1~ 0.15 mm (Recommended)
- **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

13. History Change

Revision	Date	Description
R 0.1	2011/5/20	Release 0.1
R 0.2	2011/9/16	Add Extended temperature device
R 0.3	2011/9/22	Add Power Consumption