1. Description

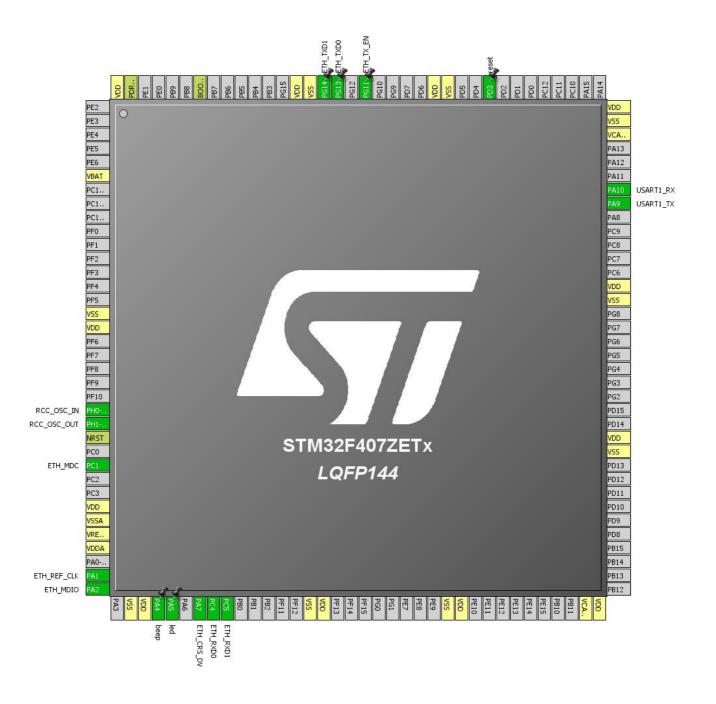
1.1. Project

Project Name	F407_temp
Board Name	F407_temp
Generated with:	STM32CubeMX 4.21.0
Date	09/27/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



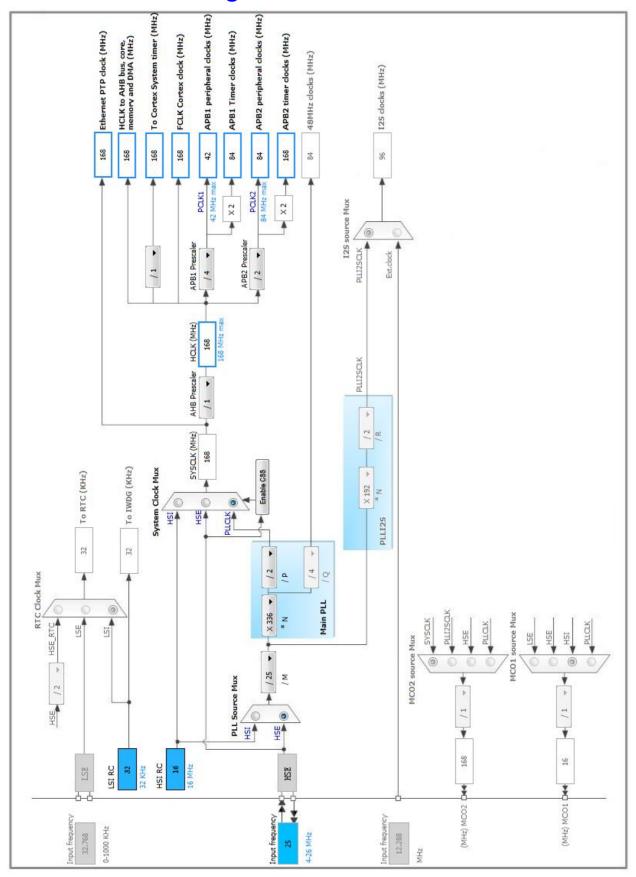
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Output	beep
41	PA5 *	I/O	GPIO_Output	led
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
117	PD3 *	I/O	GPIO_Output	reset

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	
128	PG13	I/O	ETH_TXD0	
129	PG14	I/O	ETH_TXD1	
130	VSS	Power		
131	VDD	Power		
138	воото	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ETH

Mode: RMII

5.1.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation Enabled

General: Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

PHY Address 1

Ethernet Basic Configuration:

Rx Mode Polling Mode
TX IP Header Checksum Computation By hardware

5.1.2. Advanced Parameters:

External PHY Configuration:

PHY LAN8742A_PHY_ADDRESS

PHY Address Value 1

PHY Reset delay these values are based on a 1 ms

Systick interrupt

0x000000FF *

PHY Configuration delay

PHY Read TimeOut

Ox0000FFF *

PHY Write TimeOut

Ox0000FFF *

Common: External PHY Configuration:

Transceiver Basic Control Register 0x00 *

Transceiver Basic Status Register 0x01 *

PHY Reset 0x8000 *

Select loop-back mode 0x4000 *

Set the full-duplex mode at 100 Mb/s 0x2100 *

Set the half-duplex mode at 100 Mb/s 0x2000 *

Set the full-duplex mode at 10 Mb/s **0x0100** *

Set the half-duplex mode at 10 Mb/s 0x0000 *

Enable auto-negotiation function 0x1000 *

Restart auto-negotiation function

Select the power down mode

Isolate PHY from MII

Auto-Negotiation process completed

Valid link established

Jabber condition detected

0x020 *

0x0004 *

Extended: External PHY Configuration:

PHY special control/status register Offset

Ox10 *

PHY Speed mask

Ox0002 *

PHY Duplex mask

Ox0004 *

PHY Interrupt Source Flag register Offset

Ox000B *

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

5.3. USART1

Mode: Asynchronous

5.3.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

^{*} User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	Very High	
GPIO	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	beep
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	led
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	reset

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

^{*} User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407ZETx
Datasheet	022152 Rev7

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F407_temp
Project Folder	E:\Project\Practise\F407\F407_temp
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	