

**a-Si TFT LCD Single Chip Driver
320(RGB) x 480 Resolution, 16.7M-color
With Internal GRAM**

**Specification
Preliminary**

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1. Introduction

The ILI9488 is a 16.7M single-chip SoC driver for a-Si TFT liquid crystal display panels with a resolution of 320(RGB) x 480 dots. The ILI9488 is comprised of a 960-channel source driver, a 480-channel gate driver, 345,600 bytes GRAM for graphic data of 320 (RGB) x 480 dots, and power supply circuit.

The ILI9488 supports parallel DBI Type B 8-/9-/16-/18-/24-bit data bus interfaces and DBI Type C 3-/4-line serial peripheral interfaces (SPI) to input commands. The ILI9488 supports DPI (16-/18-/24-bit) data bus for video image display. For MIPI*-DSI* high-speed interface mode, the ILI9488 also provides one data lane and one clock lane that can support up to 500Mbps on MIPI-DSI link.

The ILI9488 can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The ILI9488 supports 8-colors display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

Notes:

- ◆ MIPI: Mobile Industry Processor Interface
- ◆ DSI: Display Serial Interface

2. Features

- ◆ Display resolution: 320 (RGB) (H) x 480 (V)
- ◆ Display color modes:
 - Full color modes:
 - 16.7M colors with dithering function (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
 - 262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)
 - Reduced color modes:
 - 65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)
 - 8 colors (3-bit data, R: 1-bit, G: 1-bit, B: 1-bit)
- ◆ Display module:
 - On-chip Frame Memory size 345,600 bytes, 320 (RGB) (H) x 480 (V) x 18 bits
 - Supports 960 source channel outputs
 - Supports up to a maximum of 480 gate lines
 - Supports 24-bits input image function
 - Supports column/1-/2-dot inversion
 - On-module DC VCOM control (-2 to 0V common electrode output voltage range)
 - Source/VCOM/Gate power supply voltage
 - DDVDH – GND = 4.5 to 6V
 - DDVDSL – GND = -6 to -4.5V
 - VCL – GND = -3 to -2V
 - DC VCOM – GND = -2 to 0V, a step = 16mV
 - VREG1OUT – GND = 3.625 to 5.5 V
 - VREG2OUT – GND = -5.5 to -3.625V
 - VGH – GND = 10 to 20V
 - VGL – GND = -15 to -5V
- ◆ Display Interface types:
 - MIPI-DBI (Display Bus Interface)
 - Type B (i-80 system), 8-/9-/16-/18-/24-bit bus
 - Type C (Serial data transfer interface, 3/4-line SPI)
 - MIPI-DPI (Display Pixel Interface)
 - Supports 24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)
 - Supports 18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)
 - Supports 16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)
 - MIPI-DSI (Display Serial Interface)
 - Supports one data lane/maximum speed 500Mbps
 - Supports DSI version 1.01
 - Supports D-PHY version 1.00
- ◆ Input power
 - Low operating power supplies
 - IOVCC = 1.65 to 3.3V (Interface I/O)
 - VCI = 2.5 to 3.3V (Analog)
 - OTP programming voltage (DDVDH) = 7V
- ◆ Power saving modes:
 - Deep-standby mode
 - Sleep mode

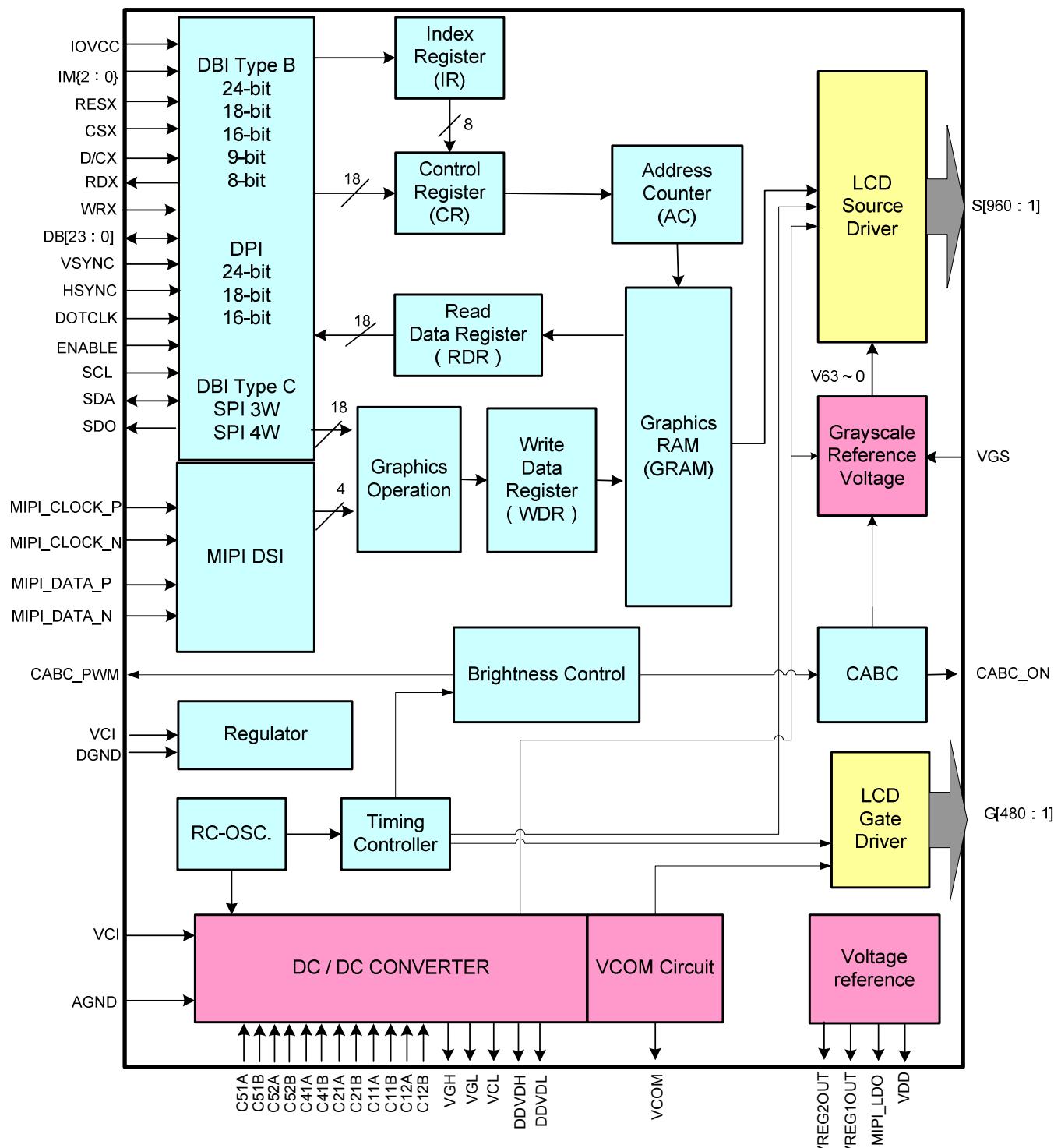
- ◆ Other on-chip functions/Miscellaneous
 - Supports partial display mode
 - Supports inversion mode
 - Oscillator for display clock generation
 - LVD function (GAS bit) prevents image sticking for abnormal power off
 - Supports DC VCOM driving
 - DC VCOM voltage generator and adjustment
 - OTP memory store initialization register settings (MATCDL, VRH1, VRH2 and BT)
 - MTP (provides 4 times OTP to store DC VCOM setting, ID1/ID2/ID3 setting)
 - Supports CABC function
 - Supports 3-Gamma DGC function
 - Supports dither function. (The dither function is only available in Bypass mode of DPI 24-bit and MIPI-DSI.)
 - Supports color enhancement function
- ◆ Operate temperature range: -40°C to 85°C

Notes:

- ◆ CABC: Content Adaptive Brightness Control
- ◆ DGC: Digital Gamma Correction
- ◆ LVD: Low Voltage Detection
- ◆ MTP: Multiple Time Programming
- ◆ OTP: One Time Programming

3. Device Overview

3.1. Block Diagram



3.2. Block Function Description

3.2.1. System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [2:0], as shown in **Table 1** below.

Table 1: MIPI-DBI Operating Mode

| MIPI-DBI Type B | | | | |
|-----------------|-----|-----|----------------------|-----------------|
| IM2 | IM1 | IM0 | Interface | Data Pin in Use |
| 0 | 0 | 0 | 24-bit bus (DB_EN=1) | DB [23:0] |
| 0 | 0 | 0 | 18-bit bus (DB_EN=0) | DB [17:0] |
| 0 | 0 | 1 | 9-bit bus | DB [9:0] |
| 0 | 1 | 0 | 16-bit bus | DB [15:0] |
| 0 | 1 | 1 | 8-bit bus | DB [7:0] |
| MIPI-DBI Type C | | | | |
| IM2 | IM1 | IM0 | Interface | Data Pin in Use |
| 1 | 0 | 1 | Option1 (3-line SPI) | SDA,SDO |
| 1 | 1 | 1 | Option3 (4-line SPI) | SDA,SDO |

Table 2: MIPI-DSI Operating Mode

| IM [2:0] | | | Interface | Data Pin in Use |
|----------|-----|-----|-----------|--|
| IM2 | IM1 | IM0 | | |
| 1 | 1 | 0 | MIPI-DSI | MIPI_DATA_P MIPI_DATA_N MIPI_CLOCK_P MIPI_CLOCK_N |

The ILI9488 supports MIPI DBI Type B (8-/9-/16-/18-/24-bits) that uses command method which has an 8-bit index register (IR) and an 8-bit control register (CR). The ILI9488 also has an 18-bit write-data register (WDR) and read-data register (RDR). The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in the internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9488 reads the first data from the internal GRAM. Valid data are read out after the ILI9488 performs the second read operation.

| MIPI-DBI Type B | | | Operation |
|-----------------|-----|-----|-----------------|
| D/CX | RDX | WRX | |
| "L" | "H" | ↑ | Write command |
| "H" | ↑ | "H" | Read parameter |
| "H" | "H" | ↑ | Write parameter |

3.2.2. Video Image Interface (TE-Signal and DPI)

When the DBI is selected, display data is written in synchronization with the TE signal which is generated from the internal clock to prevent flicker on the panel.

When the DPI is selected, externally supplied VSYNC, HSYNC, and DOTCLK signals will drive the chip. Display Data (DB [23:0]) is written in synchronization with those synchronous signals after Data Enable (ENABLE). This enables updating image data without flicker on the panel.

3.2.3. Address Counter (AC)

The Address Counter (AC) assigns an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. When writing data to the internal GRAM, the address in the AC is automatically increased/decreased by 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.2.4. Graphic RAM (GRAM)

The GRAM is used to store the display pattern data with a maximum of 345,600 bytes for 320 (RGB) x 480 display resolution.

3.2.5. Grayscale Voltage Generating Circuit

The Grayscale Voltage Generating Circuit generates a liquid crystal drive voltage that corresponds to the grayscale level setting in the Gamma correction register. The ILI9488 can display 262k colors at maximum.

3.2.6. Power Supply Circuit

The LCD drive power supply circuit generates VREG1OUT, VREG2OUT, VGH, VGL, and DC VCOM levels to drive the TFT LCD panel.

3.2.7. Timing Generating

The Timing Generator generates timing signals for internal circuits, such as the internal GRAM. Timing for display operation, such as RAM read operation, and timing for internal operations, such as RAM access by the MCU, is outputted separately so that they do not interfere with each other.

3.2.8. Oscillator

The ILI9488 includes an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.9. Panel Driver Circuit

The LCD Driver Circuit has a 960-channel source driver (S1~S960) and a maximum of 480 gate lines (G1~G480). When 320 (RGB) pixels of data are input, the display pattern data is latched. The voltage is output from the source driver according to the latched data.

3.2.10. MIPI-DSI Controller Circuit

The MIPI-DSI Controller Circuit consists of a D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer, and analog transceiver. The D-PHY controls communication with the analog block, and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams, and the PPU controls packet distribution and merging. The internal data/command buffer is used for temporary storage of incoming commands and display data.

3.3. Pin Descriptions

| Bus Interface Pins | | | | | |
|--------------------|-----|--|---|-----|--|
| Pin Name | I/O | Type | Descriptions | | |
| IM2, IM1, IM0 | I | Digital Input | Select the interface mode | | |
| | | | IM2 | IM1 | |
| | | | 0 | 0 | |
| | | | 0 | 0 | |
| | | | 0 | 1 | |
| | | | 0 | 1 | |
| | | | 1 | 0 | |
| | | | 1 | 1 | |
| | | | 1 | 1 | |
| | | Interface | | | |
| | | MIPI-DBI Type B 24-bit bus (DB_EN = 1) | | | |
| | | MIPI-DBI Type B 18-bit bus (DB_EN = 0) | | | |
| | | MIPI-DBI Type B 9-bit bus | | | |
| | | MIPI-DBI Type B 16-bit bus | | | |
| | | MIPI-DBI Type B 8-bit bus | | | |
| | | MIPI-DBI Type C Option 1 (3-line SPI) | | | |
| | | MIPI DSI | | | |
| | | MIPI-DBI Type C Option 3 (4-line SPI) | | | |
| RESX | I | Digital Input | Reset input signal Initialize the chip with a low input. Be sure to execute a power-on reset after supplying power. | | |
| CSX | I | Digital Input | DBI Type B: Chip select input signal Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC or DGND level when not in use. | | |
| D/CX | I | Digital Input | DBI Type B: Data/Command Selection pin Low: Command High: Parameter Fix to IOVCC or DGND level when not in use. | | |
| WRX/SCL | I | Digital Input | DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the serial interface Fix to IOVCC or DGND level when not in use. | | |
| RDX | I | Digital Input | DBI Type B: serve as a read signal Fix to IOVCC or DGND level when not in use. | | |
| SDA | I/O | Digital I/O | DBI Type C DIN/SDA: serial data input/output bi-direction pin Fix to IOVCC or DGND level when not in use. | | |
| SDO | O | Digital Output | DBI Type C SDO: Serial data output Leave the pin open when not in use. | | |
| TE | O | Digital Output | Serve as a TE (Tearing Effect) output signal Leave the pin open when not in use. | | |
| CABC_PWM | O | Digital Output | The PWM frequency output for LED driver control | | |

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| | | | <i>Leave the pin open when not in use.</i> | | | | | | | | | | | | | | | | | | |
|--|-----------------|----------------|---|----------------|-----------------|--|-----------|--|-----------|----------------------------|-----------|---------------------------|----------|---------------------------|----------|-----------------|-----------|-----------------|-----------|-----------------|-----------|
| MIPI_CLOCK_P | I | MIPI-DSI Input | DSI Positive polarity of low voltage differential clock signal <i>Leave the pin open when not in use.</i> | | | | | | | | | | | | | | | | | | |
| MIPI_CLOCK_N | I | MIPI-DSI Input | DSI Negative polarity of low voltage differential clock signal <i>Leave the pin open when not in use.</i> | | | | | | | | | | | | | | | | | | |
| MIPI_DATA_P | I/O | MIPI-DSI I/O | DSI Positive polarity of low voltage differential data signal <i>Leave the pin open when not in use.</i> | | | | | | | | | | | | | | | | | | |
| MIPI_DATA_N | I/O | MIPI-DSI I/O | DSI Negative polarity of low voltage differential data signal <i>Leave the pin open when not in use.</i> | | | | | | | | | | | | | | | | | | |
| DB [23:0] | I/O | Digital I/O | <table border="1"> <thead> <tr> <th>Interface Mode</th> <th>Data Pin in Use</th> </tr> </thead> <tbody> <tr> <td>MIPI-DBI Type B 24-bit bus (DB_EN = 1)</td> <td>DB [23:0]</td> </tr> <tr> <td>MIPI-DBI Type B 18-bit bus (DB_EN = 0)</td> <td>DB [17:0]</td> </tr> <tr> <td>MIPI-DBI Type B 16-bit bus</td> <td>DB [15:0]</td> </tr> <tr> <td>MIPI-DBI Type B 9-bit bus</td> <td>DB [8:0]</td> </tr> <tr> <td>MIPI-DBI Type B 8-bit bus</td> <td>DB [7:0]</td> </tr> <tr> <td>MIPI-DPI 24-bit</td> <td>DB [23:0]</td> </tr> <tr> <td>MIPI-DPI 18-bit</td> <td>DB [17:0]</td> </tr> <tr> <td>MIPI-DPI 16-bit</td> <td>DB [15:0]</td> </tr> </tbody> </table> <i>Fix to DGND level when not in use.</i> | Interface Mode | Data Pin in Use | MIPI-DBI Type B 24-bit bus (DB_EN = 1) | DB [23:0] | MIPI-DBI Type B 18-bit bus (DB_EN = 0) | DB [17:0] | MIPI-DBI Type B 16-bit bus | DB [15:0] | MIPI-DBI Type B 9-bit bus | DB [8:0] | MIPI-DBI Type B 8-bit bus | DB [7:0] | MIPI-DPI 24-bit | DB [23:0] | MIPI-DPI 18-bit | DB [17:0] | MIPI-DPI 16-bit | DB [15:0] |
| Interface Mode | Data Pin in Use | | | | | | | | | | | | | | | | | | | | |
| MIPI-DBI Type B 24-bit bus (DB_EN = 1) | DB [23:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DBI Type B 18-bit bus (DB_EN = 0) | DB [17:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DBI Type B 16-bit bus | DB [15:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DBI Type B 9-bit bus | DB [8:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DBI Type B 8-bit bus | DB [7:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DPI 24-bit | DB [23:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DPI 18-bit | DB [17:0] | | | | | | | | | | | | | | | | | | | | |
| MIPI-DPI 16-bit | DB [15:0] | | | | | | | | | | | | | | | | | | | | |
| VSYNC | I | Digital Input | DPI: Frame synchronizing signal <i>Fix to DGND level when not in use.</i> | | | | | | | | | | | | | | | | | | |
| H SYNC | I | Digital Input | DPI: Line synchronizing signal <i>Fix to DGND level when not in use.</i> | | | | | | | | | | | | | | | | | | |
| ENABLE | I | Digital Input | DPI: A data ENABLE input signal <i>Fix to DGND level when not in use.</i> | | | | | | | | | | | | | | | | | | |
| DOTCLK | I | Digital Input | DPI: Dot clock signal <i>Fix to IOVCC level when not in use.</i> | | | | | | | | | | | | | | | | | | |

| LCD Driving Signals | | | |
|---------------------|-----|---------------|--|
| Pin Name | I/O | Type | Descriptions |
| S960~S1 | O | Source Output | Source output voltage signals applied to the liquid crystal <i>Leave the pin open when not in use.</i> |

| | | | |
|---------|---|-------------|--|
| G480~G1 | O | Gate Output | Gate driver output pins VGH: the level selecting gate lines VGL: the level not selecting gate lines <i>Leave the pin open when not in use.</i> |
| VCOM | O | LCD Output | The common voltage in DC VCOM driving The voltage range is set between -2V to 0V. |
| VGS | I | Power GND | Reference level for grayscale generating circuit <i>Fix to GND level</i> |

| Charge-pump and Regulator Circuit | | | |
|--|-----|--------------------|--|
| Pin Name | I/O | Type | Descriptions |
| DDVDH | O | Charge Pump Output | Power supply for the source driver and VCOM driver. Input voltage from the set-up circuit (4.5 to 6V). <i>Connect to a stabilizing capacitor between DDVDH and GND.</i> |
| DDVDL | O | Charge Pump Output | Power supply for the source driver and VCOM driver. Input voltage from the set-up circuit (-6 to -4.5V). <i>Connect to a stabilizing capacitor between DDVDL and GND.</i> |
| VGH | O | Charge Pump Output | Power supply for the gate driver <i>Connect to a stabilizing capacitor between VGH and GND.</i> |
| VGL | O | Charge Pump Output | Power supply for the gate driver <i>Connect to a stabilizing capacitor between VGL and GND.</i> |
| VCL | O | Charge Pump Output | VCL = -VCI ~ -2 <i>Connect to a stabilizing capacitor between VCL and GND.</i> |
| MIPI_LDO | O | LDO Output | MIPI DSI core power pad <i>Connect to a stabilizing capacitor between MIPI_LDO and GND when operating in the MIPI DSI Interface.</i> <i>Leave the pin open when not in use.</i> |
| C52A, C52B C51A, C51B C41A, C41B C11A, C11B C12A, C12B | O | Analog Output | Capacitor connection pins for the step-up circuit 1 <i>Connect to a stabilizing capacitor between C51A and C51B.</i> <i>Connect to a stabilizing capacitor between C52A and C52B.</i> <i>Connect to a stabilizing capacitor between C41A and C41B.</i> <i>Connect to a stabilizing capacitor between C11A and C11B.</i> <i>Connect to a stabilizing capacitor between C12A and C12B.</i> |
| C21A, C21B | O | Analog Output | Capacitor connection pins for the step-up circuit 2. <i>Connect to a stabilizing capacitor between C21A and C21B.</i> |

| Power Pads | | | |
|------------|-----|------|--------------|
| Pin Name | I/O | Type | Descriptions |

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| | | | |
|-------------|---|--------------|---|
| VCI | P | Power Supply | A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V. <i>Connect to a stabilizing capacitor between VCI and GND.</i> |
| IOVCC | P | Power Supply | A supply voltage to the digital circuit. Connect to an external power supply of 1.65 ~ 3.3V. |
| VDD (VCORE) | O | Power Supply | Internal logic voltage output <i>Connect to a stabilizing capacitor between VDD and GND.</i> |
| DGND | P | Power GND | Ground for the internal logic: DGND = 0V <i>When using COG, connect to GND on the FPC to prevent noise.</i> |
| AGND | P | Power GND | AGND for the analog side: AGND = 0V <i>When using COG, connect to GND on the FPC to prevent noise.</i> |

| Test Pads | | | |
|-----------|-----|-----------|--|
| Pin Name | I/O | Type | Descriptions |
| DUMMY | - | - | Dummy pad <i>Leave the pin open when not in use.</i> |
| TS [2:0] | I | - | Test pins, these pins are internal weak pull low. <i>Leave the pin open when not in use.</i> |
| TESTP | I | Power GND | Test pins. <i>Fix to GND level</i> |

3.4. Pad Assignment

Chip Size: 22828um x 758um

Chip thickness : 280um (typ.)

Pad Location: Pad Center.

Coordinate Origin: Chip center location

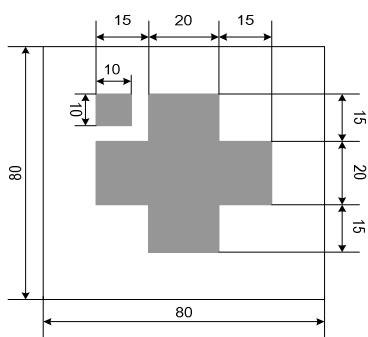
Au bump height: 9um (typ.)

Au Bump Size:

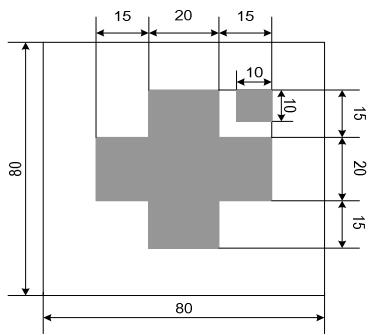
1. 15um x 100um
Gate: G1 ~ G480
Source: S1 ~ S960

2. 50um x 80um
Input Pads
Pad 1 to 320.

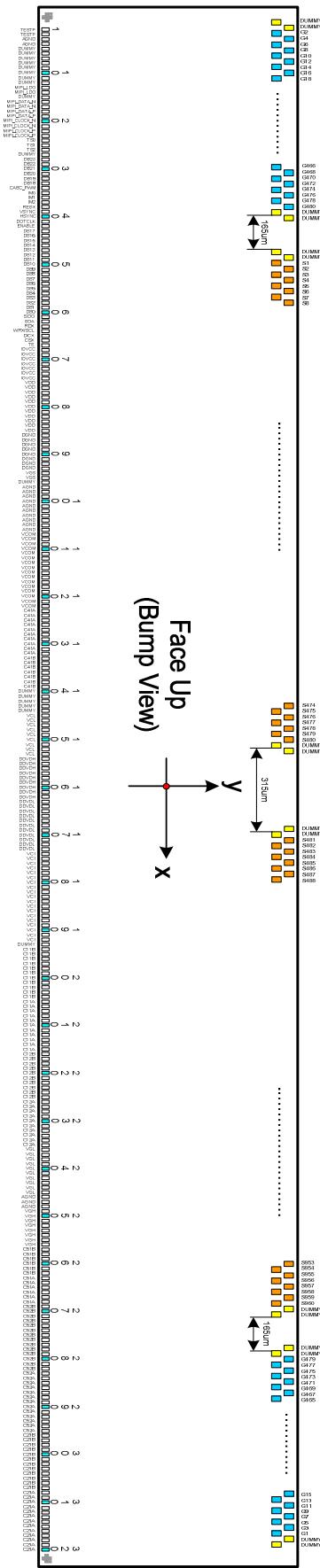
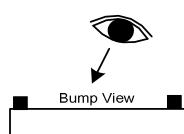
Alignment Marks



Alignment Mark: Left



Alignment Mark: Right



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3.5.Pad Coordination

| No. | Name | X | Y | No. | Name | X | Y | No. | Name | X | Y |
|-----|--------------|--------|------|-----|---------|-------|------|-----|-------|-------|------|
| 1 | TESTP | -11165 | -279 | 49 | DB11 | -7805 | -279 | 97 | AGND | -4445 | -279 |
| 2 | TESTP | -11095 | -279 | 50 | DB10 | -7735 | -279 | 98 | AGND | -4375 | -279 |
| 3 | AGND | -11025 | -279 | 51 | DB9 | -7665 | -279 | 99 | AGND | -4305 | -279 |
| 4 | AGND | -10955 | -279 | 52 | DB8 | -7595 | -279 | 100 | AGND | -4235 | -279 |
| 5 | DUMMY | -10885 | -279 | 53 | DB7 | -7525 | -279 | 101 | AGND | -4165 | -279 |
| 6 | DUMMY | -10815 | -279 | 54 | DB6 | -7455 | -279 | 102 | AGND | -4095 | -279 |
| 7 | DUMMY | -10745 | -279 | 55 | DB5 | -7385 | -279 | 103 | AGND | -4025 | -279 |
| 8 | DUMMY | -10675 | -279 | 56 | DB4 | -7315 | -279 | 104 | AGND | -3955 | -279 |
| 9 | DUMMY | -10605 | -279 | 57 | DB3 | -7245 | -279 | 105 | AGND | -3885 | -279 |
| 10 | DUMMY | -10535 | -279 | 58 | DB2 | -7175 | -279 | 106 | AGND | -3815 | -279 |
| 11 | DUMMY | -10465 | -279 | 59 | DB1 | -7105 | -279 | 107 | VCOM | -3745 | -279 |
| 12 | DUMMY | -10395 | -279 | 60 | DB0 | -7035 | -279 | 108 | VCOM | -3675 | -279 |
| 13 | MIPI_LDO | -10325 | -279 | 61 | SDO | -6965 | -279 | 109 | VCOM | -3605 | -279 |
| 14 | MIPI_LDO | -10255 | -279 | 62 | SDA | -6895 | -279 | 110 | VCOM | -3535 | -279 |
| 15 | DUMMY | -10185 | -279 | 63 | RDX | -6825 | -279 | 111 | VCOM | -3465 | -279 |
| 16 | MIPI_DATA_N | -10115 | -279 | 64 | WRX/SCL | -6755 | -279 | 112 | VCOM | -3395 | -279 |
| 17 | MIPI_DATA_N | -10045 | -279 | 65 | D/CX | -6685 | -279 | 113 | VCOM | -3325 | -279 |
| 18 | MIPI_DATA_P | -9975 | -279 | 66 | CSX | -6615 | -279 | 114 | VCOM | -3255 | -279 |
| 19 | MIPI_DATA_P | -9905 | -279 | 67 | TE | -6545 | -279 | 115 | VCOM | -3185 | -279 |
| 20 | MIPI_CLOCK_N | -9835 | -279 | 68 | IOVCC | -6475 | -279 | 116 | VCOM | -3115 | -279 |
| 21 | MIPI_CLOCK_N | -9765 | -279 | 69 | IOVCC | -6405 | -279 | 117 | VCOM | -3045 | -279 |
| 22 | MIPI_CLOCK_P | -9695 | -279 | 70 | IOVCC | -6335 | -279 | 118 | VCOM | -2975 | -279 |
| 23 | MIPI_CLOCK_P | -9625 | -279 | 71 | IOVCC | -6265 | -279 | 119 | VCOM | -2905 | -279 |
| 24 | TS0 | -9555 | -279 | 72 | IOVCC | -6195 | -279 | 120 | VCOM | -2835 | -279 |
| 25 | TS1 | -9485 | -279 | 73 | IOVCC | -6125 | -279 | 121 | VCOM | -2765 | -279 |
| 26 | TS2 | -9415 | -279 | 74 | IOVCC | -6055 | -279 | 122 | VCOM | -2695 | -279 |
| 27 | DUMMY | -9345 | -279 | 75 | VDD | -5985 | -279 | 123 | C41A | -2625 | -279 |
| 28 | DB23 | -9275 | -279 | 76 | VDD | -5915 | -279 | 124 | C41A | -2555 | -279 |
| 29 | DB22 | -9205 | -279 | 77 | VDD | -5845 | -279 | 125 | C41A | -2485 | -279 |
| 30 | DB21 | -9135 | -279 | 78 | VDD | -5775 | -279 | 126 | C41A | -2415 | -279 |
| 31 | DB20 | -9065 | -279 | 79 | VDD | -5705 | -279 | 127 | C41A | -2345 | -279 |
| 32 | DB19 | -8995 | -279 | 80 | VDD | -5635 | -279 | 128 | C41A | -2275 | -279 |
| 33 | DB18 | -8925 | -279 | 81 | VDD | -5565 | -279 | 129 | C41A | -2205 | -279 |
| 34 | CABC_PWM | -8855 | -279 | 82 | VDD | -5495 | -279 | 130 | C41A | -2135 | -279 |
| 35 | IM0 | -8785 | -279 | 83 | VDD | -5425 | -279 | 131 | C41A | -2065 | -279 |
| 36 | IM1 | -8715 | -279 | 84 | VDD | -5355 | -279 | 132 | C41A | -1995 | -279 |
| 37 | IM2 | -8645 | -279 | 85 | VDD | -5285 | -279 | 133 | C41B | -1925 | -279 |
| 38 | RESX | -8575 | -279 | 86 | DGND | -5215 | -279 | 134 | C41B | -1855 | -279 |
| 39 | VSYNC | -8505 | -279 | 87 | DGND | -5145 | -279 | 135 | C41B | -1785 | -279 |
| 40 | HSYNC | -8435 | -279 | 88 | DGND | -5075 | -279 | 136 | C41B | -1715 | -279 |
| 41 | DOTCLK | -8365 | -279 | 89 | DGND | -5005 | -279 | 137 | C41B | -1645 | -279 |
| 42 | ENABLE | -8295 | -279 | 90 | DGND | -4935 | -279 | 138 | C41B | -1575 | -279 |
| 43 | DB17 | -8225 | -279 | 91 | DGND | -4865 | -279 | 139 | C41B | -1505 | -279 |
| 44 | DB16 | -8155 | -279 | 92 | DGND | -4795 | -279 | 140 | DUMMY | -1435 | -279 |
| 45 | DB15 | -8085 | -279 | 93 | DGND | -4725 | -279 | 141 | DUMMY | -1365 | -279 |
| 46 | DB14 | -8015 | -279 | 94 | VGS | -4655 | -279 | 142 | DUMMY | -1295 | -279 |
| 47 | DB13 | -7945 | -279 | 95 | VGS | -4585 | -279 | 143 | DUMMY | -1225 | -279 |
| 48 | DB12 | -7875 | -279 | 96 | DUMMY | -4515 | -279 | 144 | DUMMY | -1155 | -279 |

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|-----|-------|-------|------|-----|------|------|------|-----|------|------|------|-----|-------|-------|------|
| 145 | VCL | -1085 | -279 | 195 | C11B | 2415 | -279 | 245 | VGL | 5915 | -279 | 295 | C52A | 9415 | -279 |
| 146 | VCL | -1015 | -279 | 196 | C11B | 2485 | -279 | 246 | AGND | 5985 | -279 | 296 | C21B | 9485 | -279 |
| 147 | VCL | -945 | -279 | 197 | C11B | 2555 | -279 | 247 | AGND | 6055 | -279 | 297 | C21B | 9555 | -279 |
| 148 | VCL | -875 | -279 | 198 | C11B | 2625 | -279 | 248 | AGND | 6125 | -279 | 298 | C21B | 9625 | -279 |
| 149 | VCL | -805 | -279 | 199 | C11B | 2695 | -279 | 249 | VGH | 6195 | -279 | 299 | C21B | 9695 | -279 |
| 150 | VCL | -735 | -279 | 200 | C11B | 2765 | -279 | 250 | VGH | 6265 | -279 | 300 | C21B | 9765 | -279 |
| 151 | VCL | -665 | -279 | 201 | C11B | 2835 | -279 | 251 | VGH | 6335 | -279 | 301 | C21B | 9835 | -279 |
| 152 | VCL | -595 | -279 | 202 | C11B | 2905 | -279 | 252 | VGH | 6405 | -279 | 302 | C21B | 9905 | -279 |
| 153 | VCL | -525 | -279 | 203 | C11B | 2975 | -279 | 253 | VGH | 6475 | -279 | 303 | C21B | 9975 | -279 |
| 154 | DDVDH | -455 | -279 | 204 | C11B | 3045 | -279 | 254 | VGH | 6545 | -279 | 304 | C21B | 10045 | -279 |
| 155 | DDVDH | -385 | -279 | 205 | C11A | 3115 | -279 | 255 | VGH | 6615 | -279 | 305 | C21B | 10115 | -279 |
| 156 | DDVDH | -315 | -279 | 206 | C11A | 3185 | -279 | 256 | VGH | 6685 | -279 | 306 | C21B | 10185 | -279 |
| 157 | DDVDH | -245 | -279 | 207 | C11A | 3255 | -279 | 257 | C51B | 6755 | -279 | 307 | C21B | 10255 | -279 |
| 158 | DDVDH | -175 | -279 | 208 | C11A | 3325 | -279 | 258 | C51B | 6825 | -279 | 308 | C21A | 10325 | -279 |
| 159 | DDVDH | -105 | -279 | 209 | C11A | 3395 | -279 | 259 | C51B | 6895 | -279 | 309 | C21A | 10395 | -279 |
| 160 | DDVDH | -35 | -279 | 210 | C11A | 3465 | -279 | 260 | C51B | 6965 | -279 | 310 | C21A | 10465 | -279 |
| 161 | DDVDH | 35 | -279 | 211 | C11A | 3535 | -279 | 261 | C51B | 7035 | -279 | 311 | C21A | 10535 | -279 |
| 162 | DDVDH | 105 | -279 | 212 | C11A | 3605 | -279 | 262 | C51B | 7105 | -279 | 312 | C21A | 10605 | -279 |
| 163 | DDVDL | 175 | -279 | 213 | C11A | 3675 | -279 | 263 | C51A | 7175 | -279 | 313 | C21A | 10675 | -279 |
| 164 | DDVDL | 245 | -279 | 214 | C11A | 3745 | -279 | 264 | C51A | 7245 | -279 | 314 | C21A | 10745 | -279 |
| 165 | DDVDL | 315 | -279 | 215 | C11A | 3815 | -279 | 265 | C51A | 7315 | -279 | 315 | C21A | 10815 | -279 |
| 166 | DDVDL | 385 | -279 | 216 | C12B | 3885 | -279 | 266 | C51A | 7385 | -279 | 316 | C21A | 10885 | -279 |
| 167 | DDVDL | 455 | -279 | 217 | C12B | 3955 | -279 | 267 | C51A | 7455 | -279 | 317 | C21A | 10955 | -279 |
| 168 | DDVDL | 525 | -279 | 218 | C12B | 4025 | -279 | 268 | C51A | 7525 | -279 | 318 | C21A | 11025 | -279 |
| 169 | DDVDL | 595 | -279 | 219 | C12B | 4095 | -279 | 269 | C52B | 7595 | -279 | 319 | C21A | 11095 | -279 |
| 170 | DDVDL | 665 | -279 | 220 | C12B | 4165 | -279 | 270 | C52B | 7665 | -279 | 320 | C21A | 11165 | -279 |
| 171 | DDVDL | 735 | -279 | 221 | C12B | 4235 | -279 | 271 | C52B | 7735 | -279 | 321 | DUMMY | 11205 | 164 |
| 172 | DDVDL | 805 | -279 | 222 | C12B | 4305 | -279 | 272 | C52B | 7805 | -279 | 322 | DUMMY | 11190 | 289 |
| 173 | DDVDL | 875 | -279 | 223 | C12B | 4375 | -279 | 273 | C52B | 7875 | -279 | 323 | G1 | 11175 | 164 |
| 174 | VCI | 945 | -279 | 224 | C12B | 4445 | -279 | 274 | C52B | 7945 | -279 | 324 | G3 | 11160 | 289 |
| 175 | VCI | 1015 | -279 | 225 | C12B | 4515 | -279 | 275 | C52B | 8015 | -279 | 325 | G5 | 11145 | 164 |
| 176 | VCI | 1085 | -279 | 226 | C12A | 4585 | -279 | 276 | C52B | 8085 | -279 | 326 | G7 | 11130 | 289 |
| 177 | VCI | 1155 | -279 | 227 | C12A | 4655 | -279 | 277 | C52B | 8155 | -279 | 327 | G9 | 11115 | 164 |
| 178 | VCI | 1225 | -279 | 228 | C12A | 4725 | -279 | 278 | C52B | 8225 | -279 | 328 | G11 | 11100 | 289 |
| 179 | VCI | 1295 | -279 | 229 | C12A | 4795 | -279 | 279 | C52B | 8295 | -279 | 329 | G13 | 11085 | 164 |
| 180 | VCI | 1365 | -279 | 230 | C12A | 4865 | -279 | 280 | C52B | 8365 | -279 | 330 | G15 | 11070 | 289 |
| 181 | VCI | 1435 | -279 | 231 | C12A | 4935 | -279 | 281 | C52B | 8435 | -279 | 331 | G17 | 11055 | 164 |
| 182 | VCI | 1505 | -279 | 232 | C12A | 5005 | -279 | 282 | C52B | 8505 | -279 | 332 | G19 | 11040 | 289 |
| 183 | VCI | 1575 | -279 | 233 | C12A | 5075 | -279 | 283 | C52A | 8575 | -279 | 333 | G21 | 11025 | 164 |
| 184 | VCI | 1645 | -279 | 234 | C12A | 5145 | -279 | 284 | C52A | 8645 | -279 | 334 | G23 | 11010 | 289 |
| 185 | VCI | 1715 | -279 | 235 | C12A | 5215 | -279 | 285 | C52A | 8715 | -279 | 335 | G25 | 10995 | 164 |
| 186 | VCI | 1785 | -279 | 236 | VGL | 5285 | -279 | 286 | C52A | 8785 | -279 | 336 | G27 | 10980 | 289 |
| 187 | VCI | 1855 | -279 | 237 | VGL | 5355 | -279 | 287 | C52A | 8855 | -279 | 337 | G29 | 10965 | 164 |
| 188 | VCI | 1925 | -279 | 238 | VGL | 5425 | -279 | 288 | C52A | 8925 | -279 | 338 | G31 | 10950 | 289 |
| 189 | VCI | 1995 | -279 | 239 | VGL | 5495 | -279 | 289 | C52A | 8995 | -279 | 339 | G33 | 10935 | 164 |
| 190 | VCI | 2065 | -279 | 240 | VGL | 5565 | -279 | 290 | C52A | 9065 | -279 | 340 | G35 | 10920 | 289 |
| 191 | VCI | 2135 | -279 | 241 | VGL | 5635 | -279 | 291 | C52A | 9135 | -279 | 341 | G37 | 10905 | 164 |
| 192 | VCI | 2205 | -279 | 242 | VGL | 5705 | -279 | 292 | C52A | 9205 | -279 | 342 | G39 | 10890 | 289 |
| 193 | DUMMY | 2275 | -279 | 243 | VGL | 5775 | -279 | 293 | C52A | 9275 | -279 | 343 | G41 | 10875 | 164 |
| 194 | C11B | 2345 | -279 | 244 | VGL | 5845 | -279 | 294 | C52A | 9345 | -279 | 344 | G43 | 10860 | 289 |

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|-----|------|-------|-----|-----|------|-------|-----|-----|------|------|-----|-----|------|------|-----|
| 345 | G45 | 10845 | 164 | 395 | G145 | 10095 | 164 | 445 | G245 | 9345 | 164 | 495 | G345 | 8595 | 164 |
| 346 | G47 | 10830 | 289 | 396 | G147 | 10080 | 289 | 446 | G247 | 9330 | 289 | 496 | G347 | 8580 | 289 |
| 347 | G49 | 10815 | 164 | 397 | G149 | 10065 | 164 | 447 | G249 | 9315 | 164 | 497 | G349 | 8565 | 164 |
| 348 | G51 | 10800 | 289 | 398 | G151 | 10050 | 289 | 448 | G251 | 9300 | 289 | 498 | G351 | 8550 | 289 |
| 349 | G53 | 10785 | 164 | 399 | G153 | 10035 | 164 | 449 | G253 | 9285 | 164 | 499 | G353 | 8535 | 164 |
| 350 | G55 | 10770 | 289 | 400 | G155 | 10020 | 289 | 450 | G255 | 9270 | 289 | 500 | G355 | 8520 | 289 |
| 351 | G57 | 10755 | 164 | 401 | G157 | 10005 | 164 | 451 | G257 | 9255 | 164 | 501 | G357 | 8505 | 164 |
| 352 | G59 | 10740 | 289 | 402 | G159 | 9990 | 289 | 452 | G259 | 9240 | 289 | 502 | G359 | 8490 | 289 |
| 353 | G61 | 10725 | 164 | 403 | G161 | 9975 | 164 | 453 | G261 | 9225 | 164 | 503 | G361 | 8475 | 164 |
| 354 | G63 | 10710 | 289 | 404 | G163 | 9960 | 289 | 454 | G263 | 9210 | 289 | 504 | G363 | 8460 | 289 |
| 355 | G65 | 10695 | 164 | 405 | G165 | 9945 | 164 | 455 | G265 | 9195 | 164 | 505 | G365 | 8445 | 164 |
| 356 | G67 | 10680 | 289 | 406 | G167 | 9930 | 289 | 456 | G267 | 9180 | 289 | 506 | G367 | 8430 | 289 |
| 357 | G69 | 10665 | 164 | 407 | G169 | 9915 | 164 | 457 | G269 | 9165 | 164 | 507 | G369 | 8415 | 164 |
| 358 | G71 | 10650 | 289 | 408 | G171 | 9900 | 289 | 458 | G271 | 9150 | 289 | 508 | G371 | 8400 | 289 |
| 359 | G73 | 10635 | 164 | 409 | G173 | 9885 | 164 | 459 | G273 | 9135 | 164 | 509 | G373 | 8385 | 164 |
| 360 | G75 | 10620 | 289 | 410 | G175 | 9870 | 289 | 460 | G275 | 9120 | 289 | 510 | G375 | 8370 | 289 |
| 361 | G77 | 10605 | 164 | 411 | G177 | 9855 | 164 | 461 | G277 | 9105 | 164 | 511 | G377 | 8355 | 164 |
| 362 | G79 | 10590 | 289 | 412 | G179 | 9840 | 289 | 462 | G279 | 9090 | 289 | 512 | G379 | 8340 | 289 |
| 363 | G81 | 10575 | 164 | 413 | G181 | 9825 | 164 | 463 | G281 | 9075 | 164 | 513 | G381 | 8325 | 164 |
| 364 | G83 | 10560 | 289 | 414 | G183 | 9810 | 289 | 464 | G283 | 9060 | 289 | 514 | G383 | 8310 | 289 |
| 365 | G85 | 10545 | 164 | 415 | G185 | 9795 | 164 | 465 | G285 | 9045 | 164 | 515 | G385 | 8295 | 164 |
| 366 | G87 | 10530 | 289 | 416 | G187 | 9780 | 289 | 466 | G287 | 9030 | 289 | 516 | G387 | 8280 | 289 |
| 367 | G89 | 10515 | 164 | 417 | G189 | 9765 | 164 | 467 | G289 | 9015 | 164 | 517 | G389 | 8265 | 164 |
| 368 | G91 | 10500 | 289 | 418 | G191 | 9750 | 289 | 468 | G291 | 9000 | 289 | 518 | G391 | 8250 | 289 |
| 369 | G93 | 10485 | 164 | 419 | G193 | 9735 | 164 | 469 | G293 | 8985 | 164 | 519 | G393 | 8235 | 164 |
| 370 | G95 | 10470 | 289 | 420 | G195 | 9720 | 289 | 470 | G295 | 8970 | 289 | 520 | G395 | 8220 | 289 |
| 371 | G97 | 10455 | 164 | 421 | G197 | 9705 | 164 | 471 | G297 | 8955 | 164 | 521 | G397 | 8205 | 164 |
| 372 | G99 | 10440 | 289 | 422 | G199 | 9690 | 289 | 472 | G299 | 8940 | 289 | 522 | G399 | 8190 | 289 |
| 373 | G101 | 10425 | 164 | 423 | G201 | 9675 | 164 | 473 | G301 | 8925 | 164 | 523 | G401 | 8175 | 164 |
| 374 | G103 | 10410 | 289 | 424 | G203 | 9660 | 289 | 474 | G303 | 8910 | 289 | 524 | G403 | 8160 | 289 |
| 375 | G105 | 10395 | 164 | 425 | G205 | 9645 | 164 | 475 | G305 | 8895 | 164 | 525 | G405 | 8145 | 164 |
| 376 | G107 | 10380 | 289 | 426 | G207 | 9630 | 289 | 476 | G307 | 8880 | 289 | 526 | G407 | 8130 | 289 |
| 377 | G109 | 10365 | 164 | 427 | G209 | 9615 | 164 | 477 | G309 | 8865 | 164 | 527 | G409 | 8115 | 164 |
| 378 | G111 | 10350 | 289 | 428 | G211 | 9600 | 289 | 478 | G311 | 8850 | 289 | 528 | G411 | 8100 | 289 |
| 379 | G113 | 10335 | 164 | 429 | G213 | 9585 | 164 | 479 | G313 | 8835 | 164 | 529 | G413 | 8085 | 164 |
| 380 | G115 | 10320 | 289 | 430 | G215 | 9570 | 289 | 480 | G315 | 8820 | 289 | 530 | G415 | 8070 | 289 |
| 381 | G117 | 10305 | 164 | 431 | G217 | 9555 | 164 | 481 | G317 | 8805 | 164 | 531 | G417 | 8055 | 164 |
| 382 | G119 | 10290 | 289 | 432 | G219 | 9540 | 289 | 482 | G319 | 8790 | 289 | 532 | G419 | 8040 | 289 |
| 383 | G121 | 10275 | 164 | 433 | G221 | 9525 | 164 | 483 | G321 | 8775 | 164 | 533 | G421 | 8025 | 164 |
| 384 | G123 | 10260 | 289 | 434 | G223 | 9510 | 289 | 484 | G323 | 8760 | 289 | 534 | G423 | 8010 | 289 |
| 385 | G125 | 10245 | 164 | 435 | G225 | 9495 | 164 | 485 | G325 | 8745 | 164 | 535 | G425 | 7995 | 164 |
| 386 | G127 | 10230 | 289 | 436 | G227 | 9480 | 289 | 486 | G327 | 8730 | 289 | 536 | G427 | 7980 | 289 |
| 387 | G129 | 10215 | 164 | 437 | G229 | 9465 | 164 | 487 | G329 | 8715 | 164 | 537 | G429 | 7965 | 164 |
| 388 | G131 | 10200 | 289 | 438 | G231 | 9450 | 289 | 488 | G331 | 8700 | 289 | 538 | G431 | 7950 | 289 |
| 389 | G133 | 10185 | 164 | 439 | G233 | 9435 | 164 | 489 | G333 | 8685 | 164 | 539 | G433 | 7935 | 164 |
| 390 | G135 | 10170 | 289 | 440 | G235 | 9420 | 289 | 490 | G335 | 8670 | 289 | 540 | G435 | 7920 | 289 |
| 391 | G137 | 10155 | 164 | 441 | G237 | 9405 | 164 | 491 | G337 | 8655 | 164 | 541 | G437 | 7905 | 164 |
| 392 | G139 | 10140 | 289 | 442 | G239 | 9390 | 289 | 492 | G339 | 8640 | 289 | 542 | G439 | 7890 | 289 |
| 393 | G141 | 10125 | 164 | 443 | G241 | 9375 | 164 | 493 | G341 | 8625 | 164 | 543 | G441 | 7875 | 164 |
| 394 | G143 | 10110 | 289 | 444 | G243 | 9360 | 289 | 494 | G343 | 8610 | 289 | 544 | G443 | 7860 | 289 |

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|-----|-------|------|-----|-----|------|------|-----|-----|------|------|-----|-----|------|------|-----|
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| 551 | G457 | 7755 | 164 | 601 | S926 | 6855 | 164 | 651 | S876 | 6105 | 164 | 701 | S826 | 5355 | 164 |
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| 553 | G461 | 7725 | 164 | 603 | S924 | 6825 | 164 | 653 | S874 | 6075 | 164 | 703 | S824 | 5325 | 164 |
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| 560 | G475 | 7620 | 289 | 610 | S917 | 6720 | 289 | 660 | S867 | 5970 | 289 | 710 | S817 | 5220 | 289 |
| 561 | G477 | 7605 | 164 | 611 | S916 | 6705 | 164 | 661 | S866 | 5955 | 164 | 711 | S816 | 5205 | 164 |
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| 564 | DUMMY | 7560 | 289 | 614 | S913 | 6660 | 289 | 664 | S863 | 5910 | 289 | 714 | S813 | 5160 | 289 |
| 565 | DUMMY | 7395 | 164 | 615 | S912 | 6645 | 164 | 665 | S862 | 5895 | 164 | 715 | S812 | 5145 | 164 |
| 566 | DUMMY | 7380 | 289 | 616 | S911 | 6630 | 289 | 666 | S861 | 5880 | 289 | 716 | S811 | 5130 | 289 |
| 567 | S960 | 7365 | 164 | 617 | S910 | 6615 | 164 | 667 | S860 | 5865 | 164 | 717 | S810 | 5115 | 164 |
| 568 | S959 | 7350 | 289 | 618 | S909 | 6600 | 289 | 668 | S859 | 5850 | 289 | 718 | S809 | 5100 | 289 |
| 569 | S958 | 7335 | 164 | 619 | S908 | 6585 | 164 | 669 | S858 | 5835 | 164 | 719 | S808 | 5085 | 164 |
| 570 | S957 | 7320 | 289 | 620 | S907 | 6570 | 289 | 670 | S857 | 5820 | 289 | 720 | S807 | 5070 | 289 |
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| 574 | S953 | 7260 | 289 | 624 | S903 | 6510 | 289 | 674 | S853 | 5760 | 289 | 724 | S803 | 5010 | 289 |
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| 576 | S951 | 7230 | 289 | 626 | S901 | 6480 | 289 | 676 | S851 | 5730 | 289 | 726 | S801 | 4980 | 289 |
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| 756 | S771 | 4530 | 289 | 806 | S721 | 3780 | 289 | 856 | S671 | 3030 | 289 | 906 | S621 | 2280 | 289 |
| 757 | S770 | 4515 | 164 | 807 | S720 | 3765 | 164 | 857 | S670 | 3015 | 164 | 907 | S620 | 2265 | 164 |
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| 1155 | S376 | -1740 | 289 | 1205 | S326 | -2490 | 289 | 1255 | S276 | -3240 | 289 | 1305 | S226 | -3990 | 289 |
| 1156 | S375 | -1755 | 164 | 1206 | S325 | -2505 | 164 | 1256 | S275 | -3255 | 164 | 1306 | S225 | -4005 | 164 |
| 1157 | S374 | -1770 | 289 | 1207 | S324 | -2520 | 289 | 1257 | S274 | -3270 | 289 | 1307 | S224 | -4020 | 289 |
| 1158 | S373 | -1785 | 164 | 1208 | S323 | -2535 | 164 | 1258 | S273 | -3285 | 164 | 1308 | S223 | -4035 | 164 |
| 1159 | S372 | -1800 | 289 | 1209 | S322 | -2550 | 289 | 1259 | S272 | -3300 | 289 | 1309 | S222 | -4050 | 289 |
| 1160 | S371 | -1815 | 164 | 1210 | S321 | -2565 | 164 | 1260 | S271 | -3315 | 164 | 1310 | S221 | -4065 | 164 |
| 1161 | S370 | -1830 | 289 | 1211 | S320 | -2580 | 289 | 1261 | S270 | -3330 | 289 | 1311 | S220 | -4080 | 289 |
| 1162 | S369 | -1845 | 164 | 1212 | S319 | -2595 | 164 | 1262 | S269 | -3345 | 164 | 1312 | S219 | -4095 | 164 |
| 1163 | S368 | -1860 | 289 | 1213 | S318 | -2610 | 289 | 1263 | S268 | -3360 | 289 | 1313 | S218 | -4110 | 289 |
| 1164 | S367 | -1875 | 164 | 1214 | S317 | -2625 | 164 | 1264 | S267 | -3375 | 164 | 1314 | S217 | -4125 | 164 |
| 1165 | S366 | -1890 | 289 | 1215 | S316 | -2640 | 289 | 1265 | S266 | -3390 | 289 | 1315 | S216 | -4140 | 289 |
| 1166 | S365 | -1905 | 164 | 1216 | S315 | -2655 | 164 | 1266 | S265 | -3405 | 164 | 1316 | S215 | -4155 | 164 |
| 1167 | S364 | -1920 | 289 | 1217 | S314 | -2670 | 289 | 1267 | S264 | -3420 | 289 | 1317 | S214 | -4170 | 289 |
| 1168 | S363 | -1935 | 164 | 1218 | S313 | -2685 | 164 | 1268 | S263 | -3435 | 164 | 1318 | S213 | -4185 | 164 |
| 1169 | S362 | -1950 | 289 | 1219 | S312 | -2700 | 289 | 1269 | S262 | -3450 | 289 | 1319 | S212 | -4200 | 289 |
| 1170 | S361 | -1965 | 164 | 1220 | S311 | -2715 | 164 | 1270 | S261 | -3465 | 164 | 1320 | S211 | -4215 | 164 |
| 1171 | S360 | -1980 | 289 | 1221 | S310 | -2730 | 289 | 1271 | S260 | -3480 | 289 | 1321 | S210 | -4230 | 289 |
| 1172 | S359 | -1995 | 164 | 1222 | S309 | -2745 | 164 | 1272 | S259 | -3495 | 164 | 1322 | S209 | -4245 | 164 |
| 1173 | S358 | -2010 | 289 | 1223 | S308 | -2760 | 289 | 1273 | S258 | -3510 | 289 | 1323 | S208 | -4260 | 289 |
| 1174 | S357 | -2025 | 164 | 1224 | S307 | -2775 | 164 | 1274 | S257 | -3525 | 164 | 1324 | S207 | -4275 | 164 |
| 1175 | S356 | -2040 | 289 | 1225 | S306 | -2790 | 289 | 1275 | S256 | -3540 | 289 | 1325 | S206 | -4290 | 289 |
| 1176 | S355 | -2055 | 164 | 1226 | S305 | -2805 | 164 | 1276 | S255 | -3555 | 164 | 1326 | S205 | -4305 | 164 |
| 1177 | S354 | -2070 | 289 | 1227 | S304 | -2820 | 289 | 1277 | S254 | -3570 | 289 | 1327 | S204 | -4320 | 289 |
| 1178 | S353 | -2085 | 164 | 1228 | S303 | -2835 | 164 | 1278 | S253 | -3585 | 164 | 1328 | S203 | -4335 | 164 |
| 1179 | S352 | -2100 | 289 | 1229 | S302 | -2850 | 289 | 1279 | S252 | -3600 | 289 | 1329 | S202 | -4350 | 289 |
| 1180 | S351 | -2115 | 164 | 1230 | S301 | -2865 | 164 | 1280 | S251 | -3615 | 164 | 1330 | S201 | -4365 | 164 |
| 1181 | S350 | -2130 | 289 | 1231 | S300 | -2880 | 289 | 1281 | S250 | -3630 | 289 | 1331 | S200 | -4380 | 289 |
| 1182 | S349 | -2145 | 164 | 1232 | S299 | -2895 | 164 | 1282 | S249 | -3645 | 164 | 1332 | S199 | -4395 | 164 |
| 1183 | S348 | -2160 | 289 | 1233 | S298 | -2910 | 289 | 1283 | S248 | -3660 | 289 | 1333 | S198 | -4410 | 289 |
| 1184 | S347 | -2175 | 164 | 1234 | S297 | -2925 | 164 | 1284 | S247 | -3675 | 164 | 1334 | S197 | -4425 | 164 |
| 1185 | S346 | -2190 | 289 | 1235 | S296 | -2940 | 289 | 1285 | S246 | -3690 | 289 | 1335 | S196 | -4440 | 289 |
| 1186 | S345 | -2205 | 164 | 1236 | S295 | -2955 | 164 | 1286 | S245 | -3705 | 164 | 1336 | S195 | -4455 | 164 |
| 1187 | S344 | -2220 | 289 | 1237 | S294 | -2970 | 289 | 1287 | S244 | -3720 | 289 | 1337 | S194 | -4470 | 289 |
| 1188 | S343 | -2235 | 164 | 1238 | S293 | -2985 | 164 | 1288 | S243 | -3735 | 164 | 1338 | S193 | -4485 | 164 |
| 1189 | S342 | -2250 | 289 | 1239 | S292 | -3000 | 289 | 1289 | S242 | -3750 | 289 | 1339 | S192 | -4500 | 289 |
| 1190 | S341 | -2265 | 164 | 1240 | S291 | -3015 | 164 | 1290 | S241 | -3765 | 164 | 1340 | S191 | -4515 | 164 |
| 1191 | S340 | -2280 | 289 | 1241 | S290 | -3030 | 289 | 1291 | S240 | -3780 | 289 | 1341 | S190 | -4530 | 289 |
| 1192 | S339 | -2295 | 164 | 1242 | S289 | -3045 | 164 | 1292 | S239 | -3795 | 164 | 1342 | S189 | -4545 | 164 |
| 1193 | S338 | -2310 | 289 | 1243 | S288 | -3060 | 289 | 1293 | S238 | -3810 | 289 | 1343 | S188 | -4560 | 289 |
| 1194 | S337 | -2325 | 164 | 1244 | S287 | -3075 | 164 | 1294 | S237 | -3825 | 164 | 1344 | S187 | -4575 | 164 |

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|------|------|-------|-----|------|------|-------|-----|------|------|-------|-----|------|-------|-------|-----|
| 1345 | S186 | -4590 | 289 | 1395 | S136 | -5340 | 289 | 1445 | S86 | -6090 | 289 | 1495 | S36 | -6840 | 289 |
| 1346 | S185 | -4605 | 164 | 1396 | S135 | -5355 | 164 | 1446 | S85 | -6105 | 164 | 1496 | S35 | -6855 | 164 |
| 1347 | S184 | -4620 | 289 | 1397 | S134 | -5370 | 289 | 1447 | S84 | -6120 | 289 | 1497 | S34 | -6870 | 289 |
| 1348 | S183 | -4635 | 164 | 1398 | S133 | -5385 | 164 | 1448 | S83 | -6135 | 164 | 1498 | S33 | -6885 | 164 |
| 1349 | S182 | -4650 | 289 | 1399 | S132 | -5400 | 289 | 1449 | S82 | -6150 | 289 | 1499 | S32 | -6900 | 289 |
| 1350 | S181 | -4665 | 164 | 1400 | S131 | -5415 | 164 | 1450 | S81 | -6165 | 164 | 1500 | S31 | -6915 | 164 |
| 1351 | S180 | -4680 | 289 | 1401 | S130 | -5430 | 289 | 1451 | S80 | -6180 | 289 | 1501 | S30 | -6930 | 289 |
| 1352 | S179 | -4695 | 164 | 1402 | S129 | -5445 | 164 | 1452 | S79 | -6195 | 164 | 1502 | S29 | -6945 | 164 |
| 1353 | S178 | -4710 | 289 | 1403 | S128 | -5460 | 289 | 1453 | S78 | -6210 | 289 | 1503 | S28 | -6960 | 289 |
| 1354 | S177 | -4725 | 164 | 1404 | S127 | -5475 | 164 | 1454 | S77 | -6225 | 164 | 1504 | S27 | -6975 | 164 |
| 1355 | S176 | -4740 | 289 | 1405 | S126 | -5490 | 289 | 1455 | S76 | -6240 | 289 | 1505 | S26 | -6990 | 289 |
| 1356 | S175 | -4755 | 164 | 1406 | S125 | -5505 | 164 | 1456 | S75 | -6255 | 164 | 1506 | S25 | -7005 | 164 |
| 1357 | S174 | -4770 | 289 | 1407 | S124 | -5520 | 289 | 1457 | S74 | -6270 | 289 | 1507 | S24 | -7020 | 289 |
| 1358 | S173 | -4785 | 164 | 1408 | S123 | -5535 | 164 | 1458 | S73 | -6285 | 164 | 1508 | S23 | -7035 | 164 |
| 1359 | S172 | -4800 | 289 | 1409 | S122 | -5550 | 289 | 1459 | S72 | -6300 | 289 | 1509 | S22 | -7050 | 289 |
| 1360 | S171 | -4815 | 164 | 1410 | S121 | -5565 | 164 | 1460 | S71 | -6315 | 164 | 1510 | S21 | -7065 | 164 |
| 1361 | S170 | -4830 | 289 | 1411 | S120 | -5580 | 289 | 1461 | S70 | -6330 | 289 | 1511 | S20 | -7080 | 289 |
| 1362 | S169 | -4845 | 164 | 1412 | S119 | -5595 | 164 | 1462 | S69 | -6345 | 164 | 1512 | S19 | -7095 | 164 |
| 1363 | S168 | -4860 | 289 | 1413 | S118 | -5610 | 289 | 1463 | S68 | -6360 | 289 | 1513 | S18 | -7110 | 289 |
| 1364 | S167 | -4875 | 164 | 1414 | S117 | -5625 | 164 | 1464 | S67 | -6375 | 164 | 1514 | S17 | -7125 | 164 |
| 1365 | S166 | -4890 | 289 | 1415 | S116 | -5640 | 289 | 1465 | S66 | -6390 | 289 | 1515 | S16 | -7140 | 289 |
| 1366 | S165 | -4905 | 164 | 1416 | S115 | -5655 | 164 | 1466 | S65 | -6405 | 164 | 1516 | S15 | -7155 | 164 |
| 1367 | S164 | -4920 | 289 | 1417 | S114 | -5670 | 289 | 1467 | S64 | -6420 | 289 | 1517 | S14 | -7170 | 289 |
| 1368 | S163 | -4935 | 164 | 1418 | S113 | -5685 | 164 | 1468 | S63 | -6435 | 164 | 1518 | S13 | -7185 | 164 |
| 1369 | S162 | -4950 | 289 | 1419 | S112 | -5700 | 289 | 1469 | S62 | -6450 | 289 | 1519 | S12 | -7200 | 289 |
| 1370 | S161 | -4965 | 164 | 1420 | S111 | -5715 | 164 | 1470 | S61 | -6465 | 164 | 1520 | S11 | -7215 | 164 |
| 1371 | S160 | -4980 | 289 | 1421 | S110 | -5730 | 289 | 1471 | S60 | -6480 | 289 | 1521 | S10 | -7230 | 289 |
| 1372 | S159 | -4995 | 164 | 1422 | S109 | -5745 | 164 | 1472 | S59 | -6495 | 164 | 1522 | S9 | -7245 | 164 |
| 1373 | S158 | -5010 | 289 | 1423 | S108 | -5760 | 289 | 1473 | S58 | -6510 | 289 | 1523 | S8 | -7260 | 289 |
| 1374 | S157 | -5025 | 164 | 1424 | S107 | -5775 | 164 | 1474 | S57 | -6525 | 164 | 1524 | S7 | -7275 | 164 |
| 1375 | S156 | -5040 | 289 | 1425 | S106 | -5790 | 289 | 1475 | S56 | -6540 | 289 | 1525 | S6 | -7290 | 289 |
| 1376 | S155 | -5055 | 164 | 1426 | S105 | -5805 | 164 | 1476 | S55 | -6555 | 164 | 1526 | S5 | -7305 | 164 |
| 1377 | S154 | -5070 | 289 | 1427 | S104 | -5820 | 289 | 1477 | S54 | -6570 | 289 | 1527 | S4 | -7320 | 289 |
| 1378 | S153 | -5085 | 164 | 1428 | S103 | -5835 | 164 | 1478 | S53 | -6585 | 164 | 1528 | S3 | -7335 | 164 |
| 1379 | S152 | -5100 | 289 | 1429 | S102 | -5850 | 289 | 1479 | S52 | -6600 | 289 | 1529 | S2 | -7350 | 289 |
| 1380 | S151 | -5115 | 164 | 1430 | S101 | -5865 | 164 | 1480 | S51 | -6615 | 164 | 1530 | S1 | -7365 | 164 |
| 1381 | S150 | -5130 | 289 | 1431 | S100 | -5880 | 289 | 1481 | S50 | -6630 | 289 | 1531 | DUMMY | -7380 | 289 |
| 1382 | S149 | -5145 | 164 | 1432 | S99 | -5895 | 164 | 1482 | S49 | -6645 | 164 | 1532 | DUMMY | -7395 | 164 |
| 1383 | S148 | -5160 | 289 | 1433 | S98 | -5910 | 289 | 1483 | S48 | -6660 | 289 | 1533 | DUMMY | -7560 | 289 |
| 1384 | S147 | -5175 | 164 | 1434 | S97 | -5925 | 164 | 1484 | S47 | -6675 | 164 | 1534 | DUMMY | -7575 | 164 |
| 1385 | S146 | -5190 | 289 | 1435 | S96 | -5940 | 289 | 1485 | S46 | -6690 | 289 | 1535 | G480 | -7590 | 289 |
| 1386 | S145 | -5205 | 164 | 1436 | S95 | -5955 | 164 | 1486 | S45 | -6705 | 164 | 1536 | G478 | -7605 | 164 |
| 1387 | S144 | -5220 | 289 | 1437 | S94 | -5970 | 289 | 1487 | S44 | -6720 | 289 | 1537 | G476 | -7620 | 289 |
| 1388 | S143 | -5235 | 164 | 1438 | S93 | -5985 | 164 | 1488 | S43 | -6735 | 164 | 1538 | G474 | -7635 | 164 |
| 1389 | S142 | -5250 | 289 | 1439 | S92 | -6000 | 289 | 1489 | S42 | -6750 | 289 | 1539 | G472 | -7650 | 289 |
| 1390 | S141 | -5265 | 164 | 1440 | S91 | -6015 | 164 | 1490 | S41 | -6765 | 164 | 1540 | G470 | -7665 | 164 |
| 1391 | S140 | -5280 | 289 | 1441 | S90 | -6030 | 289 | 1491 | S40 | -6780 | 289 | 1541 | G468 | -7680 | 289 |
| 1392 | S139 | -5295 | 164 | 1442 | S89 | -6045 | 164 | 1492 | S39 | -6795 | 164 | 1542 | G466 | -7695 | 164 |
| 1393 | S138 | -5310 | 289 | 1443 | S88 | -6060 | 289 | 1493 | S38 | -6810 | 289 | 1543 | G464 | -7710 | 289 |
| 1394 | S137 | -5325 | 164 | 1444 | S87 | -6075 | 164 | 1494 | S37 | -6825 | 164 | 1544 | G462 | -7725 | 164 |

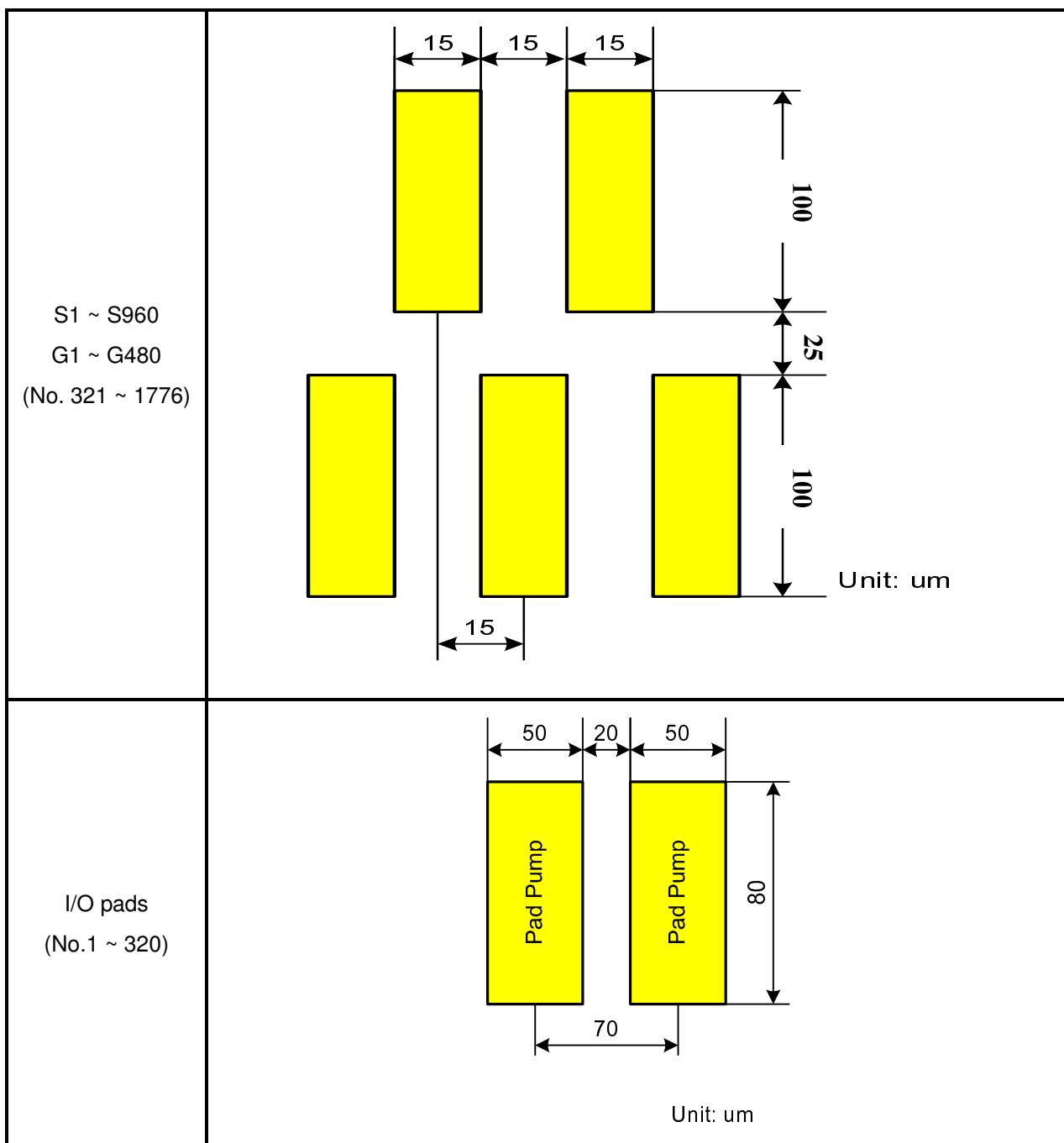
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|------|------|-------|-----|------|------|-------|-----|------|------|-------|-----|------|------|--------|-----|
| 1545 | G460 | -7740 | 289 | 1595 | G360 | -8490 | 289 | 1645 | G260 | -9240 | 289 | 1695 | G160 | -9990 | 289 |
| 1546 | G458 | -7755 | 164 | 1596 | G358 | -8505 | 164 | 1646 | G258 | -9255 | 164 | 1696 | G158 | -10005 | 164 |
| 1547 | G456 | -7770 | 289 | 1597 | G356 | -8520 | 289 | 1647 | G256 | -9270 | 289 | 1697 | G156 | -10020 | 289 |
| 1548 | G454 | -7785 | 164 | 1598 | G354 | -8535 | 164 | 1648 | G254 | -9285 | 164 | 1698 | G154 | -10035 | 164 |
| 1549 | G452 | -7800 | 289 | 1599 | G352 | -8550 | 289 | 1649 | G252 | -9300 | 289 | 1699 | G152 | -10050 | 289 |
| 1550 | G450 | -7815 | 164 | 1600 | G350 | -8565 | 164 | 1650 | G250 | -9315 | 164 | 1700 | G150 | -10065 | 164 |
| 1551 | G448 | -7830 | 289 | 1601 | G348 | -8580 | 289 | 1651 | G248 | -9330 | 289 | 1701 | G148 | -10080 | 289 |
| 1552 | G446 | -7845 | 164 | 1602 | G346 | -8595 | 164 | 1652 | G246 | -9345 | 164 | 1702 | G146 | -10095 | 164 |
| 1553 | G444 | -7860 | 289 | 1603 | G344 | -8610 | 289 | 1653 | G244 | -9360 | 289 | 1703 | G144 | -10110 | 289 |
| 1554 | G442 | -7875 | 164 | 1604 | G342 | -8625 | 164 | 1654 | G242 | -9375 | 164 | 1704 | G142 | -10125 | 164 |
| 1555 | G440 | -7890 | 289 | 1605 | G340 | -8640 | 289 | 1655 | G240 | -9390 | 289 | 1705 | G140 | -10140 | 289 |
| 1556 | G438 | -7905 | 164 | 1606 | G338 | -8655 | 164 | 1656 | G238 | -9405 | 164 | 1706 | G138 | -10155 | 164 |
| 1557 | G436 | -7920 | 289 | 1607 | G336 | -8670 | 289 | 1657 | G236 | -9420 | 289 | 1707 | G136 | -10170 | 289 |
| 1558 | G434 | -7935 | 164 | 1608 | G334 | -8685 | 164 | 1658 | G234 | -9435 | 164 | 1708 | G134 | -10185 | 164 |
| 1559 | G432 | -7950 | 289 | 1609 | G332 | -8700 | 289 | 1659 | G232 | -9450 | 289 | 1709 | G132 | -10200 | 289 |
| 1560 | G430 | -7965 | 164 | 1610 | G330 | -8715 | 164 | 1660 | G230 | -9465 | 164 | 1710 | G130 | -10215 | 164 |
| 1561 | G428 | -7980 | 289 | 1611 | G328 | -8730 | 289 | 1661 | G228 | -9480 | 289 | 1711 | G128 | -10230 | 289 |
| 1562 | G426 | -7995 | 164 | 1612 | G326 | -8745 | 164 | 1662 | G226 | -9495 | 164 | 1712 | G126 | -10245 | 164 |
| 1563 | G424 | -8010 | 289 | 1613 | G324 | -8760 | 289 | 1663 | G224 | -9510 | 289 | 1713 | G124 | -10260 | 289 |
| 1564 | G422 | -8025 | 164 | 1614 | G322 | -8775 | 164 | 1664 | G222 | -9525 | 164 | 1714 | G122 | -10275 | 164 |
| 1565 | G420 | -8040 | 289 | 1615 | G320 | -8790 | 289 | 1665 | G220 | -9540 | 289 | 1715 | G120 | -10290 | 289 |
| 1566 | G418 | -8055 | 164 | 1616 | G318 | -8805 | 164 | 1666 | G218 | -9555 | 164 | 1716 | G118 | -10305 | 164 |
| 1567 | G416 | -8070 | 289 | 1617 | G316 | -8820 | 289 | 1667 | G216 | -9570 | 289 | 1717 | G116 | -10320 | 289 |
| 1568 | G414 | -8085 | 164 | 1618 | G314 | -8835 | 164 | 1668 | G214 | -9585 | 164 | 1718 | G114 | -10335 | 164 |
| 1569 | G412 | -8100 | 289 | 1619 | G312 | -8850 | 289 | 1669 | G212 | -9600 | 289 | 1719 | G112 | -10350 | 289 |
| 1570 | G410 | -8115 | 164 | 1620 | G310 | -8865 | 164 | 1670 | G210 | -9615 | 164 | 1720 | G110 | -10365 | 164 |
| 1571 | G408 | -8130 | 289 | 1621 | G308 | -8880 | 289 | 1671 | G208 | -9630 | 289 | 1721 | G108 | -10380 | 289 |
| 1572 | G406 | -8145 | 164 | 1622 | G306 | -8895 | 164 | 1672 | G206 | -9645 | 164 | 1722 | G106 | -10395 | 164 |
| 1573 | G404 | -8160 | 289 | 1623 | G304 | -8910 | 289 | 1673 | G204 | -9660 | 289 | 1723 | G104 | -10410 | 289 |
| 1574 | G402 | -8175 | 164 | 1624 | G302 | -8925 | 164 | 1674 | G202 | -9675 | 164 | 1724 | G102 | -10425 | 164 |
| 1575 | G400 | -8190 | 289 | 1625 | G300 | -8940 | 289 | 1675 | G200 | -9690 | 289 | 1725 | G100 | -10440 | 289 |
| 1576 | G398 | -8205 | 164 | 1626 | G298 | -8955 | 164 | 1676 | G198 | -9705 | 164 | 1726 | G98 | -10455 | 164 |
| 1577 | G396 | -8220 | 289 | 1627 | G296 | -8970 | 289 | 1677 | G196 | -9720 | 289 | 1727 | G96 | -10470 | 289 |
| 1578 | G394 | -8235 | 164 | 1628 | G294 | -8985 | 164 | 1678 | G194 | -9735 | 164 | 1728 | G94 | -10485 | 164 |
| 1579 | G392 | -8250 | 289 | 1629 | G292 | -9000 | 289 | 1679 | G192 | -9750 | 289 | 1729 | G92 | -10500 | 289 |
| 1580 | G390 | -8265 | 164 | 1630 | G290 | -9015 | 164 | 1680 | G190 | -9765 | 164 | 1730 | G90 | -10515 | 164 |
| 1581 | G388 | -8280 | 289 | 1631 | G288 | -9030 | 289 | 1681 | G188 | -9780 | 289 | 1731 | G88 | -10530 | 289 |
| 1582 | G386 | -8295 | 164 | 1632 | G286 | -9045 | 164 | 1682 | G186 | -9795 | 164 | 1732 | G86 | -10545 | 164 |
| 1583 | G384 | -8310 | 289 | 1633 | G284 | -9060 | 289 | 1683 | G184 | -9810 | 289 | 1733 | G84 | -10560 | 289 |
| 1584 | G382 | -8325 | 164 | 1634 | G282 | -9075 | 164 | 1684 | G182 | -9825 | 164 | 1734 | G82 | -10575 | 164 |
| 1585 | G380 | -8340 | 289 | 1635 | G280 | -9090 | 289 | 1685 | G180 | -9840 | 289 | 1735 | G80 | -10590 | 289 |
| 1586 | G378 | -8355 | 164 | 1636 | G278 | -9105 | 164 | 1686 | G178 | -9855 | 164 | 1736 | G78 | -10605 | 164 |
| 1587 | G376 | -8370 | 289 | 1637 | G276 | -9120 | 289 | 1687 | G176 | -9870 | 289 | 1737 | G76 | -10620 | 289 |
| 1588 | G374 | -8385 | 164 | 1638 | G274 | -9135 | 164 | 1688 | G174 | -9885 | 164 | 1738 | G74 | -10635 | 164 |
| 1589 | G372 | -8400 | 289 | 1639 | G272 | -9150 | 289 | 1689 | G172 | -9900 | 289 | 1739 | G72 | -10650 | 289 |
| 1590 | G370 | -8415 | 164 | 1640 | G270 | -9165 | 164 | 1690 | G170 | -9915 | 164 | 1740 | G70 | -10665 | 164 |
| 1591 | G368 | -8430 | 289 | 1641 | G268 | -9180 | 289 | 1691 | G168 | -9930 | 289 | 1741 | G68 | -10680 | 289 |
| 1592 | G366 | -8445 | 164 | 1642 | G266 | -9195 | 164 | 1692 | G166 | -9945 | 164 | 1742 | G66 | -10695 | 164 |
| 1593 | G364 | -8460 | 289 | 1643 | G264 | -9210 | 289 | 1693 | G164 | -9960 | 289 | 1743 | G64 | -10710 | 289 |
| 1594 | G362 | -8475 | 164 | 1644 | G262 | -9225 | 164 | 1694 | G162 | -9975 | 164 | 1744 | G62 | -10725 | 164 |

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| No. | Name | X | Y |
|-----------------------|-------|--------|------|
| 1745 | G60 | -10740 | 289 |
| 1746 | G58 | -10755 | 164 |
| 1747 | G56 | -10770 | 289 |
| 1748 | G54 | -10785 | 164 |
| 1749 | G52 | -10800 | 289 |
| 1750 | G50 | -10815 | 164 |
| 1751 | G48 | -10830 | 289 |
| 1752 | G46 | -10845 | 164 |
| 1753 | G44 | -10860 | 289 |
| 1754 | G42 | -10875 | 164 |
| 1755 | G40 | -10890 | 289 |
| 1756 | G38 | -10905 | 164 |
| 1757 | G36 | -10920 | 289 |
| 1758 | G34 | -10935 | 164 |
| 1759 | G32 | -10950 | 289 |
| 1760 | G30 | -10965 | 164 |
| 1761 | G28 | -10980 | 289 |
| 1762 | G26 | -10995 | 164 |
| 1763 | G24 | -11010 | 289 |
| 1764 | G22 | -11025 | 164 |
| 1765 | G20 | -11040 | 289 |
| 1766 | G18 | -11055 | 164 |
| 1767 | G16 | -11070 | 289 |
| 1768 | G14 | -11085 | 164 |
| 1769 | G12 | -11100 | 289 |
| 1770 | G10 | -11115 | 164 |
| 1771 | G8 | -11130 | 289 |
| 1772 | G6 | -11145 | 164 |
| 1773 | G4 | -11160 | 289 |
| 1774 | G2 | -11175 | 164 |
| 1775 | DUMMY | -11190 | 289 |
| 1776 | DUMMY | -11205 | 164 |
| | | | |
| Alignment mark -Left | | -11300 | -270 |
| Alignment mark -Right | | 11300 | -270 |

3.6.Bump Arrangement



4. System Interfaces

The ILI9488 supports MIPI DBI, DPI, and DSI. DBI supports (8-/9-/16-/18-/24-bit interface) Parallel Interface (Type B) and Serial Interface (Type C). The interface mode can be selected by IM [2:0] pins, as shown in Table 3 below.

Table 3: Interface Selection

| IM2 | IM1 | IM0 | Interface | Data Pins in Use | |
|-----|-----|-----|----------------------------------|---|-------------------------|
| | | | | Command/Parameter | GRAM |
| 0 | 0 | 0 | DBI Type B 24-bit (DB_EN = 1) | DB [7:0] | DB [23:0]: 24-bits Data |
| 0 | 0 | 0 | DBI Type B 18-bit (DB_EN = 0) | DB [7:0] | DB [17:0]: 18-bits Data |
| 0 | 0 | 1 | DBI Type B 9-bit | DB [7:0] | DB [8:0]: 9-bits Data |
| 0 | 1 | 0 | DBI Type B 16-bit | DB [7:0] | DB [15:0]: 16-bits Data |
| 0 | 1 | 1 | DBI Type B 8-bit | DB [7:0] | DB [7:0]: 8-bits Data |
| 1 | 0 | 1 | DBI Type C Option 1 (3-line SPI) | SDA/SDO | |
| 1 | 1 | 0 | DSI | MIPI_DATA_P, MIPI_DATA_N, MIPI_CLOCK_P, MIPI_CLOCK_N | |
| 1 | 1 | 1 | DBI Type C Option 3 (4-line SPI) | SDA/SDO | |

4.1. DBI Type B Parallel Interface

The ILI9488 includes an Index Register (IR), which stores the index data of internal Control Register (CR) and GRAM. The chip-select D/CX (active low) is used to enable or disable the ILI9488 chip. The RESX (active low) is an external reset signal, the WRX is a parallel data write strobe, the RDX is a parallel data read strobe, and DB [23:0] is a parallel data bus.

The ILI9488 latches the input data at the rising edge of the WRX signal. The D/CX is the signal for data/command selection. When D/CX = 1, DB [23:0] bits are RAM data or command parameters. When D/CX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MCU controller and the LCD driver chip. The selection and operation of the parallel interface is shown in Table 4.

Table 4: DBI Type B Parallel Interface

| IM2 | IM1 | IM0 | MPU-Interface Mode | WRX | RDX | D/CX | Function |
|-----|-----|-----|-------------------------------|-----|-----|------|---------------------------------|
| 0 | 0 | 0 | DBI Type B 24-bit (DB_EN = 1) | ↑ | "H" | "L" | Write command code |
| | | | | "H" | ↑ | "H" | Read internal status |
| | | | | ↑ | "H" | "H" | Write parameter or display data |
| | | | | "H" | ↑ | "H" | Read parameter or display data |
| 0 | 0 | 0 | DBI Type B 18-bit (DB_EN = 0) | ↑ | "H" | "L" | Write command code |
| | | | | "H" | ↑ | "H" | Read internal status |
| | | | | ↑ | "H" | "H" | Write parameter or display data |
| | | | | "H" | ↑ | "H" | Read parameter or display data |
| 0 | 0 | 1 | DBI Type B 9-bit | ↑ | "H" | "L" | Write command code |
| | | | | "H" | ↑ | "H" | Read internal status |
| | | | | ↑ | "H" | "H" | Write parameter or display data |
| | | | | "H" | ↑ | "H" | Read parameter or display data |
| 0 | 1 | 0 | DBI Type B 16-bit | ↑ | "H" | "L" | Write command code |
| | | | | "H" | ↑ | "H" | Read internal status |
| | | | | ↑ | "H" | "H" | Write parameter or display data |
| | | | | "H" | ↑ | "H" | Read parameter or display data |
| 0 | 1 | 1 | DBI Type B 8-bit | ↑ | "H" | "L" | Write command code |
| | | | | "H" | ↑ | "H" | Read internal status |
| | | | | ↑ | "H" | "H" | Write parameter or display data |
| | | | | "H" | ↑ | "H" | Read parameter or display data |

4.1.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. Figure 1 below shows the write cycle of the DBI Type B interface.

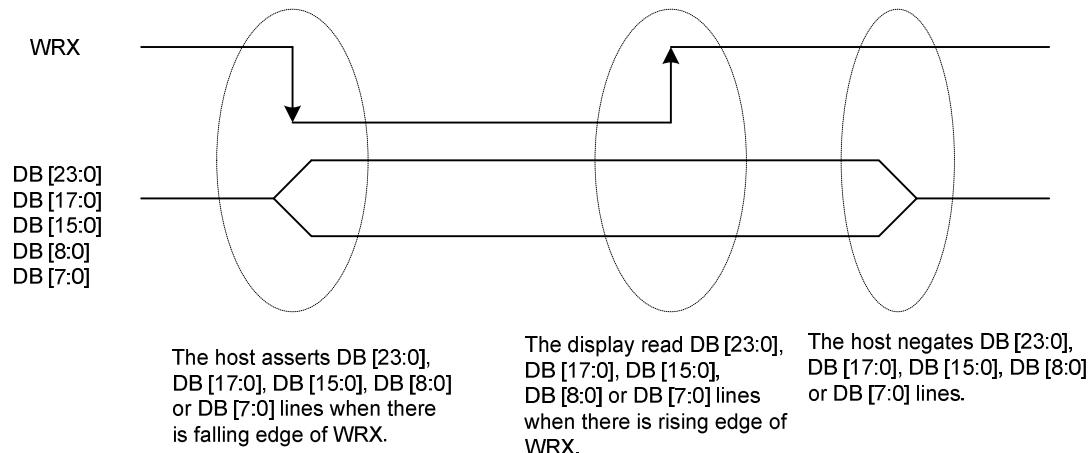


Figure 1: DBI Type B Write Cycle

Note: WRX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to low level, the input data on the interface is interpreted as command information.

The D/CX signal can also be pulled to high level when the data is RAM data or command parameter.

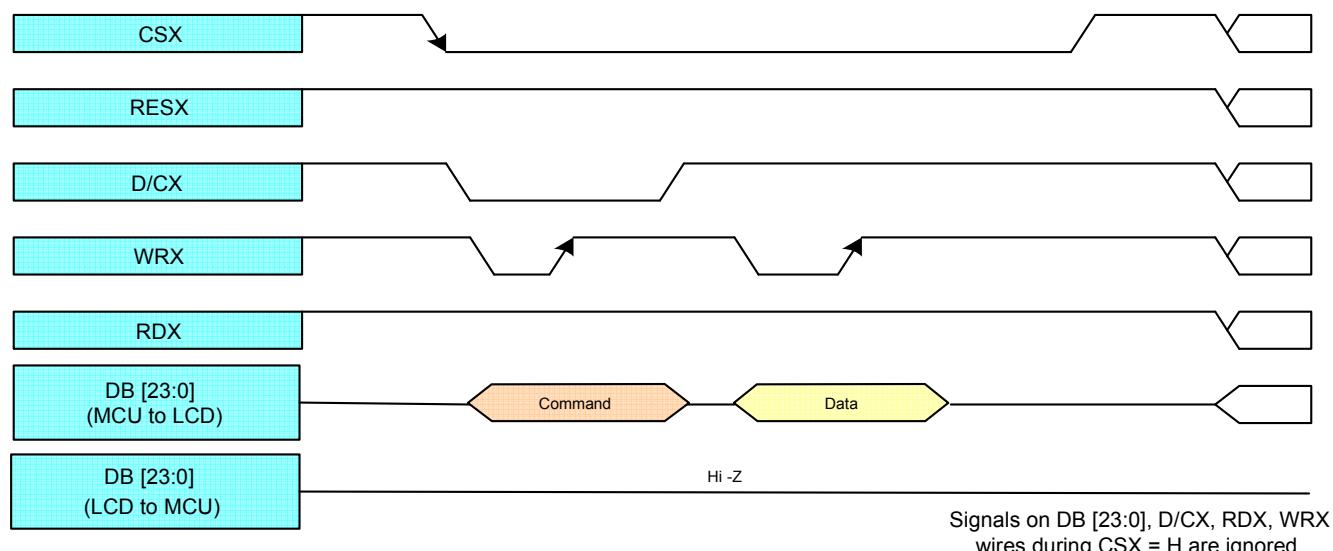


Figure 2: DBI Type B Write Cycle Sequence

4.1.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. Figure 3 below shows the read cycle of the DBI Type B interface.

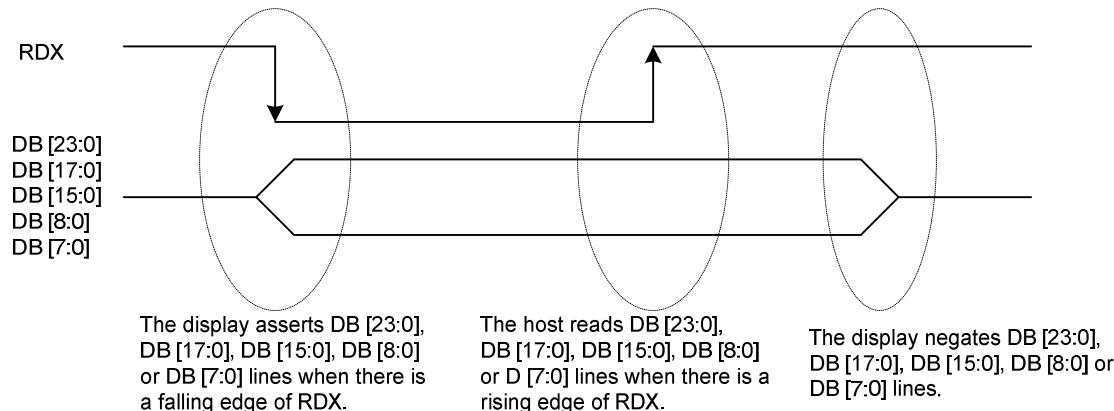


Figure 3: DBI Type B Read Cycle

Note: RDX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The D/CX signal can also be pulled to a high level when the data on the interface is RAM data or a command parameter data.

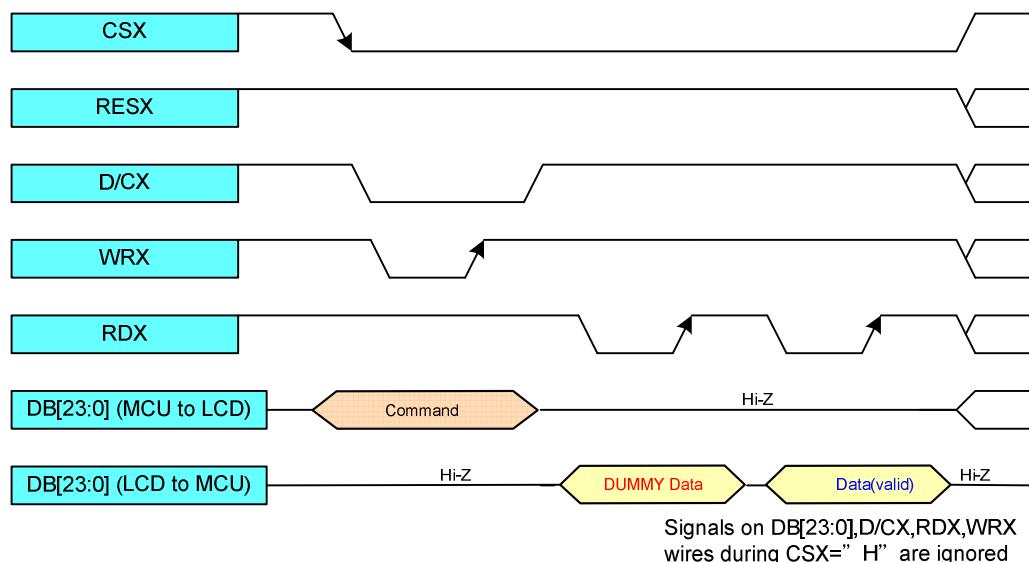


Figure 4: DBI Type B Read Cycle Sequence

Note: Read Data is only valid when the D/CX input is pulled high. If the D/CX signal is driven to low during the read cycle then the display information outputs will be High-Z.

4.2.DBI Type C Serial Interface

The selection of this interface is done by the IM [2:0] pins, as shown in the table below.

Table 5: DBI Type C Serial Interface

| IM2 | IM1 | IM0 | DBI Type C | D/CX | CSX | SCL | Function |
|-----|-----|-----|-----------------------|---------|-----|---|---|
| 1 | 0 | 1 | Option 1 (3-line SPI) | - | "L" |  | Read/Write command, parameter or display data |
| 1 | 1 | 1 | Option 3 (4-line SPI) | "L"/"H" | "L" |  | Read/Write command, parameter or display data |

The ILI9488 uses 3-line 9-bit and 4-line 8-bit serial interfaces for communication between the host and the ILI9488. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). The 4-line serial interface consists of the Data/Command and selection input (D/CX), chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the DPI interface data transfer, the unused pins will not be affected. The Serial clock (SCL) is used only for the interface with the MCU, so it can be stopped when no communication is necessary.

4.2.1. Write Cycle Sequence

In the write mode of the interface, the host writes commands and data to the ILI9488. The 3-line serial data packet contains a D/CX (data/command) select bit and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored in the GRAM as display data, or stored in the command register as parameter data.

Any instruction can be sent in any order to the ILI9488, and the MSB is transmitted first. The serial interface is initialized when the CSX is in high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See detailed formats for 3-/4-line serial interface in the following two figures.

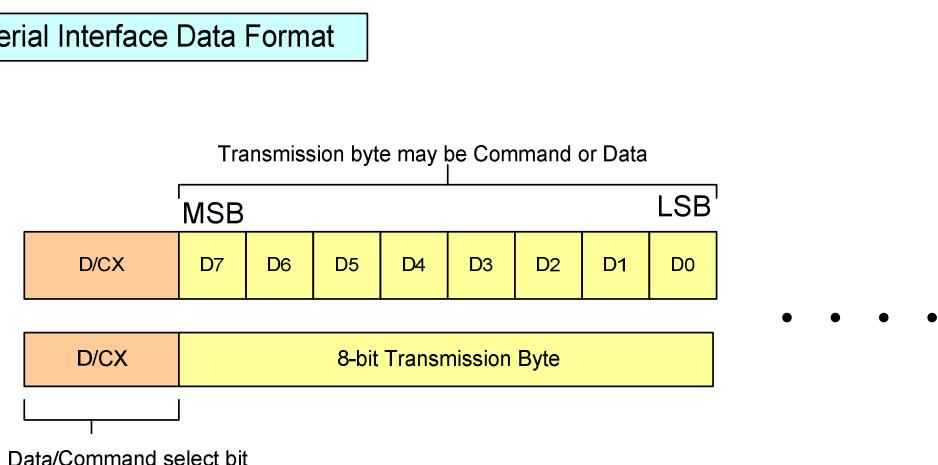


Figure 5: DBI Type C (Option 1) Data Format

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4-line Serial Interface Data Format

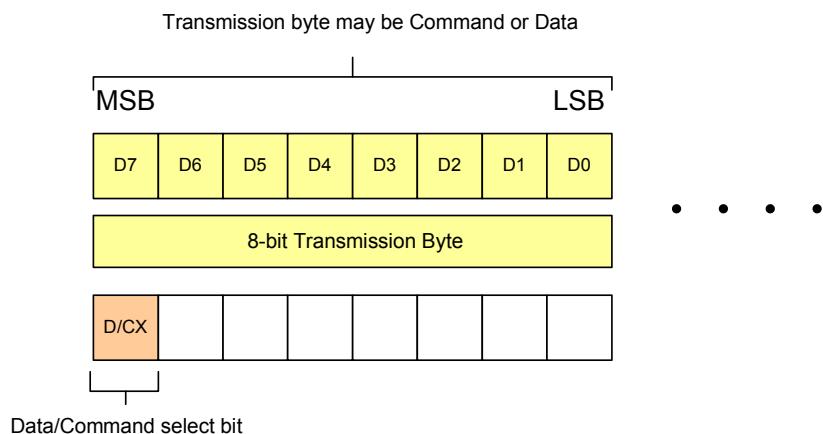


Figure 6: DBI Type C (Option 3) Data Format

The host drives the CSX pin to low and sets the D/CX bit on the SDA pin. The bit is read by the ILI9488 on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDA pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDA pin. If the optional D/CX signal is used, a byte is eight read cycles long. The 3-/4-line serial interface writing sequences are described in Figure 7 and Figure 8 below.

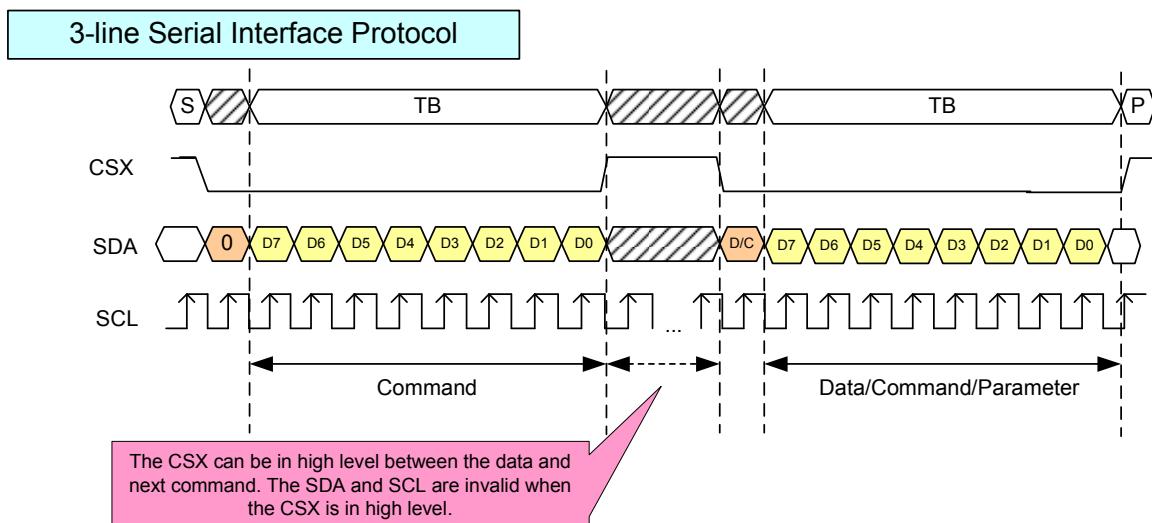


Figure 7: DBI Type C (Option 1) Protocol

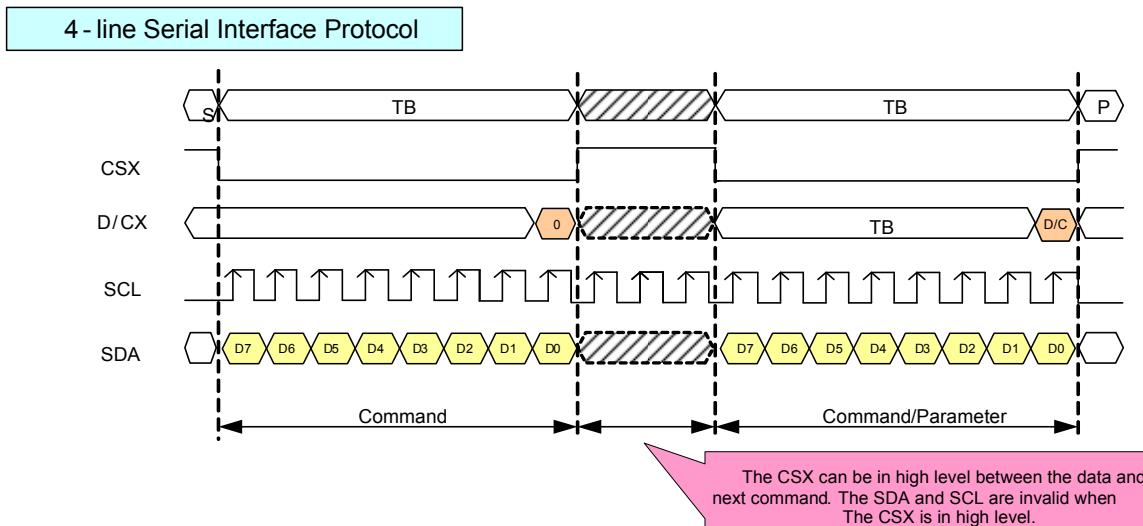
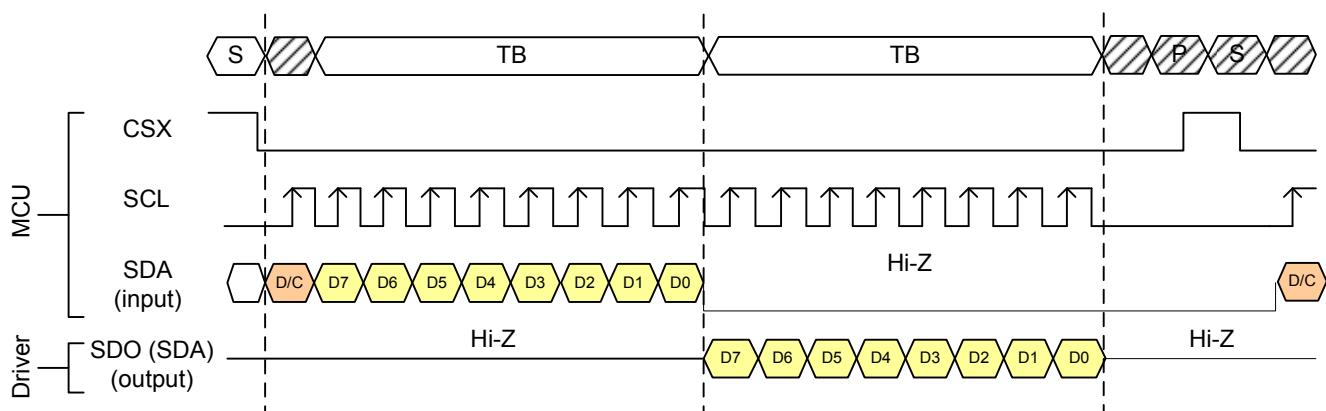
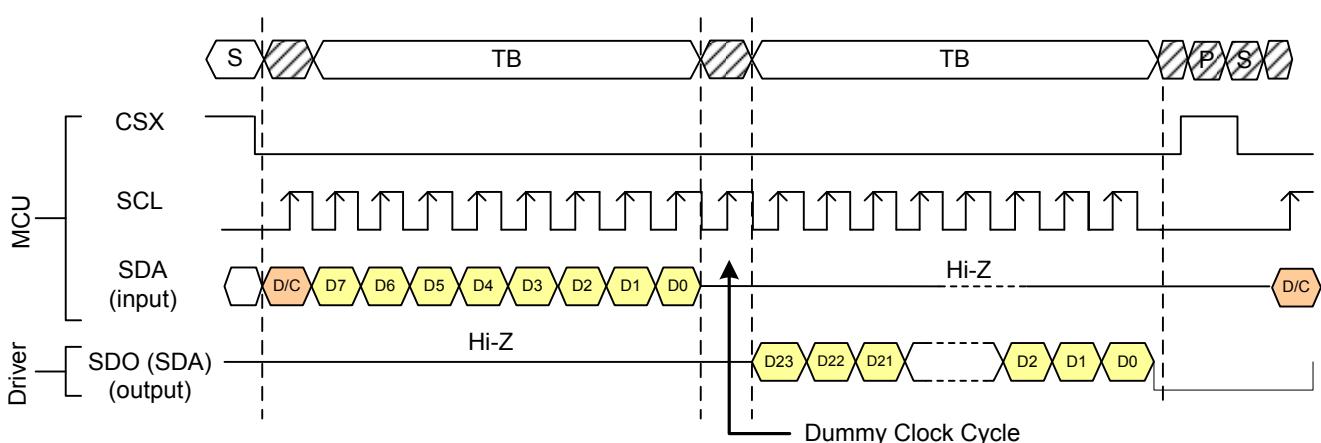
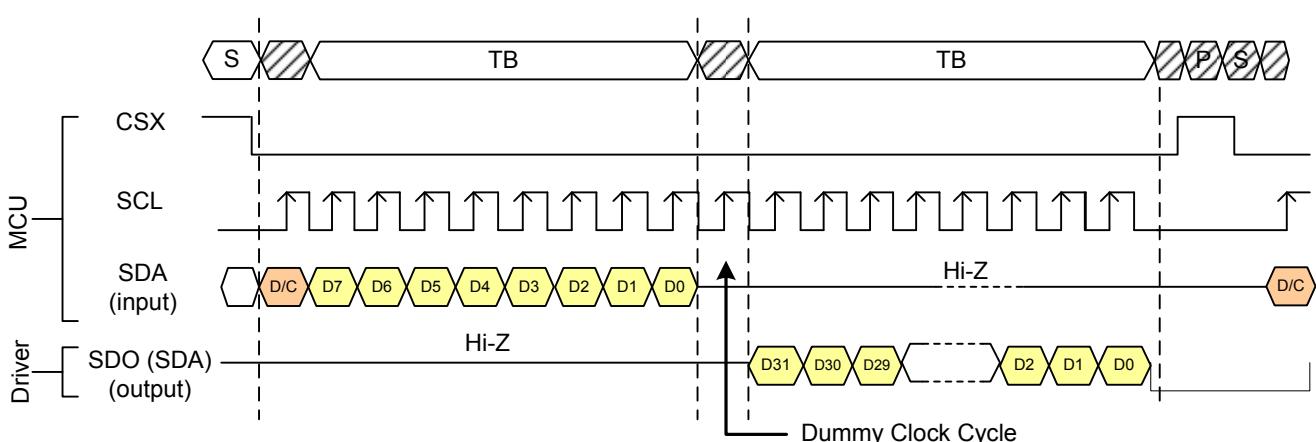
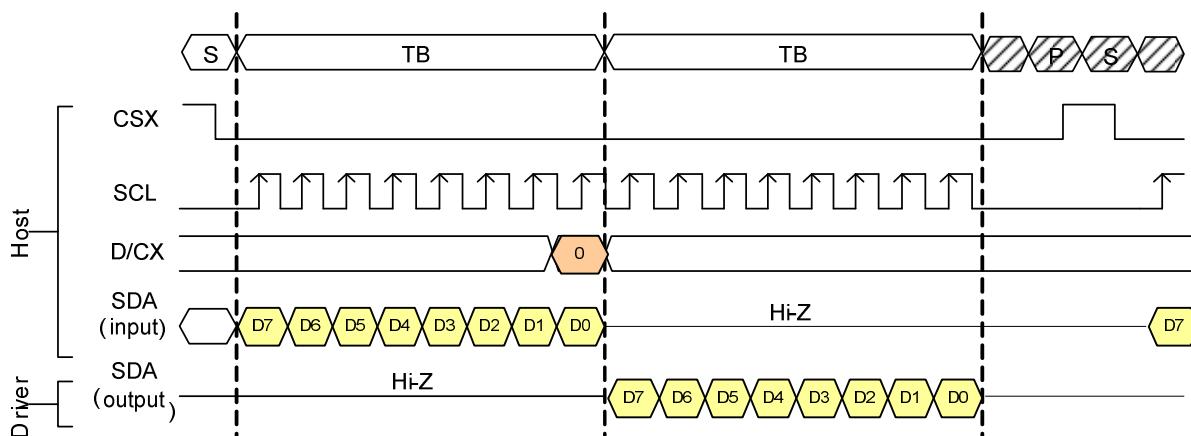
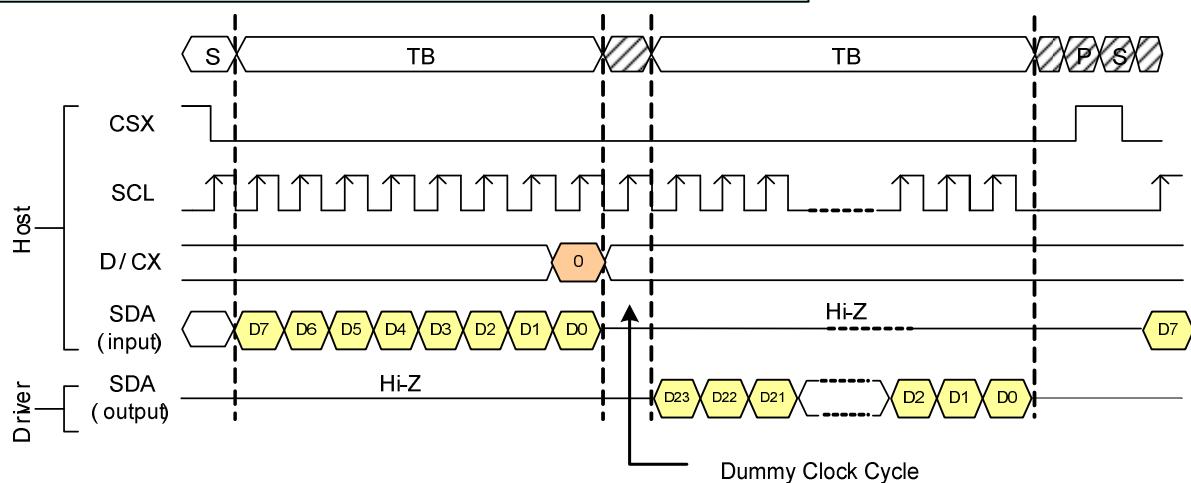
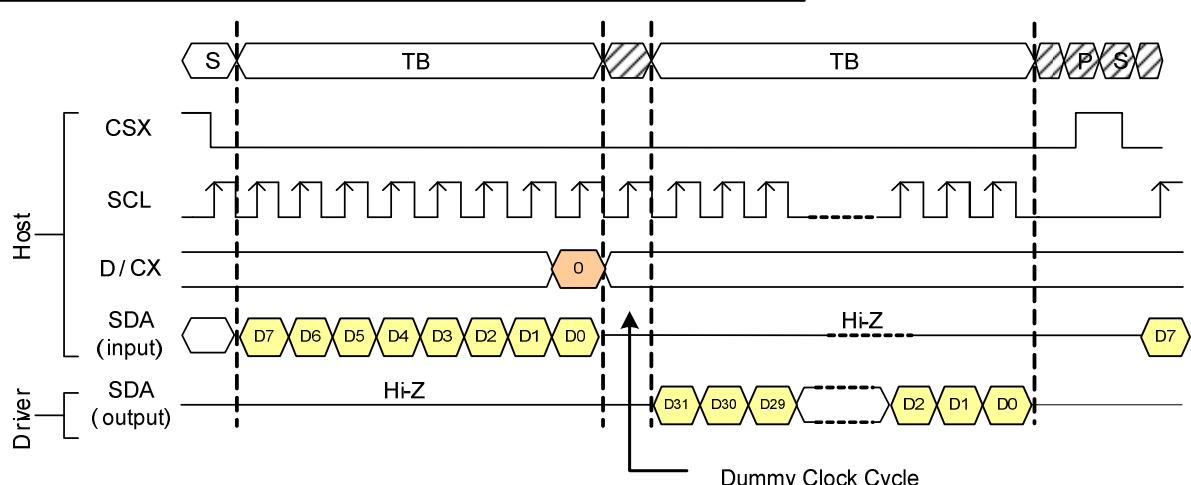


Figure 8: DBI Type C (Option 3) Protocol

4.2.2. Read Cycle Sequence

In the read mode of the interface, the host reads the register value from the ILI9488. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9488 samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

3-line Serial Protocol (for RDDID command: 24-bit read)

3-line Serial Protocol (for RDDST command: 32-bit read)

Figure 9: DBI Type C (Option 1) Read Cycle Sequence

4-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

4-line Serial Protocol (for RDDID command: 24-bit read)

4-line Serial Protocol (for RDDST command: 32-bit read)

Figure 10: DBI Type C (Option 3) Read Cycle Sequence

4.2.3. Data Transfer Break and Recovery

If data transmission is interrupted by the CSX pulse while transferring a Command, Frame Memory Data, or Multiple Parameter Command before Bit D0 of the byte is completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is activated again.

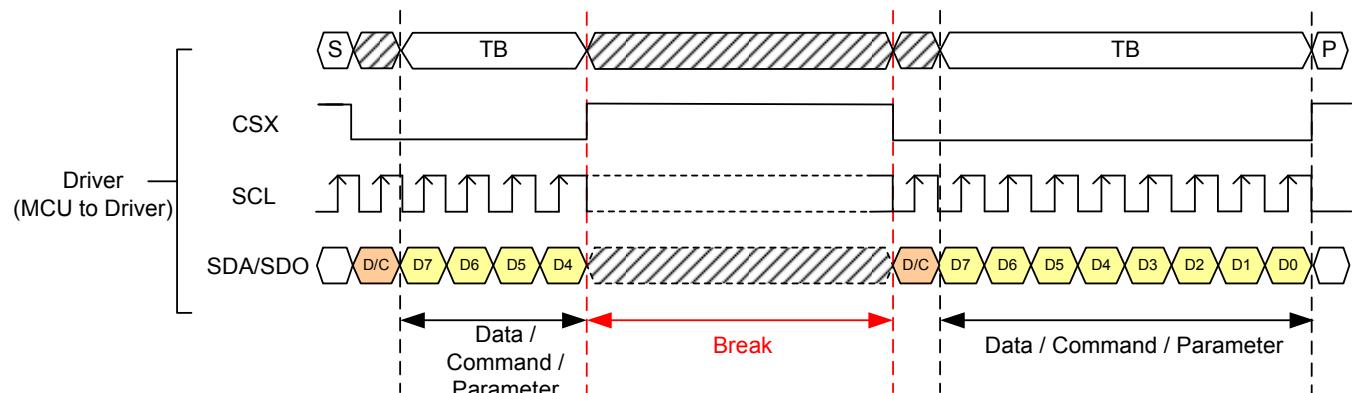


Figure 11: Data Transfer Break and Recovery

If there is a break when transmitting a command with multiple parameters, and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below.

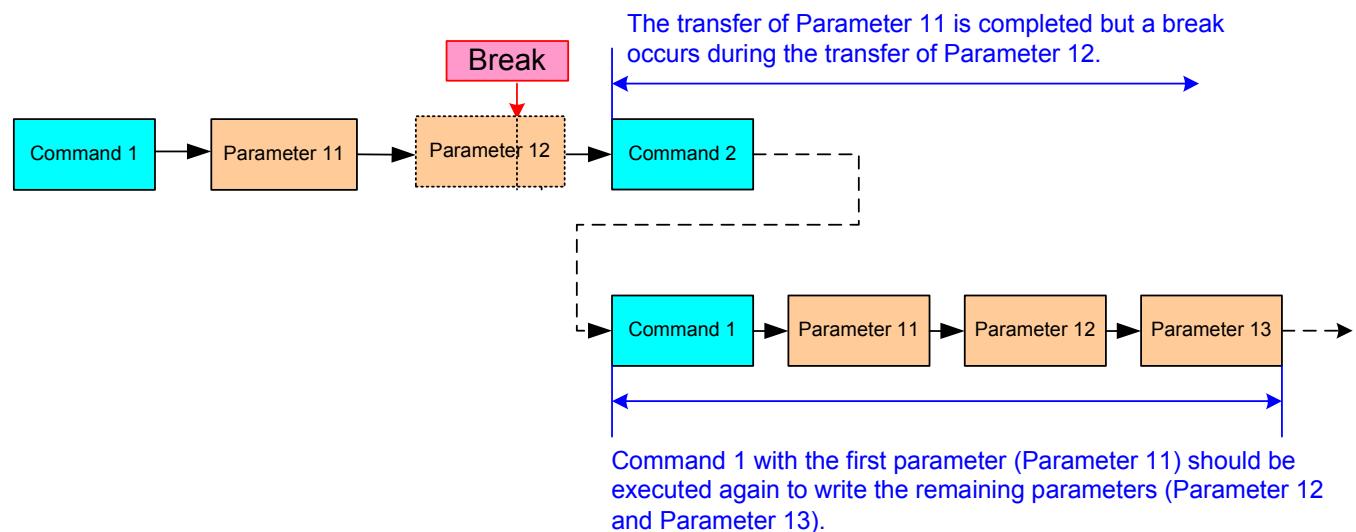


Figure 12: Data Transfer Break – Case 1

If a command with multiple parameters is sent and a break occurs by a new command before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command will remain at the previous value.

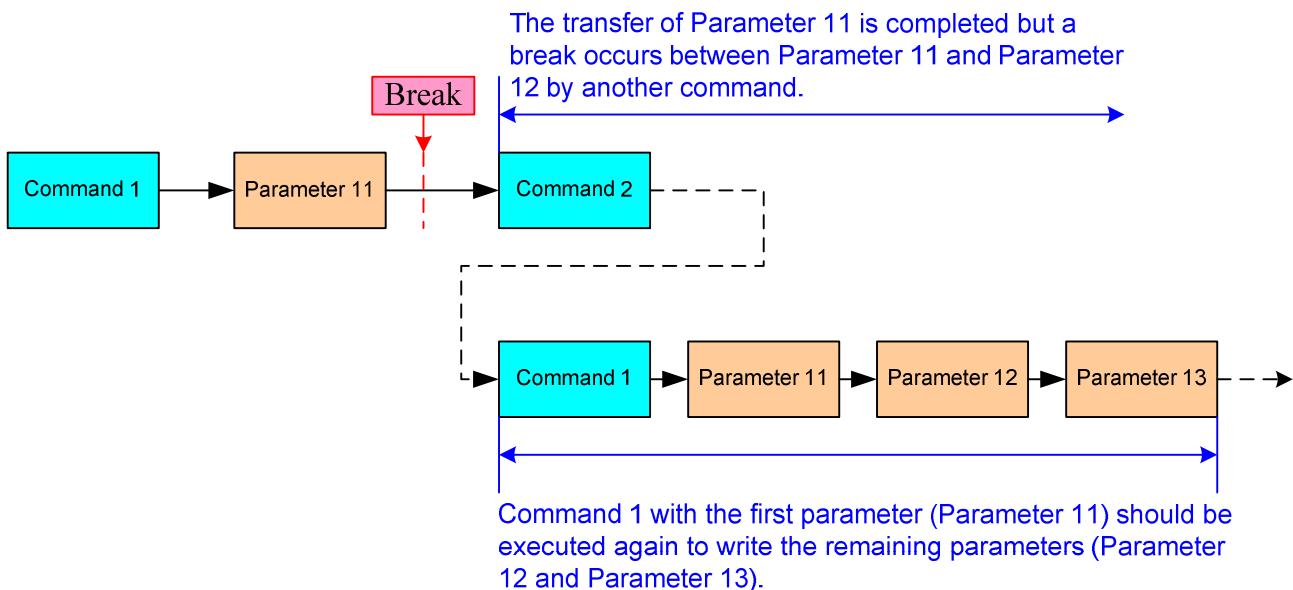


Figure 13: Data Transfer Break – Case 2

4.3. Data Transfer Pause

Transferring a Command, Frame Memory Data or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ILI9488 will wait and continue the Frame Memory Data or Parameter Data transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

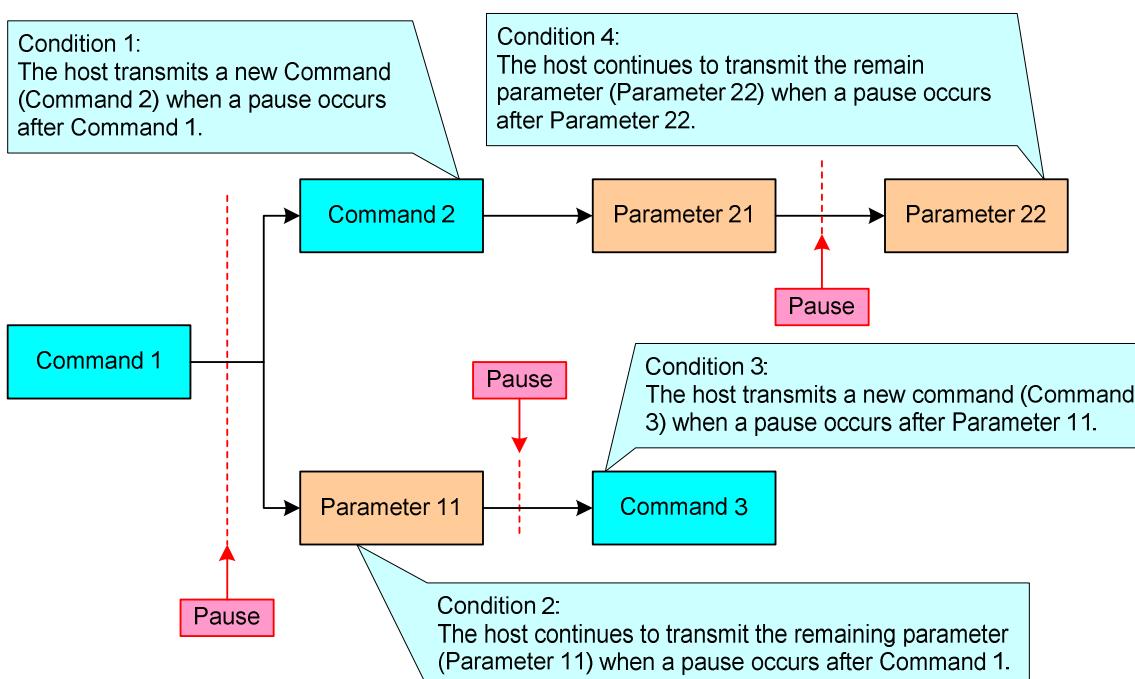


Figure 14: Data Transfer Pause

4.3.1. Serial Interface Pause

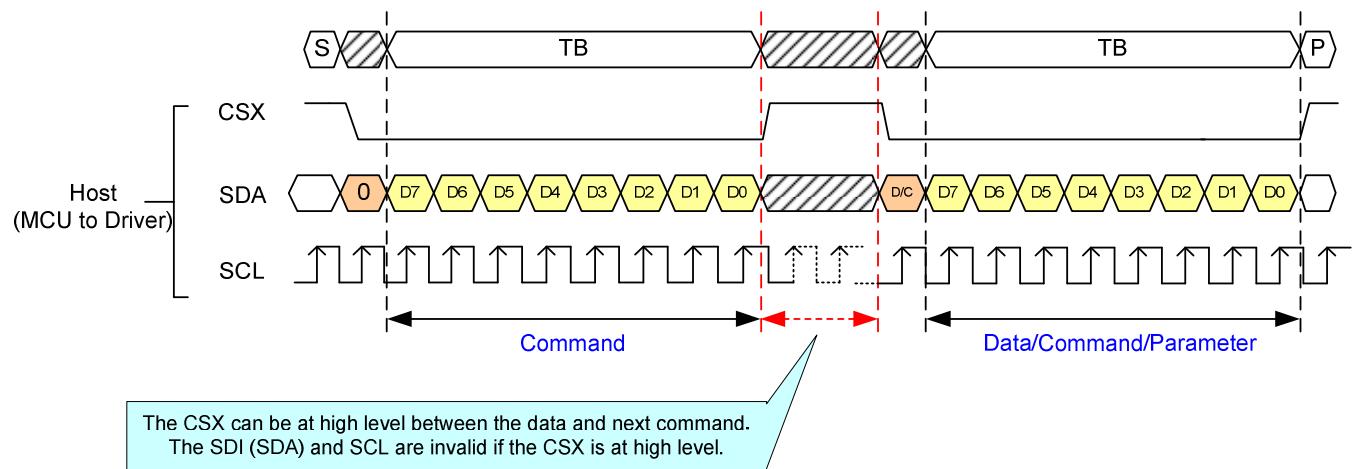


Figure 15: DBI Type C Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

4.3.2. Parallel Interface Pause

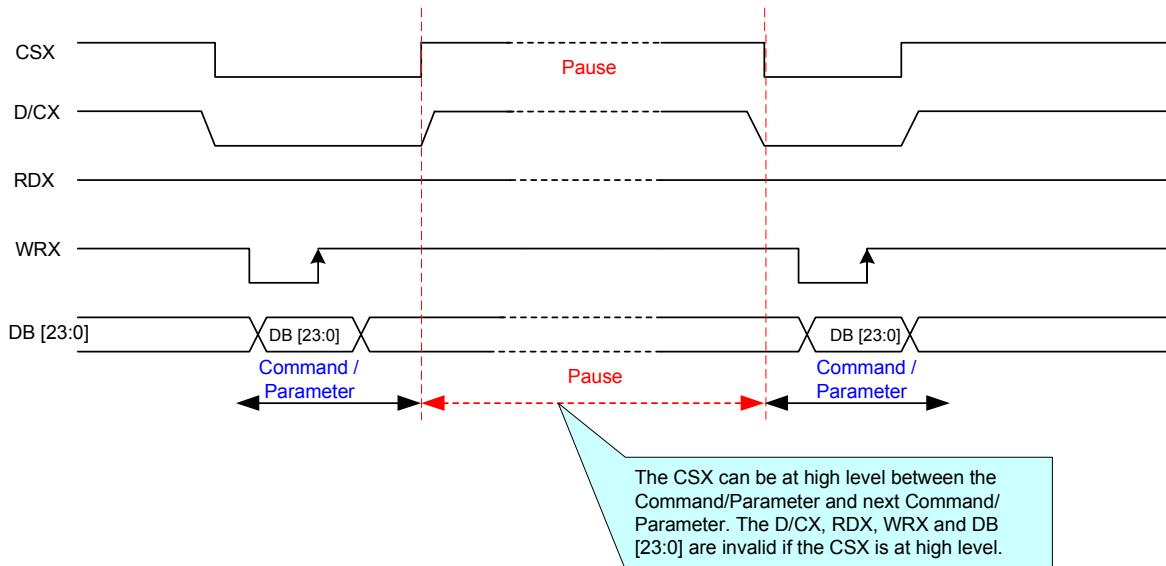


Figure 16: DBI Type B Data Transfer Pause

This applies to the following 4 conditions:

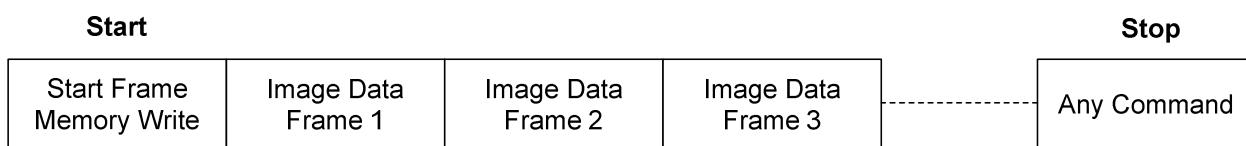
- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

4.4. Data Transfer Mode

The ILI9488 can provide five different kinds of color depth (8-bit/pixel, 9-bit/pixel, 16-bit/pixel, 18-bit/pixel, and 24-bit/pixel) for display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

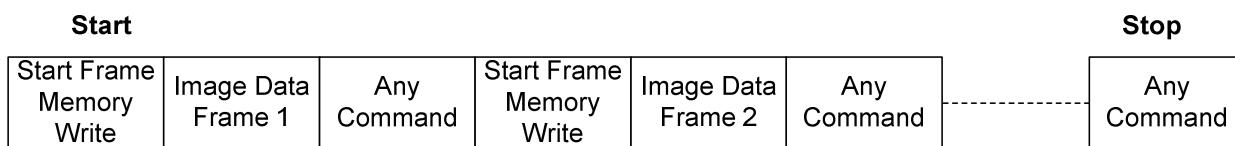
4.4.1. Method 1

The image data is sent to the Frame Memory in the successive Frame writing. Each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and then the next Frame is written.



4.4.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is then sent to stop Frame Memory Writing. Then the Start Memory Write command is sent, and a new Frame is downloaded.



Notes:

1. These two methods can apply to all five kinds of color depth on both serial and parallel interfaces.
2. The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.5.DPI Parallel Interface (RGB Interface)

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM (bypass GRAM) and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

| BPGRAM | Display Data Path |
|--------|--------------------------|
| 1 | Direct to shift register |
| 0 | Write into Memory |
| RM | Interface for RAM access |
| 0 | System interface |
| 1 | RGB interface |

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DOTCLK cannot be stopped unless it enters the Sleep-In mode.

| DM | RGB Interface Operating Clock Selection |
|----|---|
| 0 | Internal system clock |
| 1 | RGB interface (DOTCLK) |

4.5.1. RGB Interface Selection

The DPI can be selected by the RCM bit. When the RCM is set to 0, the DE mode is selected by VSYNC, HSYNC, DOTCLK, ENABLE, and DB [23:0] pins. When RCM is set to 1, the SYNC mode is selected by VSYNC, HSYNC, DOTCLK, and DB [23:0] pins. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in Table 6 and Figure 17.

Table 6: DPI Interface Selection

| RCM | DPI [2:0] | | | RGB Interface Mode | RGB Mode | Used Pins |
|-----|-----------|---|---|-------------------------------------|---|---|
| 0 | 1 | 1 | 1 | 24-bit RGB interface (16.7M colors) | DE Mode Valid data is determined by the ENABLE signal. | VSYNC, HSYNC, ENABLE, DOTCLK, DB [23:0] |
| 0 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, ENABLE, DOTCLK, DB [17:0] |
| 0 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | | VSYNC, HSYNC, ENABLE, DOTCLK, DB [15:0] |
| 1 | 1 | 1 | 1 | 24-bit RGB interface (16.7M colors) | SYNC Mode In the SYNC mode, ENABLE signal is ignored; blanking porch is determined by B5h command. | VSYNC, HSYNC, DOTCLK, DB [23:0] |
| 1 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, DOTCLK, DB [17:0] |
| 1 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | | VSYNC, HSYNC, DOTCLK, DB [15:0] |

24-bit DPI interface connection (DB [23:0] is used): set pixel format DPI [2:0] = 3'h7

| | | | | | | | | | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

| | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| | | | | | | | | | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | | | | |
| | | | | | | | | | | | | | | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0] |

Figure 17: DPI Interface 24/18/16 Pixel Format Selection

The Pixel clock (DOTCLK) runs all the time without stop. It is used to enter VSYNC, HSYNC, ENABLE and DB [23:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DOTCLK signal.

DB [23:0] is used to indicate what is the information of the image that is transferred on the display (when ENABLE = 0 (low) and there is a rising edge of DOTCLK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

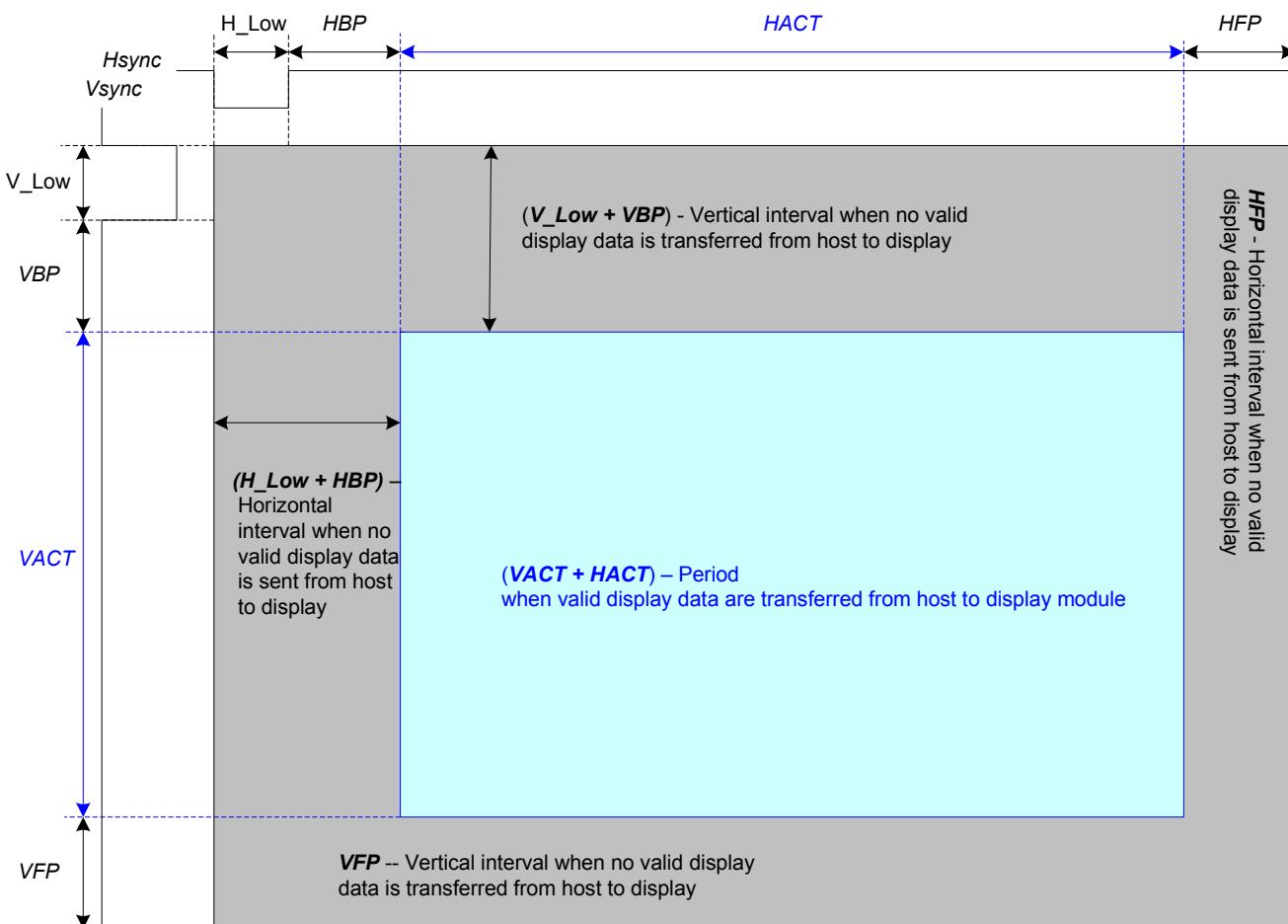


Figure 18: General DPI Timing Diagram

| Parameters | Symbols | Min. | Typ. | Max. | Units |
|----------------------------|---------|------|------|------|--------|
| Horizontal Synchronization | H_Low | 3 | - | - | DOTCLK |
| Horizontal Back Porch | HBP | 3 | - | - | DOTCLK |
| Horizontal Address | HACT | - | 320 | - | DOTCLK |
| Horizontal Front Porch | HFP | 3 | - | - | DOTCLK |
| Horizontal Frequency | | - | - | 33 | KHz |
| Vertical Synchronization | V_Low | 1 | - | - | Line |
| Vertical Back Porch | VBP | 2 | - | - | Line |
| Vertical Address | VACT | - | 480 | - | Line |
| Vertical Front Porch | VFP | 2 | - | - | Line |
| Vertical Frequency | | 60 | - | 70 | Hz |
| DOTCLK cycle | | 100 | - | 50 | ns |
| DOTCLK Frequency | | 10 | - | 20 | MHz |

Example : DOTCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

4.5.2. RGB Interface Timing

The timing chart of 16-/18-/24-bit DPI interface mode is illustrated in Figure 19.

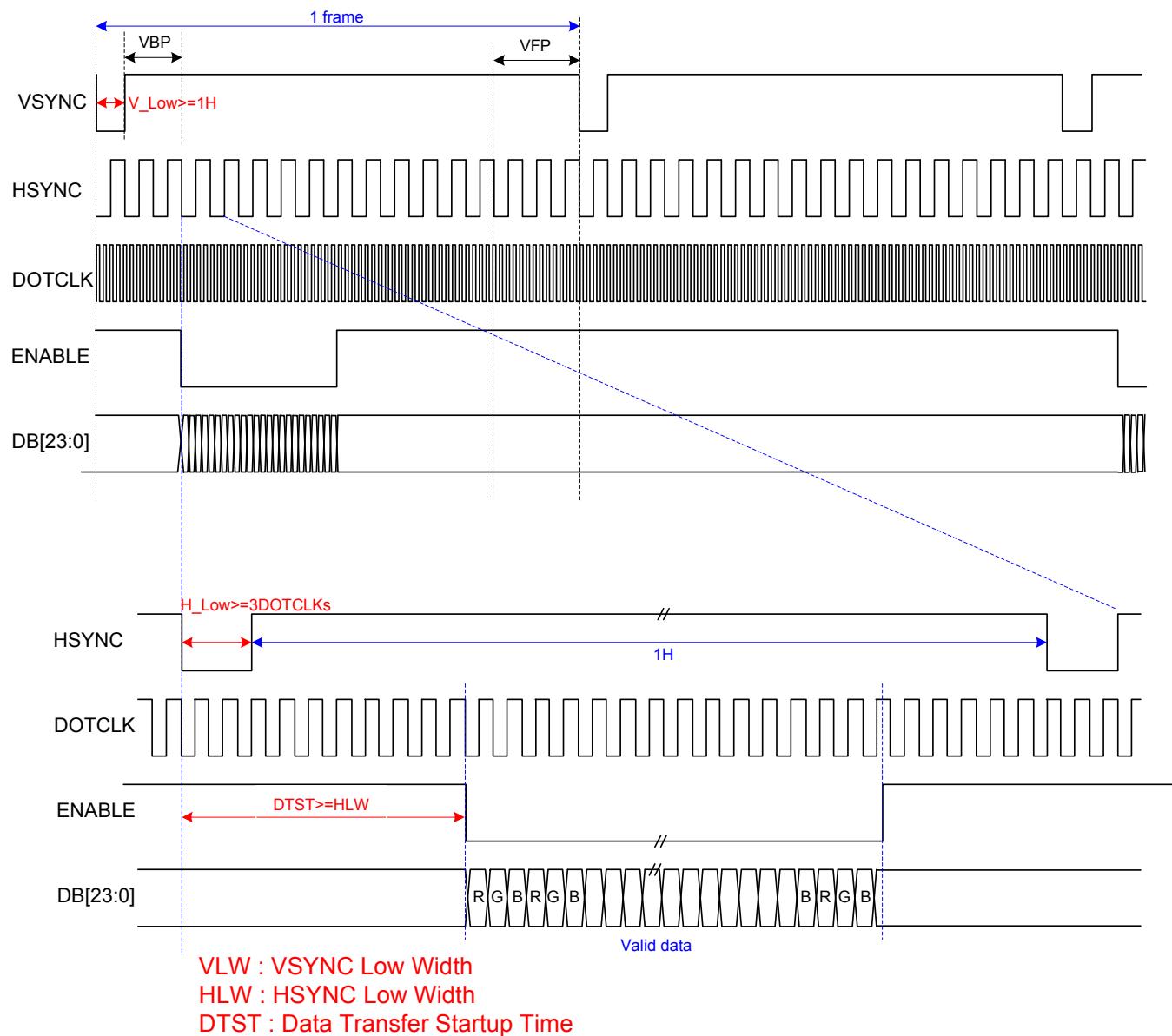


Figure 19: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

4.6.DSI System Interface

4.6.1. General Description

The MIPI-DSI is enabled or disabled by the external IM [2:0] pin.

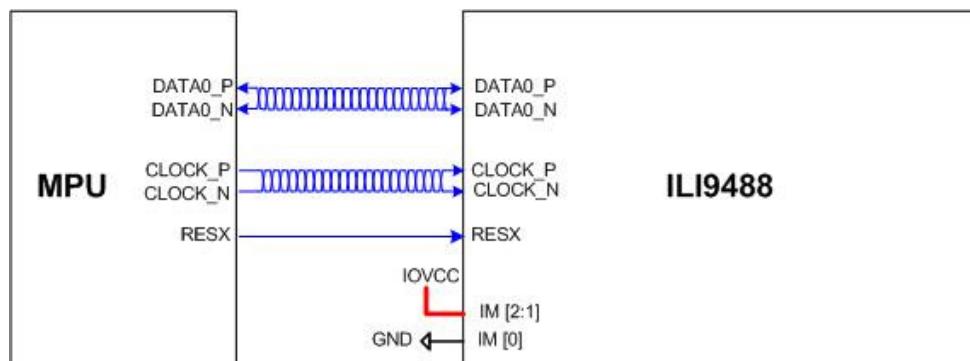


Figure 20: DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- ◆ Low level communication is done on the interface level.
- ◆ High level communication is done on the packet level.

4.6.2. Interface Level Communication

4.6.2.1. General

The display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in the single ended mode, and a differential receiver is disable (the termination resistor of the receiver is disable), and it can be driven into a low power mode. High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode. Different modes and protocols are used in each mode when information is to be transferred from the MCU to the display module and vice versa. The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 7: High Speed and Low Power Lane Pair State Codes

| Lane Pair State Code | Line DC Voltage Levels | | High Speed (HS) | Low Power | |
|----------------------|------------------------|-----------|------------------|--------------|----------|
| | DATA_P | DATA_N | | CLOCK_P | CLOCK_N |
| HS-0 | Low (HS) | High (HS) | Differential – 0 | Note 1 | Note1 |
| HS-1 | High (HS) | Low (HS) | Differential – 1 | Note 1 | Note 1 |
| LP-00 | Low (LP) | Low (LP) | Not Defined | Bridge | Space |
| LP-01 | Low (LP) | High (LP) | Not Defined | HS – Request | Mark - 0 |
| LP-10 | High (LP) | Low (LP) | Not Defined | LP - Request | Mark - 1 |
| LP-11 | High (LP) | High (LP) | Not Defined | Stop | Note 2 |

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

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2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair will return to LP-11 of the Control Mode.

4.6.2.2. MIPI_CLOCK Lanes

MIPI_CLOCK_P/N lanes can be driven into three different power modes:

- ◆ Low Power Mode (LPM)
- ◆ Ultra Low Power Mode (ULPM)
- ◆ High Speed Clock Mode (HSCM)

Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different clock lanes power modes is illustrated below.

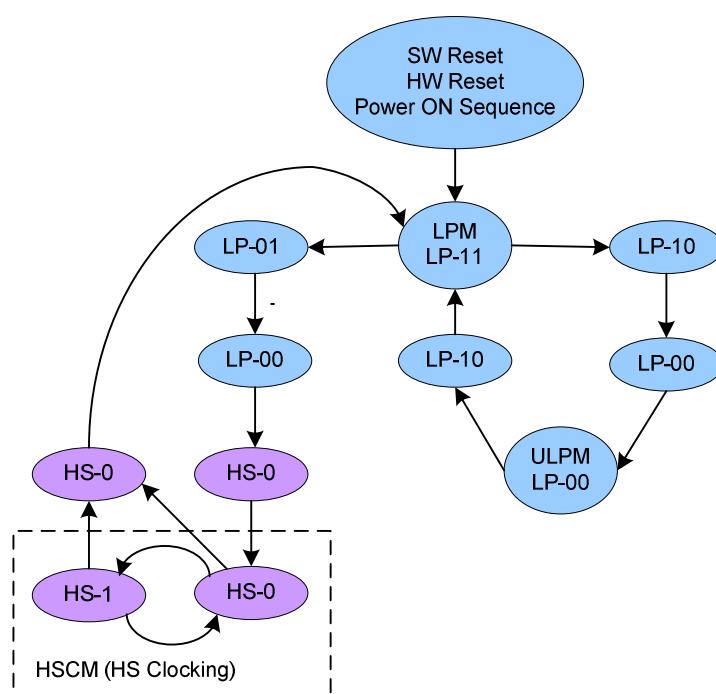


Figure 21: Clock Lanes Power Mode

4.6.2.2.1. Low Power Mode (LPM)

MIPI_CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when MIPI_CLOCK lanes enter the LP-11 State Code, in three different ways:

- (1) After SW Reset, HW Reset or Power On Sequence => LP-11
- (2) After MIPI_CLOCK_P/N lanes leave the Ultra Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11

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(LPM).

This sequence is illustrated below.

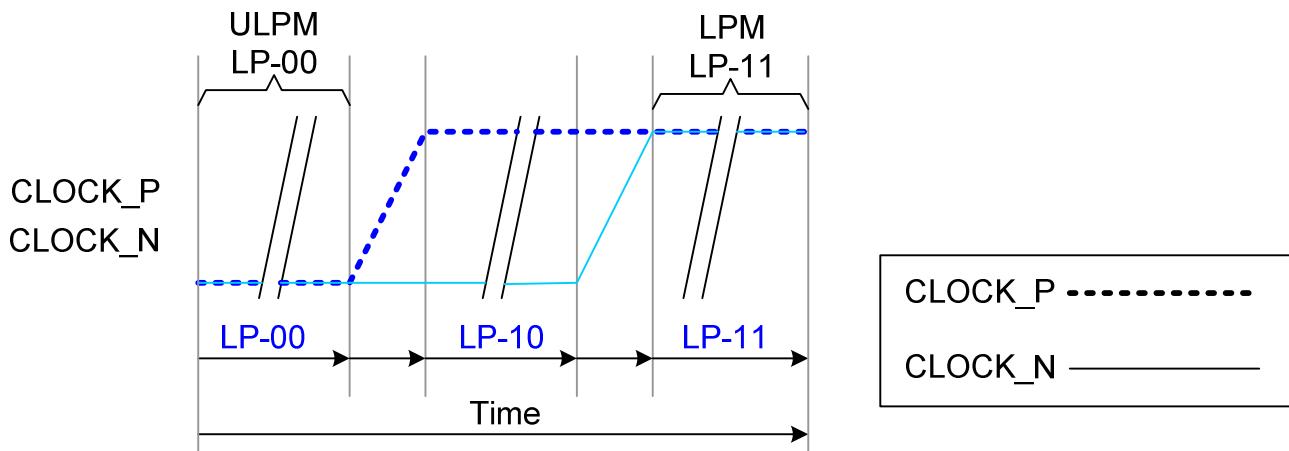


Figure 22: From ULPM to LPM

- (3) After MIPI_CLOCK_P/N lanes leave the High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0 => LP-11 (LPM).

This sequence is illustrated below.

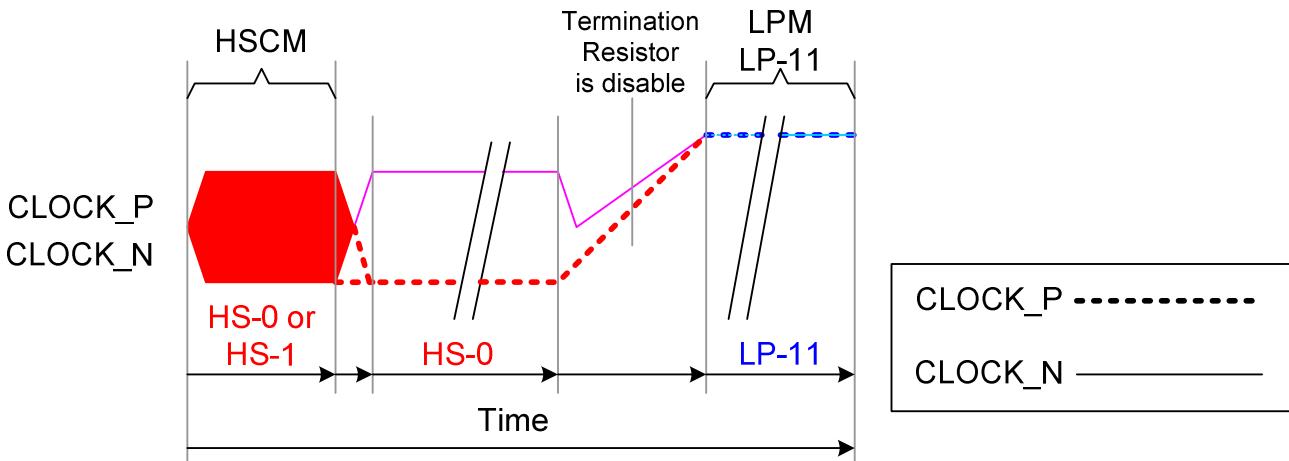


Figure 23: From High Speed Clock Mode (HSCM) to LPM

All changes of the three modes are illustrated in the flow chart below.

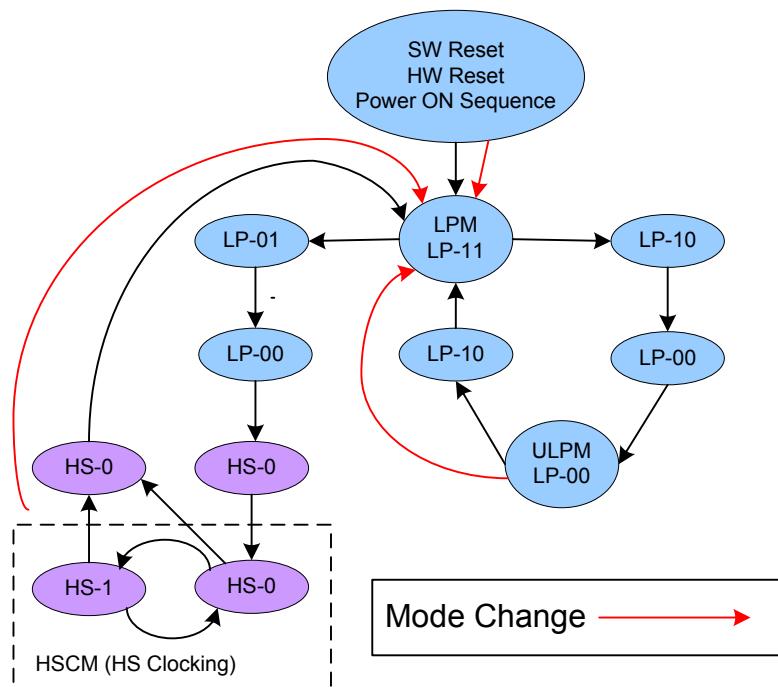


Figure 24: All Changes of the Three Modes to LPM

4.6.2.2.2. Ultra Low Power Mode (ULPM)

MIPI_CLOCK_P/N lanes can be driven to the Ultra Low Power Mode (ULPM) when MIPI_CLOCK lanes enter the LP-00 State Code. The only possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

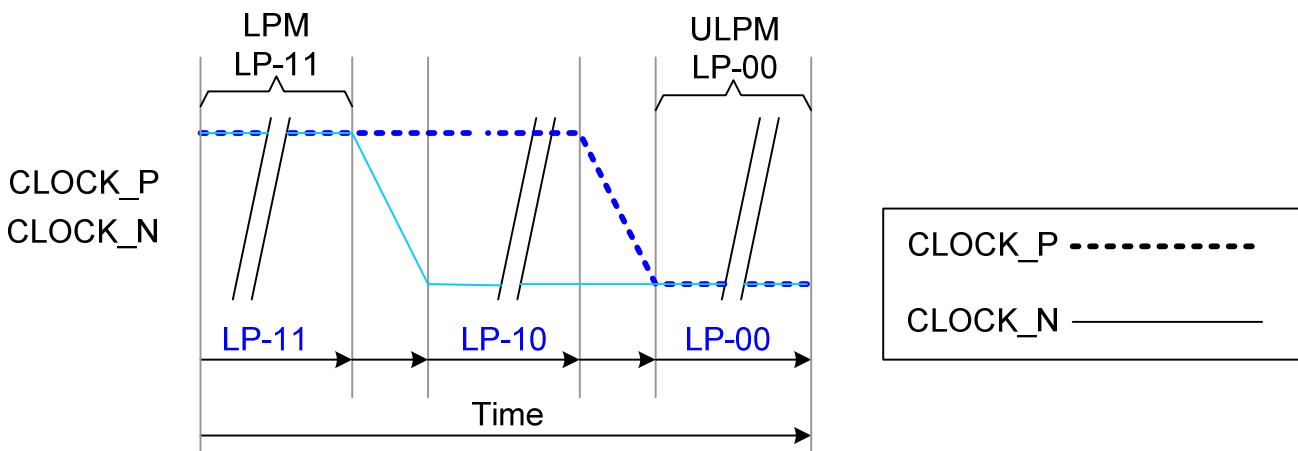


Figure 25: From LPM to ULPM

The mode change is also illustrated below.

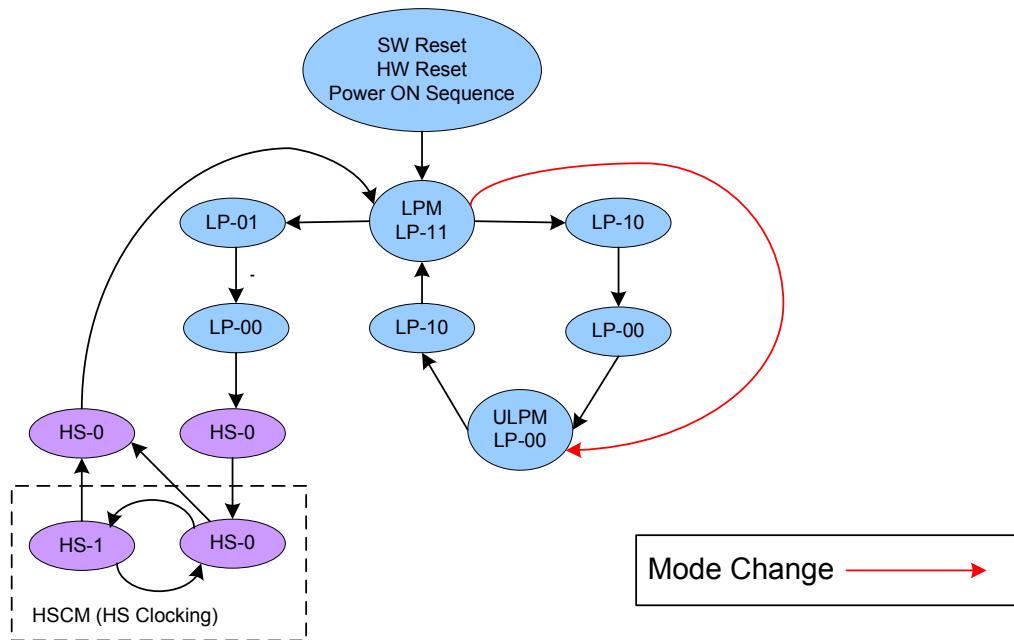


Figure 26: Mode Change from LPM to ULPM

4.6.2.2.3. High-Speed Clock Mode (HSCM)

MIPI_CLOCK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when MIPI_CLOCK lanes start to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

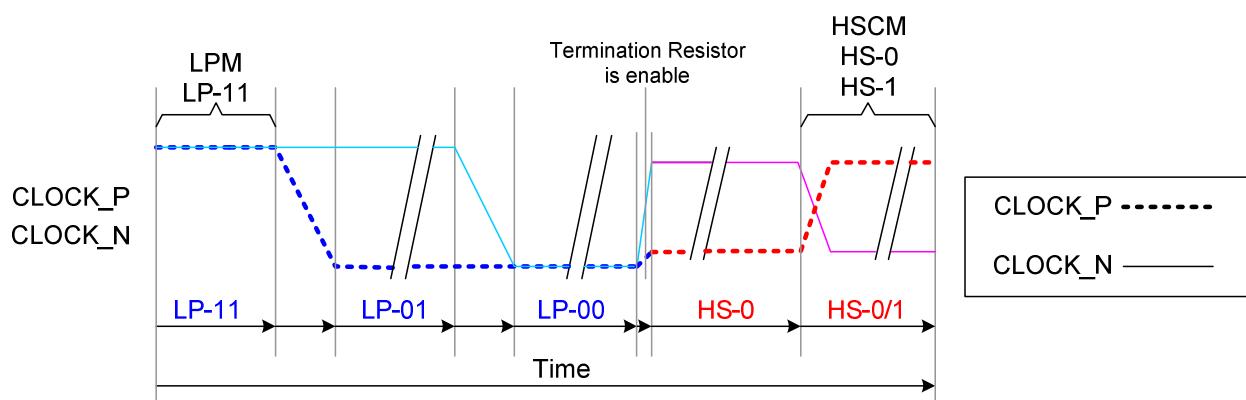


Figure 27: From LPM to HSCM

The mode change is also illustrated below.

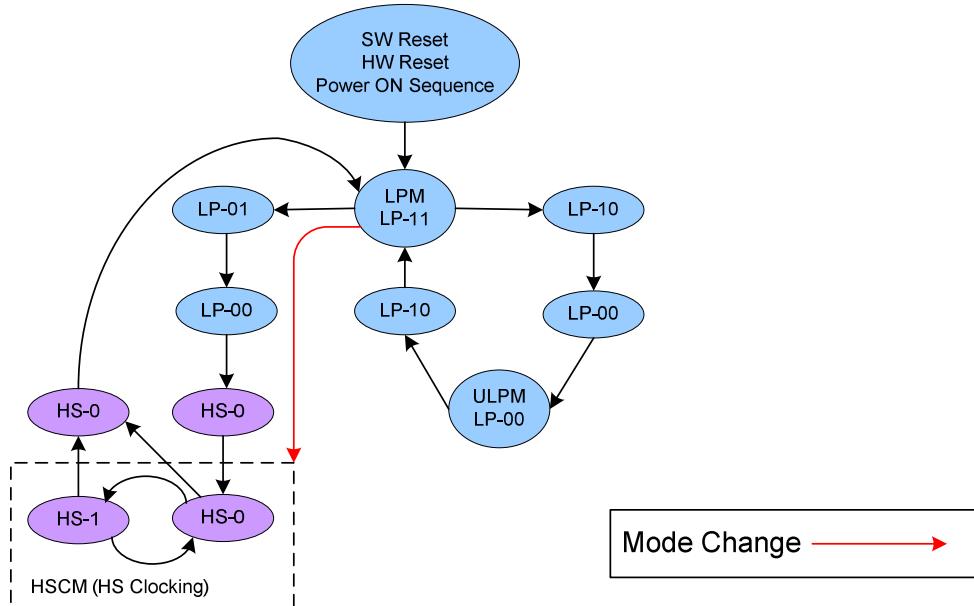
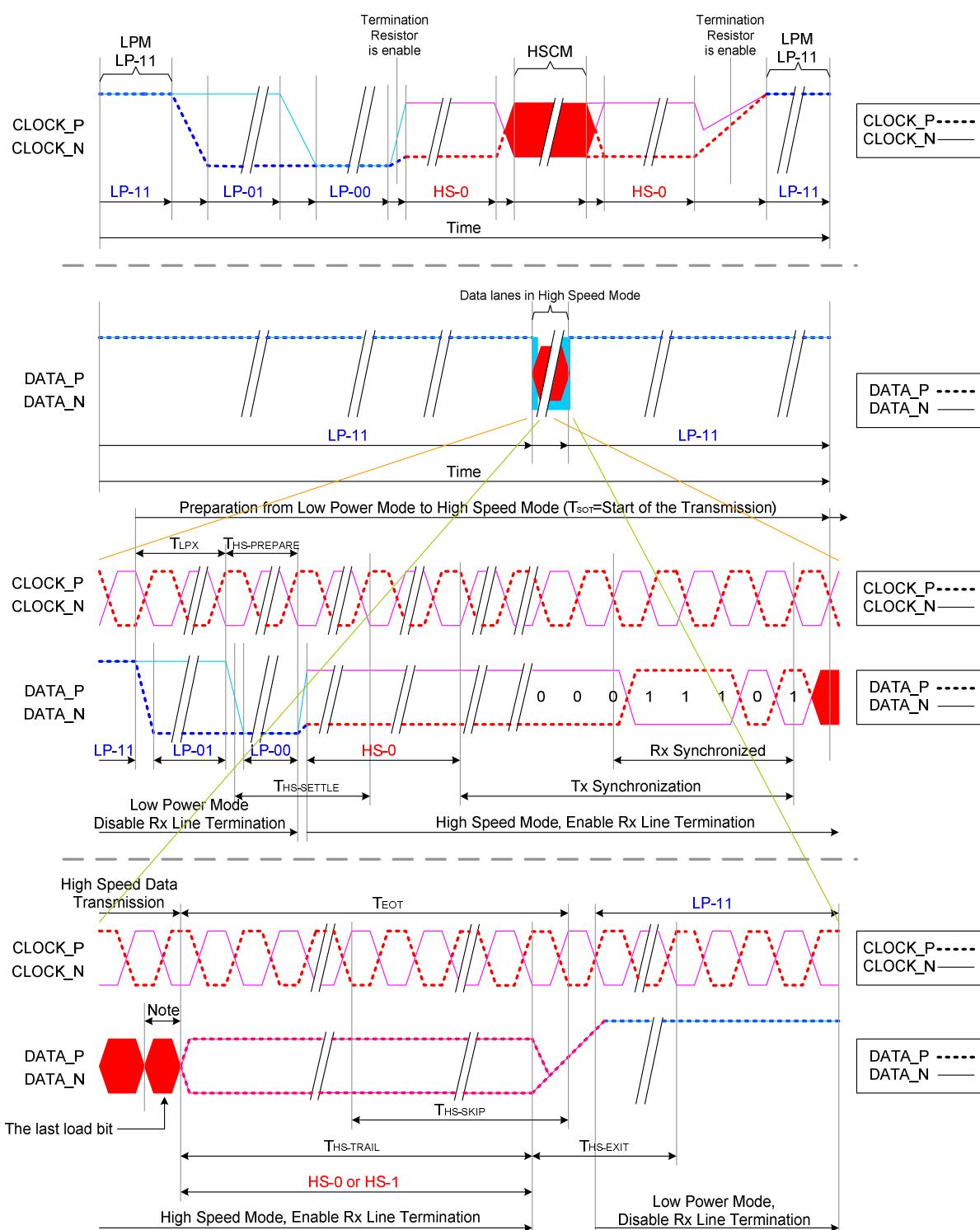


Figure 28: Mode Change from LPM to HSCM

The high speed clock (MIPI_CLOCK_P/N) starts before high speed data is sent via MIPI_DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- ◆ Even number of transitions
- ◆ Start state is HS-0
- ◆ End state is HS-0


Figure 29: High Speed Clock Burst
Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.6.2.3. MIPI_DATA Lanes

4.6.2.3.1. General

MIPI_DATA_P/N Data Lanes can be driven in different modes:

- ◆ Escape Mode
- ◆ High-Speed Data Transmission
- ◆ Bus Turnaround Request

These modes and their entering codes are defined in the following table.

Table 8: Entering and Leaving Sequence

| Mode | Entering Mode Sequence | Leaving Mode Sequence |
|------------------------------|---------------------------------------|--------------------------------|
| Escape Mode | LP-11 → LP-10 → LP-00 → LP-01 → LP-00 | LP-00 → LP-10 → LP-11 (Mark-1) |
| High-Speed Data Transmission | LP-11 → LP-01 → LP-00 → HS-0 | (HS-0 or HS-1) → LP-11 |
| Bus Turnaround Request | LP-11 → LP-10 → LP-00 → LP-10 → LP-00 | Hi-Z |

4.6.2.3.2. Escape Modes

Data lanes (MIPI_DATA_P/N) can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

These Escape Modes are used to:

- ◆ Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- ◆ Drive data lanes to “Ultra-Low Power State” (ULPS),
- ◆ Indicate “Remote Application Reset” (RAR), which can reset the display module,
- ◆ Indicate “Tearing Effect” (TEE), which is used to transmit a TE line event from the display module to the MCU,
- ◆ Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Escape Command (EC), which is coded when one of the data lanes changes from low-to-high-to-low, then this changed data lane presents the value of the current data bit (MIPI_DATA_P = 1, MIPI_DATA_N = 0). For example, when MIPI_DATA_N changes from low-to-high-to-low, the receiver latches a data bit, which value is the logical 0. The receiver uses this low-to-high-to-low transition for its internal clock.
- ◆ A load if necessary
- ◆ Exit Escape (Mark-1): LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This basic construction is illustrated below:

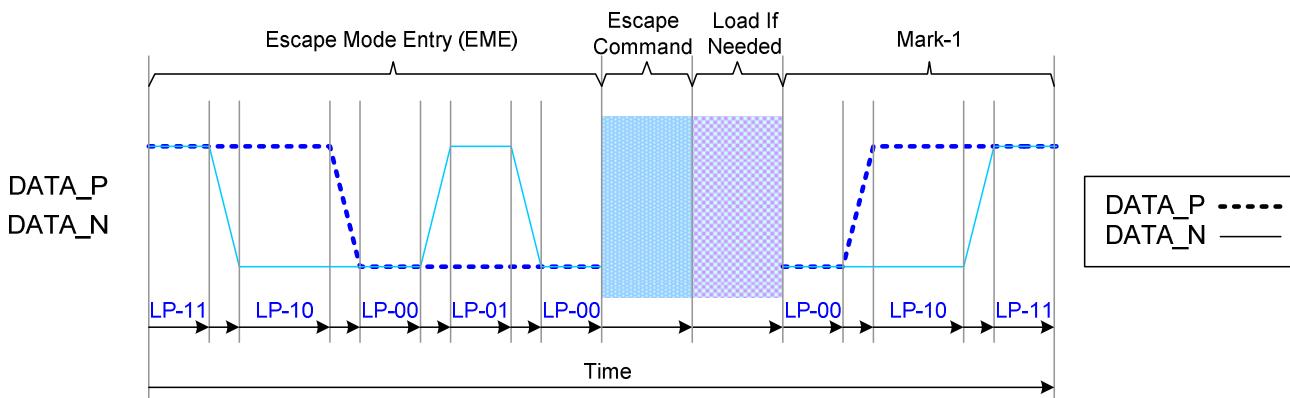


Figure 30: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as described in Table 9.

An example of Mode Type Escape Commands is Ultra-Low Power Mode, by which the MCU instructs the display module how to enter its Ultra-Low Power Mode.

An example of Trigger type Escape Commands is Tearing Effect. In this case, the MCU has already instructed the display module to provide the TE trigger and is waiting for a response. The display module will then send a TE Trigger (TEE) on the next V-sync event.

Table 9: Escape Commands

| Escape command | Command Type Mode/Trigger | Entry command Pattern (First → Last Bit Transmitted) |
|-----------------------------|---------------------------|---|
| Low-Power Data Transmission | Mode | 1110 0001 b |
| Ultra-Low Power Mode | Mode | 0001 1110 b |
| Undefined-1 ^{Note} | Mode | 1001 1111 b |
| Undefined-2 ^{Note} | Mode | 1101 1110 b |
| Remote Application Reset | Trigger | 0110 0010 b |
| Tearing Effect | Trigger | 0101 1101 b |
| Acknowledge | Trigger | 0010 0001 b |
| Unknown-5 ^{Note} | Trigger | 1010 0000 b |

Note: This Escape Command is not implemented in the display module.

4.6.2.3.2.1 Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and the Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module uses the same sequence as which it sends data to the MCU.

The Low Power Data Transmission (LPDT) uses the following sequence:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- ◆ Load (Data):
 - ◊ One or more bytes (one byte = 8 bit)
 - ◊ Data lanes are in the pause mode when data lanes are stopped (both lanes are low) between bytes
- ◆ Mark-1: LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This sequence is illustrated below for reference purpose:

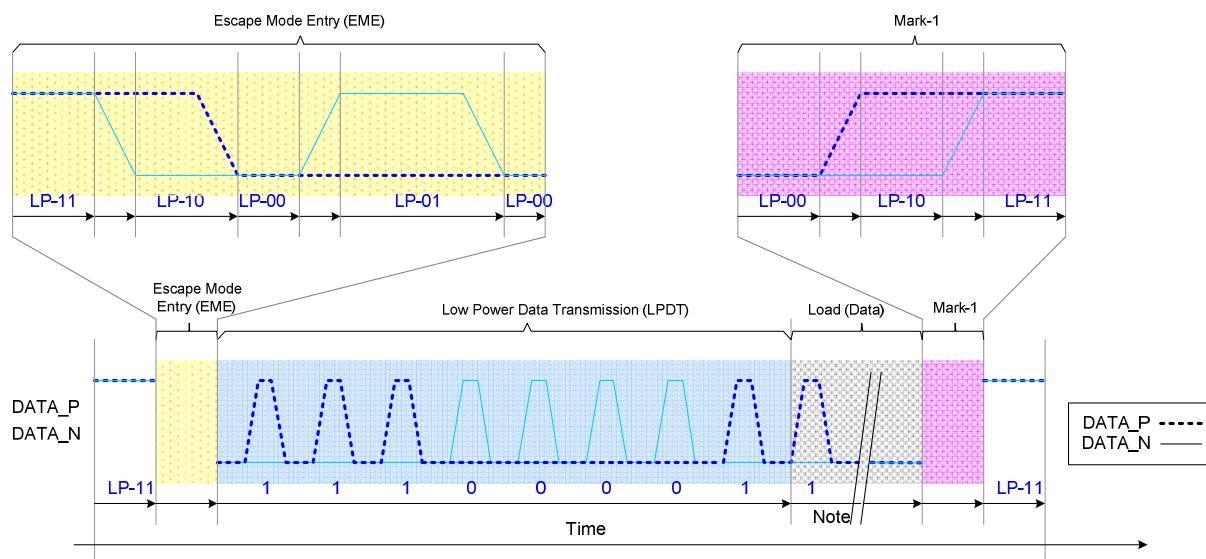


Figure 31: Low-Power Data Transmission (LPDT)

Note: Load (Data) presents that the first bit is the logical 1 in this example.

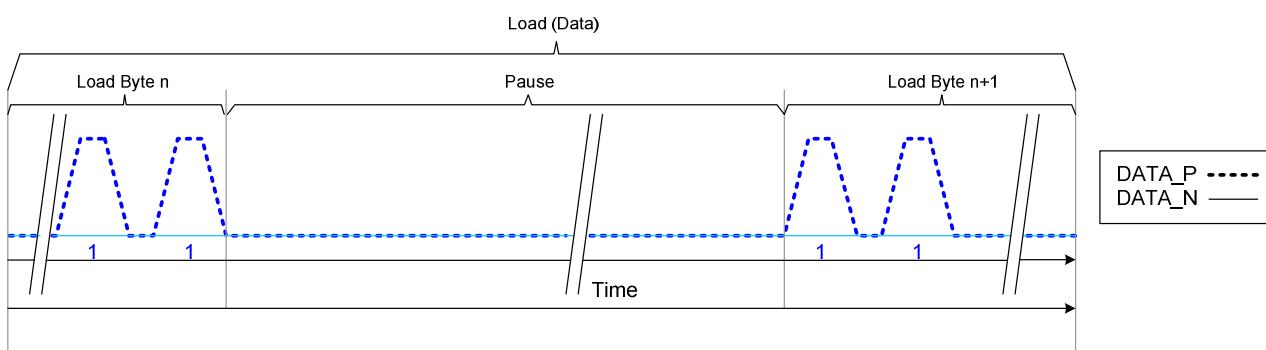


Figure 32: Pause (Example)

4.6.2.3.2.2 Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode.

The Ultra-Low Power State (ULPS) uses the following sequence:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (first to last bit)
- ◆ Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- ◆ Mark-1: LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This sequence is illustrated below for reference purpose:

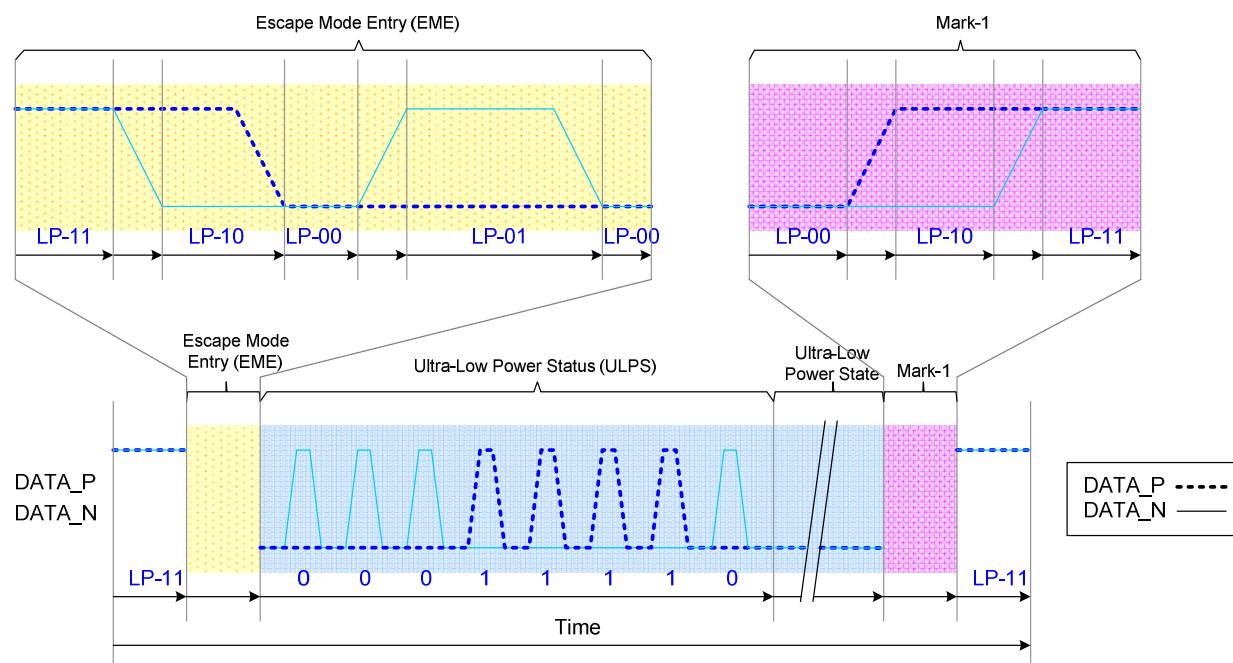


Figure 33: Ultra-Low Power State (ULPS)

4.6.2.3.2.3 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode.

The Remote Application Reset (RAR) uses the following sequence:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- ◆ Mark-1: LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This sequence is illustrated below for reference purpose:

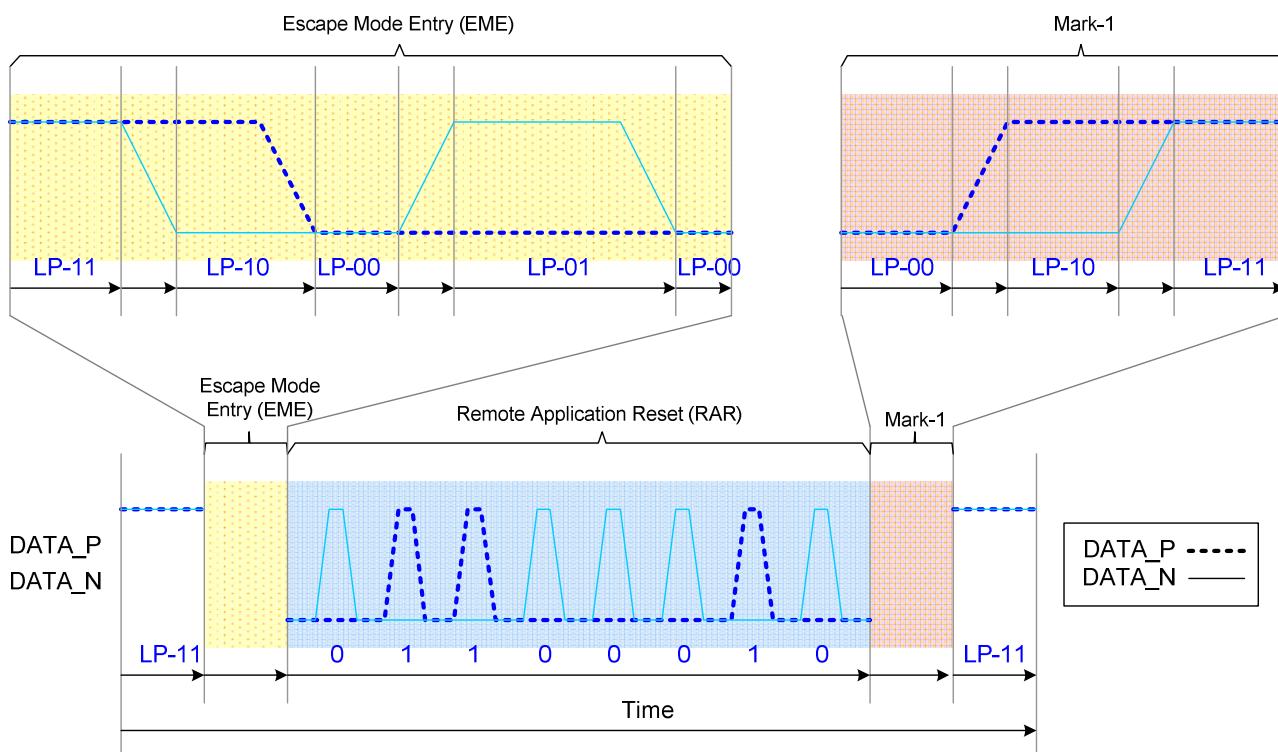


Figure 34: Remote Application Reset (RAR)

4.6.2.3.2.4 Tearing Effect (TEE)

The display module can inform the MCU by Tearing Effect (TEE) when a tearing effect event (New V-synch) has happened on the display module.

The display module sends the Tearing Effect (TEE) with the following sequence:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Tearing Effect (TEE) trigger in the Escape Mode: 0101 1101 (first to last bit)
- ◆ Mark-1: LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This sequence is illustrated below for reference purpose:

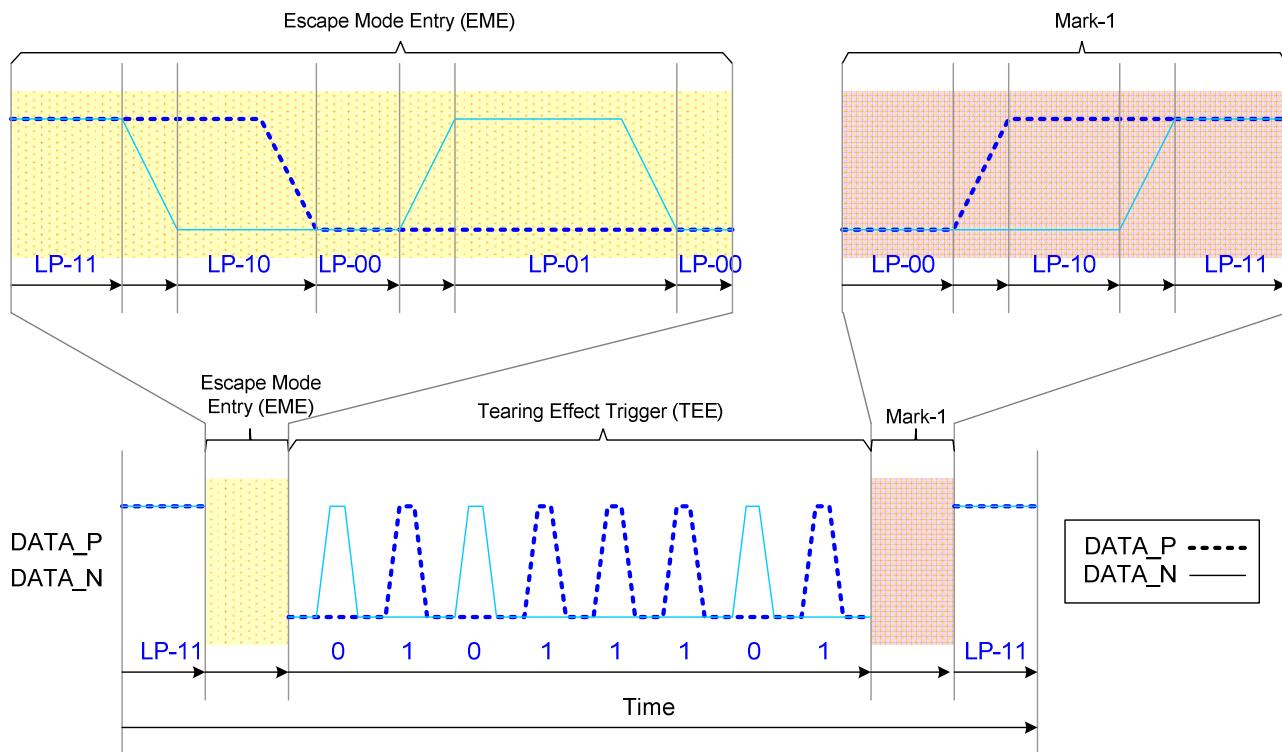


Figure 35: Tearing Effect (TEE)

4.6.2.3.2.5 Acknowledge (ACK)

The ILI9488 can inform the MCU that no errors are found by the Acknowledge (ACK).

The display module sends the Acknowledge (ACK) with the following sequence:

- ◆ Start: LP-11
- ◆ Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- ◆ Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- ◆ Mark-1: LP-00 => LP-10 => LP-11
- ◆ End: LP-11

This sequence is illustrated below for reference purpose:

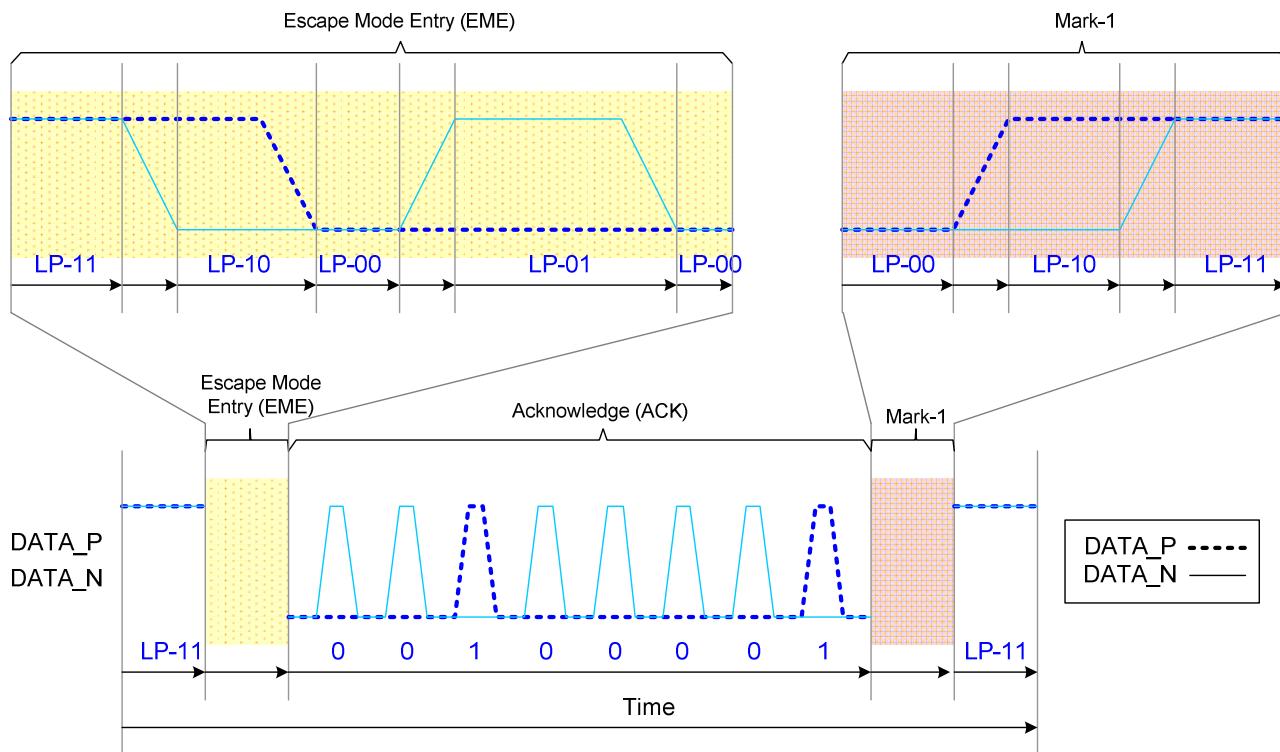


Figure 36: Acknowledge (ACK)

4.6.2.3.3. High-Speed Data Transmission (HSDT)

4.6.2.3.3.1 Enter High-Speed Data Transmission (T_{SOT} of HSDT)

The display module will enter High-Speed Data Transmission (HSDT) when Clock lanes MIPI_CLOCK_P/N have already entered the High-Speed Clock Mode (HSCM) through the MCU.

Data lanes MIPI_DATA_P/N of the display module enter (T_{SOT}) in the High-Speed Data Transmission (HSDT) with the following sequence:

- ◆ Start: LP-11
- ◆ HS-Request: LP-01
- ◆ HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- ◆ Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- ◆ End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The entering sequence of High-Speed Data Transmission (T_{SOT} of HSDT) is illustrated below:

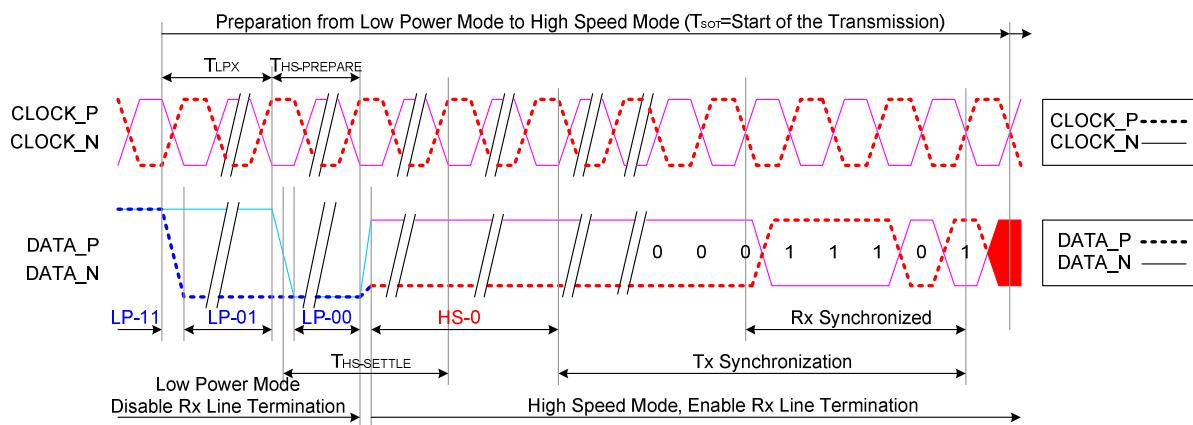


Figure 37: Entering High-Speed Data Transmission (T_{SOT} of HSDT)

4.6.2.3.3.2 Leave High-Speed Data Transmission (TEOT of HSDT)

The display module will leave the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes MIPI_CLOCK_P/N enter the High-Speed Clock Mode (HSCM) through the MCU. This HSCM is kept until data lanes MIPI_DATA_P/N of the display module leave the High-Speed Data Transmission (T_{EOT} of HSDT) with the following sequence:

- ◆ Start: High-Speed Data Transmission (HSDT)
- ◆ Stop High-Speed Data Transmission
 - ◊ MCU changes to HS-1 if the last load bit is HS-0
 - ◊ MCU changes to HS-0 if the last load bit is HS-1
- ◆ End: LP-11 (Rx: Lane Termination Disable)

The leaving sequence of High-Speed Data Transmission (T_{EOT} of HSDT) is illustrated below:

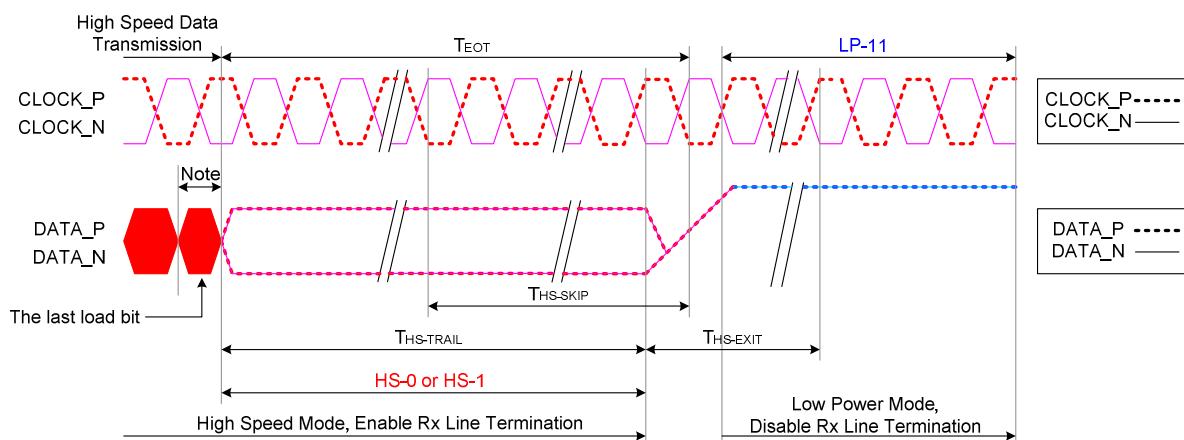


Figure 38: Leaving High-Speed Data Transmission

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.6.2.3.3.3 Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the chapter “Short Packet (SPa) and Long Packet (LPa) Structures”.

The single packet in High-Speed Data Transmission is illustrated below for reference purpose:

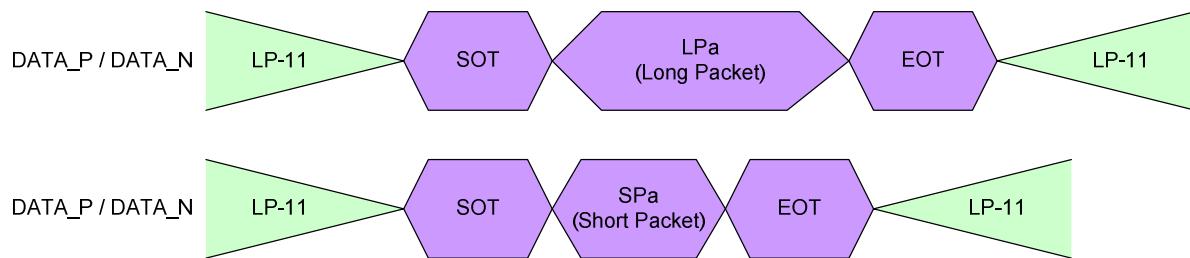


Figure 39: Single Packet in High-Speed Data Transmission

The multiple packets in High-Speed Data Transmission are illustrated below for reference purpose:

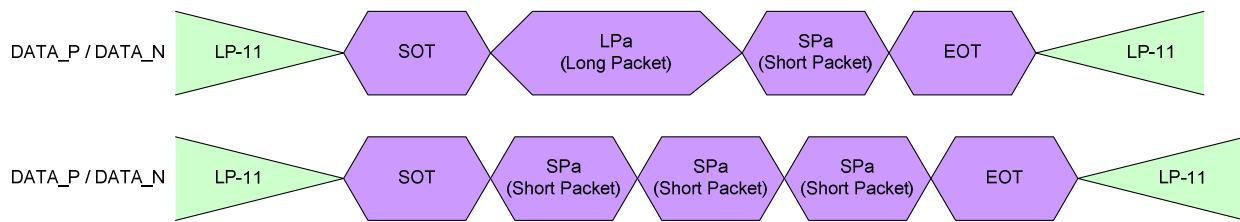


Figure 40: Multiple Packets in High-Speed Data Transmission (Examples)

Table 10: Abbreviations

| Abbreviation | Explanation |
|--------------|--|
| EOT | End of the Transmission |
| LPa | Long Packet |
| LP-11 | Low Power Mode, both of Data lanes are 1 (Stop Mode) |
| SPa | Short Packet |
| SOT | Start of the Transmission |

4.6.2.3.3.4 Bus Turnaround (BTA)

The MCU or the display module, which controls MIPI_DATA_P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or the display module. The MCU and the display module use the same sequence when this bus turnaround procedure is applied. The sequence when the MCU wants to perform the bus turnaround procedure to the display module is described below for reference purpose:

- ◆ Start (MCU): LP-11
- ◆ Turnaround Request (MCU): LP-11 => LP-10 => LP-00=> LP-10=> LP-00
- ◆ The MCU waits until the display module starts to control MIPI_DATA_P/N data lanes and the MCU stops to

- control MIPI_DATA_P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

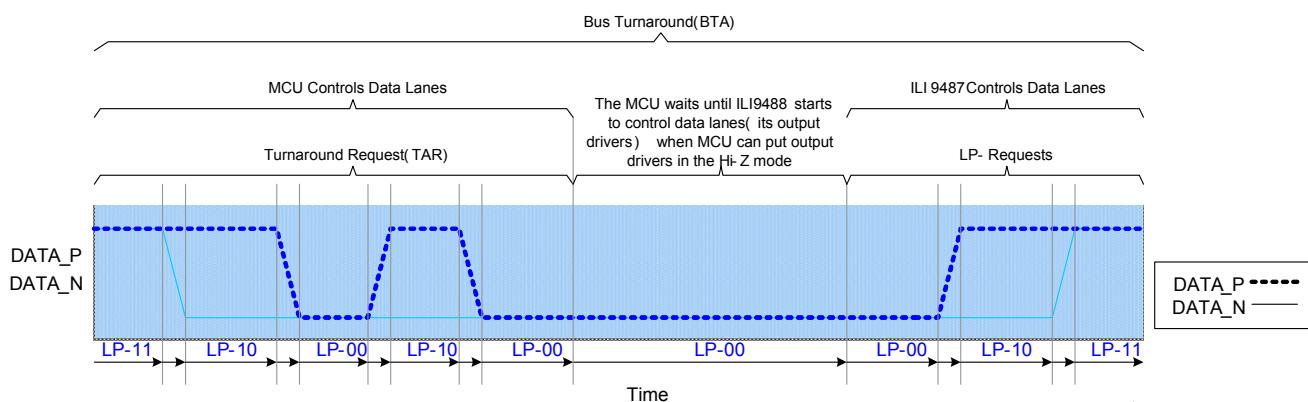


Figure 41: Bus Turnaround Procedure

MCU and display module can be switched in Figure 41 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.6.3. Packet Level Communication

4.6.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type of the packet (SPa or LPa) can be recognized from their package headers (PH).

The Short Packet structure is illustrated as below:

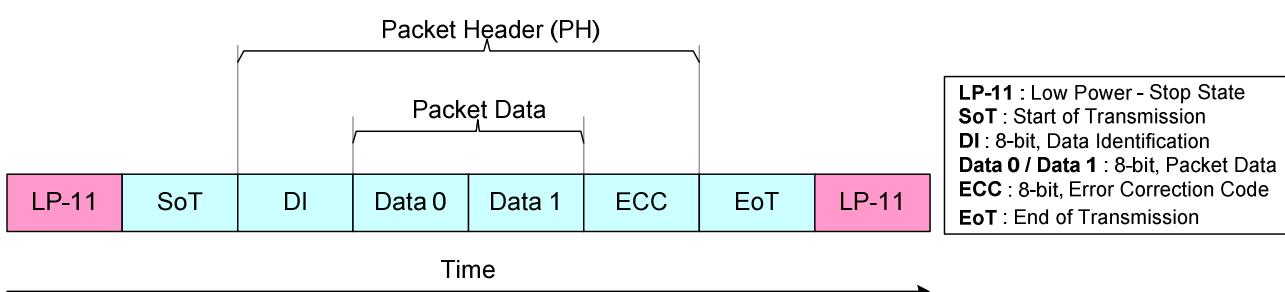


Figure 42: Short Packet (SPa) Structure

The Long Packet structure is illustrated as below:

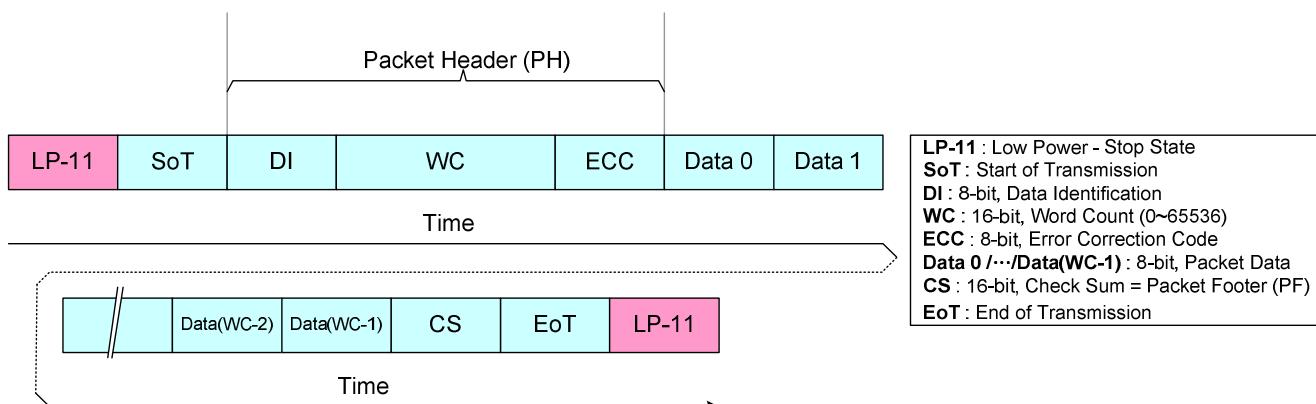


Figure 43: Long Packet (LPa) Structure

Note: Figure 42 and Figure 43 present a single packet sending (= including LP-11, SoT and EoT for each packet sending).

The other possibility is that SoT, EoT and LP-11 between packets are not necessary if packets are sent in multiple packet formats, for example:

- ◆ LP-11 => SoT => SPa => LPa => SPa => EoT => LP-11
- ◆ LP-11 => SoT => SPa => SPa => EoT => LP-11
- ◆ LP-11 => SoT => LPa => LPa => EoT => LP-11

4.6.3.1.1. Bit Order of Bytes in Packets

The bit order of bytes, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first and the Most Significant Bit (MSB) of the byte is sent last.

This sending order is illustrated below for reference purpose.

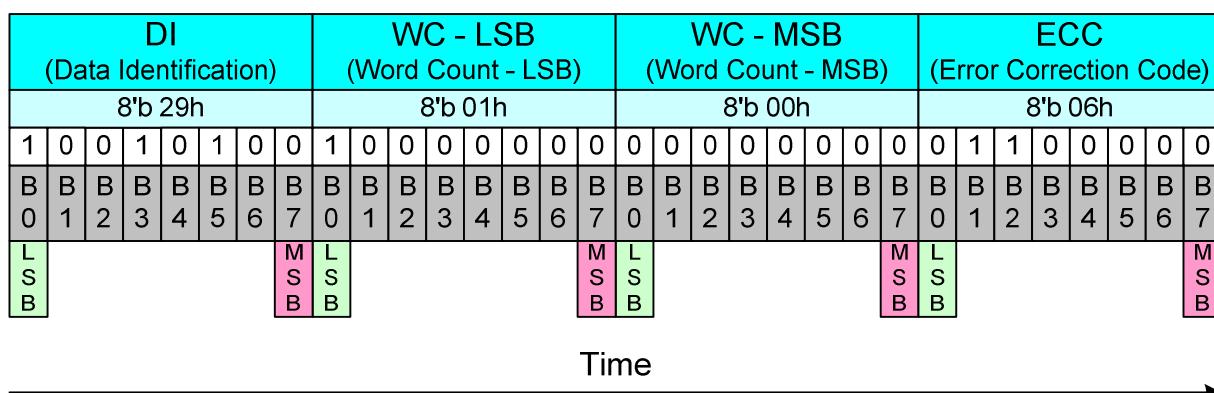


Figure 44: Bit Order of Bytes in Packets

4.6.3.1.2. Byte Order of Multiple Byte Information in Packets

Byte order of multiple byte information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte of the information is sent last. For example, word Count (WC) consists of 2 bytes (= 16 bits), and the LS byte is sent first and the MS byte last.

This order is illustrated below for reference purpose.

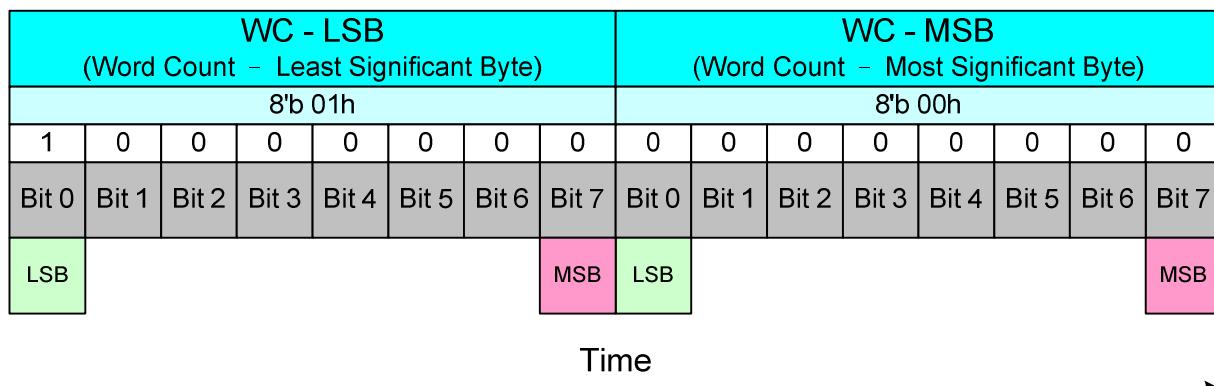


Figure 45: Byte Order of Multiple Byte Information in Packets

4.6.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa)

- 1st byte: Data Identification (DI) => identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

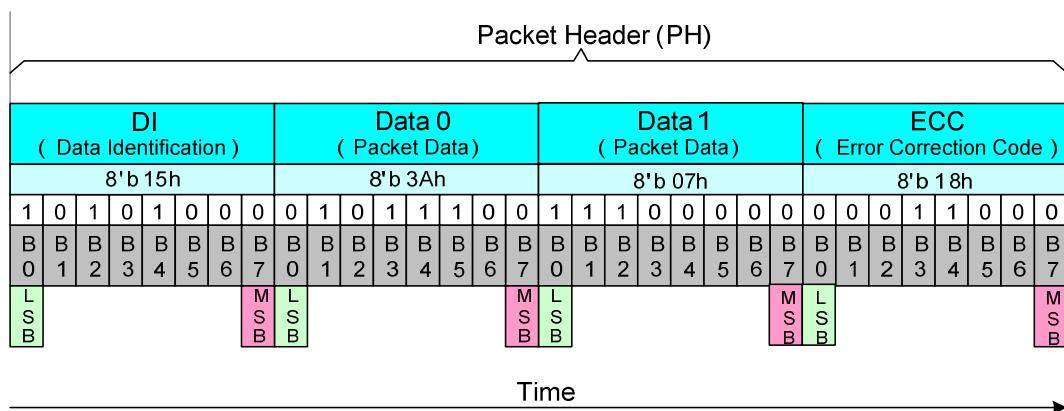
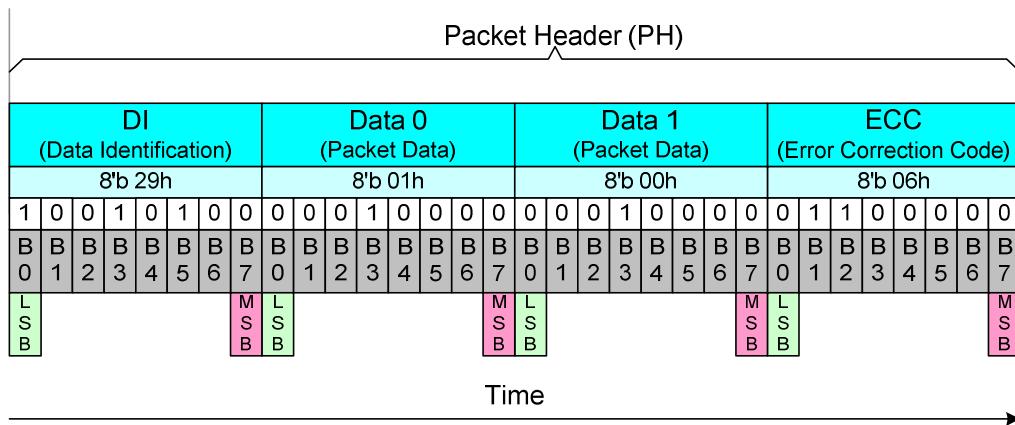


Figure 46: Packet Header (PH) of Short Packet

Long Packet (LPa):

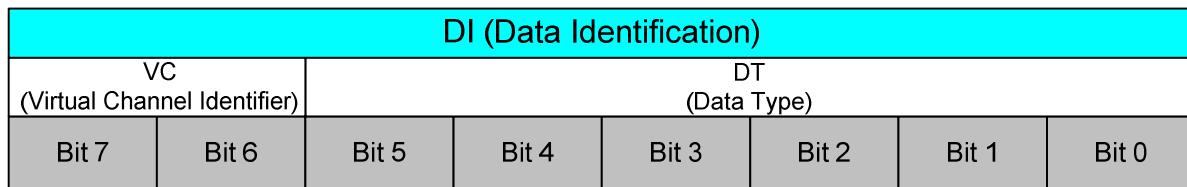
- 1st byte: Data Identification (DI) => identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)


Figure 47: Packet Header (PH) of Long Packet
4.6.3.1.3.1 Data Identification (DI)

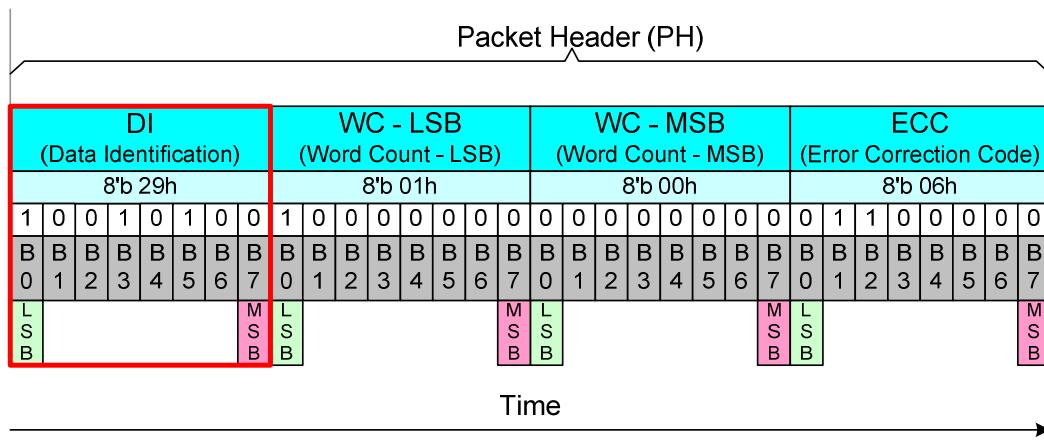
Data Identification (DI) is part of the Packet Header (PH) and it consists of 2 parts:

- ❖ Virtual Channel (VC), 2 bits, DI [7...6]
- ❖ Data Type (DT), 6 bits, DI [5...0]

The Data Identification (DI) structure is illustrated below.


Figure 48: Data Identification (DI) Structure

Data Identification (DI) of the Packet Header (PH) is illustrated below for reference purpose.


Figure 49: Data Identification (DI) of the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is part of the Data Identification (DI [7...6]) structure, and it is used to indicate where a packet is to be sent from the MCU.

Bits of the Virtual Channel (VC) are illustrated below for reference purpose.

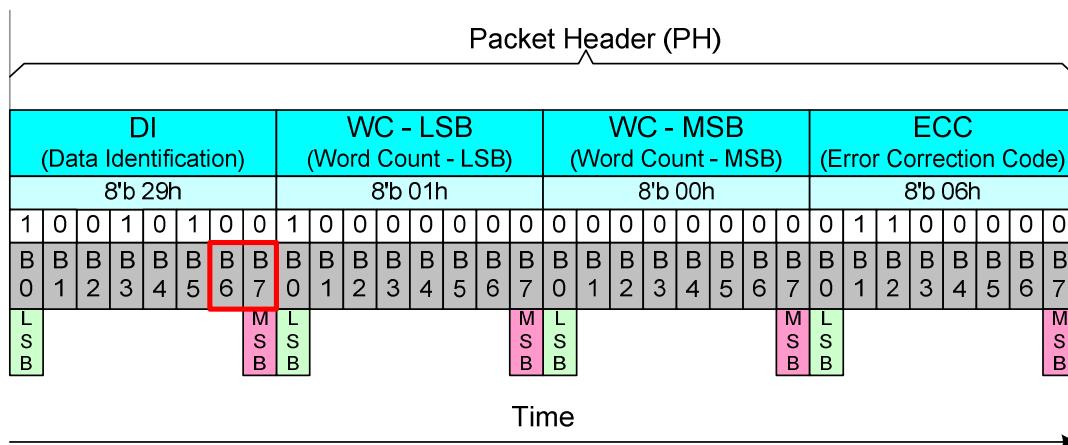
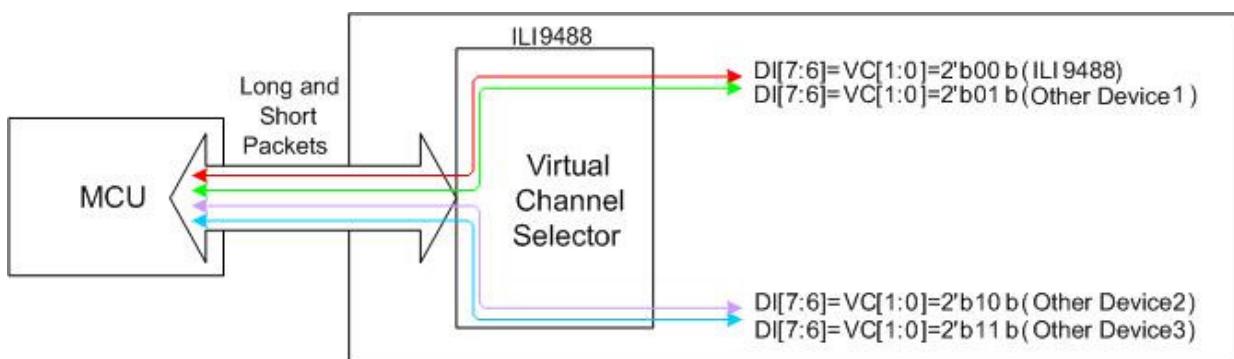


Figure 50: Virtual Channel (VC) of the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels to 4 different display modules. Devices use the same virtual channel as which the MCU uses to send packets to them, for example,

- The MCU uses the virtual channel 0 when it sends packets to the ILI9488.
 - The ILI9488 also uses the virtual channel 0 when it sends packets to the MCU.

This functionality is illustrated below.



Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00_b) when the MCU sends End of Transmission Packet to the display module.

The ILI9488 does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1...0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is part of the Data Identification (DI [5...0]) structure, and it is used to define the type of the used data in a packet.

Bits of the Data Type (DT) are illustrated below for reference purpose.

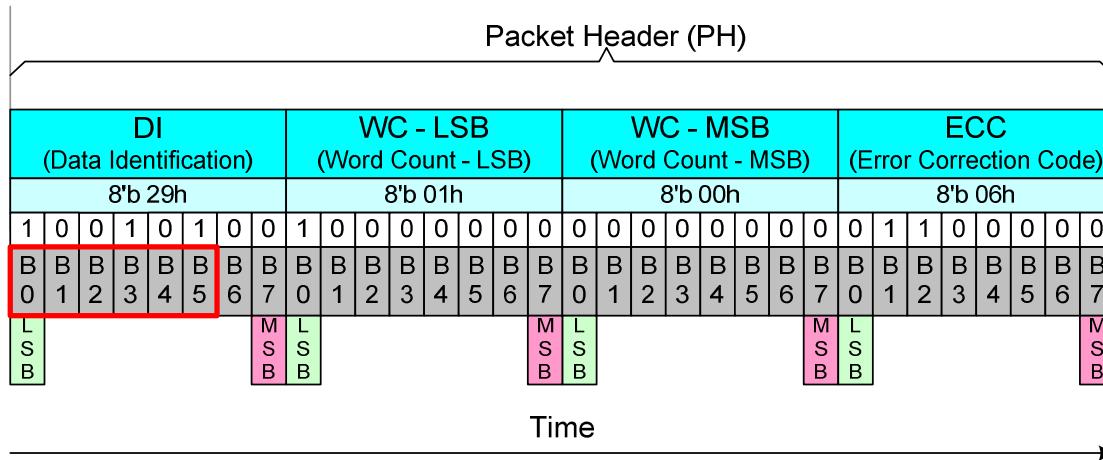


Figure 51: Data Type (DT) of the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. This Data Types (DT) is defined in the tables below.

Table 11: Data Type from the MCU to the Display Module (ILI9488)

| From the MCU to the Display Module (ILI9488) | | | | | | | | Short/Long Packet | Abbreviation |
|--|------|------|------|------|------|-----|---|--------------------|--------------|
| Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex | Description | Short/Long Packet | Abbreviation |
| 0 | 0 | 1 | 0 | 0 | 0 | 08 | End of Transmission Packet ^{Note1} | SPa (Short Packet) | EoTP |
| 0 | 0 | 0 | 1 | 0 | 1 | 05 | DCS Write, No Parameter | SPa (Short Packet) | DCSWN-S |
| 0 | 1 | 0 | 1 | 0 | 1 | 15 | DCS Write, 1 Parameter | SPa (Short Packet) | DCSW1-S |
| 0 | 0 | 0 | 1 | 1 | 0 | 06 | DCS Read, No Parameter | SPa (Short Packet) | DCSRN-S |
| 1 | 1 | 0 | 1 | 1 | 1 | 37 | Set Maximum Return Packet Size | SPa (Short Packet) | SMRPS-S |
| 0 | 0 | 1 | 0 | 0 | 1 | 09 | Null Packet, No Data ^{Note2} | LPa (Long Packet) | NP-L |
| 1 | 1 | 1 | 0 | 0 | 1 | 39 | DCS Write Long | LPa (Long Packet) | DCSW-L |

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.
2. This can be used when data lanes are to be kept in the High Speed Data Transferring (HSDT) Mode.

Table 12: Data Type from the Display Module (ILI9488) to the MCU

| From to the Display Module (ILI9488) to the MCU | | | | | | | | Short/Long Packet | Abbreviation |
|---|------|------|------|------|------|-----|--|--------------------|--------------|
| Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex | Description | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 02 | Acknowledge with Error Report | SPa (Short Packet) | AwER |
| 0 | 1 | 1 | 1 | 0 | 0 | 1C | DCS Read Long Response | LPa (Long Packet) | DCSRR-L |
| 1 | 0 | 0 | 0 | 0 | 1 | 21 | DCS Read Short Response, 1 byte returned | SPa (Short Packet) | DCSRR1-S |
| 1 | 0 | 0 | 0 | 1 | 0 | 22 | DCS Read Short Response, 2 byte returned | SPa (Short Packet) | DCSRR2-S |

The receiver will ignore other Data Types (DT) if they are not defined in the two tables above.

4.6.3.1.3.2 Packet Data of a Short Packet

Packet Data (PD) of the Short Packet (SPa) is placed after the Data Type (DT) of the Data Identification (DI), which indicates that a Short Packet (SPa) is to be sent.

The Word Count (WC) indicates the number of Bytes of Packet Data (PD) sent after the Packet Header (PH).

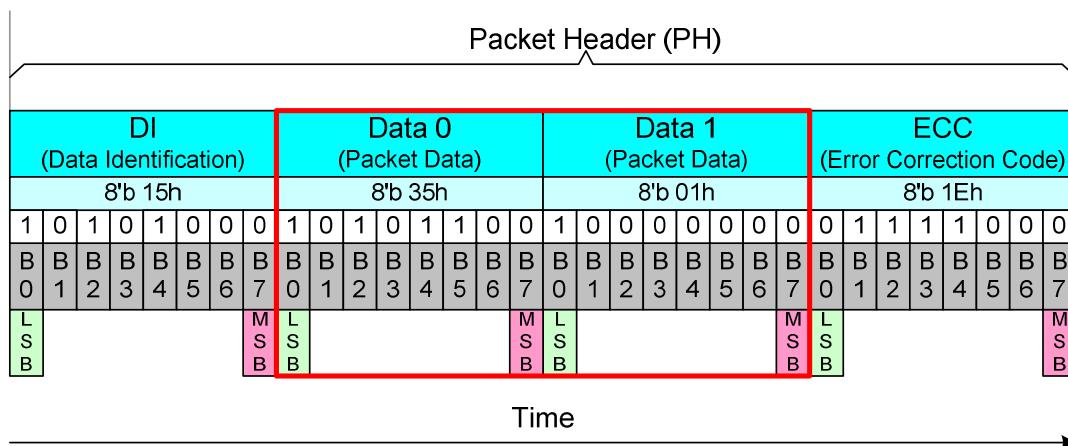
Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

The sending order of Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated below for reference purpose.

Packet Data (PD) information (2 bytes):

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)


Figure 52: Packet Data (PD) of a Short Packet, 2 Bytes Information

Packet Data (PD) information (1 byte):

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

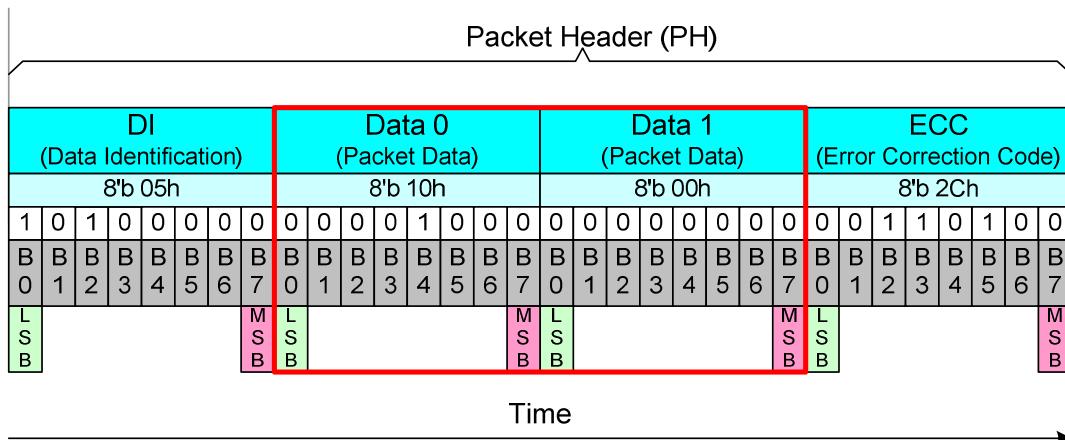


Figure 53: Packet Data (PD) of a Short Packet, 1 Byte Information

4.6.3.1.3.3 Word Count of a Long Packet

Word Count (WC) of a Long Packet (LPa) is placed after the Data Type (DT) of the Data Identification (DI), which indicates that a Long Packet (LPa) is to be sent.

Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) which are to be sent after the Packet Header (PH). The location of Word Count (WC) in a Long Packet is the same as which of Packet Data (PD) in a Short Packet, as illustrated in Figure 55 below.

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first and the Most Significant (MS) Byte is sent last.

Word Count (WC) of a Long Packet (LPa) is illustrated below for reference purpose.

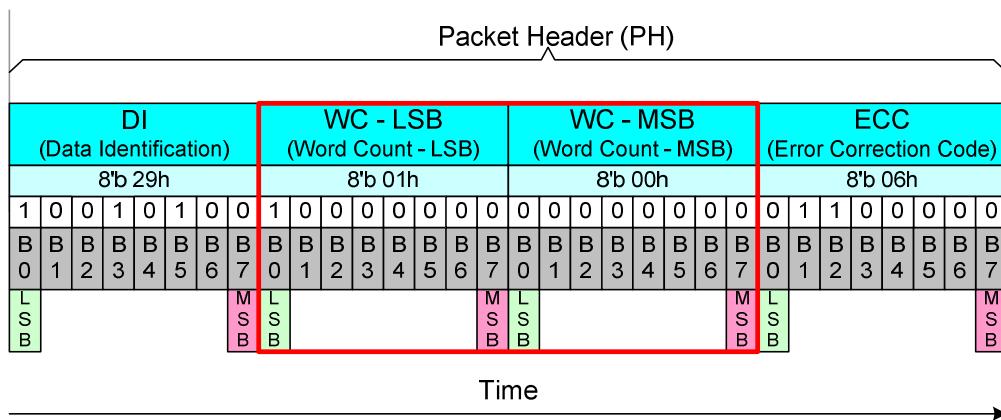


Figure 54: Word Count (WC) of a Long Packet

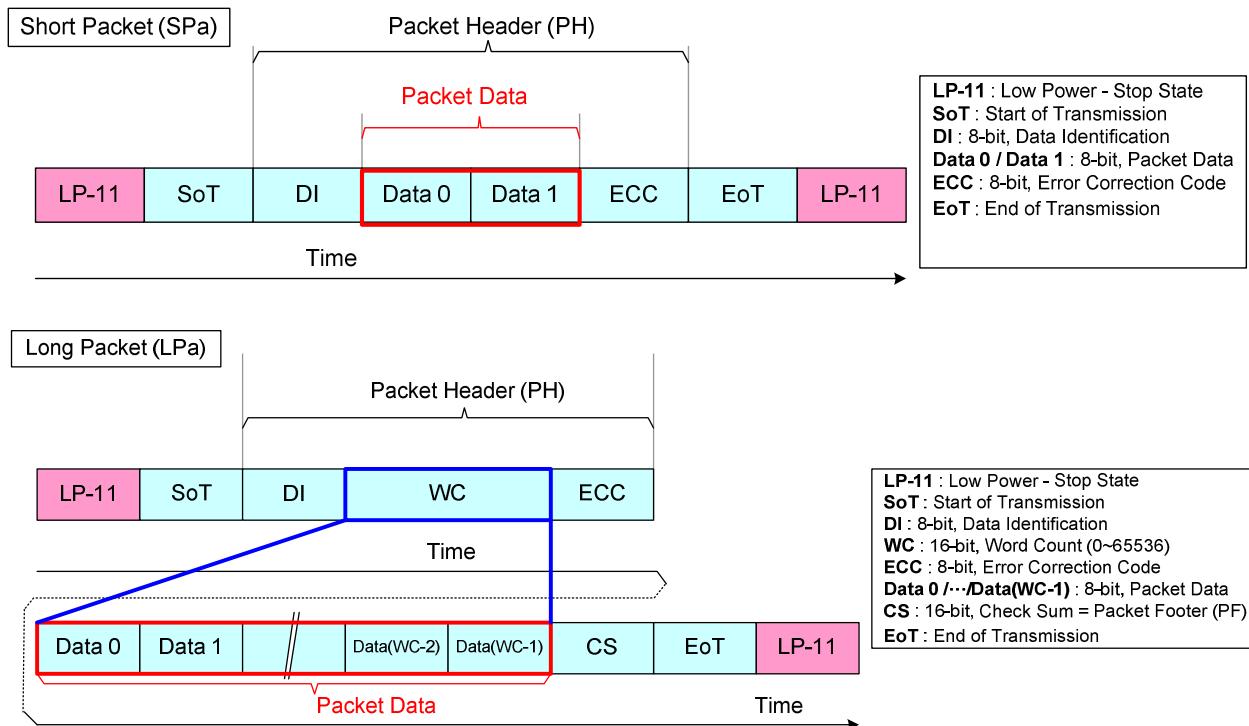


Figure 55: Packet Data in Short and Long Packets

4.6.3.1.3.4 Error Correction Code (ECC)

Error Correction Code (ECC) is part of Packet Header (PH) and its purpose is to identify an error or errors:

- ◆ Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23...0])
- ◆ Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23...0])

D [23...0] is illustrated for reference purposes below.

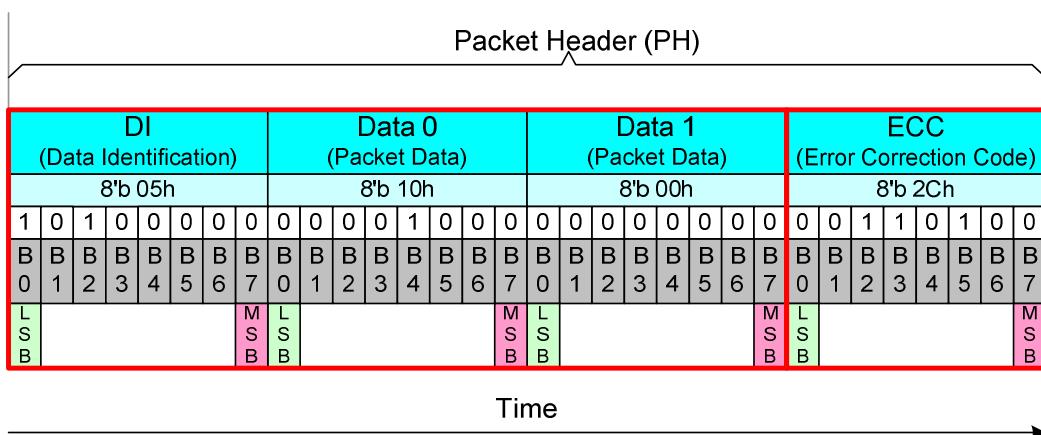


Figure 56: D [23...0] and P [7...0] in a Short Packet

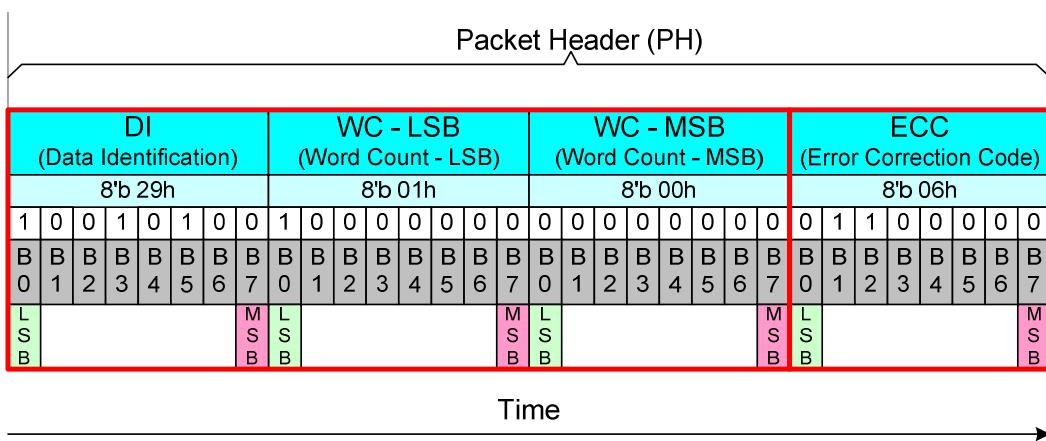


Figure 57: D [23...0] and P [7...0] in a Long Packet

Error Correction Code (ECC) can recognize one error or several errors, but only a one-bit error will be corrected.

Bits (P [7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as below:

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63...0]), but this implementation is based on 24 bit value (D [23...0]). Therefore, only 6 bits (P [5...0]) for Error Correction Code (ECC) are needed.

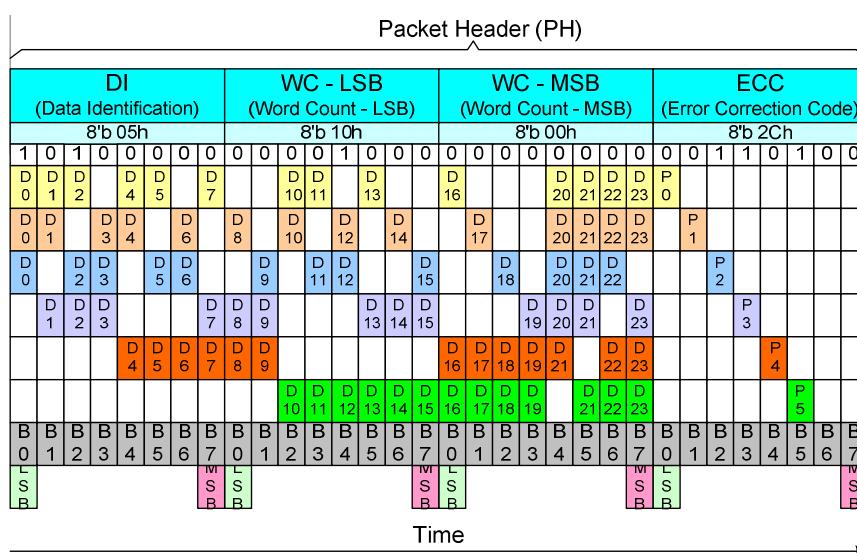


Figure 58: XOR Function on a Short Packet

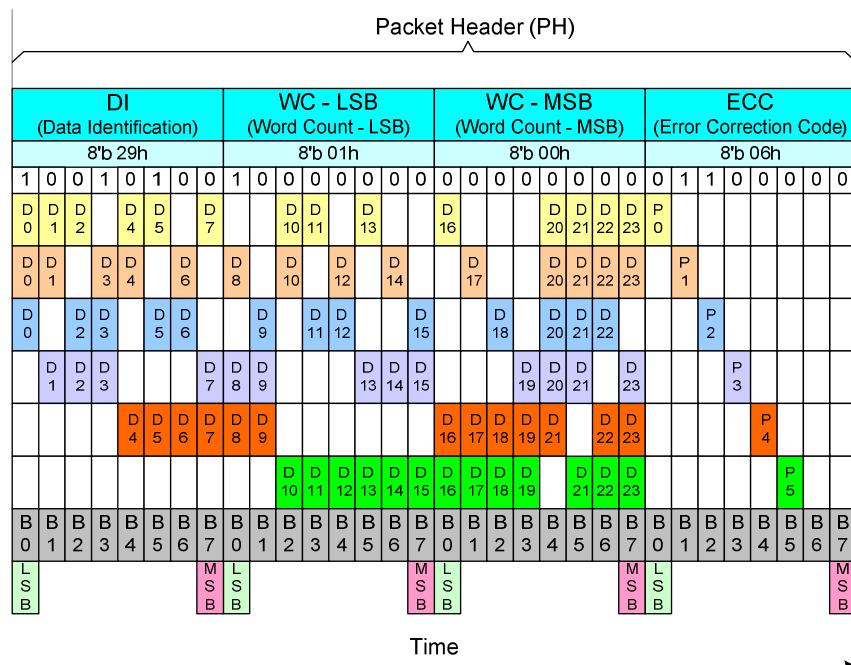
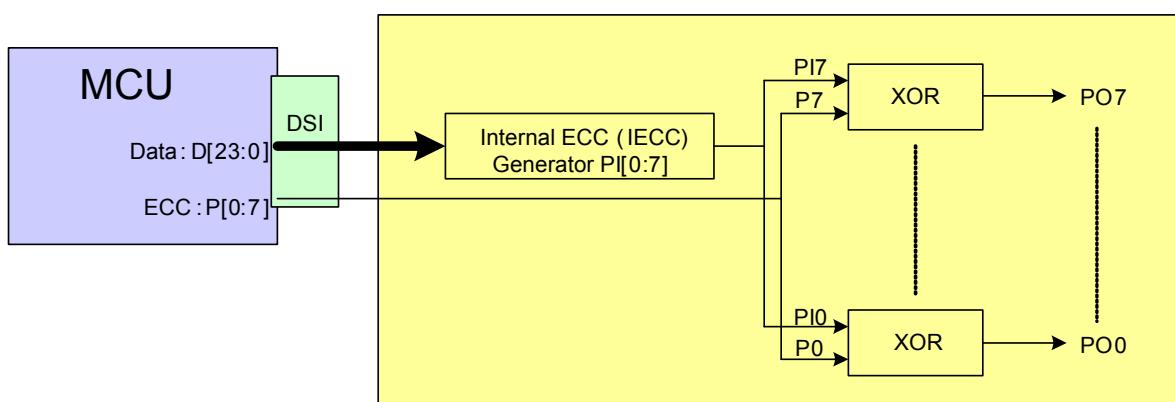


Figure 59: XOR Function on a Long Packet

The transmitter (the MCU or the Display Module) sends data bits D [23...0] and Error Correction Code (ECC) P [7...0]. The receiver (the Display Module or the MCU) calculates an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7...0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated below for reference purpose.



The sent data bits (D [23...0]) and ECC (P [7...0]) are received correctly, if the value of the PO [7...0] is 00h. The sent data bits (D [23...0]) and ECC (P [7...0]) are not received correctly, if the value of the PO [7...0] is not 00h.

| | | | | | | | | | |
|-----------------------------|---|---|---|---|---|---|---|---|-------------------|
| ECC P[7...0] | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 03h |
| IECC PI[7...0] | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 03h |
| XOR(ECC, IECC) => PO[7...0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = 00h => No Error |
| | L | | | | M | | | | |
| | S | | | | S | | | | |
| | B | | | | B | | | | |

Figure 60: Internal XOR Calculation between ECC and IECC Values – No Error

| | | | | | | | | | |
|-----------------------------|---|---|---|---|---|---|---|---|----------------|
| ECC P[7...0] | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 03h |
| IECC PI[7...0] | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0Fh |
| XOR(ECC, IECC) => PO[7...0] | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | = 0Ch => Error |
| | L | | | | M | | | | |
| | S | | | | S | | | | |
| | B | | | | B | | | | |

Figure 61: Internal XOR Calculation between ECC and IECC Values – Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D [23...0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7...0] is compared to values in the following table.

Table 13: One Bit Error Value of the Error Correction Code (ECC)

| Data Bit | PO7 | PO6 | PO5 | PO4 | PO3 | PO2 | PO1 | PO0 | Hex |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D [0] | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07h |
| D [1] | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh |
| D [2] | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh |
| D [3] | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh |
| D [4] | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13h |
| D [5] | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15h |
| D [6] | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16h |
| D [7] | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19h |
| D [8] | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1Ah |
| D [9] | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1Ch |
| D [10] | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h |
| D [11] | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25h |
| D [12] | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26h |
| D [13] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h |
| D [14] | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2Ah |
| D [15] | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch |
| D [16] | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31h |
| D [17] | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32h |
| D [18] | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h |
| D [19] | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h |
| D [20] | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1Fh |
| D [21] | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2Fh |
| D [22] | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37h |
| D [23] | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3Bh |

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One error is detected if the value of the PO [7...0] is in Table 13: One Bit Error Value of the Error Correction Code (ECC), and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, for example,

- PO [7...0] = 0Eh
- The bit of the data (D [23...0]), which is not correct, is D [3]

More than one error is detected if the value of the PO [7...0] is not in Table 13: One Bit Error Value of the Error Correction Code (ECC), for example, PO [7...0] = 0Ch.

4.6.3.1.4. Packet Data on a Long Packet

Packet Data (PD) of the Long Packet (LPa) is transmitted after the Packet Header (PH) of the Long Packet (LPa). The amount of the data bytes is defined in the chapter “Word Count (WC) of the Long Packet (LPa)”.

4.6.3.1.5. Packet Footer on a Long Packet

Packet Footer (PF) of the Long Packet (LPa) is placed after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is the checksum value which is calculated from the Packet Data of the Long Packet (LPa).

The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial $X^{16}+X^{12}+X^5+X^0$ as illustrated below.

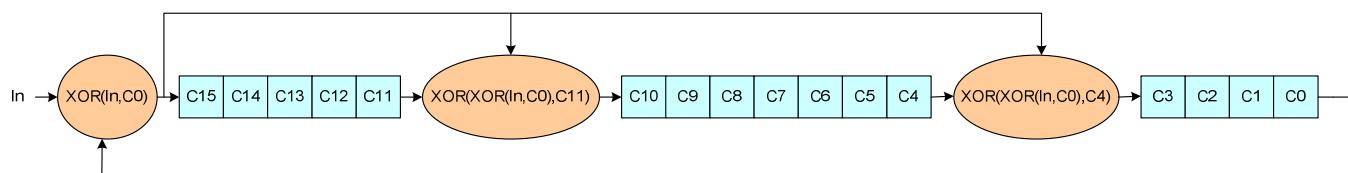


Figure 62: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

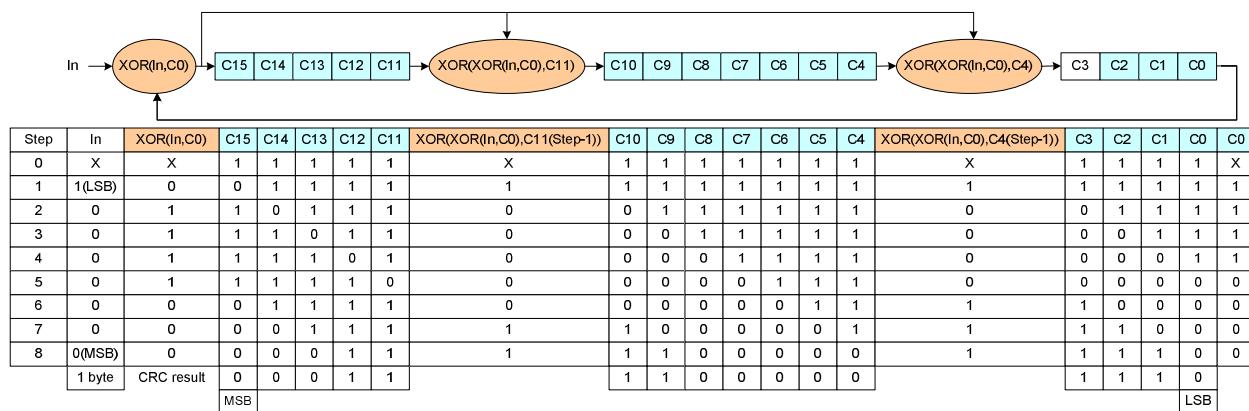


Figure 63: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

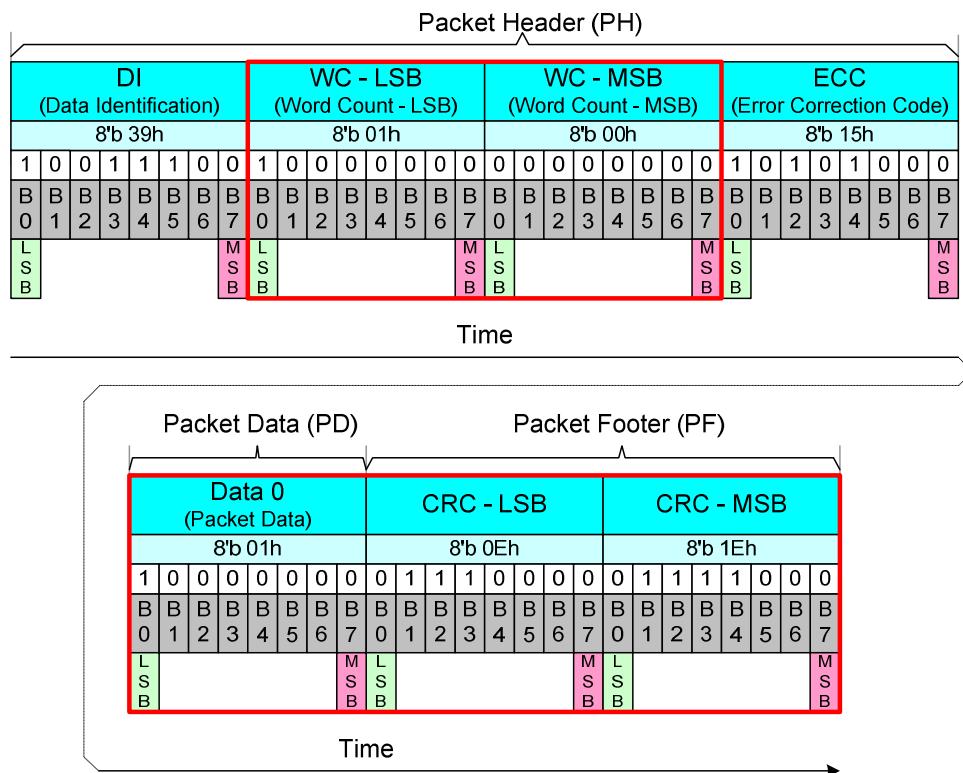


Figure 64: Packet Footer (PF) Example

The receiver calculates its own checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) which the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) is equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

4.6.3.2. Packet Transmission

4.6.3.2.1. Packet from the MCU to the Display Module

4.6.3.2.1.1 Display Command Set (DCS)

Display Command Set (DCS) is transmitted from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), which is included in Short Packets (SPa) and Long packets (LPa), as illustrated below.

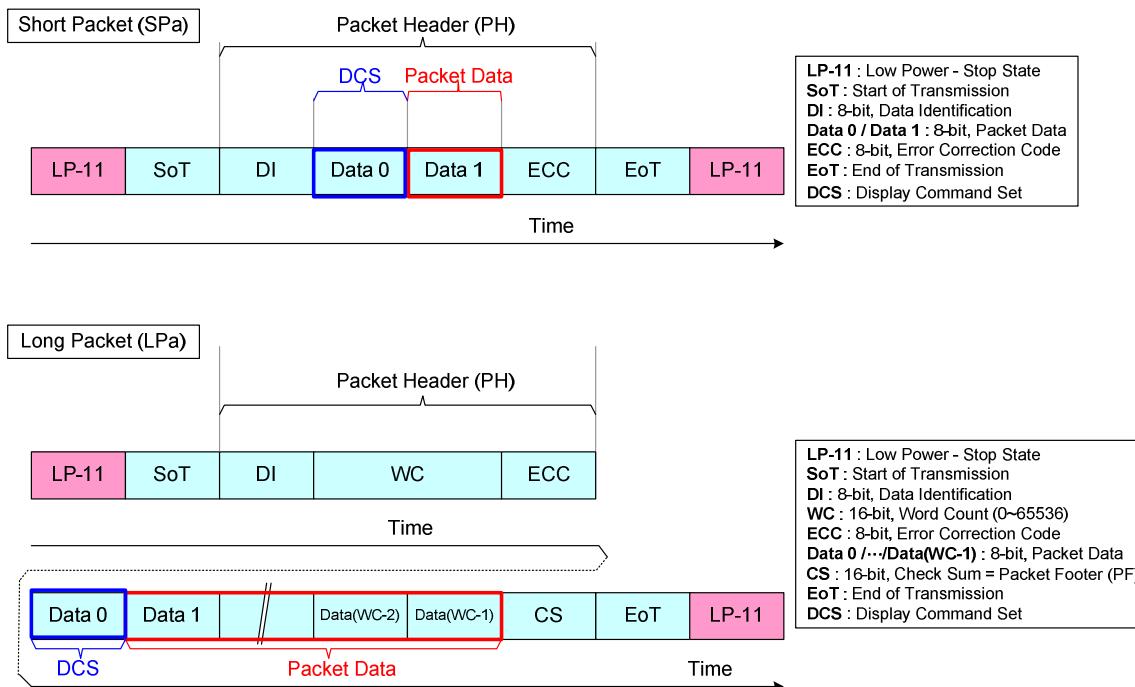


Figure 65: Display Command Set (DCS) in Short Packet and Long Packet

4.6.3.2.1.2 Display Command Set Write, no Parameter (DSCWN-S)

“Display Command Set (DCS) Write, No Parameter” is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined in the table below.

Table 14: Display Command Set Write, no Parameter (DSCWN-S)

| Command |
|-------------------------------|
| NOP (00h) |
| Software Reset (01h) |
| Sleep IN(10h) |
| Sleep Out (11h) |
| Partial Mode ON (12h) |
| Normal Display Mode ON (13h) |
| Display OFF (28h) |
| Display ON (29h) |
| Tearing Effect Line OFF (34h) |
| Idle Mode OFF (38h) |

Idle Mode ON (39h)

A Short Packet (SPa) is defined as:

- ◆ Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 0101b
 - ◆ Packet Data (PD)
 - ✧ Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - ✧ Data 1: Always 00hex
 - ◆ Error Correction Code (ECC)

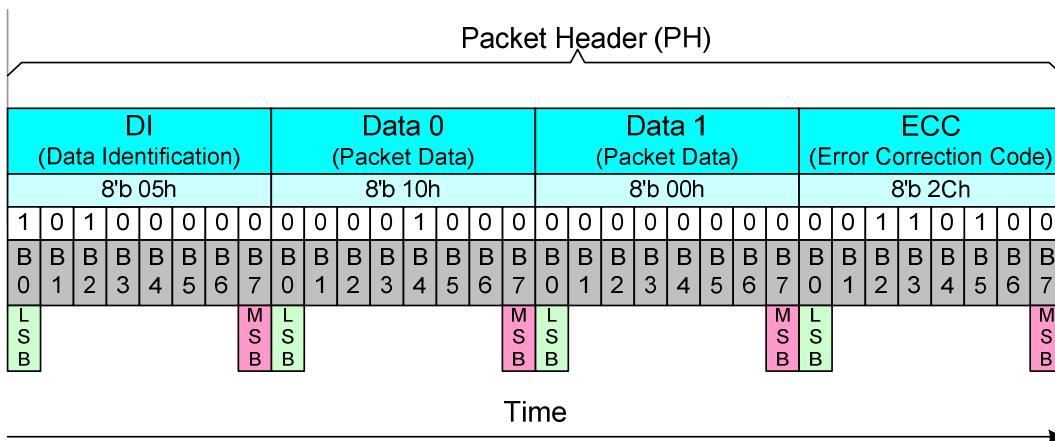


Figure 66: Display Command Set (DCS) Write, no Parameter (DCSWN-S) – Example

4.6.3.2.1.3 Display Command Set Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined in the table below.

Table 15: Display Command Set Write, 1 Parameter (DSCW1-S)

| Command |
|---|
| Gamma Set |
| Memory Write (2Ch) <small>Note</small> |
| Tearing Effect Line ON (35h) |
| Memory Access Control (36h) |
| Interface Pixel Format (3Ah) |
| Memory Write Continue (3Ch) <small>Note</small> |
| Write Display Brightness (51h) |
| Write CTRL Display (53h) |
| Write Content Adaptive Brightness control (55h) |
| Write CABC Minimum Brightness (5Eh) |

Note: One Subpixel has been written.

A Short Packet (SPa) is defined as:

- ◆ Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 01 0101b
- ◆ Packet Data (PD)
 - ✧ Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - ✧ Data 1: 01hex, Parameter of the DCS
- ◆ Error Correction Code (ECC)

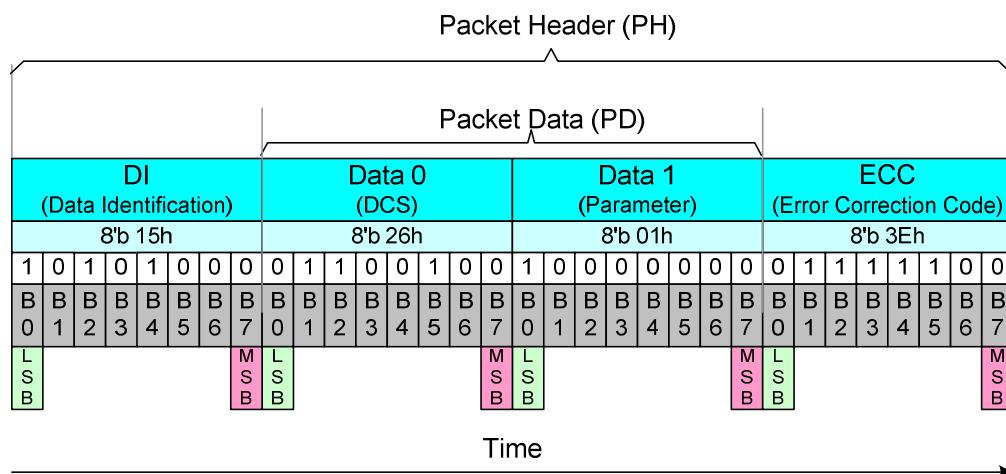


Figure 67: Display Command Set Write, 1 Parameter (DCSW1-S) – Example

4.6.3.2.1.4 Display Command Set Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in the table below.

Table 16: Display Command Set Write Long (DCSW-L)

| Command |
|--|
| NOP (00h) ^{Note 1} |
| Software Reset (01h) ^{Note 1} |
| Sleep IN(10h) ^{Note 1} |
| Sleep Out (11h) ^{Note 1} |
| Partial Mode ON (12h) ^{Note 1} |
| Normal Display Mode ON (13h) ^{Note 1} |
| Gamma Set (26h) ^{Note 2} |
| Display OFF (28h) ^{Note 1} |
| Display ON (29h) ^{Note 1} |
| Column Address Set (2Ah) |
| Page Address Set (2Bh) |
| Memory Write (2Ch) ^{Note 2} |
| Partial Area (30h) |

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| |
|---|
| Tearing Effect Line OFF (34h) ^{Note 1} |
| Tearing Effect Line ON (35h) ^{Note 2} |
| Memory Access Control (36h) ^{Note 2} |
| Idle Mode OFF (38h) ^{Note 1} |
| Idle Mode ON (39h) ^{Note 1} |
| Interface Pixel Format(3Ah) |
| Memory Write Continue (3Ch) ^{Note 2} |
| Write Display Brightness (51h) ^{Note 2} |
| Write CTRL Display (53h) ^{Note 2} |
| Write Content Adaptive Brightness control (55h) ^{Note 2} |
| Write CABC Minimum Brightness (5Eh) |

Notes:

1. It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, No Parameter”.
2. It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, 1 Parameter”.

The Long Packet (LPa), when a command (No Parameter) is sent, is defined as:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 11 1001b
- ◆ Word Count (WC)
 - ❖ Word Count (WC): 0001h
- ◆ Error Correction Code (ECC)
- ◆ Packet Data (PD): Data 0 => “Sleep In (10h)”, Display Command Set (DCS)
- ◆ Packet Footer (PF)

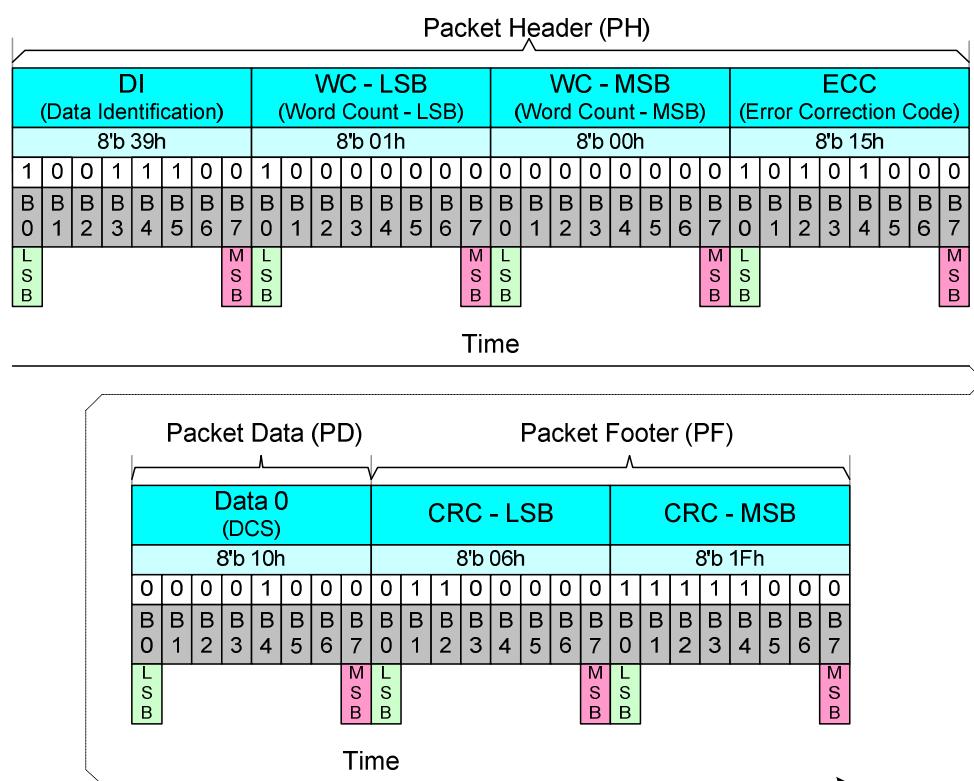
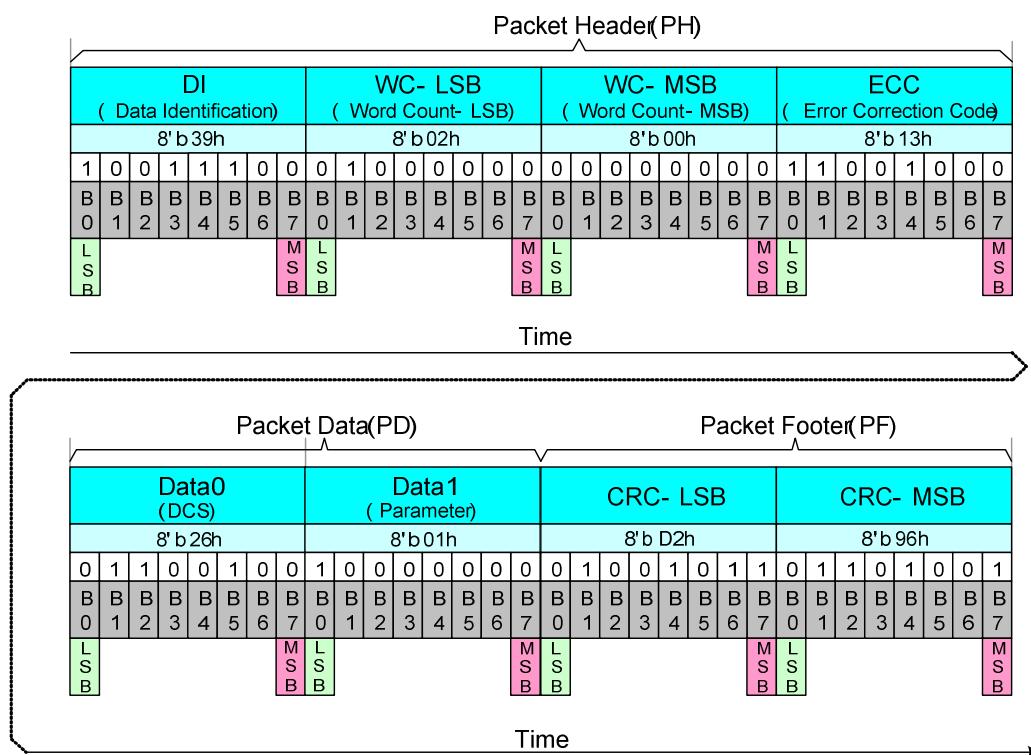


Figure 68: Display Command Set Write Long (DCSW-L) with DCS Only – Example

The Long Packet (LPA), when a Write (1 parameter) is sent, is defined as:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 11 1001b
- ◆ Word Count (WC)
 - ❖ Word Count (WC): 0002h
- ◆ Error Correction Code (ECC)
- ◆ Packet Data (PD):
 - ❖ Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
 - ❖ Data 1: 01hex, Parameter of the DCS
- ◆ Packet Footer (PF)


Figure 69: Display Command Set Write Long (DCSW-L) with DCS and 1 Parameter – Example

The Long Packet (LPA), when a Write (4 parameters) is sent, is defined as:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 11 1001b
- ◆ Word Count (WC)
 - ❖ Word Count (WC): 0005h
- ◆ Error Correction Code (ECC)
- ◆ Packet Data (PD):

- ❖ Data 0: "Column Address Set (2Ah)", Display Command Set (DCS)
- ❖ Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15...8]
- ❖ Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7...0]
- ❖ Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15...8]
- ❖ Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7...0]
- ◆ Packet Footer (PF)

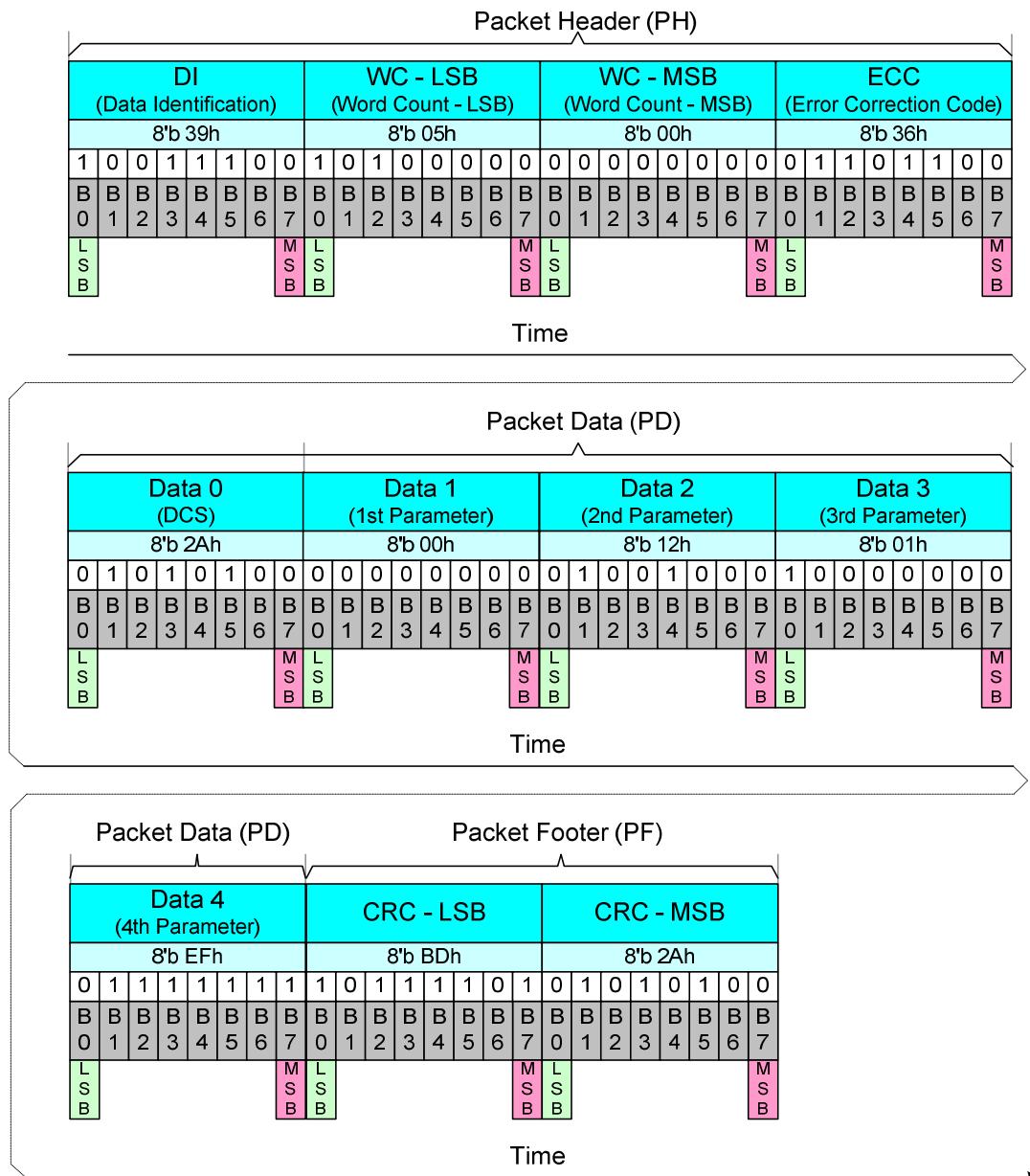


Figure 70: Display Command Set Write Long with DCS and 4 Parameters – Example

4.6.3.2.1.5 Display Command Set Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined in the table below. The 1st parameter (Dummy Data) will not return to the DSI after it is done in the MCU parallel interface. The first returned parameter is the 2nd parameter in the DSI.

Table 17: Display Command Set Read, No Parameter (DCSRN-S)

| Command |
|--|
| Read Number of the Errors on DSI (05h) |
| Read Display Power Mode (0Ah) |
| Read Display MADCTL (0Bh) |
| Read Display Pixel Format (0Ch) |
| Read Display Image Mode (0Dh) |
| Read Display Signal Mode (0Eh) |
| Read Display Self-Diagnostic Result (0Fh) |
| Memory Read (2Eh) |
| Memory Read Continue (3Eh) |
| Read Display Brightness Value (52h) |
| Read CTRL Value Display (54h) |
| Read Content Adaptive Brightness Control (56h) |
| Read CABC Minimum Brightness (5Fh) |
| Read ID1 (DAh) |
| Read ID2 (DBh) |
| Read ID3 (DCh) |

The MCU has to define to the display module the maximum size of the returned packet. The command used for this purpose is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which uses Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated below for reference purpose.

Step 1:

- ◆ The MCU sends “Set Maximum Return Packet Size” (SMRPS-S) (Short Packet (SPa)) to the display module when the display module wants to return one byte to the display module.
- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 11 0111b
- ◆ Maximum Return Packet Size (MRPS)
 - ❖ Data 0: 01hex
 - ❖ Data 1: 00hex
- ◆ Error Correction Code (ECC)

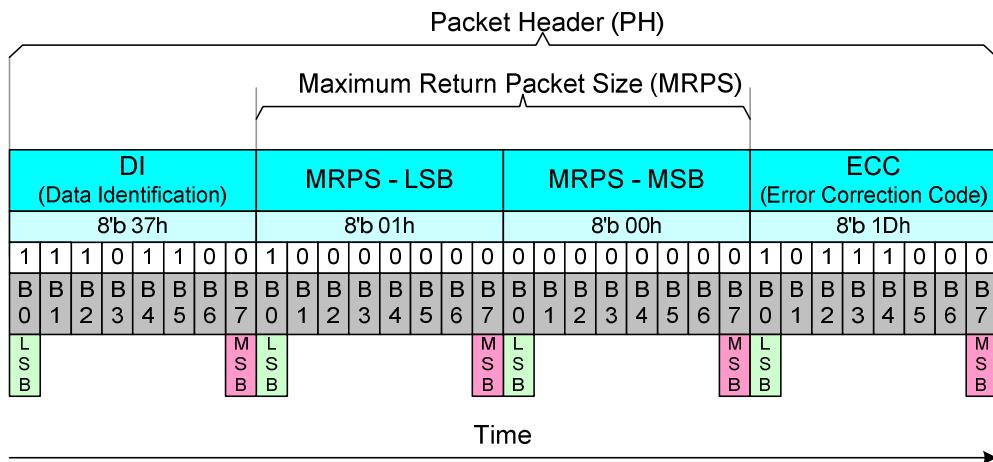


Figure 71: Set Maximum Return Packet Size (SMRPS-S) – Example

Step 2:

- ◆ The MCU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module.
- ◆ Data Identification (DI)
 - ◊ Virtual Channel (VC, DI [7...6]): 00b
 - ◊ Data Type (DT, DI [5...0]): 00 0110b
- ◆ Packet Data (PD)
 - ◊ Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - ◊ Data 1: Always 00hex
- ◆ Error Correction Code (ECC)

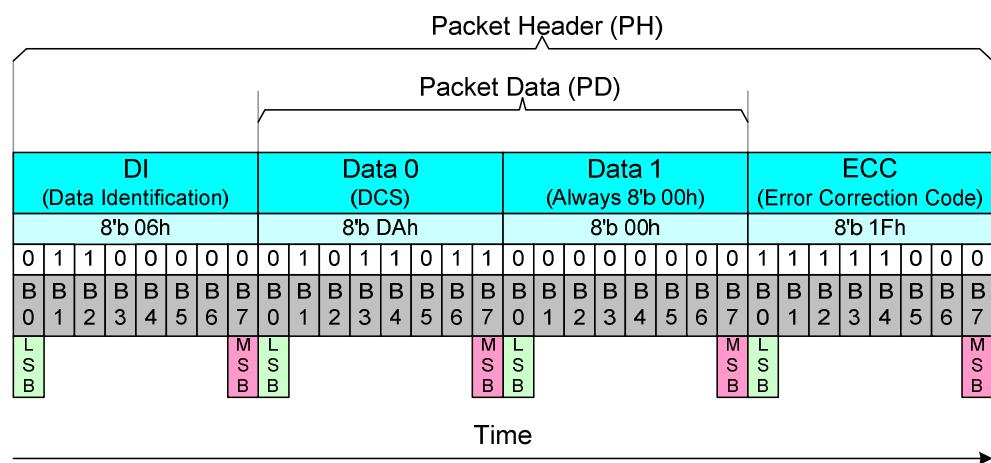


Figure 72: Display Command Set Read, No Parameter (DCSRN-S) – Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

- ❖ An Acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if an error is found while receiving a command.
- ❖ Information of the received command, which can be in a Short Packet (SPa) or Long Packet (LPa).

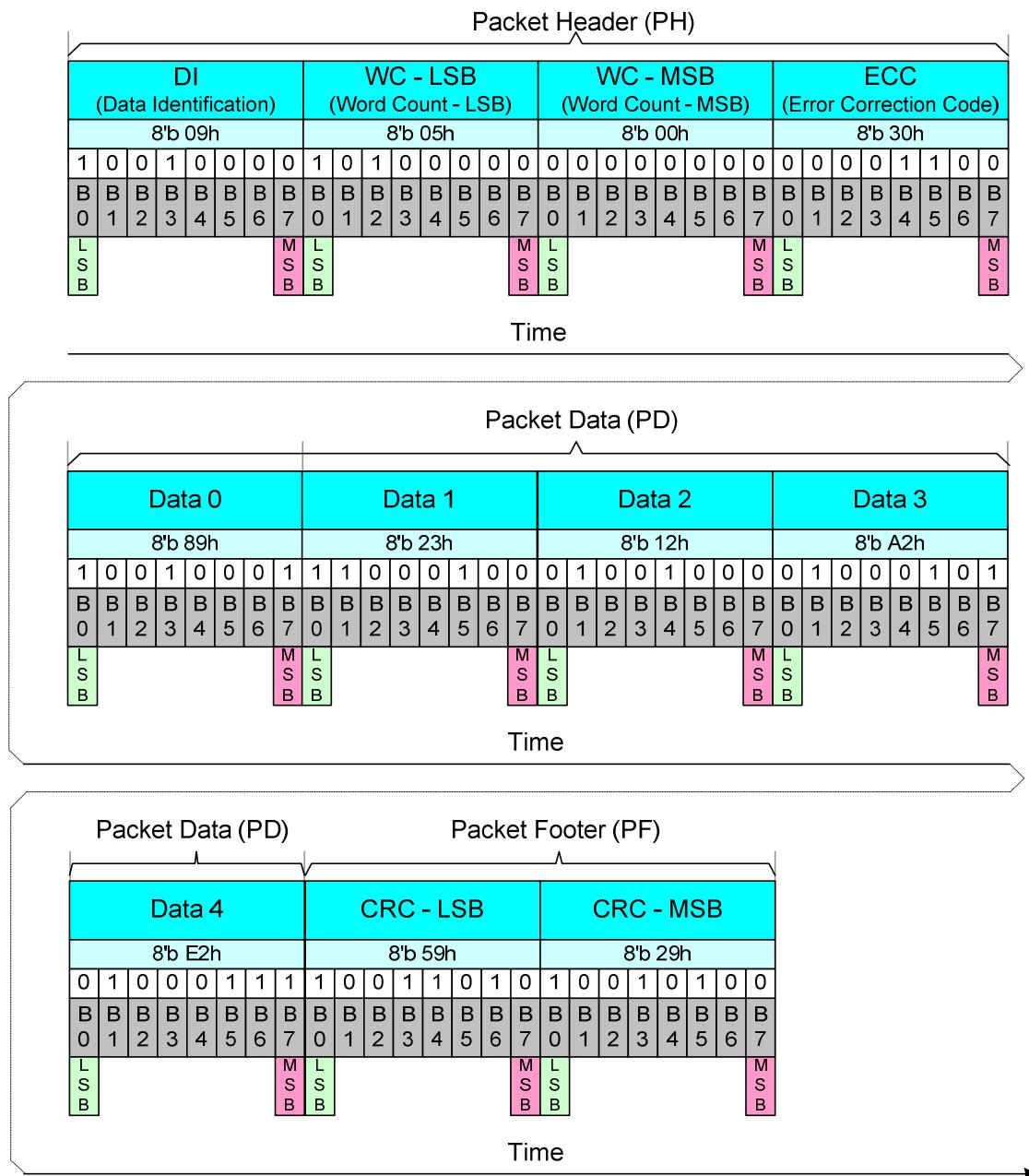
4.6.3.2.1.6 Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 00 1001b), from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT), if necessary.

The display module can ignore the Packet Data (PD), which is sent by the MCU.

The Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) are sent, is defined as:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 00 1001b
- ◆ Word Count (WC)
 - ❖ Word Count (WC): 0005hex
- ◆ Error Correction Code (ECC)
- ◆ Packet Data (PD):
 - ❖ Data 0: 89hex (Random data)
 - ❖ Data 1: 23hex (Random data)
 - ❖ Data 2: 12hex (Random data)
 - ❖ Data 3: A2hex (Random data)
 - ❖ Data 4: E2hex (Random data)
- ◆ Packet Footer (PF)


Figure 73: Null Packet, No Data (NP-L) – Example

4.6.3.2.1.7 End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP), which is optional in the interface level and is defined in the Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the High Speed Data Transmission (HSDT) mode properly when the EoTP is added after the last payload packet before “End of Transmission” (EoT).

The MCU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module will/will not receive “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= leaving Escape mode), which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 18: Receiving and Transmitting EoTP during LPDT

| Direction | Display Module (DM) in High Speed Data Transmission (HSDT) | Display Module (DM) in Low Power Data Transmission (LPDT) |
|-----------------------|---|--|
| MCU => Display Module | With or Without EoTP is Supported | With or Without EoTP is Supported |
| Display Module => MCU | HS Mode is not available (EoTP is not available) | EoTP cannot be sent by the Display Module (DM) |

Short Packet (SPa) uses a fixed format as follows:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 00 1000b
- ◆ Packet Data (PD)
 - ❖ Data 0: 0Fhex
 - ❖ Data 1: 0Fhex
- ◆ Error Correction Code (ECC)
 - ❖ ECC: 01hex

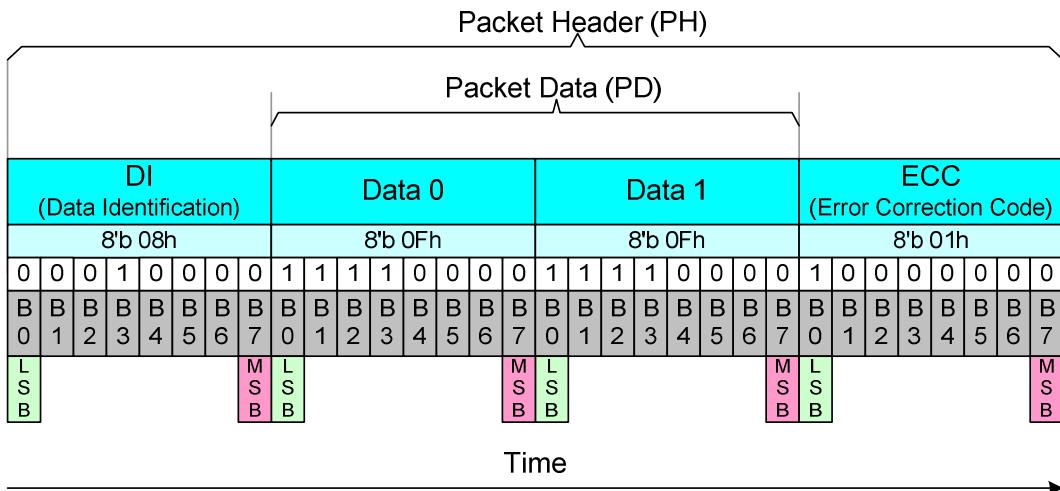


Figure 74: End of Transmission Packet (EoTP)

Some cases of the “End of Transmission Packet” (EoTP) are illustrated below for reference purpose only.

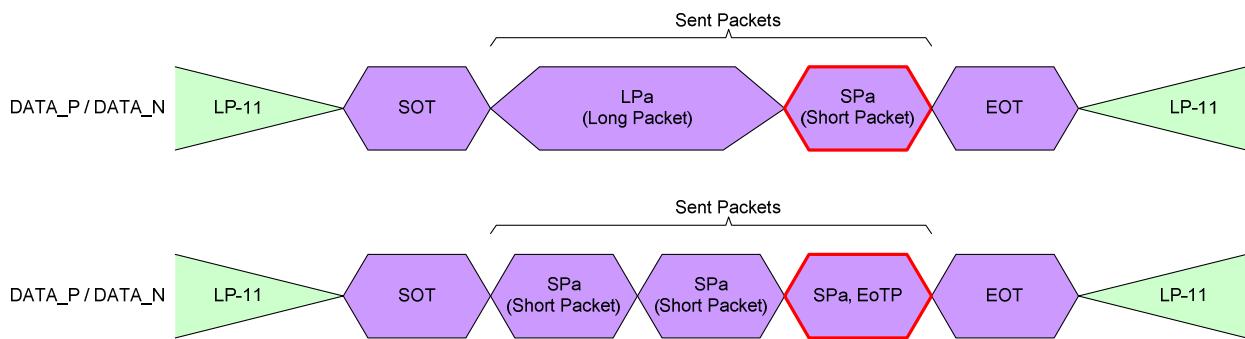


Figure 75: End of Transmission Packet (EoTP) – Examples

4.6.3.2.2. Packet from the Display Module to the MCU

4.6.3.2.2.1. Used Packet Type

The display module can use Short Packets (SPa) or Long Packets (LPa) when it returns information to the MCU after the MCU requests information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER).

The used packet type is defined in the Data Type (DT). If the maximum size of the Packet Data (PD) could be sent in one packet, then the display module cannot separate returned bytes into several packets.

Both cases are illustrated below for reference purpose.

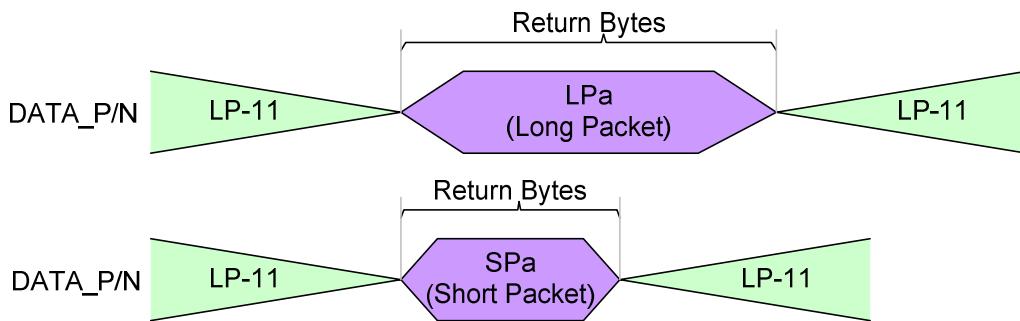


Figure 76: Return Bytes in Single Packet

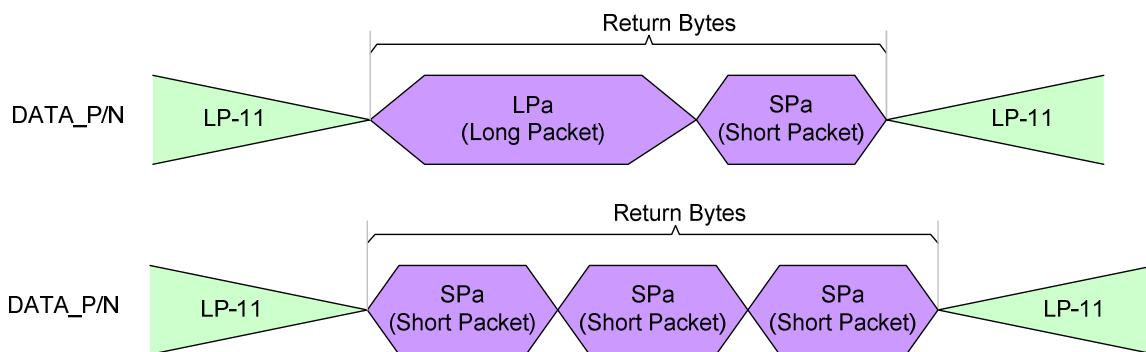


Figure 77: Return Bytes in Multiple Packets – Now Allowed

Exception:

The display module returns 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (see the chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), in which a single bit error is detected and corrected by the EEC (see bit 8 in Table 19: Acknowledge with Error Report (AwER) for Short Packet (SPA) Response). These returned packets are illustrated below for reference purpose.

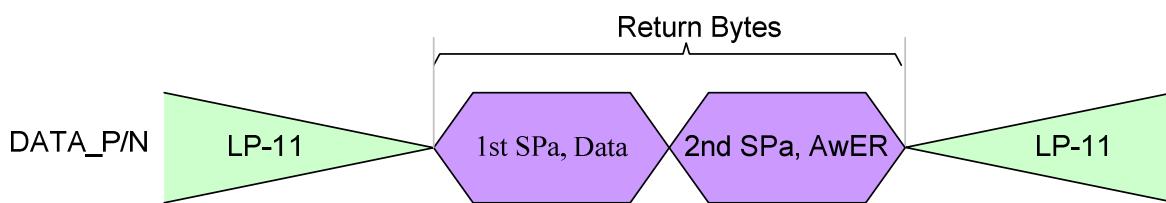


Figure 78: Exception when Return Bytes in Several Packets

AwER = Acknowledge with Error Report

4.6.3.2.2 Acknowledge with Error Report

“Acknowledge with Error Report” (AwER) is always transmitted through a Short Packet (SPa), which is defined in the Data Type (DT, 00 0010b), from the display module to the MCU. The 16 bits in the Packet Data (PD) can indicate the current error(s) if one or more than one bit(s) is/are set to 1, as defined in the following table.

Table 19: Acknowledge with Error Report (AwER)

| Bit | The Description of Acknowledge Error Report (AwER) | |
|-----|--|--|
| | Short Packet | Long Packet |
| 0 | SoT Error | SoT Error |
| 1 | SoT Sync Error | SoT Sync Error |
| 2 | EoT Sync Error | EoT Sync Error |
| 3 | Escape Mode Entry Command Error | Escape Mode Entry Command Error |
| 4 | Low-Power Transmit Error | Low-Power Transmit Error |
| 5 | Any Protocol Timer-Out | Any Protocol Timer-Out |
| 6 | False Control Error | False Control Error |
| 7 | Contention is Detected on the Display Module | Contention is Detected on the Display Module |
| 8 | ECC Error, Single-Bit (Detected and Corrected) | ECC Error, Single-Bit (Detected and Corrected) |
| 9 | ECC Error, Multi-Bit (Detected, Not Corrected) | ECC Error, Multi-Bit (Detected, Not Corrected) |
| 10 | Reserved, Set to 0 internally | Checksum Error |
| 11 | DSI Data Type (DT), Not Recognized | DSI Data Type (DT), Not Recognized |
| 12 | DSI Virtual Channel (VC) ID Invalid | DSI Virtual Channel (VC) ID Invalid |
| 13 | DSI Protocol Violation | DSI Protocol Violation |
| 14 | Reserved, Set to 0 internally | Reserved, Set to 0 internally |
| 15 | Reserved, Set to 0 internally | Reserved, Set to 0 internally |

These errors are included in all packages, which are received from the MCU to the display module before the Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) in a Short Packet (SPa) is defined as:

- ◆ Data Identification (DI)
 - ❖ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 00 0010b
- ◆ Packet Data (PD)
 - ❖ Bit 8: ECC Error, single-bit (detected and corrected)
 - ❖ AwER: 0100h
- ◆ Error Correction Code (ECC)

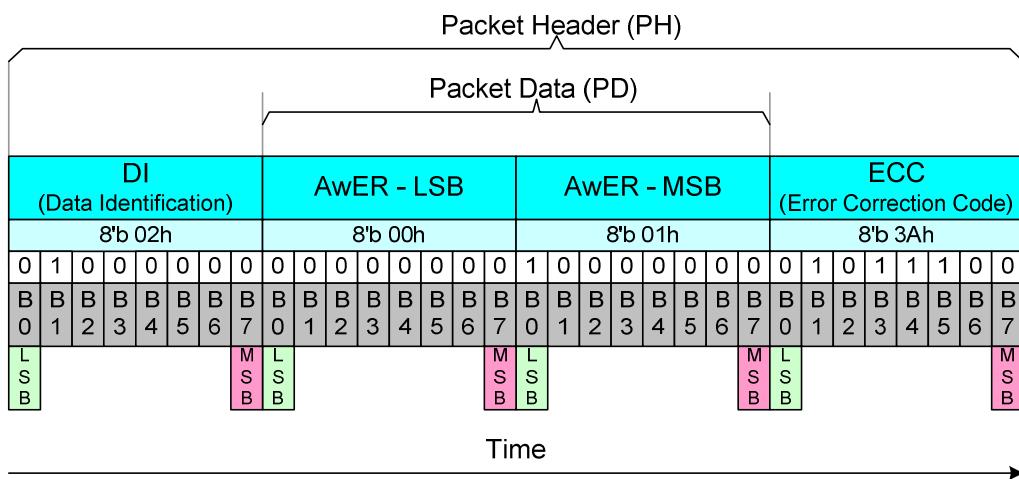
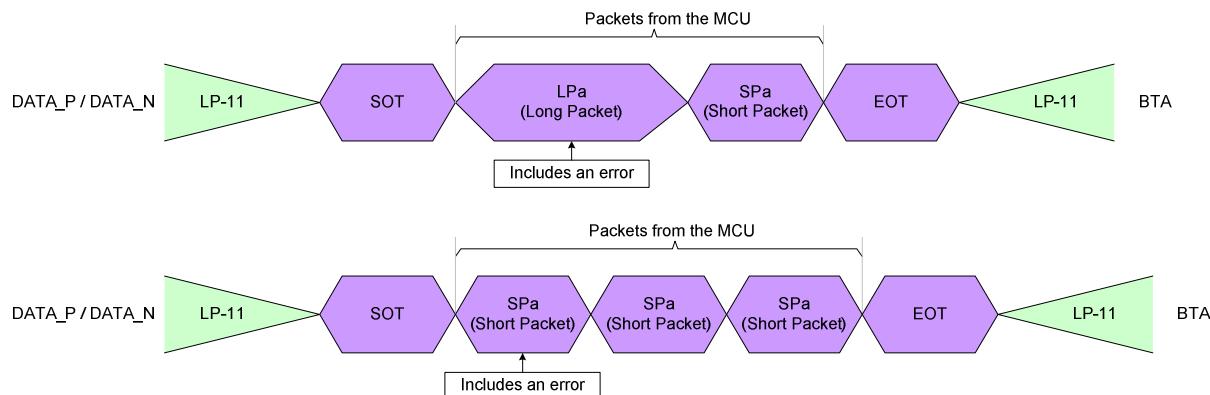


Figure 79: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated below for reference purpose.



Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets are indicated by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. If a received packet includes an error, the bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1.

The numbers of the packets, including an **ECC or CRC** error, are calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated below for reference purpose.

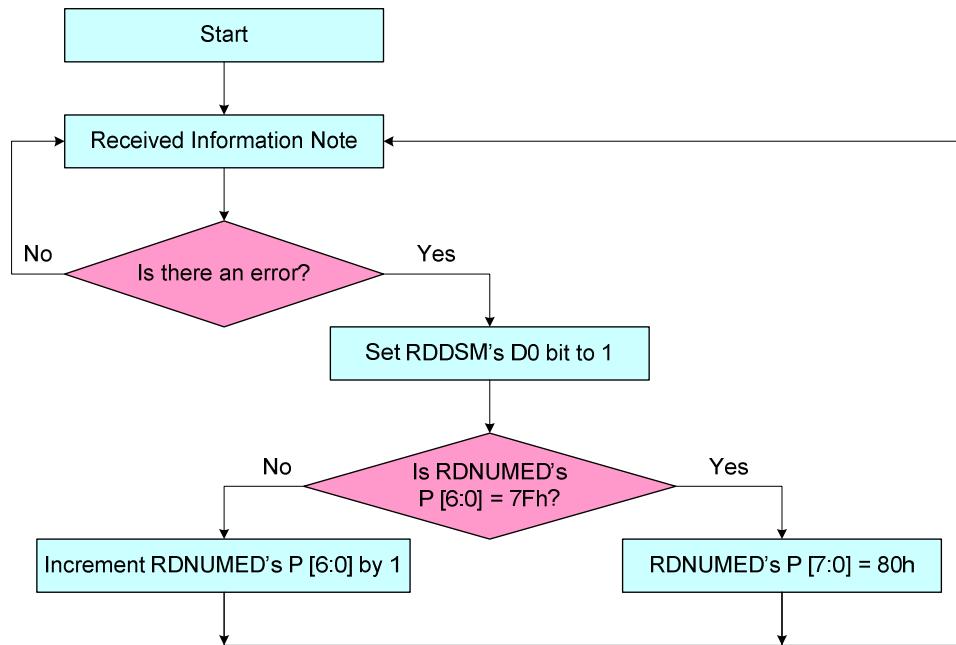


Figure 80: Flow Chart for Errors on DSI

4.6.3.2.2.3 DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 01 1100b), from the display module to the MCU.

“DCS Read Long Response” (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

The Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- ◆ Data Identification (DI)
- ◆ Virtual Channel (VC, DI [7...6]): 00b
 - ❖ Data Type (DT, DI [5...0]): 01 1100b
- ◆ Word Count (WC)
 - ❖ Word Count (WC): 0005hex
- ◆ Error Correction Code (ECC)
- ◆ Packet Data (PD):
 - ❖ Data 0: 89hex
 - ❖ Data 1: 23hex
 - ❖ Data 2: 12hex
 - ❖ Data 3: A2hex
 - ❖ Data 4: E2hex
- ◆ Packet Footer (PF)

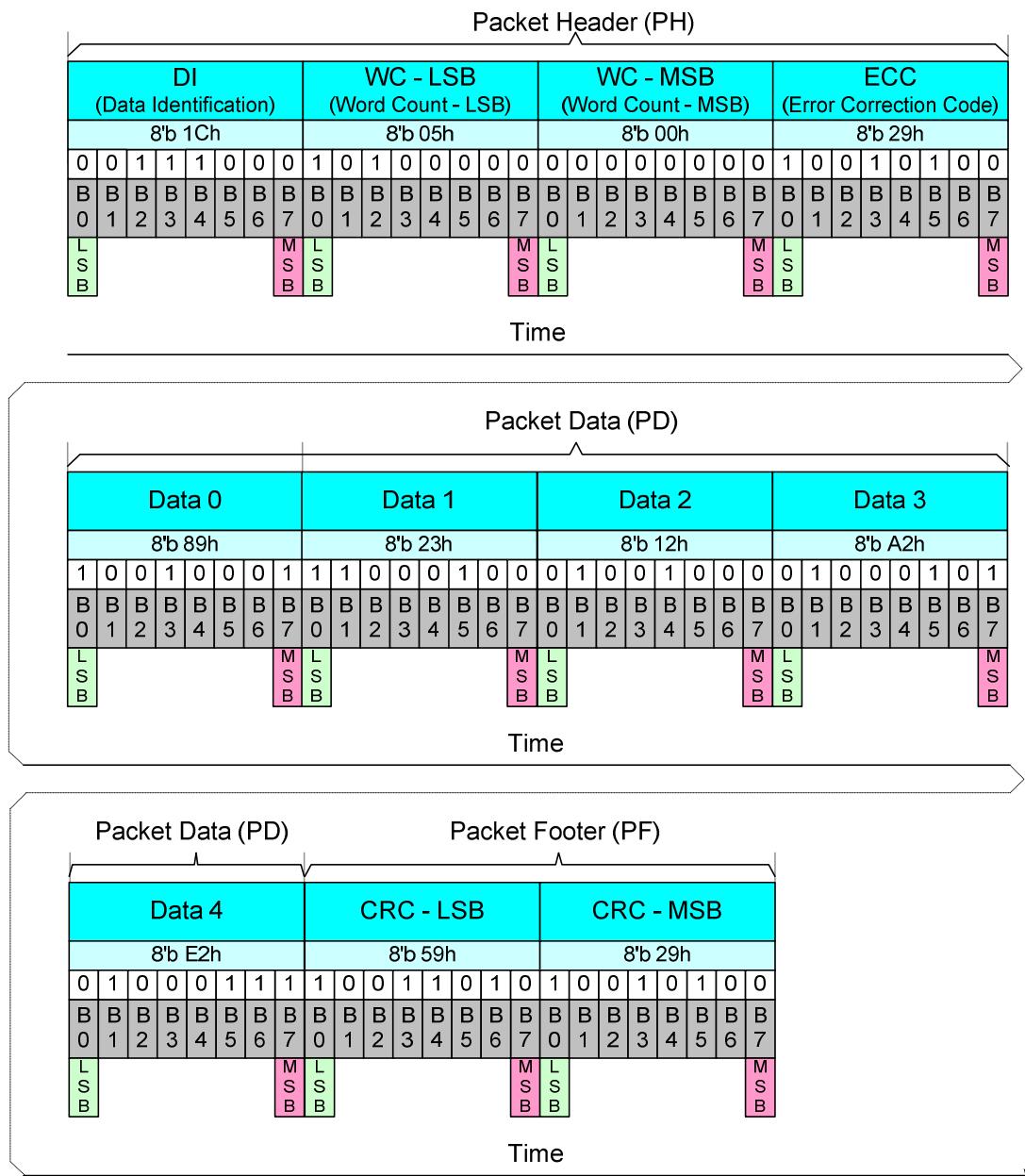


Figure 81: DCS Read Long Response (DCSRR-L) – Example

4.6.3.2.2.4 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0001b), from the display module to the MCU.

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined as:

- ◆ Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 10 0001b
 - ◆ Packet Data (PD)
 - ✧ Data 0: 45hex
 - ✧ Data 1: 00hex (Always)
 - ◆ Error Correction Code (ECC)

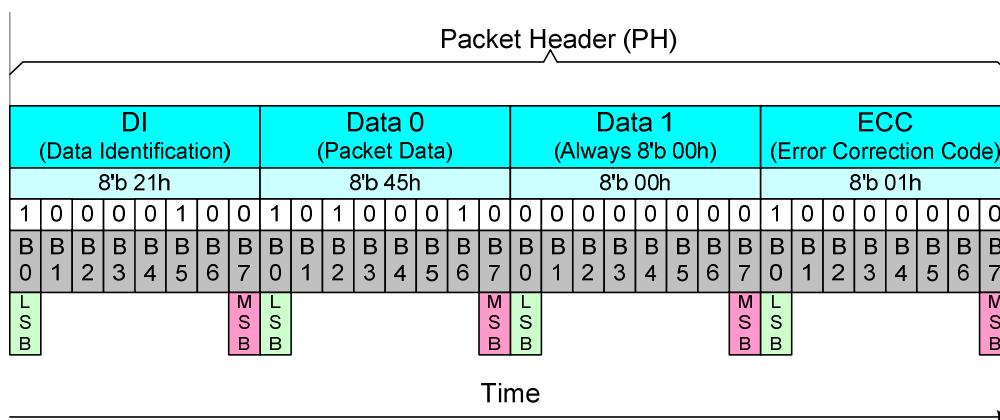


Figure 82: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) – Example

4.6.3.2.2.5 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0010b), from the display module to the MCU.

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- ◆ Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 10 0010b
 - ◆ Packet Data (PD)
 - ✧ Data 0: 45hex
 - ✧ Data 1: 32hex
 - ◆ Error Correction Code (ECC)

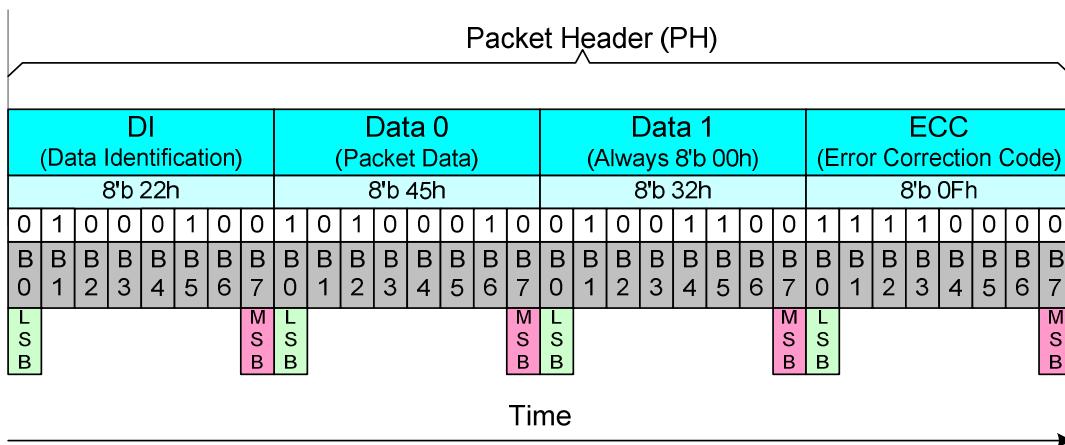


Figure 83: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) – Example

4.6.3.3. Communication Sequences

4.6.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. This communication sequence description is for DSI data lanes (MIPI_DATA_P/N), and it is assumed that the needed low level communication is done on DSI clock lanes (MIPI_CLOCK_P/N) automatically. Functions of the interface level communication are described in the following table.

Table 20: Interface Level Communication

| Interface Mode | Abbreviation | Interface Action Description |
|----------------|--------------|------------------------------|
| Low Power | LP-11 | Stop State |
| | LPDT | Low Power Data Transmission |
| | ULPS | Ultra-Low Power State |
| | RAR | Remote Application Reset |
| | TEE | Tearing Effect Event |
| | ACK | Acknowledge (No Error) |
| | BTA | Bus Turnaround |
| High Speed | HSDT | High speed Data Transmission |

Functions of the packet level communication are described in the following table.

Table 21: Packet Level Communication

| Interface Mode | Abbreviation | Packet Size | Interface Action Description |
|-----------------------------|--------------|--------------|--------------------------------|
| MCU | DCSW1-S | Short Packet | DCS Write, 1 Parameter |
| | DCSWN-S | Short Packet | DCS Write, No Parameter |
| | DCSW-L | Long Packet | DCS Write Long |
| | DCSRN-S | Short Packet | DCS Read, No Parameter |
| | SMRPS-S | Short Packet | Set Maximum Return Packet Size |
| | NP-L | Long Packet | Null Packet, No Data |
| | EoTP | Short Packet | End of Transmission Packet |
| Display Module (ILI9488) | AwER | Short Packet | Acknowledge with Error Packet |
| | DCSRR-L | Long Packet | DCS Read Long Response |
| | DCSRR1-S | Short Packet | DCS Read Short Response |
| | DCSRR2-S | Short Packet | DCS Read Short Response |

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4.6.3.3.2. Sequence

4.6.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined in the chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)”, and examples of sequences on how this packet is used are described in the following tables.

Table 22: DCS Write, 1 Parameter Sequence – Example 1

| DCS Write, 1 Parameter Sequence – Example 1 | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|---------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSW1-S | LPDT | → | -- | -- | |
| 3 | -- | LP-11 | → | -- | -- | End |

Table 23: DCS Write, 1 Parameter Sequence – Example 2

| DCS Write, 1 Parameter Sequence – Example 2 | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|----------------------------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSW1-S | HSDT | → | -- | -- | |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | End |

Table 24: DCS Write, 1 Parameter Sequence – Example 3

| DCS Write, 1 Parameter Sequence – Example 3 | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSW1-S | HSDT | → | -- | -- | |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | |
| 5 | -- | BTA | ↔ | BTA | -- | Interface Control Change from MCU to the display module |
| 6 | -- | -- | ← | LP-11 | -- | If No Error → Go to Line 8 If Error Occurs → Go to Line 13 |
| 7 | | | | | | |
| 8 | -- | -- | ← | ACK | -- | No Error |
| 9 | -- | -- | ← | LP-11 | -- | |
| 10 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 11 | -- | LP-11 | → | -- | -- | End |
| 12 | | | | | | |
| 13 | -- | -- | ← | LPDT | AwER | Error Report |
| 14 | -- | -- | ← | LP-11 | -- | |

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| | | | | | | |
|----|----|-------|---|-----|----|-----|
| 15 | -- | BTA | ↔ | BTA | -- | |
| 16 | -- | LP-11 | ➔ | -- | -- | End |

4.6.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined in the chapter “Display Command Set Write, no Parameter (DCSWN-S)”, and examples of sequences on how this packet is used are described in the following tables.

Table 25: DCS Write, No Parameter Sequence – Example 1

| DCS Write, No Parameter Sequence – Example 1 | | | | | | |
|--|---------------|------------------------|-----------------------|--------------------------|---------------|---------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | ➔ | -- | -- | Start |
| 2 | DCSWN-S | LPDT | ➔ | -- | -- | |
| 3 | -- | LP-11 | ➔ | -- | -- | End |

Table 26: DCS Write, No Parameter Sequence – Example 2

| DCS Write, No Parameter Sequence – Example 2 | | | | | | |
|--|---------------|------------------------|-----------------------|--------------------------|---------------|----------------------------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | ➔ | -- | -- | Start |
| 2 | DCSWN-S | HSDT | ➔ | -- | -- | |
| 3 | EoTP | HSDT | ➔ | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | ➔ | -- | -- | End |

Table 27: DCS Write, No Parameter Sequence – Example 3

| DCS Write, No Parameter Sequence – Example 3 | | | | | | |
|--|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | ➔ | -- | -- | Start |
| 2 | DCSWN-S | HSDT | ➔ | -- | -- | |
| 3 | EoTP | HSDT | ➔ | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | ➔ | -- | -- | |
| 5 | -- | BTA | ↔ | BTA | -- | Interface Control Change from MCU to the display module |
| 6 | -- | -- | ⬅ | LP-11 | -- | If No Error ➔ Go to Line 8 If Error Occurs ➔ Go to Line 13 |
| 7 | -- | -- | | | | |
| 8 | -- | -- | ⬅ | ACK | -- | No Error |
| 9 | -- | -- | ⬅ | LP-11 | -- | |
| 10 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 11 | -- | LP-11 | ➔ | -- | -- | End |

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| | | | | | | |
|----|----|-------|---|-------|------|--------------|
| 12 | | | | | | |
| 13 | -- | -- | ← | LPDT | AwER | Error Report |
| 14 | -- | -- | ← | LP-11 | -- | |
| 15 | -- | BTA | ↔ | BTA | -- | |
| 16 | -- | LP-11 | → | -- | -- | End |

4.6.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPA) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined in the chapter “Display Command Set Write Long (DCSW-L)”, and examples of sequences on how this packet is used are described in the following tables.

Table 28: DCS Write Long Sequence – Example 1

| DCS Write Long Sequence – Example 1 | | | | | | |
|-------------------------------------|---------------|------------------------|-----------------------|--------------------------|---------------|---------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSW-L | LPDT | → | -- | -- | |
| 3 | -- | LP-11 | → | -- | -- | End |

Table 29: DCS Write Long Sequence – Example 2

| DCS Write Long Sequence – Example 2 | | | | | | |
|-------------------------------------|---------------|------------------------|-----------------------|--------------------------|---------------|----------------------------|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSRN-S | HSDT | → | -- | -- | |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | End |

Table 30: DCS Write Long Sequence – Example 3

| DCS Write Long Sequence – Example 3 | | | | | | |
|-------------------------------------|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSRN-S | HSDT | → | -- | -- | |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | |
| 5 | -- | BTA | ↔ | BTA | -- | Interface Control Change from MCU to the display module |
| 6 | -- | -- | ← | LP-11 | -- | If No Error → Go to Line 8 If Error Occurs → Go to Line 13 |
| 7 | | | | | | |
| 8 | -- | -- | ← | ACK | -- | No Error |

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| | | | | | | |
|----|----|-------|---|-------|------|---|
| 9 | -- | -- | ← | LP-11 | -- | |
| 10 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 11 | -- | LP-11 | → | -- | -- | End |
| 12 | | | | | | |
| 13 | -- | -- | ← | LPDT | AwER | Error Report |
| 14 | -- | -- | ← | LP-11 | -- | |
| 15 | -- | BTA | ↔ | BTA | -- | |
| 16 | -- | LP-11 | → | -- | -- | End |

Table 31: DCS Write Long Sequence – Example 4

| DCS Write Long Sequence – Example 4 | | | | | | |
|-------------------------------------|---------------|------------------------|-----------------------|--------------------------|---------------|--|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | DCSW-L | HSDT | → | -- | -- | Memory Write (2Ch) |
| 3 | DCSW-L | HSDT | → | -- | -- | Memory Write Continue (3Ch) |
| 4 | DCSW-L | HSDT | → | -- | -- | Memory Write Continue (3Ch) |
| 5 | DCSW1-S | HSDT | → | -- | -- | Memory Write Continue (3Ch) with 1 Parameter |
| 6 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 7 | -- | LP-11 | → | -- | -- | End |

Note: This is an example that image data are sent in 4 packets.

4.6.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined in the chapter “Display Command Set Read, No Parameter (DCSRN-S)”, and examples of sequences on how this packet is used are described in the following tables.

Table 32: DCS Read, No Parameter Sequence – Example 1

| DCS Read, No Parameter Sequence – Example 1 | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | SMRPS-S | HSDT | → | -- | -- | Defined how many data byte is wanted to read : 1 byte |
| 3 | DCSRN-S | HSDT | → | -- | -- | Wanted to get a response ID1 (DAh) |
| 4 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 5 | -- | LP-11 | → | -- | -- | |
| 6 | -- | BTA | ↔ | BTA | -- | Interface Control Change from MCU to the display module |
| 7 | -- | -- | ← | LP-11 | -- | If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19 |
| 8 | | | | | | |

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| | | | | | | |
|----|----|-------|---|-------|----------|---|
| 9 | -- | -- | ↔ | LPDT | DCSRR1-S | Response 1 byte return |
| 10 | -- | -- | ↔ | LP-11 | -- | |
| 11 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 12 | -- | LP-11 | → | -- | -- | End |
| 13 | | | | | | |
| 14 | -- | -- | ↔ | LPDT | AwER | Error Report |
| 15 | -- | -- | ↔ | LP-11 | -- | |
| 16 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 17 | -- | LP-11 | → | -- | -- | End |
| 18 | | | | | | |
| 19 | -- | -- | ↔ | LPDT | DCSRR1-S | Response 1 byte return |
| 20 | -- | -- | ↔ | LPDT | AwER | Error Report (Error is corrected by ECC) |
| 21 | | | ↔ | LP-11 | -- | |
| 22 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 23 | -- | LP-11 | → | -- | -- | End |

Table 33: DCS Read, No Parameter Sequence – Example 2

| DCS Read, No Parameter Sequence – Example 2 | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | SMRPS-S | HSDT | → | -- | -- | Defined how many data byte is wanted to read : 200 bytes |
| 3 | DCSRN-S | HSDT | → | -- | -- | Wanted to get a response "Memory Read" (2Eh) |
| 4 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 5 | -- | LP-11 | → | -- | -- | |
| 6 | -- | BTA | ↔ | BTA | -- | Interface Control Change from MCU to the display module |
| 7 | -- | -- | ↔ | LP-11 | -- | If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19 |
| 8 | | | | | | |
| 9 | -- | -- | ↔ | LPDT | DCSRR-L | Response 200 byte return |
| 10 | -- | -- | ↔ | LP-11 | -- | |
| 11 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 12 | -- | LP-11 | → | -- | -- | End |
| 13 | | | | | | |
| 14 | -- | -- | ↔ | LPDT | AwER | Error Report |
| 15 | -- | -- | ↔ | LP-11 | -- | |
| 16 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 17 | -- | LP-11 | → | -- | -- | End |
| 18 | | | | | | |
| 19 | -- | -- | ↔ | LPDT | DCSRR-S | Response 200 byte return |
| 20 | -- | -- | ↔ | LPDT | AwER | Error Report (Error is corrected by ECC) |

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| | | | | | | |
|----|----|-------|---|-------|----|---|
| 21 | | | ← | LP-11 | -- | |
| 22 | -- | BTA | ↔ | BTA | -- | Interface Control Change from the display module to MCU |
| 23 | -- | LP-11 | → | -- | -- | End |

4.6.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined in the chapter “Null Packet, No Data (NP-L)” and an example of the sequence on how this packet is used is described in the following table.

Table 34: Null Packet, No Data Sequence -- Example

| Null Packet, No Data Sequence – Example | | | | | | |
|---|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | NP-L | HSDT | → | -- | -- | Only High Speed Data Transmission is used |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | End |

4.6.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined in the chapter “End of Transmission Packet (EoTP)” and an example of the sequence on how this packet is used is described in the following table.

Table 35: End of Transmission Packet – Example

| End of Transmission Packet – Example | | | | | | |
|--------------------------------------|---------------|------------------------|-----------------------|--------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module (ILI9488) | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | -- | LP-11 | → | -- | -- | Start |
| 2 | NP-L | HSDT | → | -- | -- | Only High Speed Data Transmission is used |
| 3 | EoTP | HSDT | → | -- | -- | End of Transmission Packet |
| 4 | -- | LP-11 | → | -- | -- | End |

4.6.3.4. 16 Bit/Pixel Writing

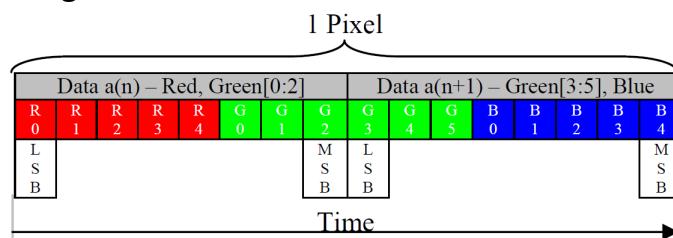


Figure 84: One Pixel Bit and Write Color Orders

The MCU can send the following packet to the display module.

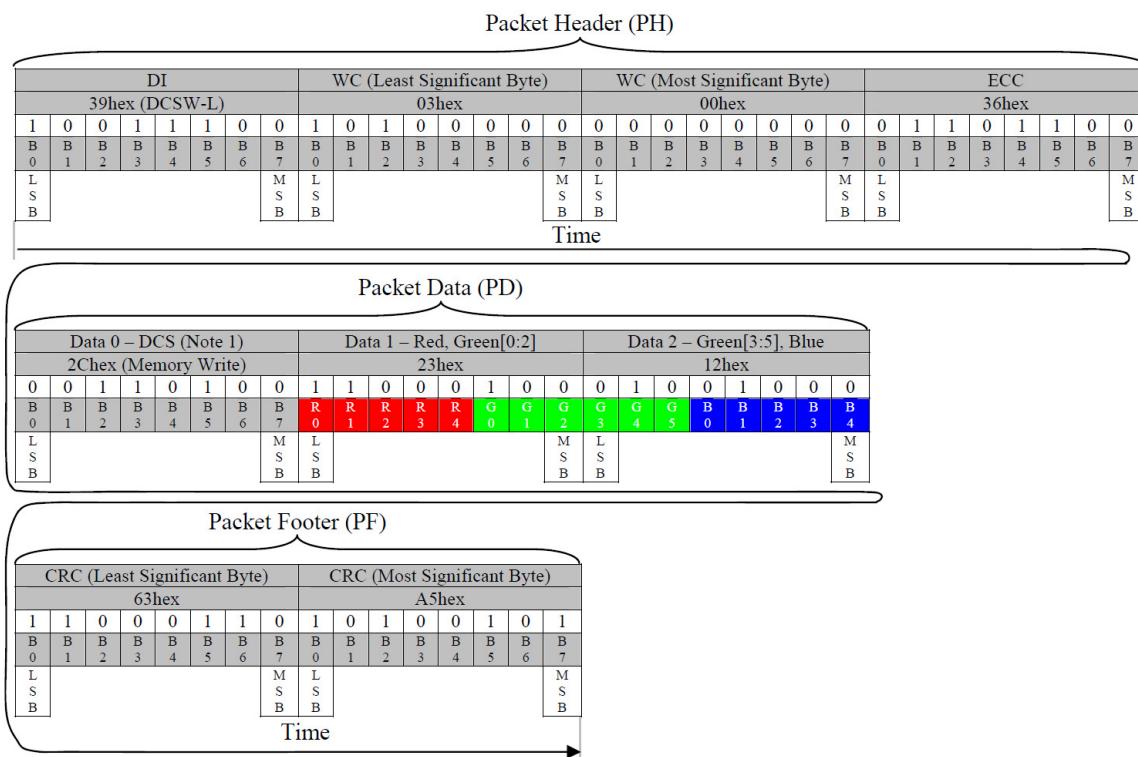


Figure 85: One Pixel Write (DCSW-L) – Example 1

Notes:

1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
2. It is possible that one pixel information is split into different packets, which ends and starts as follows: RG – GB (2 packets).
3. A packet can include several pixels (not just one pixel as in this example).

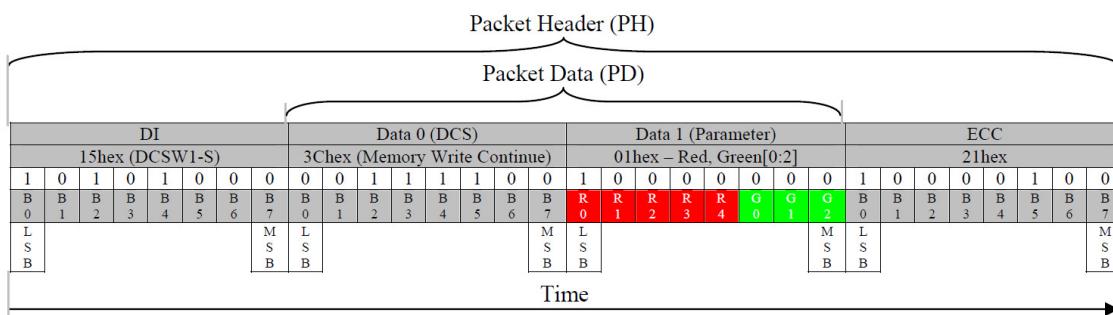


Figure 86: Red/Green [0:2] Sub-pixel Write (DCSW1-S) – Example 2

Note: DCS (Data 0) can also be “Memory Write” (2Ch) command.

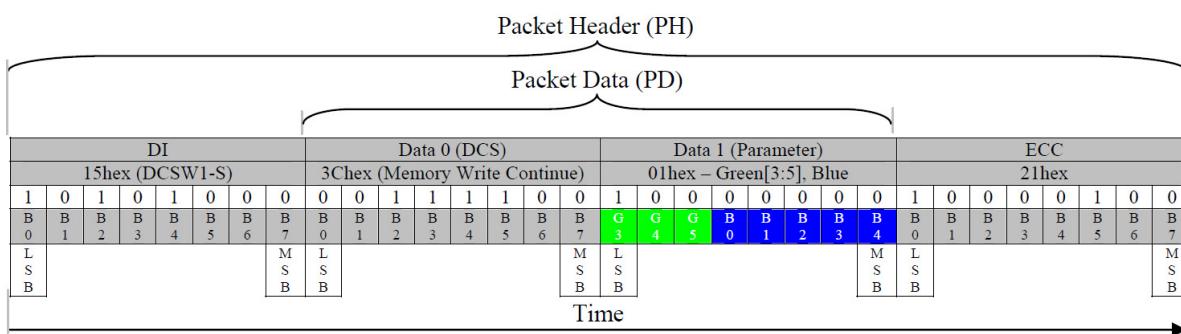


Figure 87: Green [3:5]/Blue Sub-pixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is R [0:4] G [0:2].

4.6.3.5. 24 Bit/Pixel Writing

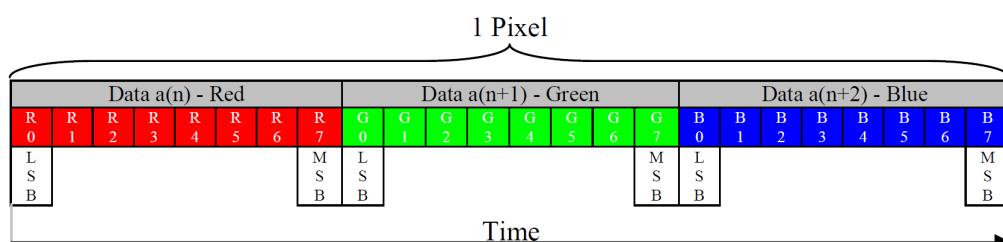


Figure 88: One Pixel Bit and Color Write Orders

The MCU can send the following packet to the display module.

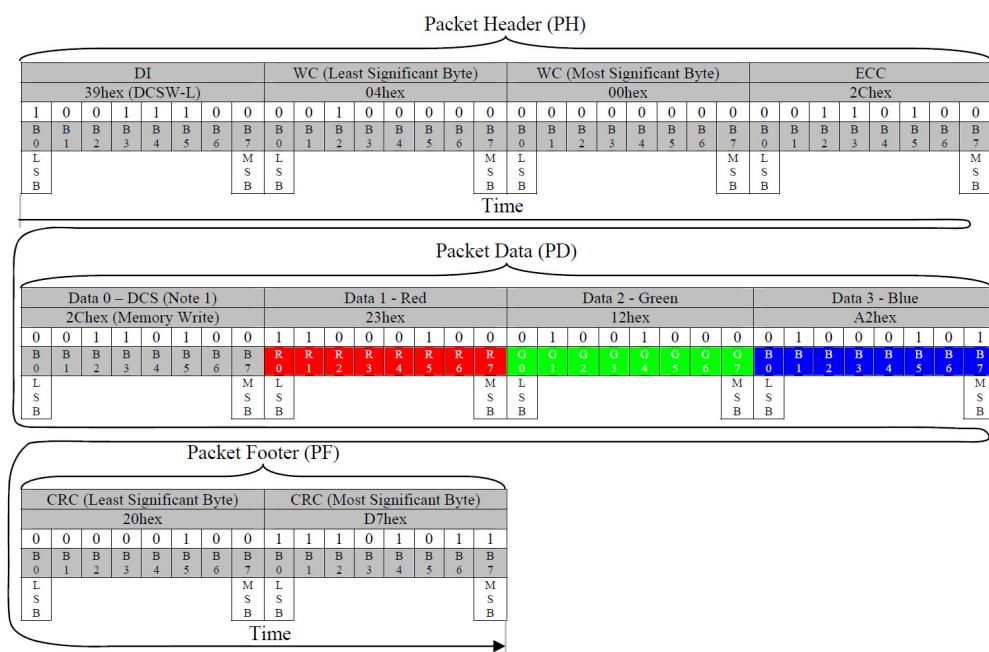


Figure 89: One Pixel Write (DCSW-L) – Example 1

Notes:

1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
2. It is possible that one pixel information is split into two or three different packets which end and start as follows:
 - R – GB (2 packets)
 - RG – B (2 packets)
 - R – G – B (3 packets)
3. A packet can include several pixels (not just one pixel as in this example).

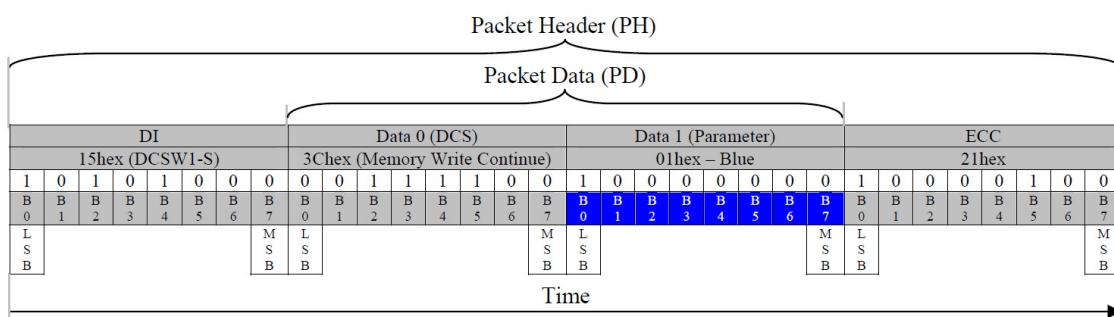


Figure 90: Blue Sub-pixel Write (DCSW1-S) – Example 2

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is G [0:7].

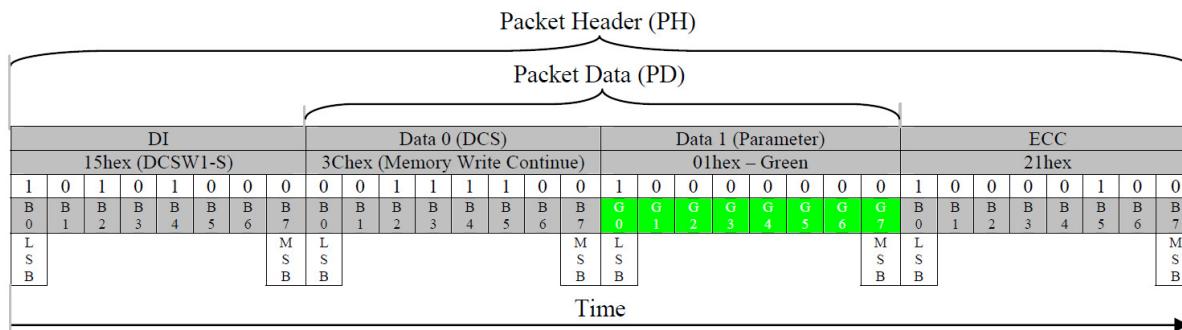


Figure 91: Green Sub-pixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is R [0:7].

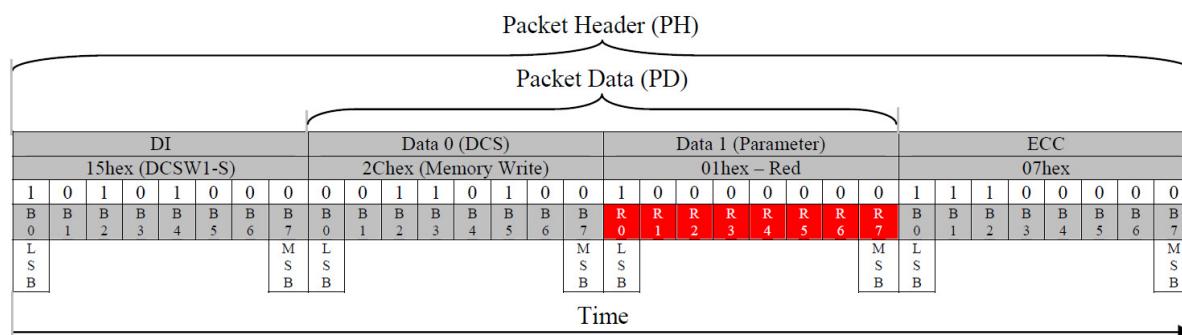


Figure 92: Red Sub-pixel Write (DCSW1-S) – Example 4

Notes:

1. DCS (Data 0) can also be “Memory Write Continue” (3Ch) command.
2. Previous data byte is B [0:7].

4.6.3.5.1. 24 Bit/Pixel Reading

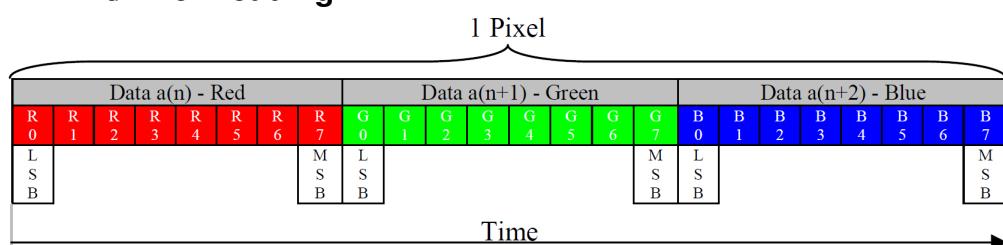


Figure 93: One Pixel Bit and Color Read Order

The display module can send following packets to the MCU after the MCU has sent a read command “Memory Read (2Eh)” or “Memory Read Continue (3Eh)”.

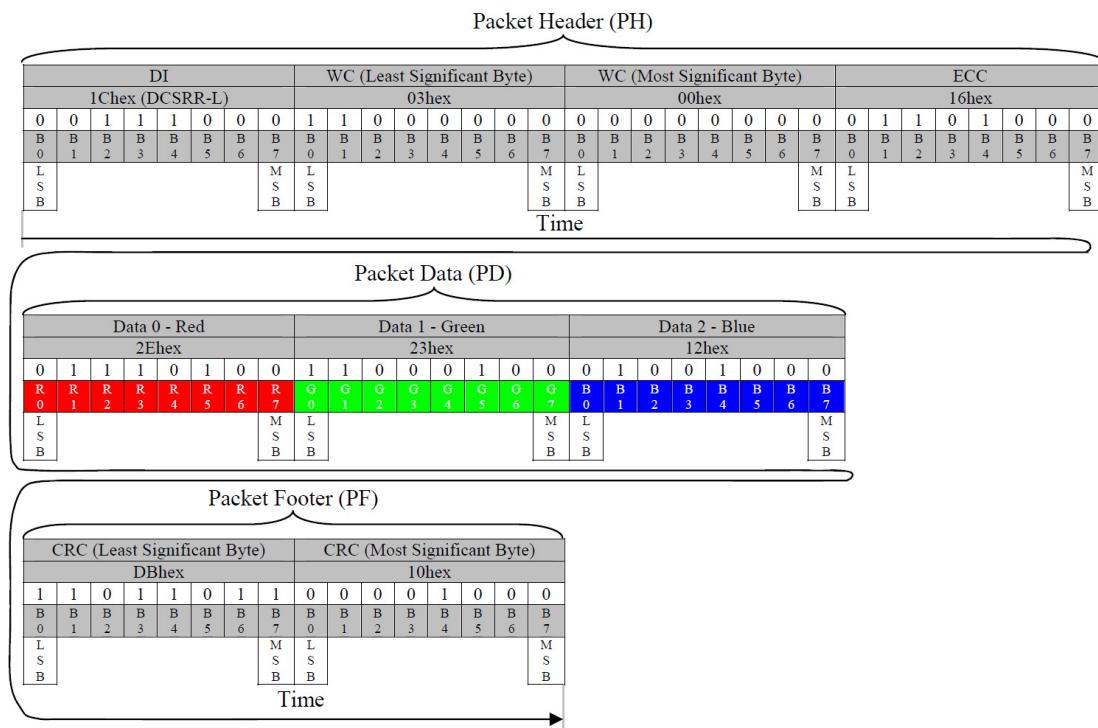


Figure 94: One Pixel Read Response (DCSRR-L) – Example 1

Note: It is possible that one pixel information is split into two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)

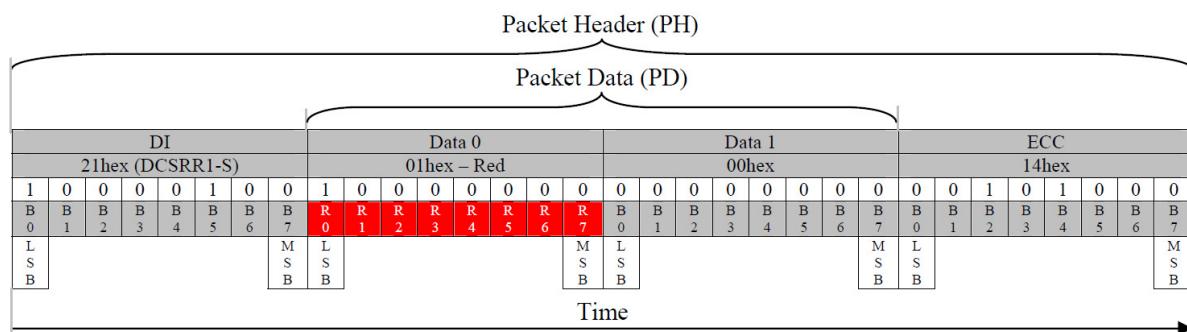
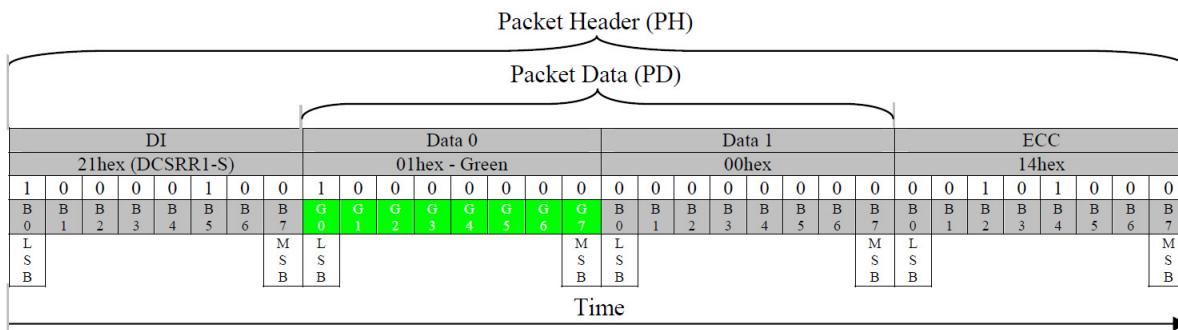


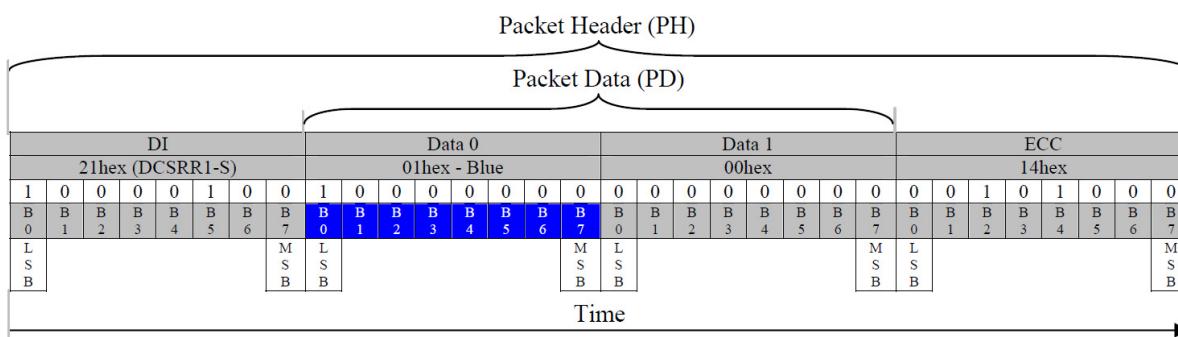
Figure 95: Red Sub-pixel Response (DCSRR1-S) – Example 2

Notes:

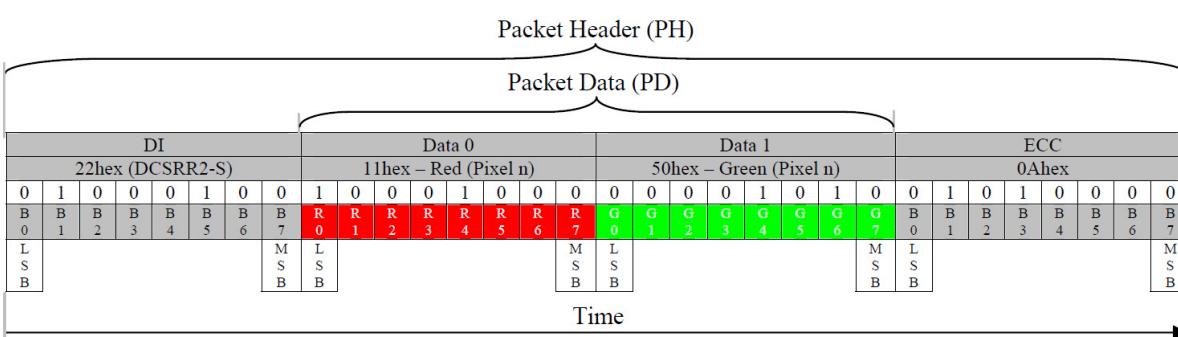
1. Data 1 is always 00h.
2. Previous data byte is B [0:7].


Figure 96: Green Sub-pixel Response (DCSRR1-S) – Example 3
Notes:

1. Data 1 is always 00h.
2. Previous data byte is R [0:7].


Figure 97: Blue Sub-pixel Response (DCSRR1-S) – Example 4
Notes:

1. Data 1 is always 00h.
2. Previous data byte is G [0:7].


Figure 98: Red and Green Sub-pixels Response (DCSRR2-S) – Example 5

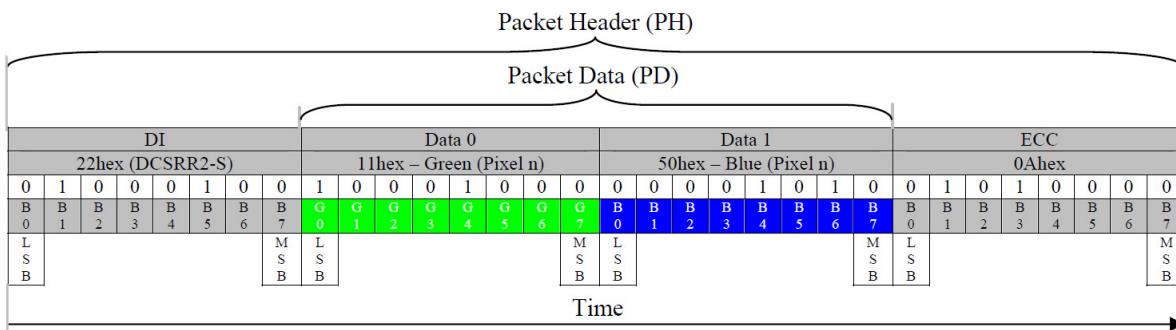


Figure 99: Green and Blue Sub-pixels Response (DCSRR2-S) – Example 6

Note: Previous data byte is R [0:7].

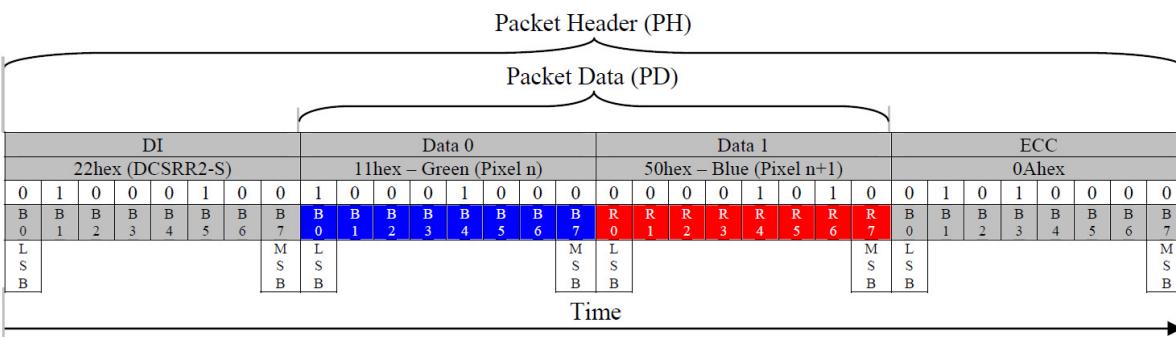


Figure 100: Blue and Red Sub-pixels Response (DCSRR2-S) – Example 7

Note: Previous data byte is G [0:7].

4.7. Display Data Format

4.7.1. DBI Type C Option 1 (3-Line Serial Interface)

The 3-line/9-bit serial bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 101. Figure 101 describes an interface with 8080 MCU system interface.

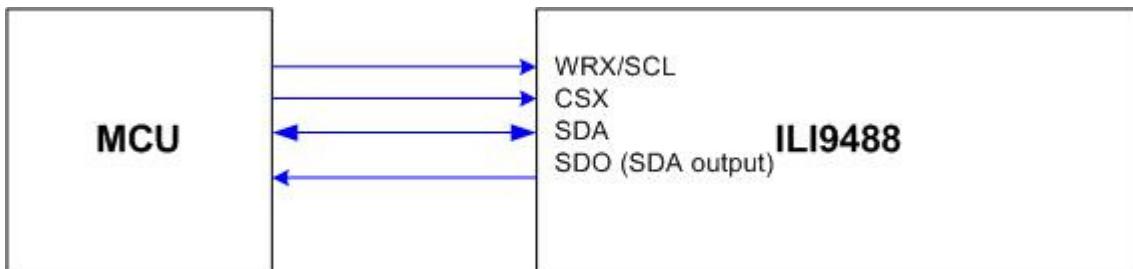


Figure 101: 3-Line Serial Interface

The available display data formats are:

- 8 colors, RGB 1, 1, 1 bits input (set Standard Command 3Ah, DBI [2:0] as 001)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.1.1. SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

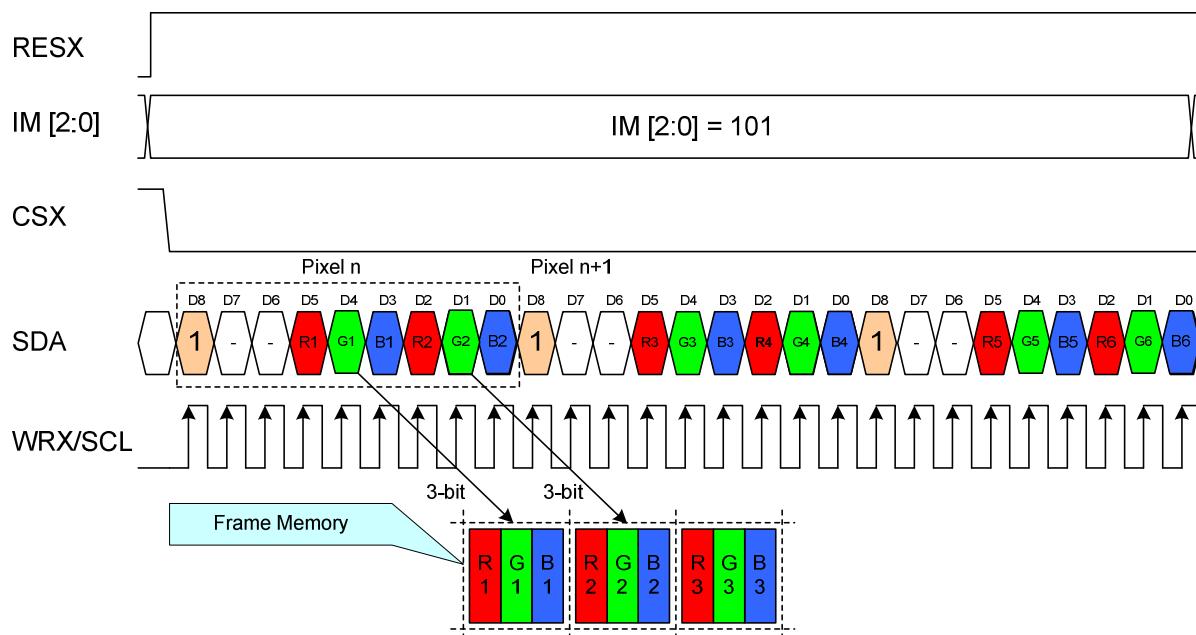


Figure 102: SPI Data for 3 bit/pixel (RGB 1-1-1 Bits Input), 8-color

Notes:

1. One pixel data contains 3-bit color depth information.
2. '-' = void

4.7.1.2. SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

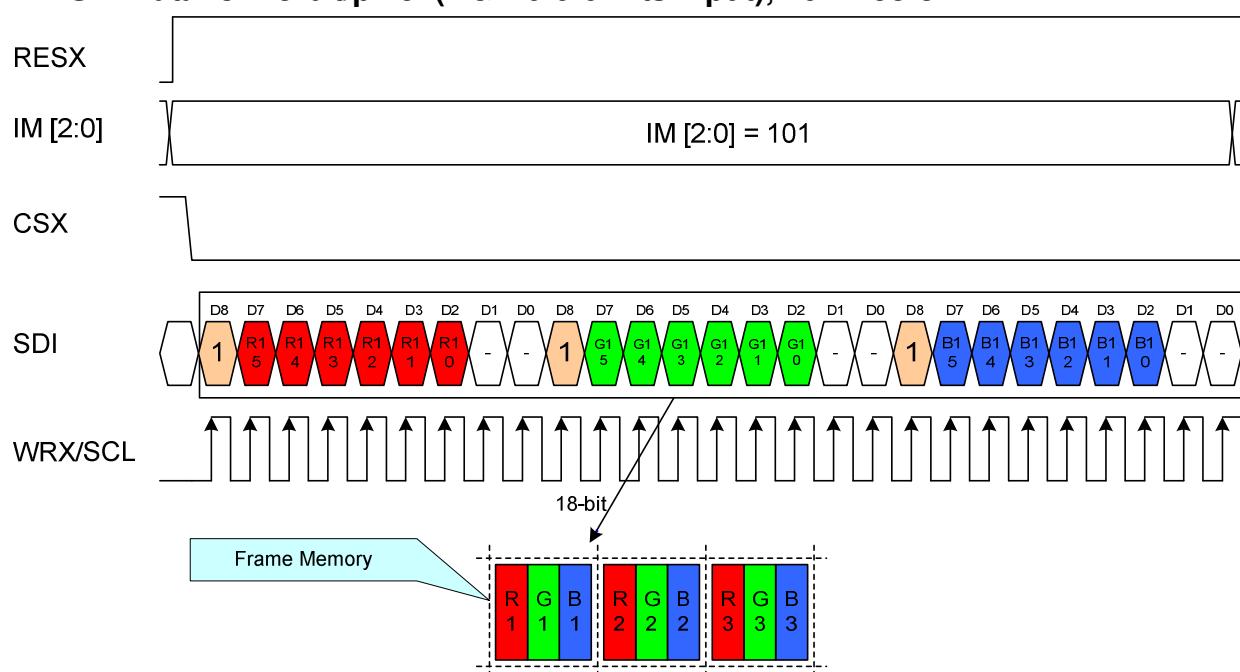


Figure 103: SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. One pixel data contains 18-bit color depth information.
2. The most significant bits are: R x 5, G x 5, and B x 5.
3. The least significant bits are: R x 0, G x 0, and B x 0.
4. '-' = void

Read data through 3-line SPI mode

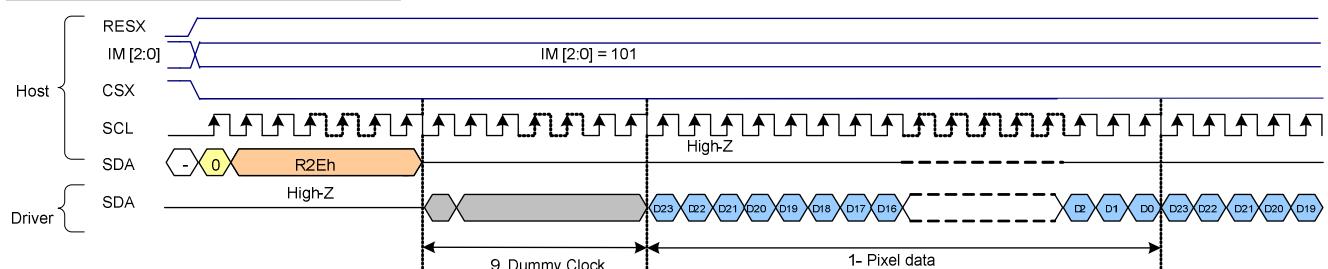


Figure 104: 3-Line SPI Mode Read Data

Note: '-' = void

4.7.2. DBI Type-C Option 3 (4-Line Serial Interface)

The 4-line/8-bit serial bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 111. Figure 105 describes an interface with 8080 MCU system interface.

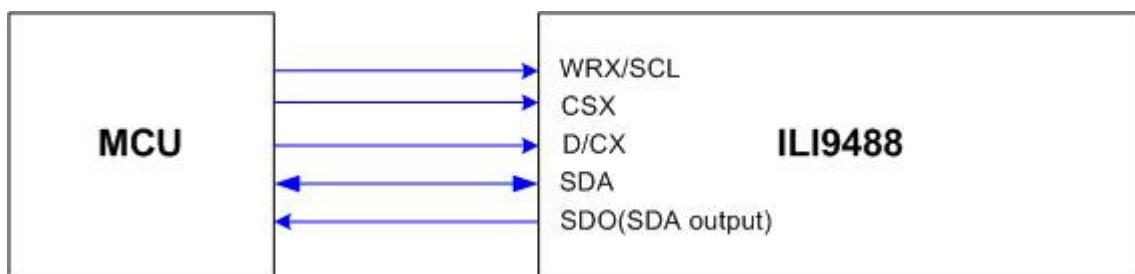


Figure 105: 4-Line Serial Interface

The available display data formats are:

- 8 colors, RGB 1, 1, 1 bits input (set Standard Command 3Ah, DBI [2:0] as 001)
- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.2.1. SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

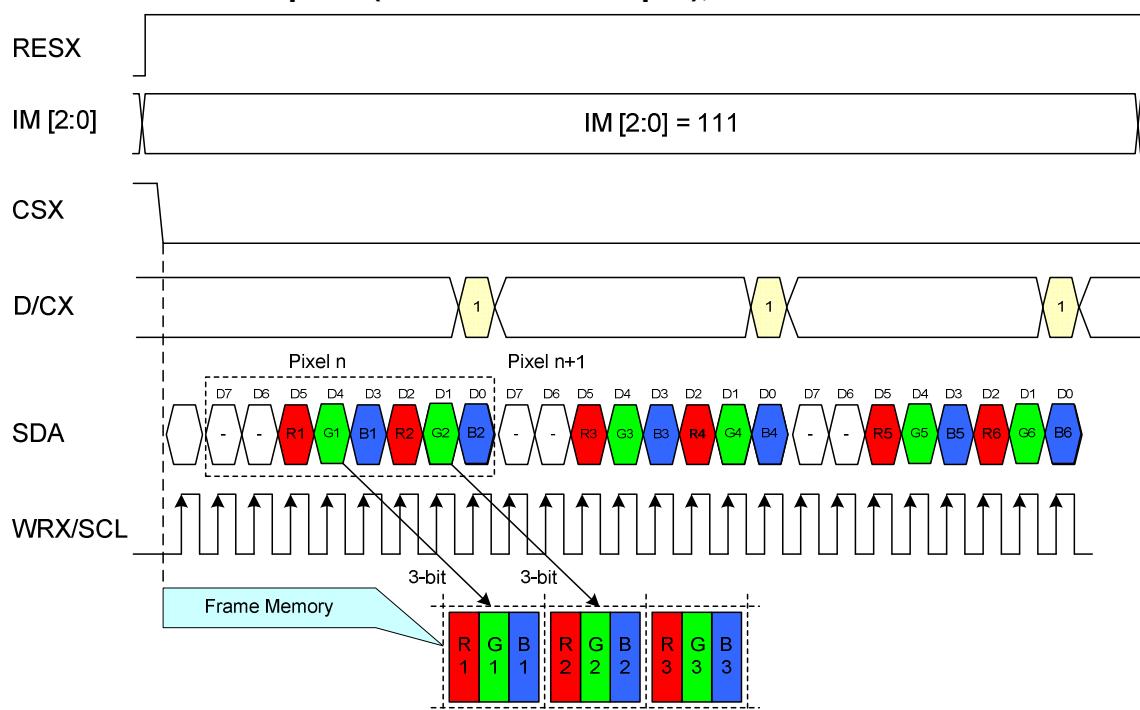


Figure 106: SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

Notes:

1. One pixel data contains 3-bit color depth information.
2. '-' = void

4.7.2.2. SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

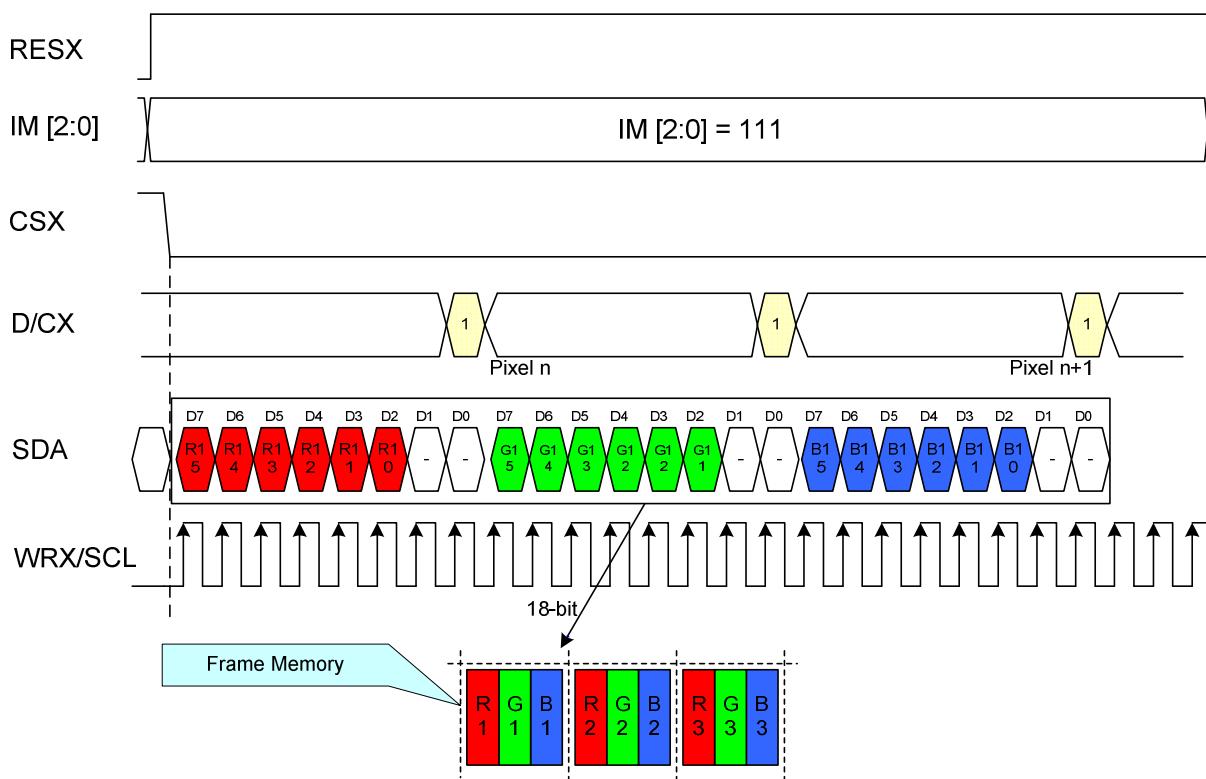


Figure 107: SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. One pixel data contains 18-bit color depth information.
2. The most significant bits are: R x 5, G x 5, and B x 5.
3. The least significant bits are: R x 0, G x 0, and B x 0.
4. '-' = void

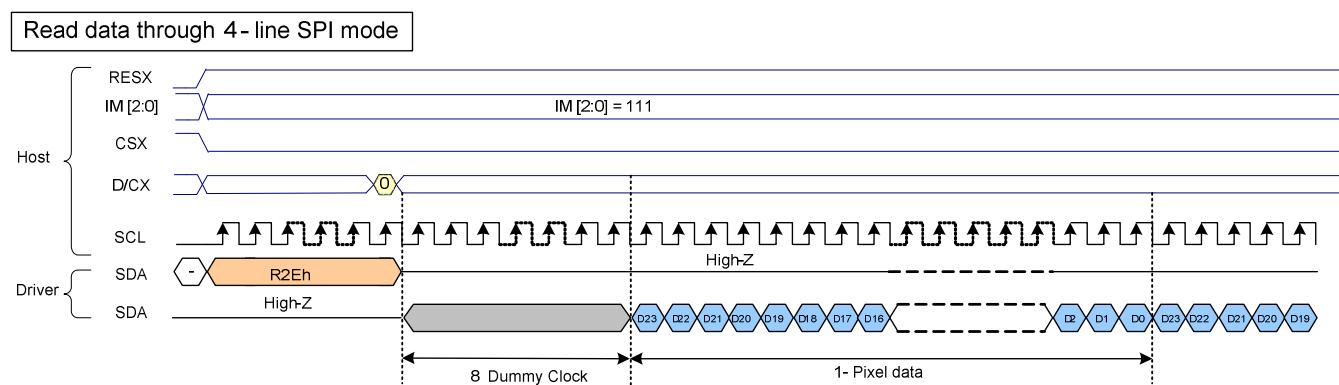


Figure 108: 4-Line SPI Mode Read Data

Note: '-' = Leave these pins open.

4.7.3. 8-bit Parallel MCU Interface

The DBI TYPE B 8-bit parallel bus interface of the ILI9488 is used by setting the external pin IM [2:0] as 011. Figure 109 shows this system interface.

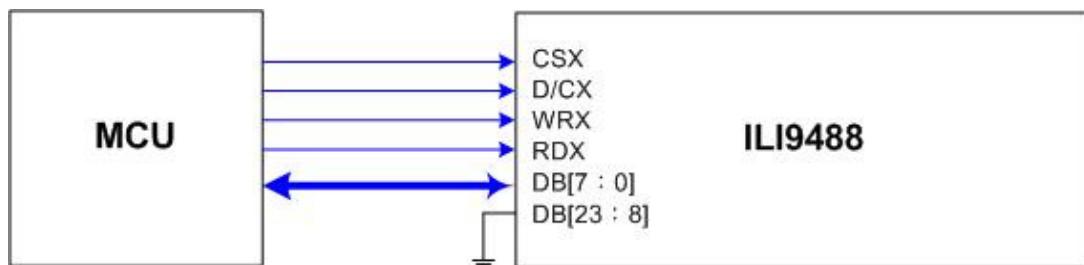


Figure 109: 8-bit Parallel MCU Interface

The available display data formats are:

- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.3.1. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

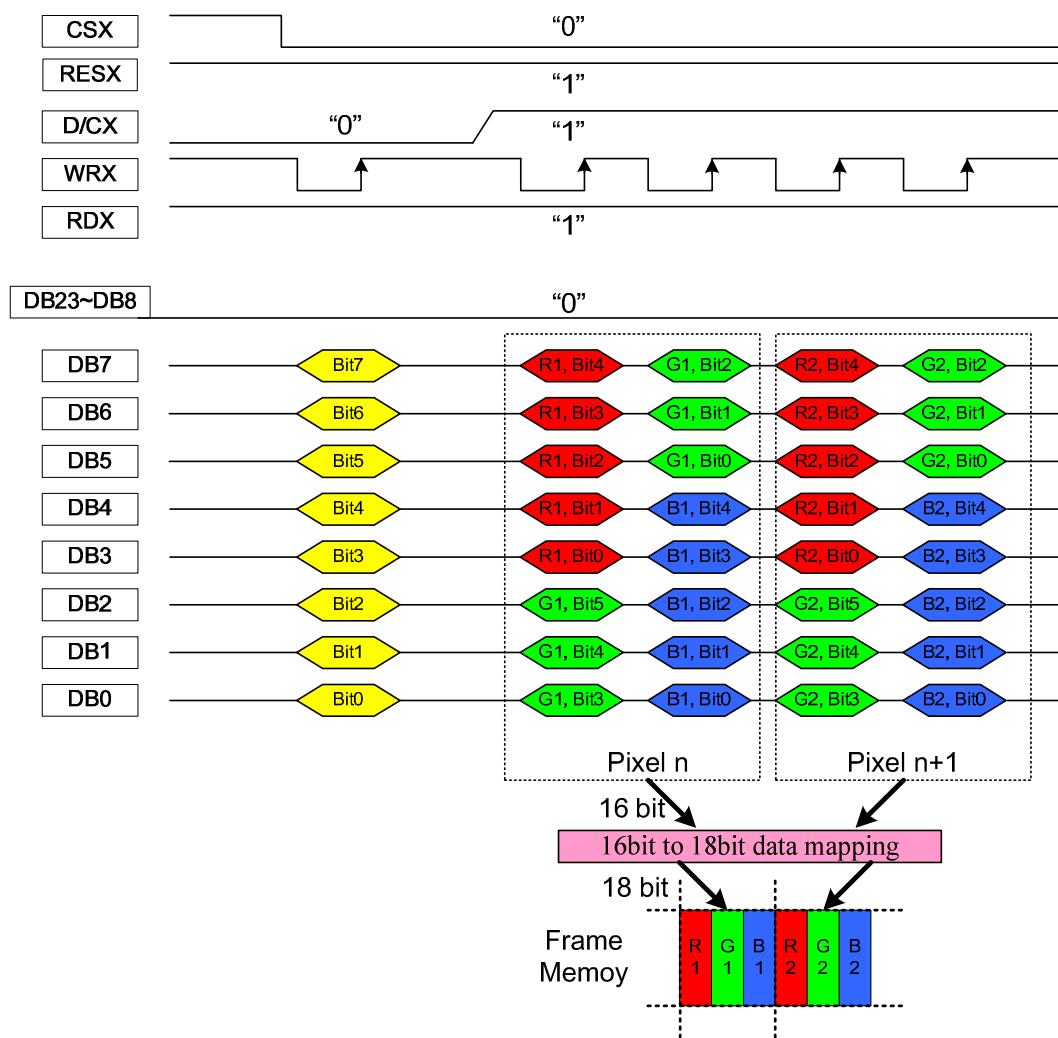


Figure 110: 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green data, and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

4.7.3.2. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

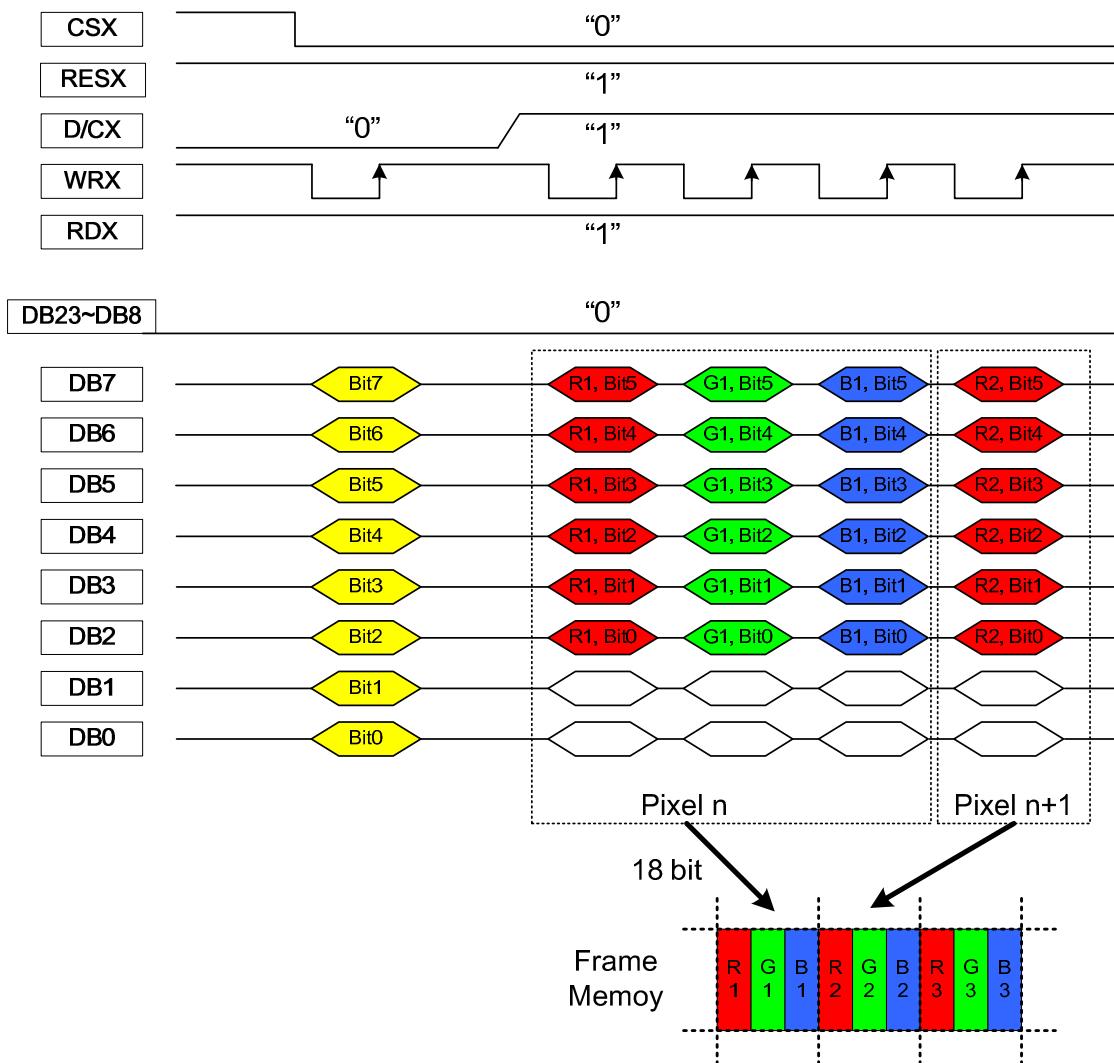


Figure 111: 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

4.7.4. 9-bit Parallel MCU Interface

The DBI TYPE B 9-bit parallel bus interface of the ILI9488 is used by setting the external pin IM [2:0] as 001. Figure 112 shows this system interface.

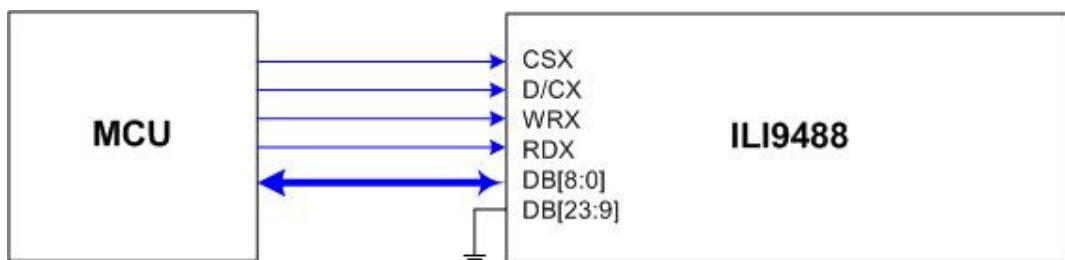


Figure 112: 9-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.4.1. 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

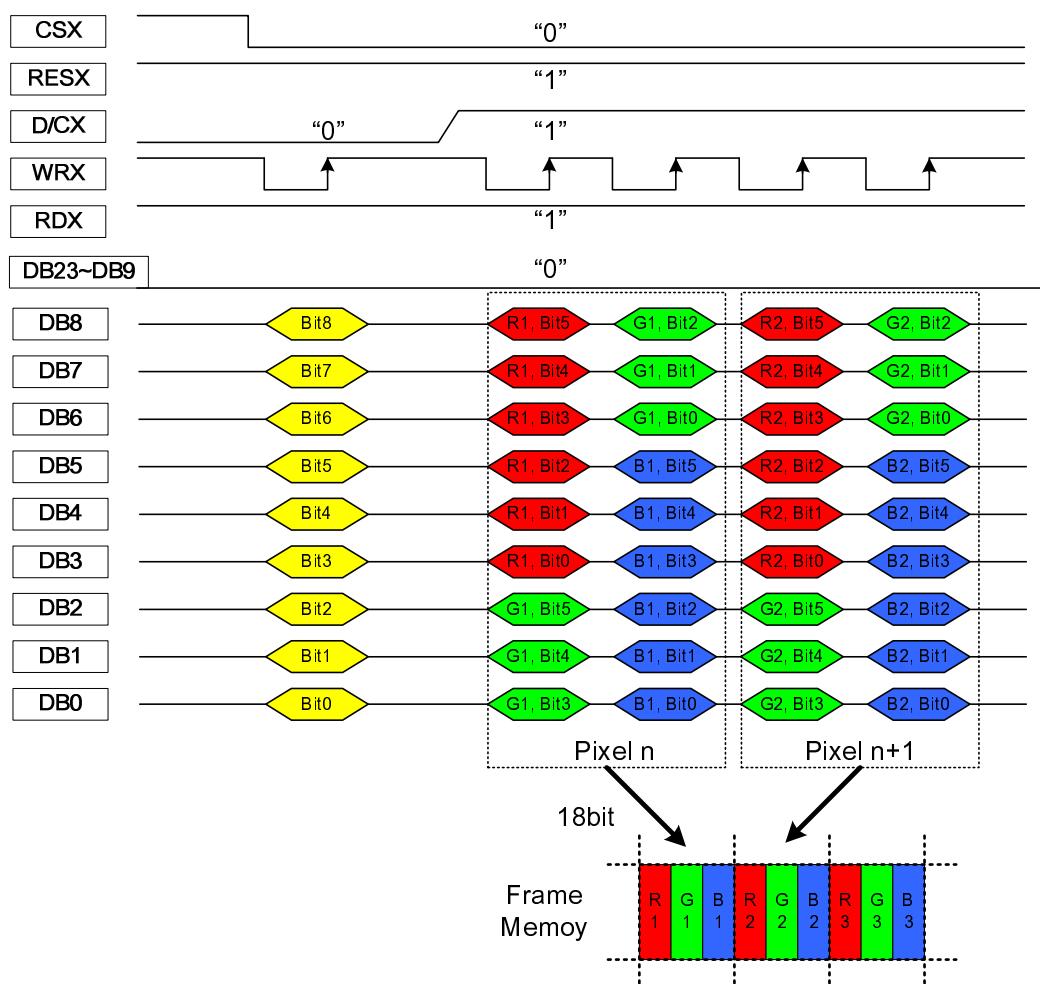


Figure 113: 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB= DB8, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red

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and Blue data.

2. 2-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

4.7.5. 16-bit Parallel MCU Interface

The 8080-system 16-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 010. Figure 114 shows this system interface.

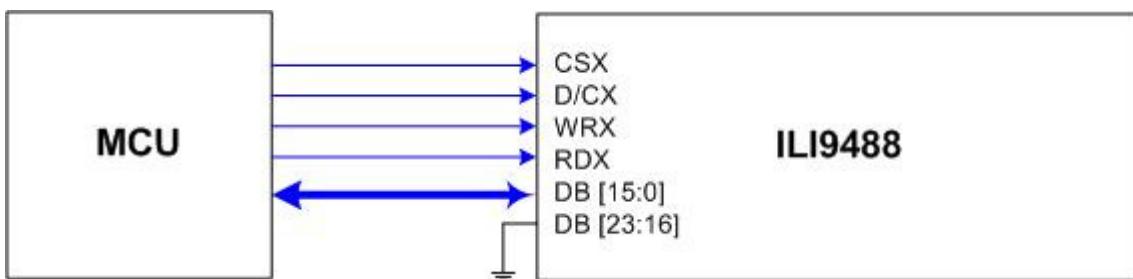


Figure 114: 16-bit Parallel MCU Interface

The available display data formats are:

- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.5.1. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

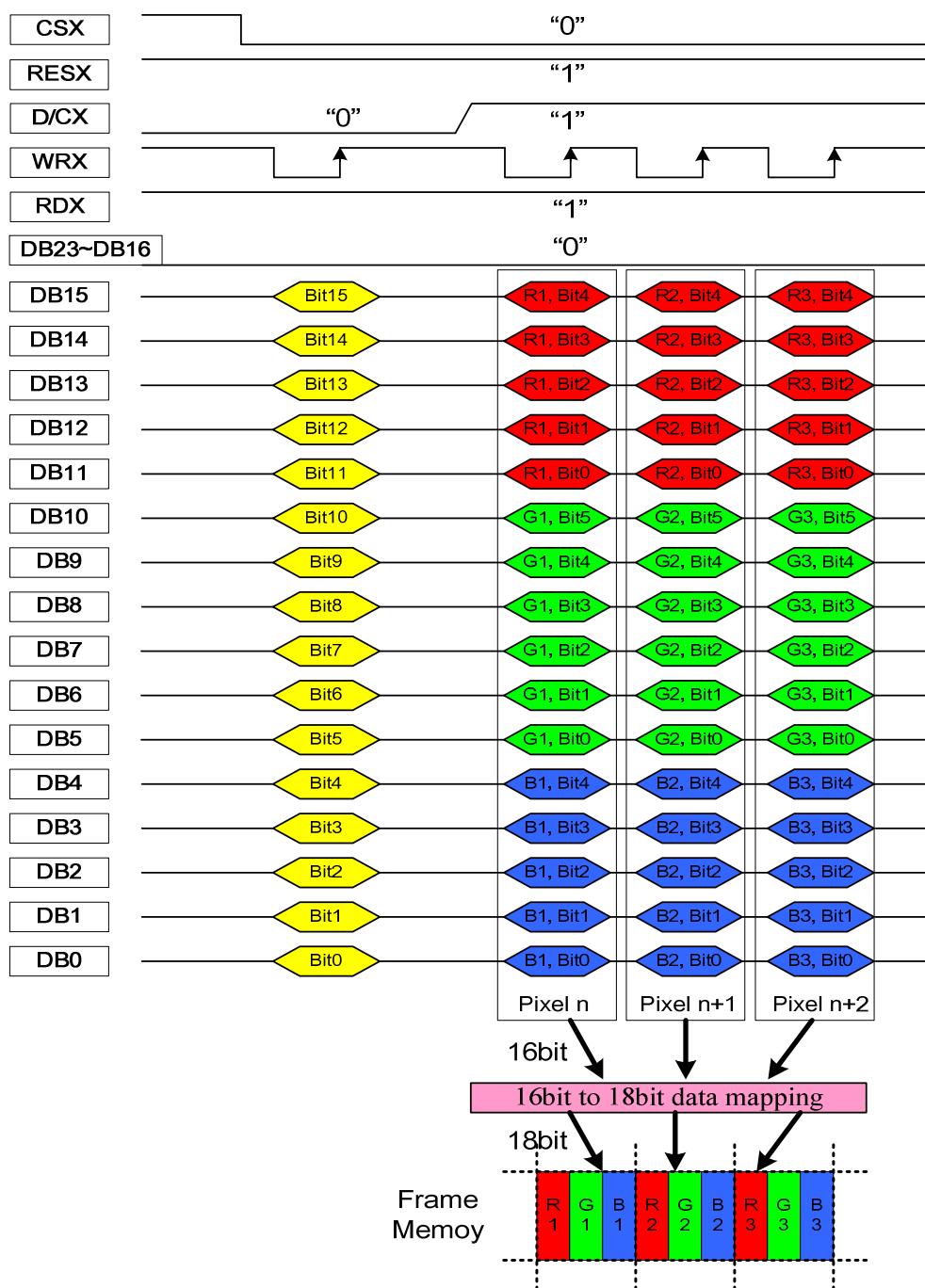


Figure 115: 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green data, and MSB = Bit 4, LSB = Bit0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

4.7.5.2. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

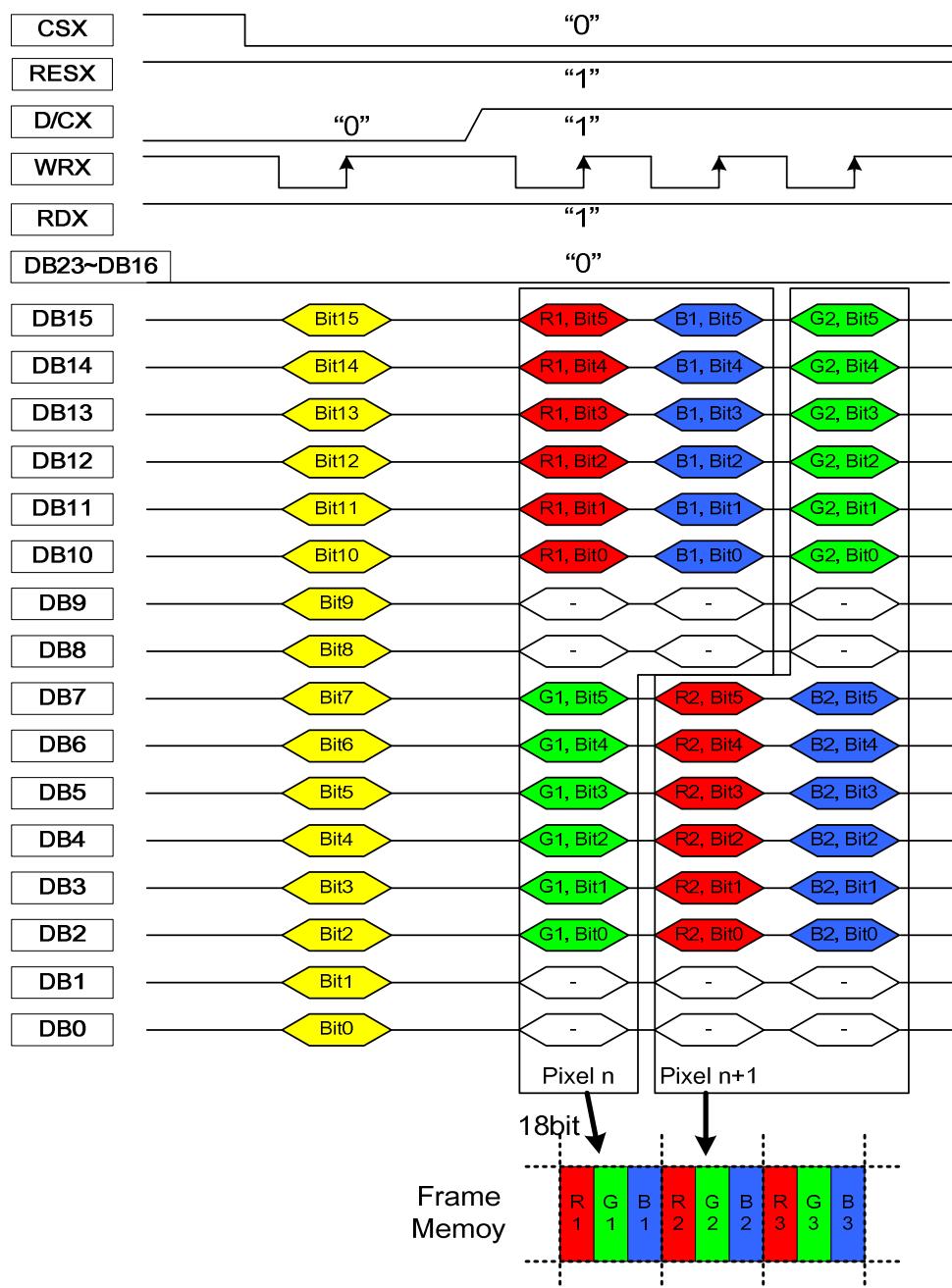


Figure 116: 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 2 pixel data to the 18-bit color depth information.
3. '-' = void

4.7.6. 18-bit Parallel MCU Interface

The 8080-system 18-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 000.

Figure 117 shows this system interface.

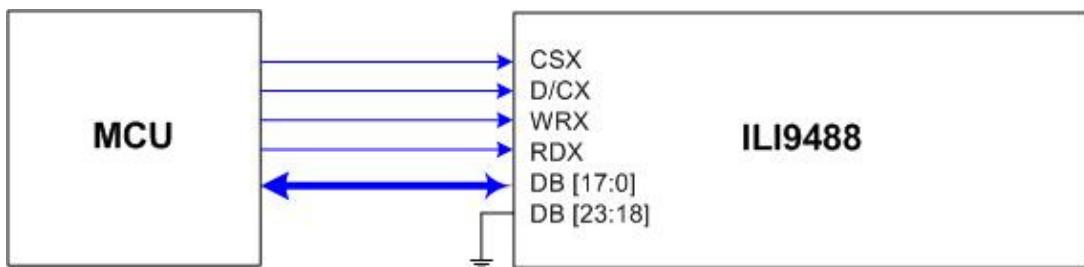


Figure 117: 18-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 6, 6, 6 -bits input data (set Standard Command 3Ah, DBI [2:0] = 110)

4.7.6.1. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

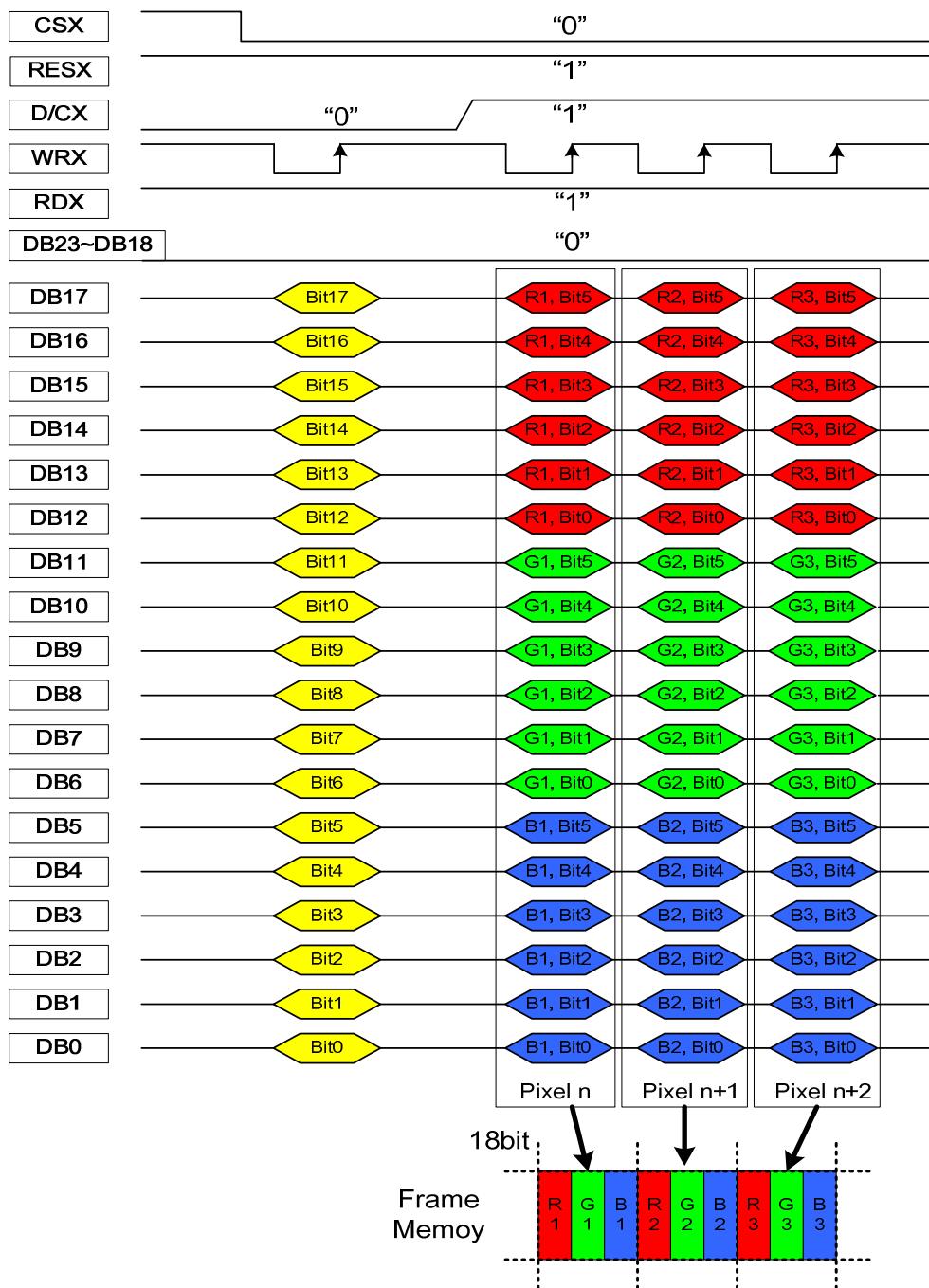


Figure 118: 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

4.7.7. 24-bit Parallel MCU Interface

The 8080-system 24-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 000 and register setting DB_EN as 1. Figure 119 shows this system interface.

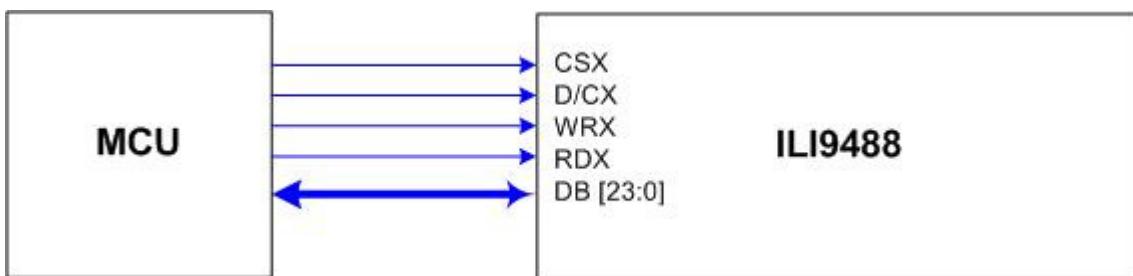


Figure 119: 24-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 8, 8, 8 -bits input data (set Standard Command 3Ah, DBI [2:0] = 111)

4.7.7.1. 24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 Bits Input), 262K-color

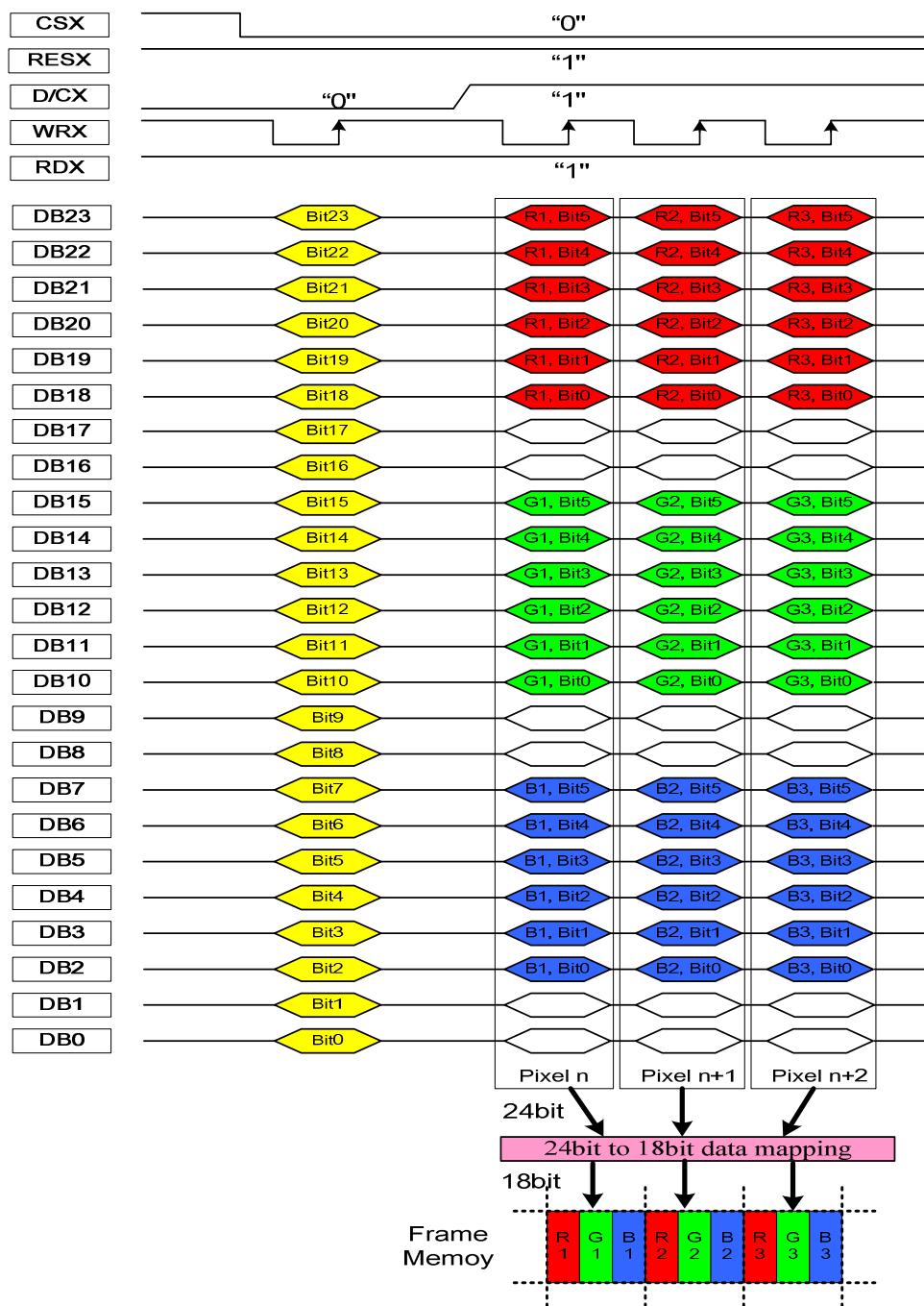


Figure 120: 24-bit Data Bus for 18-bit/pixel (RGB 8-8-8 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

4.8. DPI Parallel Interface (RGB Interface)

4.8.1. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits as 101. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 16-bit RGB data bus in synchronization with the display operation.

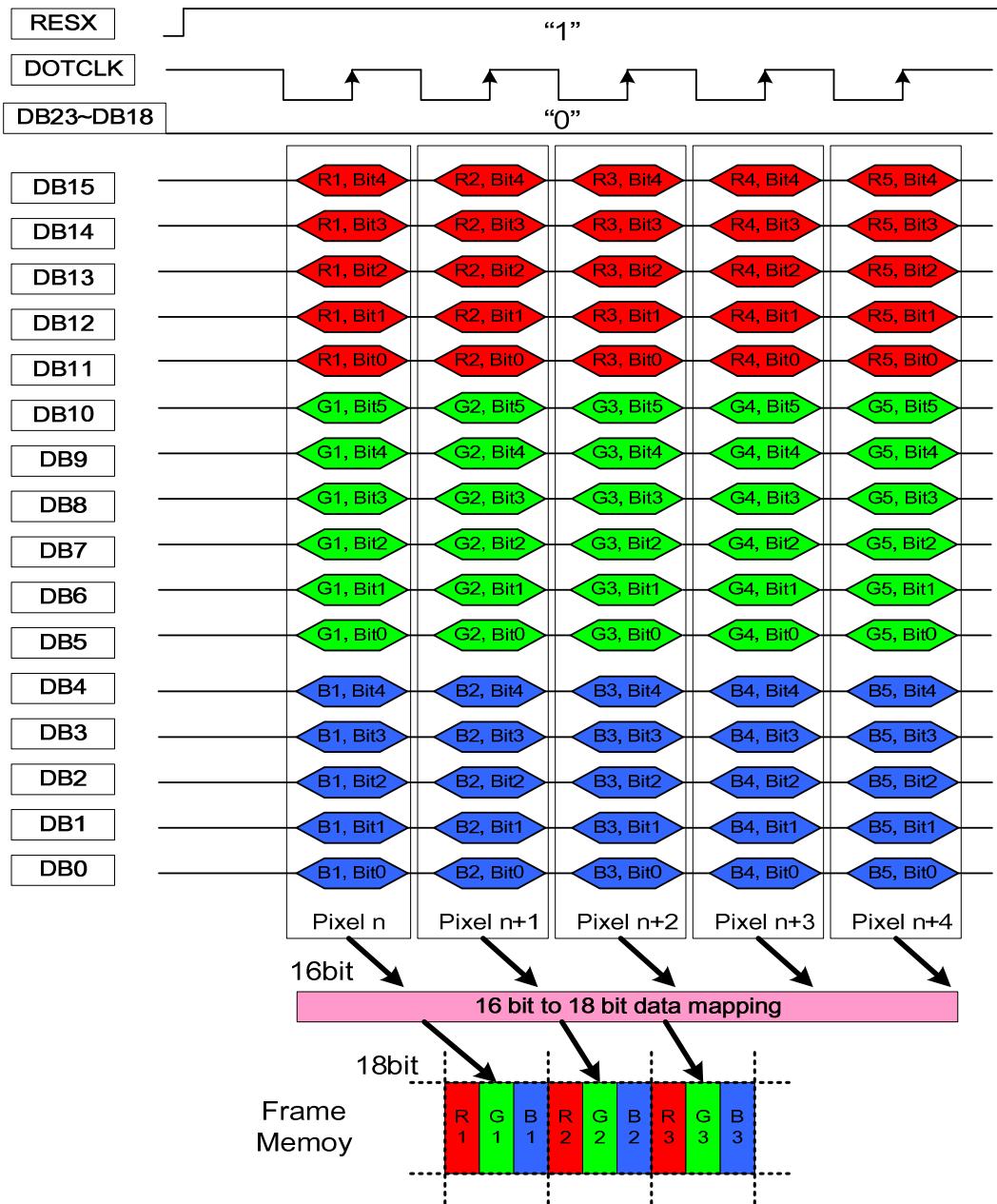


Figure 121: 16-bit/pixel 65K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.

4.8.2. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits as 110. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.

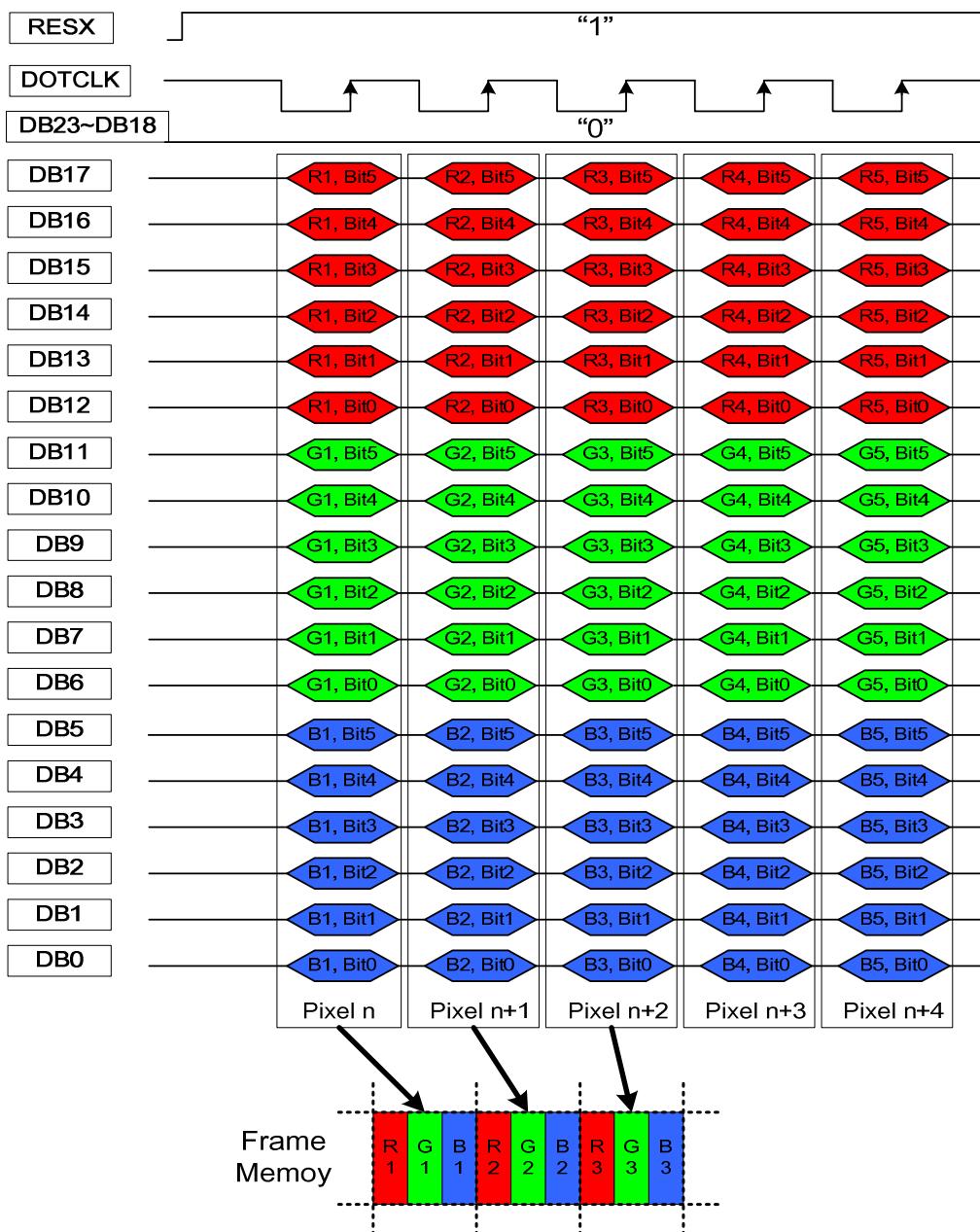


Figure 122: 18-bit/pixel 262K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

4.8.3. 24-bit Parallel RGB Interface

4.8.3.1. 18-bit/pixel

The 24-bit RGB interface is selected by setting the DPI [2:0] bits to 111 and DB_EN to 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE, and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.

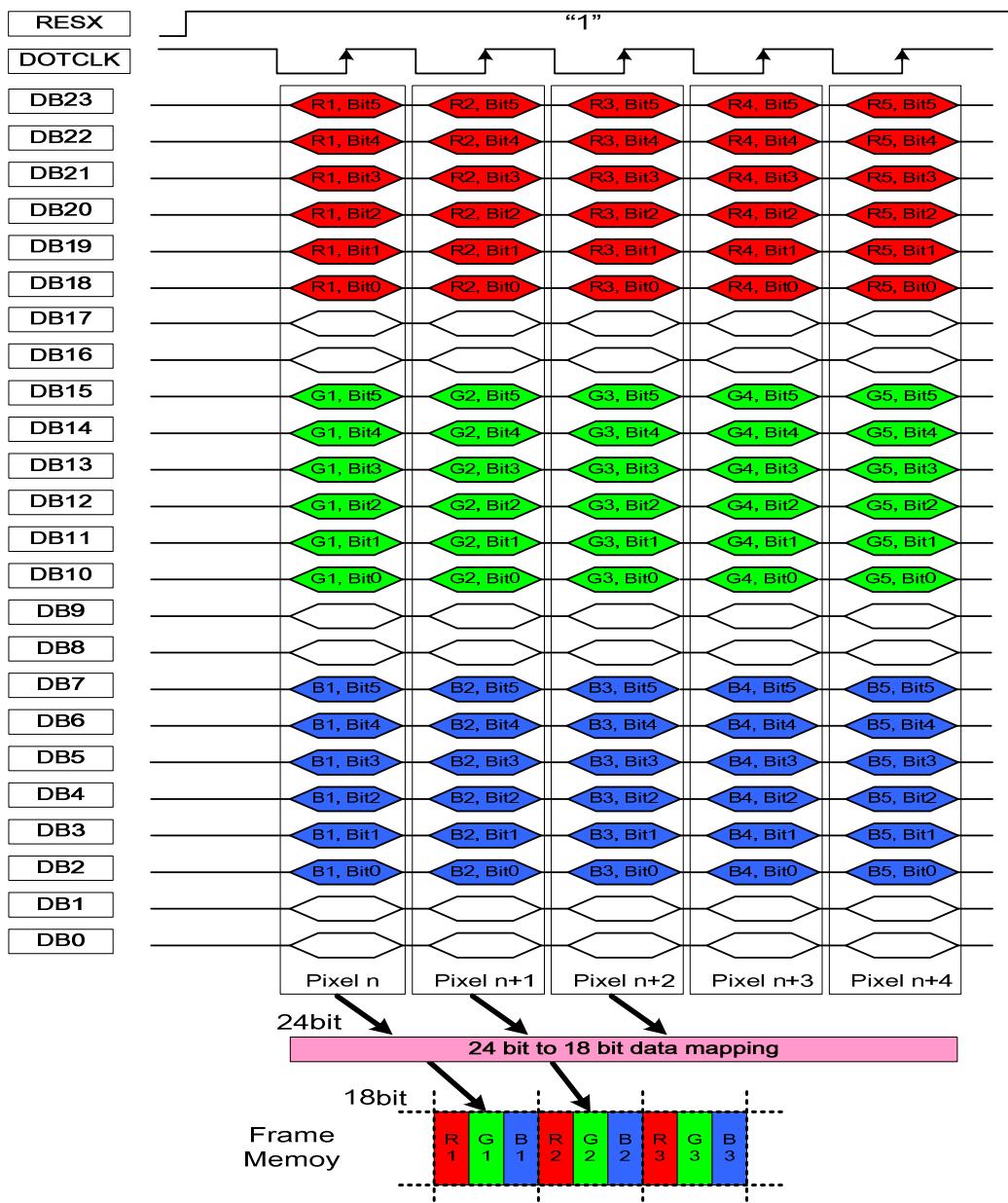


Figure 123: 24-bit/pixel 262K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

4.8.3.2. 24-bit/pixel Constrained by Dither and Bypass

The 24-bit RGB interface is selected by setting the DPI [2:0] bits as 111, DB_EN as 1, Dither_Enable as 1, and Bypass as 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE and DOTCLK signals.

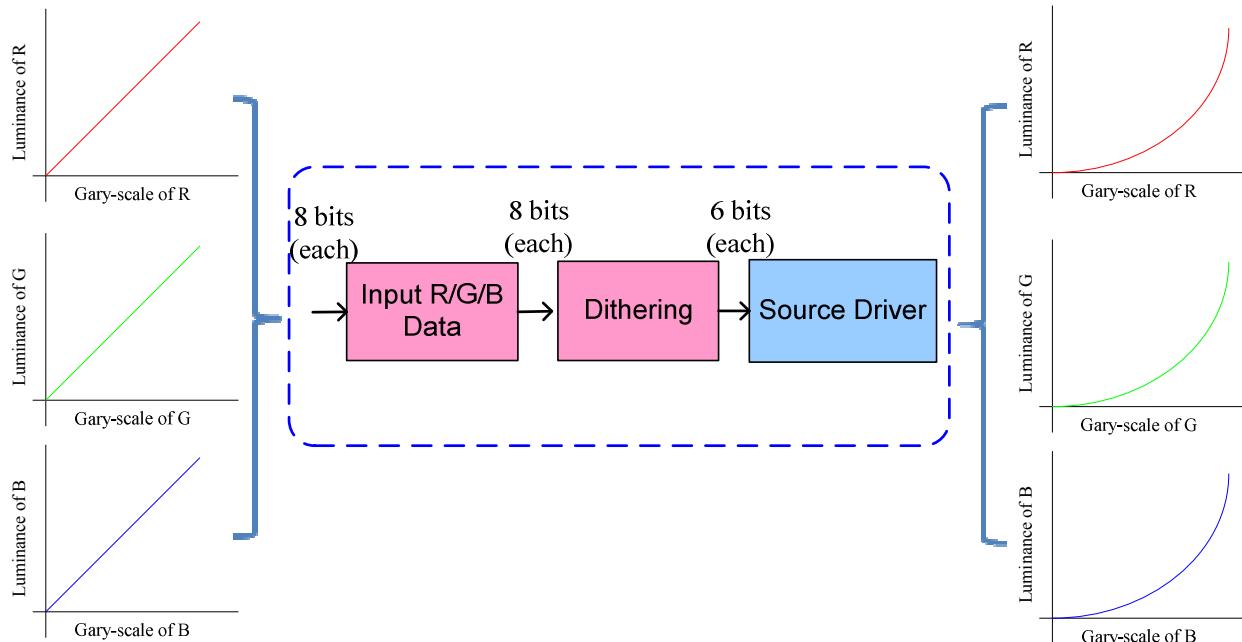


Figure 124: 24-bit/pixel 16.7M Colors Order on the DPI Interface

Notes:

1. To configure the Bypass, please refer to the Section 5.3.7 Display Function Control (B6h).
2. 1-time transfer is used to transmit 1 pixel data to the 24-bit color depth information.

4.9. DSI Transmission Data Format

4.9.1. 16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long packet, used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9488 has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

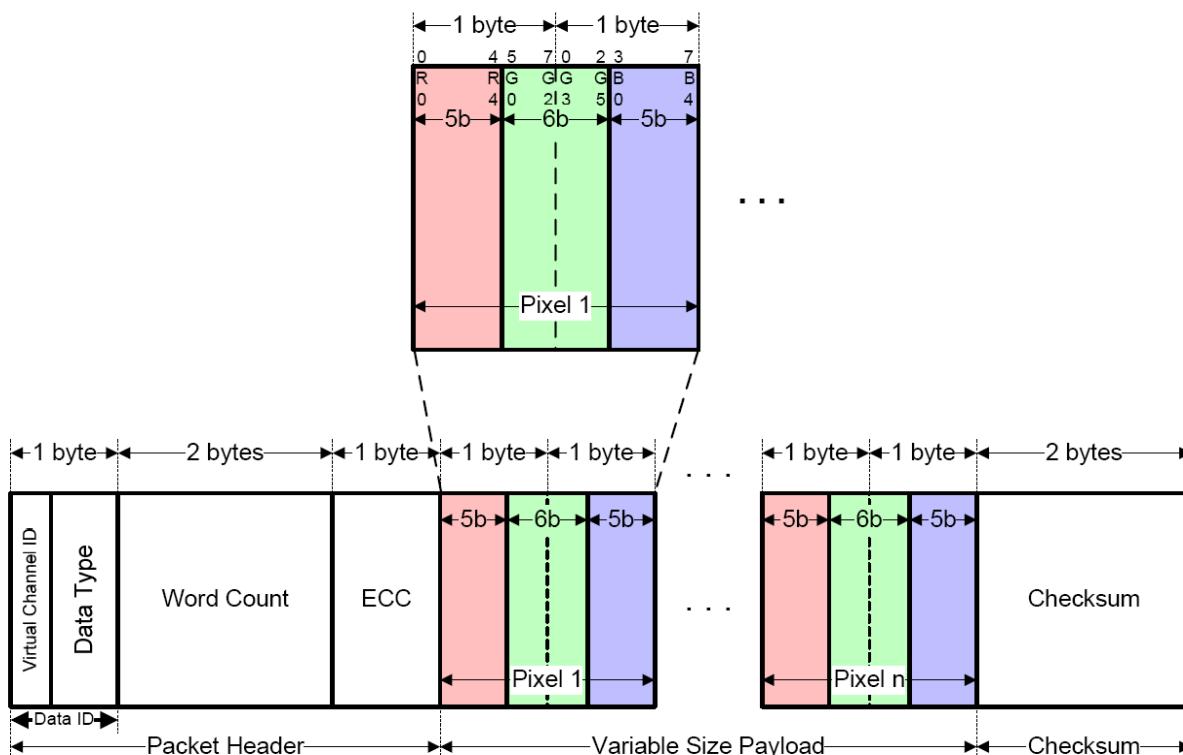


Figure 125: 16-bit per Pixel, Data Type 00 1110 (0Eh)

4.9.2. MIPI – 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

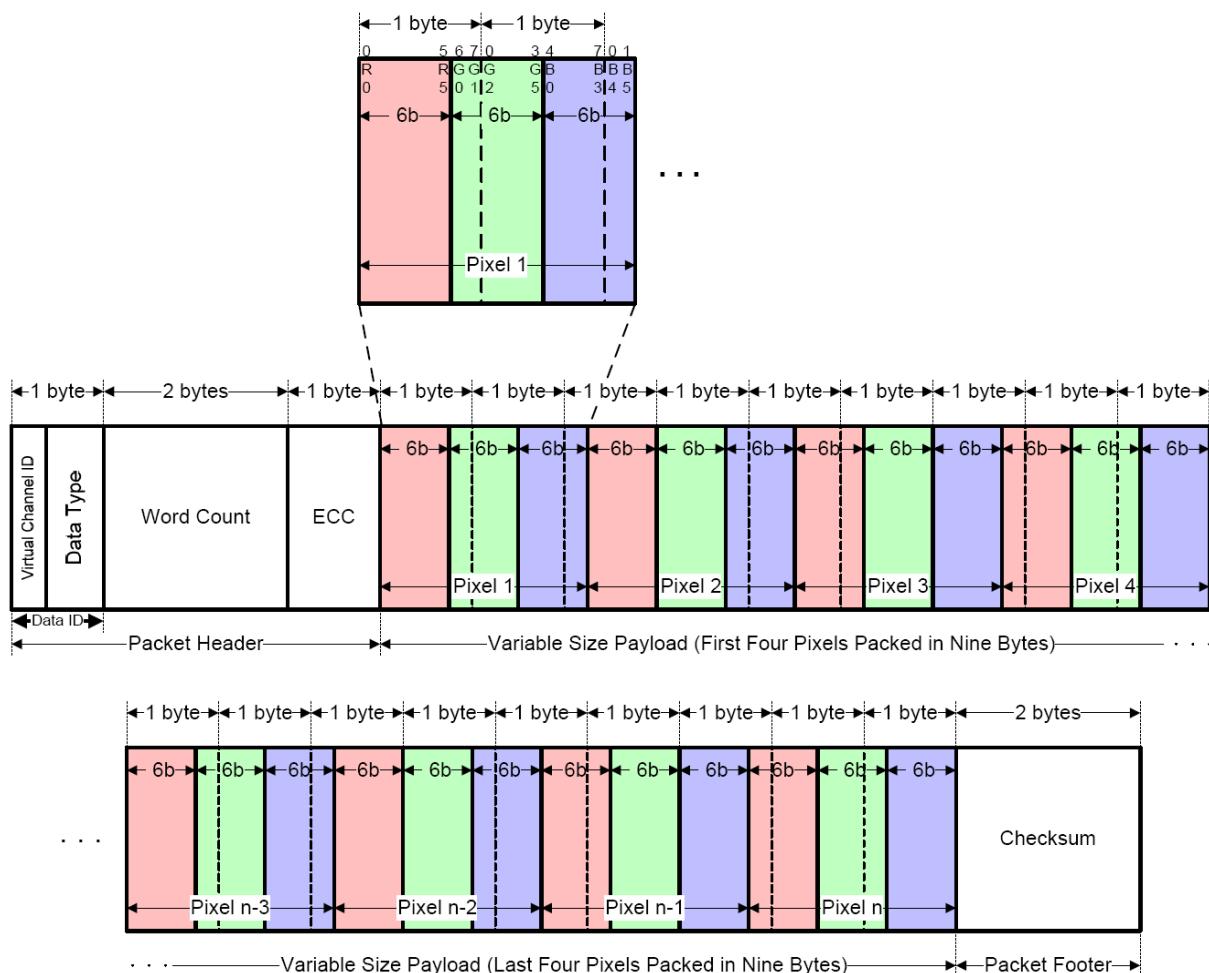


Figure 126: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.9.3. MIPI – 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte, representing active pixels, are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first and the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

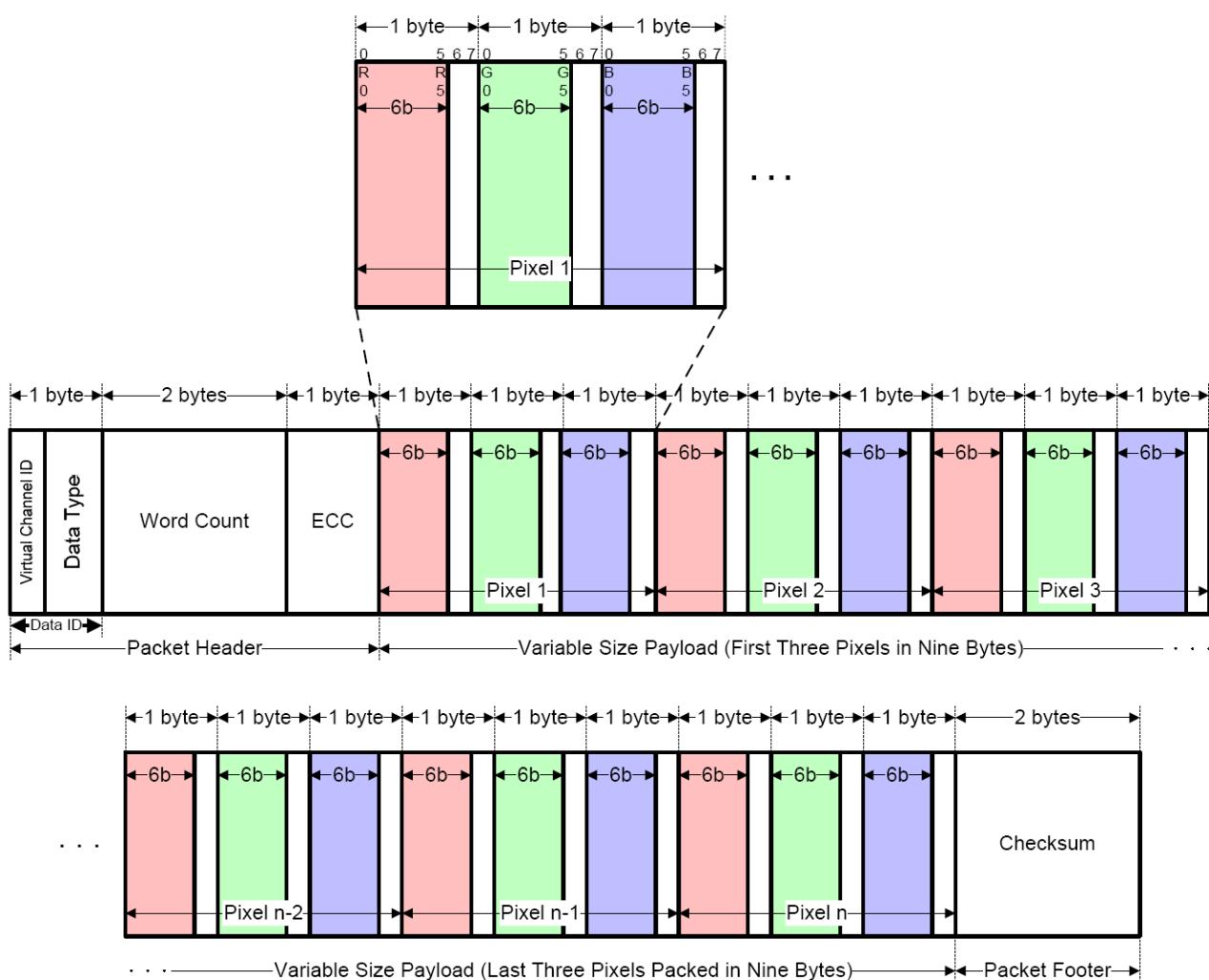


Figure 127: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

5. Command

5.1. Command List

5.1.1. Standard Command List

| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
|---|------|-----|-----|----------|----|----|-----------|----|-----------|----|-----------|----|-----|---|
| NOP | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Soft Reset | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read display identification information | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | ID1 [7:0] | | | | XX | |
| | 1 | ↑ | 1 | XX | | | | | ID2 [7:0] | | | | XX | |
| | 1 | ↑ | 1 | XX | | | | | ID3 [7:0] | | | | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Number of the Errors on DSI | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | P [7:0] | | | | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display Status | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09h | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [31:24] | | | | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [23:16] | | | | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [23:8] | | | | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [7:0] | | | | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display Power Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [7:2] | | | | 0 | 0 |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display MADCTL | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [7:2] | | | | 0 | 0 |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Pixel Format | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0Ch | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | 0 | | DPI [2:0] | | 0 | | DBI [2:0] | | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display Image Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | | | | | D [7:0] | | | | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display signal Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read Display Self-Diagnostic Result | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| | 1 | ↑ | 1 | XX | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | XX | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Sleep IN | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Sleep OUT | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Partial Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 12h | |

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| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
|-------------------------------|------|-----|-----|----------|------------|----|----|----|-----|----|----|----|-----|
| Normal Display Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display Inversion OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display Inversion ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| All Pixel OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| All Pixel ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Column Address Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2Ah |
| | 1 | 1 | ↑ | XX | SC [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | SC [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EC [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EC [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Page Address Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2Bh |
| | 1 | 1 | ↑ | XX | SP [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | SP [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EP [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EP [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Memory Write | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch |
| | 1 | 1 | ↑ | XX | D1 [23:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | Dx [23:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | Dn [23:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Memory Read | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 2Eh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D1 [23:0] | | | | | | | | XX |
| | 1 | ↑ | 1 | XX | Dx [23:0] | | | | | | | | XX |
| | 1 | ↑ | 1 | XX | Dn [23:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Partial Area | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h |
| | 1 | 1 | ↑ | XX | SR [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | SR [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | ER [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | ER [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Vertical Scrolling Definition | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33h |
| | 1 | 1 | ↑ | XX | TFA [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | TFA [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | VSA [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | VSA [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | BFA [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | BFA [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Tearing Effect Line OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Tearing Effect Line ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Memory Access Control | 0 | 1 | ↑ | XX | MY | MX | MV | ML | BGR | MH | X | X | 36h |
| | 1 | 1 | ↑ | XX | | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |

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| | | | | | | | | | | | | | |
|---|------|-----|-----|----------|----|----|-----------|-----------|------------|----|-----------|---------|-----|
| Vertical Scrolling Start Address | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37h |
| | 1 | 1 | ↑ | XX | | | | | VSP [15:8] | | | | XX |
| | 1 | 1 | ↑ | XX | | | | | VSP [7:0] | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Idle Mode OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Idle Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Interface Pixel Format | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3Ah |
| | 1 | 1 | ↑ | XX | 0 | | DPI [6:4] | | 0 | | DBI [2:0] | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Memory Write Continue | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3Ch |
| | 1 | 1 | ↑ | | | | | D1 [23:0] | | | | | XX |
| | 1 | 1 | ↑ | | | | | Dx [23:0] | | | | | XX |
| | 1 | 1 | ↑ | | | | | Dn [23:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Memory Read Continue | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3Eh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | | | | | D1 [23:0] | | | | | XX |
| | 1 | ↑ | 1 | | | | | Dx [23:0] | | | | | XX |
| | 1 | ↑ | 1 | | | | | Dn [23:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Write Tear Scan line | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44h |
| | 1 | 1 | ↑ | XX | | | | N [15:8] | | | | | XX |
| | 1 | 1 | ↑ | XX | | | | N [7:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read Tear Scan Line | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | | | | N [15:8] | | | | | XX |
| | 1 | ↑ | 1 | XX | | | | N [7:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Write Display Brightness value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51h |
| | 1 | ↑ | 1 | XX | | | | DBV [7:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read Display Brightness Value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 52h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | | | | | | | | DBV [7:0] | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Write CTRL Display value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53h |
| | 1 | 1 | ↑ | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read CTRL Display value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Write Content Adaptive Brightness Control value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | C [1:0] | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read Content Adaptive Brightness Control value | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | C [1:0] | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Write CABC Minimum Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5Eh |
| | 1 | 1 | ↑ | XX | | | | | CMB [7:0] | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read CABC Minimum Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5Fh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | | | | | CMB [7:0] | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read automatic brightness | 0 | 1 | ↑ | XX | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68h |

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| | | | | | | | | | | | | | |
|--------------------------------|------|-----|-----|----------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|
| control self-diagnostic result | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [7:6] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read ID1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Read ID2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DBh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | ID2 [7:0] | | | | | | | | XX |
| Command Function | D/CX | RDX | WRX | D [23:8] | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Hex |
| Read ID3 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | XX |

5.1.2. Extended Command List

| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
|--|------|-----|-----|----------|-----------|-----|----------|---------------------|-----------|------------|-----------|-----|-----|
| Interface Mode Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h |
| | 1 | 1 | ↑ | XX | SDA_EN | 0 | 0 | 0 | VSPL | HSPL | DPL | EPL | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Frame Rate Control (In Normal Mode/Full Colors) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1h |
| | 1 | 1 | ↑ | XX | FRS [3:0] | | | 0 | 0 | DIVA [1:0] | | | B0h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNA [4:0] | | | | | 11h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Frame Rate Control (In Idle Mode/8 colors) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVB[1:0] | | 00h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNB [4:0] | | | | | 11h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Frame Rate Control (In Partial Mode/Full colors) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVC[1:0] | | 00h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNC [4:0] | | | | | 11h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display Inversion Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | DINV[2:0] | | | 02h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Blanking Porch Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VFP [4:0] | | | | | 02h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VBP [4:0] | | | | | 02h |
| | 1 | 1 | ↑ | XX | HFP [7:0] | | | | | 0Ah | | | 0Ah |
| | 1 | 1 | ↑ | XX | HBP [7:0] | | | | | 04h | | | 04h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Display Function Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6h |
| | 1 | 1 | ↑ | XX | BYPASS | RCM | RM | DM | PTG [1:0] | | PT [1:0] | | 02h |
| | 1 | 1 | ↑ | XX | 0 | GS | SS | SM | ISC [3:0] | | | 02h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | NL [5:0] | | | | | 3Bh | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Entry Mode Set | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7h |
| | 1 | 1 | ↑ | XX | EPF [1:0] | | 0 | 0 | DSTB | GON | DTE | GAS | 06h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Color Enhancement Control 1 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | First_Axis 1 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | First_Axis 2 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | First_Axis 3 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | First_Axis 4 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Second_Axis 1 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Second_Axis 2 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Second_Axis 3 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Second_Axis 4 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Third_Axis 1 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Third_Axis 2 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Third_Axis 3 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Third_Axis 4 [4:0] | | | | | 04h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Color Enhancement Control 1 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BAh |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fourth_Axis 1 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fourth_Axis 2 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fourth_Axis 3 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fourth_Axis 4 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fifth_Axis 1 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fifth_Axis 2 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fifth_Axis 3 [4:0] | | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Fifth_Axis 4 [4:0] | | | | | 04h |

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| | | | | | | | | | | | | | |
|------------------|------|-----|-----|----------|-----------------|---------------|----|--------------------|-------------------|------------------|----|--------|-----|
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Sixth_Axis 1 [4:0] | | | | 04h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Sixth_Axis 2 [4:0] | | | | 04h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Sixth_Axis 3 [4:0] | | | | 04h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | Sixth_Axis 4 [4:0] | | | | 04h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Power Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VRH1 [4:0] | | | | 0Eh | |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VRH2 [4:0] | | | | 0Eh | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Power Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1h |
| | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | BT [2:0] | | | 43h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Power Control 3 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2h |
| | 1 | 1 | ↑ | XX | 0 | DCA1 [2:0] | | | 0 | DCA0 [2:0] | | | 33h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Power Control 4 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3h |
| | 1 | 1 | ↑ | XX | 0 | DCB1 [2:0] | | | 0 | DCB0 [2:0] | | | 33h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Power Control 5 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4h |
| | 1 | 1 | ↑ | XX | 0 | DCC2 [2:0] | | | 0 | DCC0 [2:0] | | | 33h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| VCOM Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | nVM | 00h |
| | 1 | 1 | ↑ | XX | VCM_REG [7:0] | | | | | | | | 40h |
| | 1 | 1 | ↑ | XX | VCM_REG_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| | 1 | 1 | ↑ | XX | VCM_OUT [7:0] | | | | | | | | 40h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6h |
| | 1 | 1 | ↑ | XX | SCD_VLINE [7:0] | | | | | | | | E0h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | SCD_VLINE [10:8] | | | 01h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PWMPOL | B0h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 3 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9h |
| | 1 | 1 | ↑ | XX | THRES_MOV [3:0] | | | | THRES_STILL [3:0] | | | | BBh |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 4 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CAh |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | THRES_UI [3:0] | | | | 0Bh |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 5 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CBh |
| | 1 | 1 | ↑ | XX | DTH_MOV [3:0] | | | | DTH_STILL [3:0] | | | | A8h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 6 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CCh |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | DTH_UI [3:0] | | | | 03h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 7 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CDh |
| | 1 | 1 | ↑ | XX | 0 | DIM_MOV [2:0] | | | 0 | DIM_STILL [2:0] | | | 43h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 8 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CEh |
| | 1 | 1 | ↑ | XX | DIM_MIN [3:0] | | | | 0 | DIM_UI [2:0] | | | 02h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| CABC Control 9 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | CFh |
| | 1 | 1 | ↑ | XX | PWM_DIV [7:0] | | | | | | | | F8h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| NV Memory Write | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0h |

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|----------------------------------|------|-----|-----|----------|----------------|------------|----------------------------|-----------------|---------------|------------|----|----|-----|-----|
| | 1 | 1 | ↑ | XX | PGM_ADR [7:0] | | | | | | | | 00h | |
| | 1 | 1 | ↑ | XX | PGM_DATA [7:0] | | | | | | | | 00h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| NV Memory Protection Key | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1h | |
| | 1 | 1 | ↑ | XX | | | | | KEY [23:16] | | | | 55h | |
| | 1 | 1 | ↑ | XX | | | | | KEY [15:8] | | | | AAh | |
| | 1 | 1 | ↑ | XX | | | | | KEY [7:0] | | | | 66h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| NV Memory Status Read | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2h | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | XX | | |
| | 1 | ↑ | 1 | XX | ID2_CNT [3:0] | | | | ID1_CNT [3:0] | | | | 00h | |
| | 1 | ↑ | 1 | XX | VMF_CNT [3:0] | | | | ID3_CNT [3:0] | | | | 00h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Read ID4 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3h | |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | XX | | |
| | 1 | ↑ | 1 | XX | | | | | ID1 [7:0] | | | | 00h | |
| | 1 | ↑ | 1 | XX | | | | | ID2 [7:0] | | | | 94h | |
| | 1 | ↑ | 1 | XX | | | | | ID3 [7:0] | | | | 88h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| Adjust Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D7h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | Choppe r_op_cl k_opt | Chopper_op_clk_ | sel[1:0] | 0 | 1 | 1 | 03h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| PGAMCTRL(Positive Gamma Control) | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h | |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VP0 [3:0] | | | | 0Fh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP1 [5:0] | | | | 1Fh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP2 [5:0] | | | | 1Ch |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP4 [3:0] | | | | 0Bh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP6 [4:0] | | | | 0Eh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP13 [3:0] | | | | 09h |
| | 1 | 1 | ↑ | XX | 0 | | | | | VP20 [6:0] | | | | 48h |
| | 1 | 1 | ↑ | XX | | VP36 [3:0] | | | | VP27 [3:0] | | | | 99h |
| | 1 | 1 | ↑ | XX | 0 | | | | | VP43 [6:0] | | | | 38h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VP50 [3:0] | | | | 0Ah |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | VP57 [4:0] | | | | 14h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VP59 [3:0] | | | | 06h |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP61 [5:0] | | | | 11h |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VP62 [5:0] | | | | 09h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VP63 [3:0] | | | | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |
| NGAMCTRL(Negative Gamma Control) | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | E1h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VN0 [3:0] | | | | 0Fh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VN1 [5:0] | | | | 36h |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VN2 [5:0] | | | | 2Eh |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VN4 [3:0] | | | | 09h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VN6 [4:0] | | | | 0Ah |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | VN13 [3:0] | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | | | | | VN20 [6:0] | | | | 46h |
| | 1 | 1 | ↑ | XX | | VN36 [3:0] | | | | VN27 [3:0] | | | | 66h |
| | 1 | 1 | ↑ | XX | 0 | | | | | VN43 [6:0] | | | | 37h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VN50 [3:0] | | | | 06h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | VN57 [4:0] | | | | 10h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VN59 [3:0] | | | | 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VN61 [5:0] | | | | 24h |
| | 1 | 1 | ↑ | XX | 0 | 0 | | | | VN62 [5:0] | | | | 20h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | | VN63 [3:0] | | | | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | |

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| | | | | | | | | | | | | | |
|--------------------------|------|-----|-----|----------|---------------|-------------------|--------------|----|-------------|---------------|---------------|-------------------|-----------------------|
| Digital Gamma Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2h |
| | 1 | 1 | ↑ | XX | | RCA0 [3:0] | | | BCA0 [3:0] | | | | 00h |
| | 1 | 1 | ↑ | XX | | RCAx [3:0] | | | BCAx [3:0] | | | | 00h |
| | 1 | 1 | ↑ | XX | | RCA63 [3:0] | | | BCA63 [3:0] | | | | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Digital Gamma Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3h |
| | 1 | 1 | ↑ | XX | | RFA0 [3:0] | | | BFA0 [3:0] | | | | 00h |
| | 1 | 1 | ↑ | XX | | RFAX [3:0] | | | BFAX [3:0] | | | | 00h |
| | 1 | 1 | ↑ | XX | | RFA63 [3:0] | | | BFA63 [3:0] | | | | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Set Image Function | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DB_EN | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Adjust Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2h |
| | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | Chopper_delay_opt 58h |
| | 1 | 1 | ↑ | XX | 0 | | GSW_TG1[5:0] | | | | | | 0 04h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02h |
| | 1 | 1 | ↑ | XX | 0 | | EQRTI[2:0] | | 0 | 0 | 1 | 0 | 22h |
| | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 42h |
| | 1 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFh |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah |
| | 1 | 1 | ↑ | XX | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 14h |
| | 1 | 1 | ↑ | XX | | Chopper_sel [1:0] | | | 1 | 0 | 0 | 0 | 88h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Adjust Control 3 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | F7h |
| | 1 | 1 | ↑ | XX | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A9h |
| | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch |
| | 1 | 1 | ↑ | XX | DSI_18_option | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Adjust Control 4 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 3Gamma_Enable | Dither_Enable 04h | |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Adjust Control 5 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | Chopper_opt | 0 | 0 | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| SPI Read Command Setting | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FBh |
| | 1 | 1 | ↑ | XX | SPI_REA_D_EN | 0 | 0 | 0 | | SPI_CNT [3:0] | | | 00h |
| Command Function | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| Adjust Control 6 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FCh |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | NOWI [4:0] | | | | 05h |

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5.2. Command Description

5.2.1. NOP (00h)

| 00h | NOP (No Operation) | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command is an empty command. It does not have any effect on the ILI9488. However, it can be used to terminate Frame Memory Write or Read, as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = void | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | None | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table> | | | | | | | | | | | | Status | Default Value | Power On Sequence | N/A | SW Reset | N/A | HW Reset | N/A | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | N/A | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | N/A | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | N/A | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | None | | | | | | | | | | | | | | | | | | | | | | | |

5.2.2. Software Reset (01h)

| SWRESET (Software Reset) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----|----|-----|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| 01h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>When the Software Reset command is written, it causes software reset. It resets commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>After the Software Reset is applied, the display becomes blank immediately.</p> <p>X = void</p> <p>Note: The Frame Memory contents are not affected by this command.</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec before sending the Sleep Out command.</p> <p>The Software Reset Command cannot be sent during the Sleep Out sequence.</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | N/A | SW Reset | N/A | HW Reset | N/A | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | N/A | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | N/A | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | N/A | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD Start([SWRESET(01h)]) --> DisplayBlank([Display whole blank screen]) DisplayBlank --> SetCommands([Set Commands to S/W Default Values]) SetCommands --> SleepIn([Sleep In Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.3. Read Display Identification Information (04h)

| 04h | | RDDIDIF (Read Display Identification Information) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---|-----|----------|-----------|----|----|----|----|----|----|----|-----|--|--------|---------------|--|-----------------|---|-----------------|---|-----------------|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [17:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | ↑ | 1 | XX | ID2 [7:0] | | | | | | | | | | | | | | | | | | | | | |
| 4 th Parameter | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | | | | | | | | | | | | | | |
| Description | This read byte can read 24 bits of display identification information. The 1 st parameter is a dummy data. The 2 nd parameter (ID1 [7:0]): LCD module's manufacturer ID The 3 rd parameter (ID2 [7:0]): LCD module/driver version ID The 4 th parameter (ID3 [7:0]): LCD module/driver ID X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | See description | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | See description | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | See description | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.4. Read Number of the Errors on DSI (05h)

| 05h | RDNUMED (Read Number of the Errors on DSI) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|---------|----|----|----|----|----|----|----|-----|--------|---------------|--|-------------------|---|-------------------|---|-------------------|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | P [7:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | The 1 st parameter is a dummy data. The 2 nd parameter indicates the number of errors on the DSI. More detailed description of the bits is below. P [6..0] bits indicate the number of the errors. P [7] is set to 1 if there is overflow with P [6..0] bits. P [7..0] bits are set to 0 (RDDSM(0Eh)'s D0 is set to 0 at the same time) after the second parameter information is sent (= The read function is completed). This function always returns P [7..0] = 00h if the parallel MCU interface is selected. X = void | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00_{HEX}</td></tr> <tr> <td>SW Reset</td><td>00_{HEX}</td></tr> <tr> <td>HW Reset</td><td>00_{HEX}</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 00 _{HEX} | SW Reset | 00 _{HEX} | HW Reset | 00 _{HEX} | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD RDNUMPE[RDNUMPE(05h)] --> Host Driver 1stParam{1st Parameter: Dummy Read 2nd Parameter: Read} 1stParam --> Host Driver Response{P [7:0] = 00h RDDSM (0Eh) D0 = 0} style RDNUMPE fill:#fff,stroke:#000,stroke-width:1px style 1stParam fill:#fff,stroke:#000,stroke-width:1px style Response fill:#fff,stroke:#000,stroke-width:1px style HostDriver fill:none,stroke:none style Legend fill:none,stroke:none legend[Legend] legend -- Command --> CommandShape[/\^Command\\$/] legend -- Parameter --> ParameterShape[/\^Parameter\\$/] legend -- Display --> DisplayShape[/\^Display\\$/] legend -- Action --> ActionShape[/\^Action\\$/] legend -- Mode --> ModeShape[/\^Mode\\$/] legend -- Sequential transfer --> SequentialTransferShape[/\^Sequential transfer\\$/] </pre> <p>The flowchart illustrates the process for RDNUMPE(05h). It starts with the command RDNUMPE(05h), which is sent to the Host Driver. The Host Driver then performs a '1st Parameter: Dummy Read' and a '2nd Parameter: Read'. The response is P [7:0] = 00h and RDDSM (0Eh) D0 = 0. A legend on the right side defines the symbols used in the flowchart: Command (triangular box), Parameter (trapezoid), Display (oval), Action (diamond), Mode (horizontal oval), and Sequential transfer (oval).</p> | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.5. Read Display Status (09h)

| 09h | | RDDST (Read Display Status) | | | | | | | | | | | | |
|---------------------------|------|-----------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09h | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D [31:24] | | | | | | | | | XX |
| 3 rd Parameter | 1 | ↑ | 1 | XX | D [23:16] | | | | | | | | | XX |
| 4 th Parameter | 1 | ↑ | 1 | XX | D [23:8] | | | | | | | | | XX |
| 5 th Parameter | 1 | ↑ | 1 | XX | D [7:0] | | | | | | | | | XX |

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value | Status |
|-----|---|-------|--|
| D31 | Booster voltage status | 0 | Booster OFF |
| | | 1 | Booster ON |
| D30 | Row address order | 0 | Top to Bottom (When MADCTL D7 = 0) |
| | | 1 | Bottom to Top (When MADCTL D7 = 1) |
| D29 | Column address order | 0 | Left to Right (When MADCTL D6 = 0) |
| | | 1 | Right to Left (When MADCTL D6 = 1) |
| D28 | Row/column exchange | 0 | Normal Mode (When MADCTL D5 = 0) |
| | | 1 | Reverse Mode (When MADCTL D5 = 1) |
| D27 | Vertical refresh | 0 | LCD Refresh Top to Bottom (When MADCTL D4 = 0) |
| | | 1 | LCD Refresh Bottom to Top (When MADCTL D4 = 1) |
| D26 | RGB/BGR order | 0 | RGB (When MADCTL D3 = 0) |
| | | 1 | BGR (When MADCTL D3 = 1) |
| D25 | Horizontal refresh order | 0 | LCD Refresh Left to Right (When MADCTL D2 = 0) |
| | | 1 | LCD Refresh Right to Left (When MADCTL D2 = 1) |
| D22 | Interface color pixel format definition | 101 | 16-bit/pixel |
| D21 | | 110 | 18-bit/pixel |
| D20 | | 111 | 24-bit/pixel |
| D19 | Idle mode ON/OFF | 0 | Idle Mode OFF |
| | | 1 | Idle Mode ON |
| D18 | Partial mode ON/OFF | 0 | Partial Mode OFF |
| | | 1 | Partial Mode ON |
| D17 | Sleep IN/OUT | 0 | Sleep IN Mode |
| | | 1 | Sleep OUT Mode |
| D16 | Display normal mode ON/OFF | 0 | Display Normal Mode OFF |
| | | 1 | Display Normal Mode ON |
| D15 | Vertical scrolling status | 0 | Vertical Scroll OFF |
| | | 1 | Vertical Scroll ON |
| D13 | Inversion status | 0 | Inversion OFF |
| | | 1 | Inversion ON |
| D10 | Display ON/OFF | 0 | Display is OFF |
| | | 1 | Display is ON |
| D9 | Tearing effect line ON/OFF | 0 | Tearing Effect Line OFF |
| | | 1 | Tearing Effect ON |

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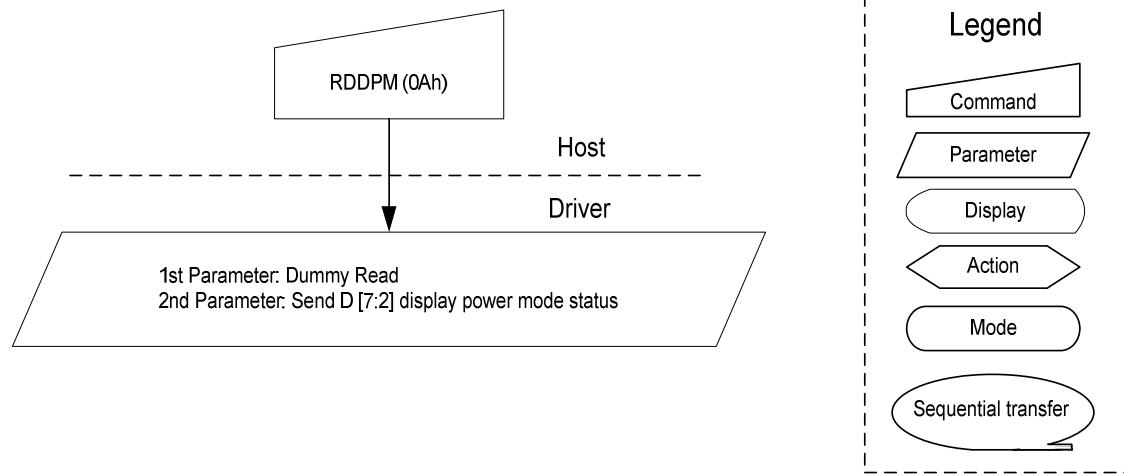
| | D [8:6] | Gamma curve selection | 000 | GC0 | | | | | | | | | | | | | |
|---|---|--------------------------|-----|--|--|--------|---------------|--|---------------|---|---------------|---|---------------|--|-----|----------|-----|
| | D5 | Tearing effect line mode | 0 | Mode 1, V-Blanking only | | | | | | | | | | | | | |
| | | | 1 | Mode 2, both H-Blanking and V-Blanking | | | | | | | | | | | | | |
| Note: This bit indicates the current status of the line when this command is sent. | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>32'h00610000h</td></tr> <tr> <td>SW Reset</td><td>32'h00610000h</td></tr> <tr> <td>HW Reset</td><td>32'h00610000h</td></tr> </tbody> </table> | | | | | Status | Default Value | Power On Sequence | 32'h00610000h | SW Reset | 32'h00610000h | HW Reset | 32'h00610000h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | |
| Power On Sequence | 32'h00610000h | | | | | | | | | | | | | | | | |
| SW Reset | 32'h00610000h | | | | | | | | | | | | | | | | |
| HW Reset | 32'h00610000h | | | | | | | | | | | | | | | | |
| Flow Chart | <p>RDDST (09h)</p> <p>Host</p> <p>Driver</p> <p>1st Parameter: Dummy Read 2nd Parameter: Send D [31:24] display status 3rd Parameter: Send D [23:16] display status 4th Parameter: Send D [15:8] display status 5th Parameter: Send D [7:0] display status</p> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | |

5.2.6. Read Display Power Mode (0Ah)

| 0Ah | RDDPM (Read Display Power Mode) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|---|----------|-----|----------|---------|----|----|----|----|----|----|----|-----|-----|-------------|---------|----|------------------------|--|----|------------------|--|----|---------------------|--|----|--------------|--|----|----------------------------|--|----|----------------|--|----|-------------|----------|----|-------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D [7:2] | | | | | | 0 | 0 | XX | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command indicates the current status of the display, as described in the table below: | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Booster Voltage Status</td><td></td></tr> <tr> <td>D6</td><td>Idle Mode On/Off</td><td></td></tr> <tr> <td>D5</td><td>Partial Mode On/Off</td><td></td></tr> <tr> <td>D4</td><td>Sleep In/Out</td><td></td></tr> <tr> <td>D3</td><td>Display Normal Mode On/Off</td><td></td></tr> <tr> <td>D2</td><td>Display On/Off</td><td></td></tr> <tr> <td>D1</td><td>Not Defined</td><td>Set to 0</td></tr> <tr> <td>D0</td><td>Not Defined</td><td>Set to 0</td></tr> </tbody> </table> | | | | | | | | | | | | | Bit | Description | Comment | D7 | Booster Voltage Status | | D6 | Idle Mode On/Off | | D5 | Partial Mode On/Off | | D4 | Sleep In/Out | | D3 | Display Normal Mode On/Off | | D2 | Display On/Off | | D1 | Not Defined | Set to 0 | D0 | Not Defined |
| Bit | Description | Comment | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Booster Voltage Status | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | Idle Mode On/Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | Partial Mode On/Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | Sleep In/Out | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | Display Normal Mode On/Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | Display On/Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D1 | Not Defined | Set to 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D0 | Not Defined | Set to 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D7 – Booster Voltage Status <ul style="list-style-type: none"> 0 = Booster Off or has a fault. 1 = Booster On and works OK. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D6 - Idle Mode On/Off <ul style="list-style-type: none"> 0 = Idle Mode Off 1 = Idle Mode On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D5 – Partial Mode On/Off <ul style="list-style-type: none"> 0 = Partial Mode Off 1 = Partial Mode On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D4 – Sleep In/Out <ul style="list-style-type: none"> 0 = Sleep In Mode 1 = Sleep Out Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D3 – Display Normal Mode On/Off <ul style="list-style-type: none"> 0 = Display Normal Mode Off 1 = Display Normal Mode On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D2 – Display On/Off <ul style="list-style-type: none"> 0 = Display is Off 1 = Display is On | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D1 – Not Defined <ul style="list-style-type: none"> This bit is not applicable for this project, so it is set to 0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ◆ Bit D0 – Not Defined <ul style="list-style-type: none"> This bit is not applicable for this project, so it is set to 0. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | |
|---|--|--------|---------------|--|-------------------|---|-------------------|---|-------------------|--|-----|----------|-----|
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>08_{HEX}</td></tr> <tr> <td>SW Reset</td><td>08_{HEX}</td></tr> <tr> <td>HW Reset</td><td>08_{HEX}</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 08 _{HEX} | SW Reset | 08 _{HEX} | HW Reset | 08 _{HEX} | | | | |
| Status | Default Value | | | | | | | | | | | | |
| Power On Sequence | 08 _{HEX} | | | | | | | | | | | | |
| SW Reset | 08 _{HEX} | | | | | | | | | | | | |
| HW Reset | 08 _{HEX} | | | | | | | | | | | | |

Flow Chart



5.2.7. Read Display MADCTL (0Bh)

| 0Bh | RDDMADCTL (Read Display MADCTL) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|----------|-----|----------|---------|----|----|----|----|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|----------------------|--|-----|-------------------|-----|----|--------------------|--|----|---------------|--|----|-------------------------------|--|----|----------|----------|----|----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D [7:2] | | | | | | 0 | 0 | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command indicates the current status of the display as described in the table below: | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address Order</td><td></td></tr> <tr> <td>D6</td><td>Column Address Order</td><td></td></tr> <tr> <td>D5</td><td>Page/Column Order</td><td></td></tr> <tr> <td>D4</td><td>Line Address Order</td><td></td></tr> <tr> <td>D3</td><td>RGB/BGR Order</td><td></td></tr> <tr> <td>D2</td><td>Display Data Latch Data Order</td><td></td></tr> <tr> <td>D1</td><td>Reserved</td><td>Set to 0</td></tr> <tr> <td>D0</td><td>Reserved</td><td>Set to 0</td></tr> </tbody> </table> | | | | | | | | | | | | | | Bit | Description | Comment | D7 | Page Address Order | | D6 | Column Address Order | | D5 | Page/Column Order | | D4 | Line Address Order | | D3 | RGB/BGR Order | | D2 | Display Data Latch Data Order | | D1 | Reserved | Set to 0 | D0 | Reserved |
| Bit | Description | Comment | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Page Address Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | Column Address Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | Page/Column Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | Line Address Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | RGB/BGR Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | Display Data Latch Data Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D1 | Reserved | Set to 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D0 | Reserved | Set to 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <ul style="list-style-type: none"> ♦ Bit D7 – Page Address Order 0 = Top to Bottom 1 = Bottom to Top ♦ Bit D6 – Column Address Order 0 = Left to Right 1 = Right to Left ♦ Bit D5 - Page/Column Order 0 = Normal Mode 1 = Reverse Mode <p>Note: For Bits D7 to D5, also refer to Section 6.3 MCU to Memory Write/Read Direction.</p> <ul style="list-style-type: none"> ♦ Bit D4 – Line Address Order 0 = LCD Refresh Top to Bottom 1 = LCD Refresh Bottom to Top ♦ Bit D3 – RGB/BGR Order 0 = RGB 1 = BGR ♦ Bit D2 – Display Data Latch Data Order 0 = LCD Refresh Left to Right 1 = LCD Refresh Right to Left <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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| Default | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc; text-align: center; padding: 2px;">Status</th><th style="background-color: #cccccc; text-align: center; padding: 2px;">Default Value</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td><td style="text-align: center; padding: 2px;">00_{HEX}</td></tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td><td style="text-align: center; padding: 2px;">00_{HEX}</td></tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td><td style="text-align: center; padding: 2px;">00_{HEX}</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 00 _{HEX} | SW Reset | 00 _{HEX} | HW Reset | 00 _{HEX} |
|-------------------|---|--------|---------------|-------------------|-------------------|----------|-------------------|----------|-------------------|
| Status | Default Value | | | | | | | | |
| Power On Sequence | 00 _{HEX} | | | | | | | | |
| SW Reset | 00 _{HEX} | | | | | | | | |
| HW Reset | 00 _{HEX} | | | | | | | | |
| Flow Chart | <pre> graph TD A[RDDMADCTL (0Bh)] --> B[Host] B --> C[Driver] C --> D["1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display status"] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | |

5.2.8. Read Display Pixel Format (0Ch)

| 0Ch | RDDCOLMOD (Read Display COLMOD) | | | | | | | | | | | | | | | | | | | | | | | | |
|--|--|-----|-----|----------------------|----|-----------|-----------|----|----|-----------------------|----|----|--------|---------------|-------------------|--|----------|---|----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0Ch | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | 0 | DPI [2:0] | | | 0 | DBI [2:0] | | | XX | | | | | | | | | | | | |
| Description | This command indicates the current status of the display, as described in the tables below: | | | | | | | | | | | | | | | | | | | | | | | | |
| | DPI [2:0] | | | RGB Interface Format | | | DBI [2:0] | | | MCU Interface Format | | | | | | | | | | | | | | | |
| | 0 | 0 | 0 | Reserved | | | 0 | 0 | 0 | Reserved | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | Reserved | | | 0 | 0 | 1 | 3 bits/pixel(8 color) | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | Reserved | | | 0 | 1 | 0 | Reserved | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | Reserved | | | 0 | 1 | 1 | Reserved | | | | | | | | | | | | | | | |
| | 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | | | | | | | | | | | | | | | |
| | 1 | 0 | 1 | 16 bits/pixel | | | 1 | 0 | 1 | 16 bits/pixel | | | | | | | | | | | | | | | |
| | 1 | 1 | 0 | 18 bits/pixel | | | 1 | 1 | 0 | 18 bits/pixel | | | | | | | | | | | | | | | |
| | 1 | 1 | 1 | 24 bits/pixel | | | 1 | 1 | 1 | 24 bits/pixel | | | | | | | | | | | | | | | |
| Restriction | X = void | | | | | | | | | | | | | | | | | | | | | | | | |
| | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. | | | | | | | | | | | | | | | | | | | | | | | | |
| | Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>06_{HEX}</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>06_{HEX}</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 06 _{HEX} | SW Reset | No Change | HW Reset | 06 _{HEX} | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 06 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 06 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.9. Read Display Image Mode (0Dh)

| 0Dh | | RDDIM (Read Display Image Mode) | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---------------------------------|-----|----------|---------|----|----|----|----|----|----|----|-----|--------|--------------|--|---------------------------|---|----------|---|------------------|--|----------|----------|----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D [7:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | The ILI9488 can read the Display Image Mode status. This command indicates the current status of the display, as described in the table below: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Vertical Scrolling Status</td></tr> <tr> <td>D6</td><td>Reserved</td></tr> <tr> <td>D5</td><td>Inversion On/Off</td></tr> <tr> <td>D4</td><td>Reserved</td></tr> <tr> <td>D3</td><td>Reserved</td></tr> </tbody> </table> <ul style="list-style-type: none"> ♦ Bit D7 – Vertical Scrolling On/Off 0 = Vertical Scrolling is Off. 1 = Vertical Scrolling is On. ♦ Bit D6 – Reserved ♦ Bit D5 – Inversion On/Off 0 = Inversion is Off. 1 = Inversion is On. ♦ Bit D4 – Reserved ♦ Bit D3 – Reserved <p style="margin-top: 20px;">X = void</p> | | | | | | | | | | | | | Bit | Description | D7 | Vertical Scrolling Status | D6 | Reserved | D5 | Inversion On/Off | D4 | Reserved | D3 | Reserved |
| Bit | Description | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Vertical Scrolling Status | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | Inversion On/Off | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |

| | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00_{HEX}</td></tr> <tr> <td>SW Reset</td><td>00_{HEX}</td></tr> <tr> <td>HW Reset</td><td>00_{HEX}</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 00 _{HEX} | SW Reset | 00 _{HEX} | HW Reset | 00 _{HEX} |
|-------------------|--|--------|---------------|-------------------|-------------------|----------|-------------------|----------|-------------------|
| Status | Default Value | | | | | | | | |
| Power On Sequence | 00 _{HEX} | | | | | | | | |
| SW Reset | 00 _{HEX} | | | | | | | | |
| HW Reset | 00 _{HEX} | | | | | | | | |
| Default | | | | | | | | | |
| Flow Chart | <pre> graph TD RDDIM[RDDIM (0Dh)] --> Host[Host] Host --> Driver[Driver] Driver -- "1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display image mode status" --> RDDIM </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | |

5.2.10. Read Display Signal Mode (0Eh)

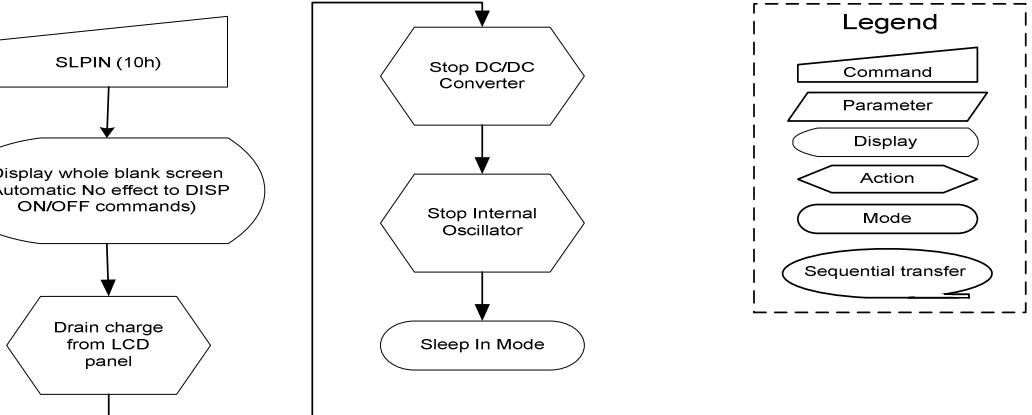
| 0Eh | | RDDSM (Read Display Signal Mode) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|----------------------------------|---|----------|----|----|----|----|----|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XX | | | | | | | | | | | | | |
| Description | This command indicates the current status of the display, as described in the table below: | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Bit | Value | Function | | | | | | | | | | | | | | | | | | | | | | | |
| | D7 | 0 | Tearing Effect Line OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Tearing Effect Line ON | | | | | | | | | | | | | | | | | | | | | | | |
| | D6 | 0 | Tearing Effect Line Mode 1 | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Tearing Effect Line Mode 2 | | | | | | | | | | | | | | | | | | | | | | | |
| | D5 | 0 | Horizontal Sync (RGB interface) OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Horizontal Sync (RGB interface) ON | | | | | | | | | | | | | | | | | | | | | | | |
| | D4 | 0 | Vertical Sync (RGB interface) OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Vertical Sync (RGB interface) ON | | | | | | | | | | | | | | | | | | | | | | | |
| | D3 | 0 | Pixel Clock (DOTCLK, RGB interface) OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Pixel Clock (DOTCLK, RGB interface) ON | | | | | | | | | | | | | | | | | | | | | | | |
| | D2 | 0 | Data Enable (ENABLE, RGB interface) OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Data Enable (ENABLE, RGB interface) ON | | | | | | | | | | | | | | | | | | | | | | | |
| | D1 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| | D0 | 0 | No Error on DSI | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Error on DSI | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

| | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00_{HEX}</td></tr> <tr> <td>SW Reset</td><td>00_{HEX}</td></tr> <tr> <td>HW Reset</td><td>00_{HEX}</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 00 _{HEX} | SW Reset | 00 _{HEX} | HW Reset | 00 _{HEX} |
|-------------------|--|--------|---------------|-------------------|-------------------|----------|-------------------|----------|-------------------|
| Status | Default Value | | | | | | | | |
| Power On Sequence | 00 _{HEX} | | | | | | | | |
| SW Reset | 00 _{HEX} | | | | | | | | |
| HW Reset | 00 _{HEX} | | | | | | | | |
| Default | | | | | | | | | |
| Flow Chart | <pre> graph TD A[RDDSM (0Eh)] --> B[Host Driver] B --> C[1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display mode status] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | |

5.2.11. Read Display Self-Diagnostic Result (0Fh)

| 0Fh | RDDSDR (Read Display Self-Diagnostic Result) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-----|----------|----|----|----|----|----|----|----|----|-----|--------|---------------|--|-------------------|---|--|---|-------------------------|---|-----|----------|-----|----|----------|---|----|----------|---|----|----------|---|----|----------|---|----|----------------------|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D7 | D6 | 0 | 0 | 0 | 0 | 0 | D0 | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command indicates the status of the display self-diagnostic results after Sleep Out command, as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Action</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Register Loading Detection</td><td>Invert the D7 bit if register values loading work properly</td></tr> <tr> <td>D6</td><td>Functionality Detection</td><td>Invert the D6 bit if the display is working</td></tr> <tr> <td>D5</td><td>Not Used</td><td>0</td></tr> <tr> <td>D4</td><td>Not Used</td><td>0</td></tr> <tr> <td>D3</td><td>Not Used</td><td>0</td></tr> <tr> <td>D2</td><td>Not Used</td><td>0</td></tr> <tr> <td>D1</td><td>Not Used</td><td>0</td></tr> <tr> <td>D0</td><td>Checksums Comparison</td><td>0 = Checksums are same 1 = Checksums are not same</td></tr> </tbody> </table> X = void | | | | | | | | | | | | | Bit | Description | Action | D7 | Register Loading Detection | Invert the D7 bit if register values loading work properly | D6 | Functionality Detection | Invert the D6 bit if the display is working | D5 | Not Used | 0 | D4 | Not Used | 0 | D3 | Not Used | 0 | D2 | Not Used | 0 | D1 | Not Used | 0 | D0 | Checksums Comparison | 0 = Checksums are same 1 = Checksums are not same |
| Bit | Description | Action | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Register Loading Detection | Invert the D7 bit if register values loading work properly | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | Functionality Detection | Invert the D6 bit if the display is working | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | Not Used | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | Not Used | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | Not Used | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | Not Used | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D1 | Not Used | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D0 | Checksums Comparison | 0 = Checksums are same 1 = Checksums are not same | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | It is necessary to wait 300ms after the last write access to registers on the User area before the Bit D0 value can be read. The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00_{HEX}</td></tr> <tr> <td>SW Reset</td><td>00_{HEX}</td></tr> <tr> <td>HW Reset</td><td>00_{HEX}</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 00 _{HEX} | SW Reset | 00 _{HEX} | HW Reset | 00 _{HEX} | | | | | | | | | | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 00 _{HEX} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display self-diagnostic status</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.12. Sleep IN (10h)

| 10h | | SLPIN (Sleep IN) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|---------------|---|---------------|---|---------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command will cause the ILI9488 enter the minimum power consumption mode.</p> <p>In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.</p>  <p>The MCU interface and memory are still working, and the memory keeps its contents.</p> <p>Dimming function does not work when the mode changes from Sleep OUT to Sleep IN.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>This command has no effect when the module is already in the Sleep In mode. To exit the Sleep In mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for supply voltages and clock circuits to stabilize. It is necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Sleep IN Mode</td></tr> <tr> <td>SW Reset</td><td>Sleep IN Mode</td></tr> <tr> <td>HW Reset</td><td>Sleep IN Mode</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Sleep IN Mode | SW Reset | Sleep IN Mode | HW Reset | Sleep IN Mode | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Sleep IN Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Sleep IN Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Sleep IN Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <pre> graph TD Start[SLPIN (10h)] --> Blank[Display whole blank screen Automatic No effect to DISP ON/OFF commands] Blank --> Drain[Drain charge from LCD panel] Drain --> StopDC[Stop DC/DC Converter] StopDC --> StopIO[Stop Internal Oscillator] StopIO --> SleepMode[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.13. Sleep OUT (11h)

| 11h | | SLPOUT (Sleep OUT) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|----------------|---|----------------|---|----------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command turns off the sleep mode.</p> <p>In this mode, the DC/DC converter is enabled, and Internal oscillator and panel scanning are activated.</p>  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>To exit the Sleep Out Mode, only the Sleep In Command (10h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for supply voltages and clock circuits to stabilize.</p> <p>The ILI9488 loads all factory default values of the display supplier to the registers during this 5msec. There cannot be any abnormal visual effects on the display image if factory defaults and register values are the same when this load is done and when the ILI9488 is already in the Sleep Out mode.</p> <p>The ILI9488 performs self-diagnostic functions during this 5msec. It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Sleep Out Mode</td></tr> <tr> <td>SW Reset</td><td>Sleep Out Mode</td></tr> <tr> <td>HW Reset</td><td>Sleep Out Mode</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Sleep Out Mode | SW Reset | Sleep Out Mode | HW Reset | Sleep Out Mode | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Sleep Out Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Sleep Out Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Sleep Out Mode | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD A[SLPOUT (11h)] --> B{Start Internal Oscillator} B --> C{Start up DC-DC Converter} C --> D[Charge Offset voltage for LCD Panel] D --> E[Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)] E --> F[Display Memory contents in accordance with the current command table settings] F --> G[Sleep Out Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

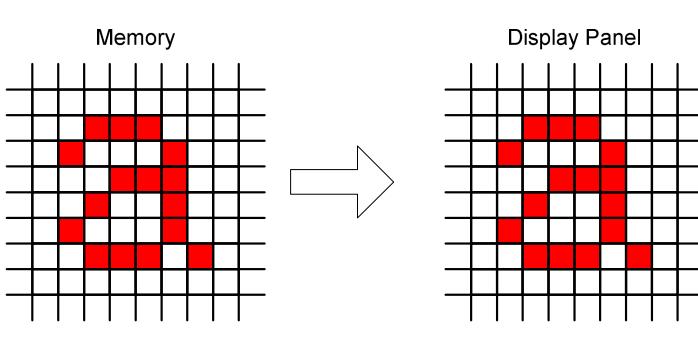
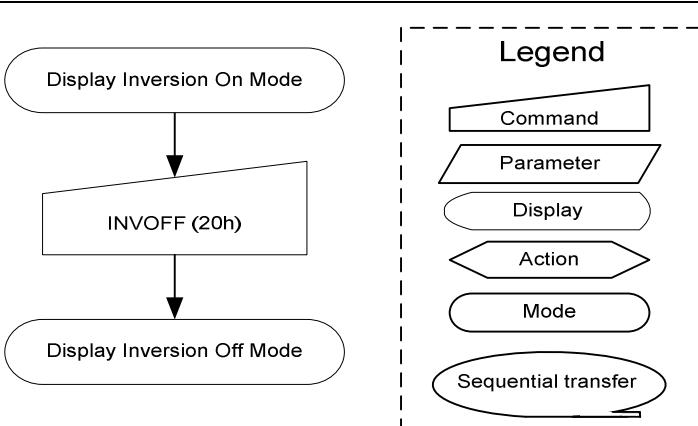
5.2.14. Partial Mode ON (12h)

| 12h | | PTLON (Partial Mode ON) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-----------------|---|-----------------|---|-----------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command will turn on the Partial mode. The Partial mode window is described in the Partial Area command (30H).</p> <p>To leave the Partial mode, the Normal Display Mode On command (13H) should be written.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the Partial Display Mode is already active. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Partial Mode On</td></tr> <tr> <td>SW Reset</td><td>Partial Mode On</td></tr> <tr> <td>HW Reset</td><td>Partial Mode On</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Partial Mode On | SW Reset | Partial Mode On | HW Reset | Partial Mode On | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Partial Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Partial Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Partial Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | See Partial Area (30h) | | | | | | | | | | | | | | | | | | | | | | | | | |

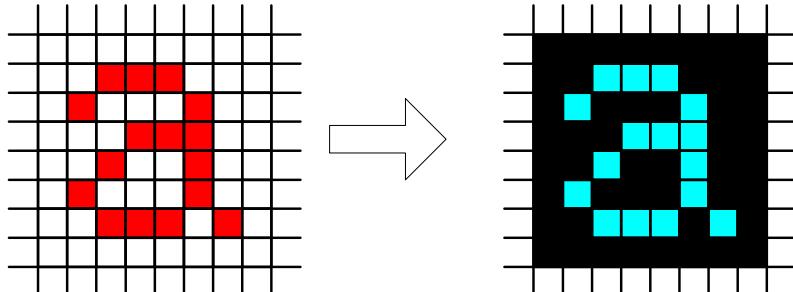
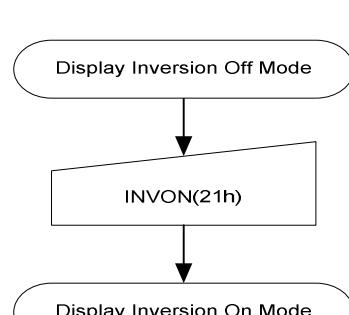
5.2.15. Normal Display Mode ON (13h)

| 13h | | NORON (Normal Display Mode ON) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|------------------------|---|------------------------|---|------------------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command will make the display return to the normal mode. Normal Display Mode On means Partial mode off and Scroll mode off.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the Normal Display mode is active. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Normal Display Mode On</td></tr> <tr> <td>SW Reset</td><td>Normal Display Mode On</td></tr> <tr> <td>HW Reset</td><td>Normal Display Mode On</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Normal Display Mode On | SW Reset | Normal Display Mode On | HW Reset | Normal Display Mode On | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Normal Display Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Normal Display Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Normal Display Mode On | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | See Partial Area Descriptions for details when using this command. | | | | | | | | | | | | | | | | | | | | | | | | | |

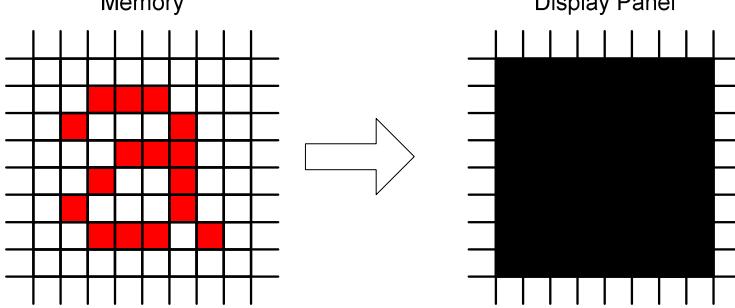
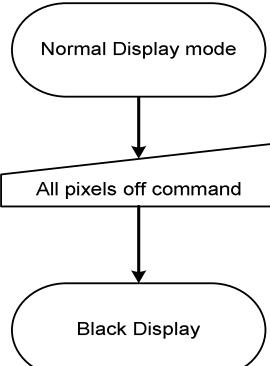
5.2.16. Display Inversion OFF (20h)

| 20h | | INVOFF (Display Inversion OFF) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-----------------------|---|-----------------------|---|-----------------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used to recover from the Display Inversion mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change to the content of the frame memory.</p> <p>This command does not change any other status.</p>  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Inversion Off mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display Inversion OFF</td></tr> <tr> <td>SW Reset</td><td>Display Inversion OFF</td></tr> <tr> <td>HW Reset</td><td>Display Inversion OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display Inversion OFF | SW Reset | Display Inversion OFF | HW Reset | Display Inversion OFF | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <pre> graph TD A([Display Inversion On Mode]) --> B[INVOFF (20h)] B --> C([Display Inversion Off Mode]) </pre> | | | | | | | | | | | | | | | | | | | | | | | | | |

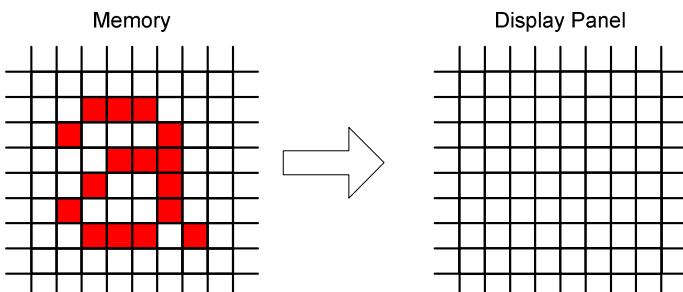
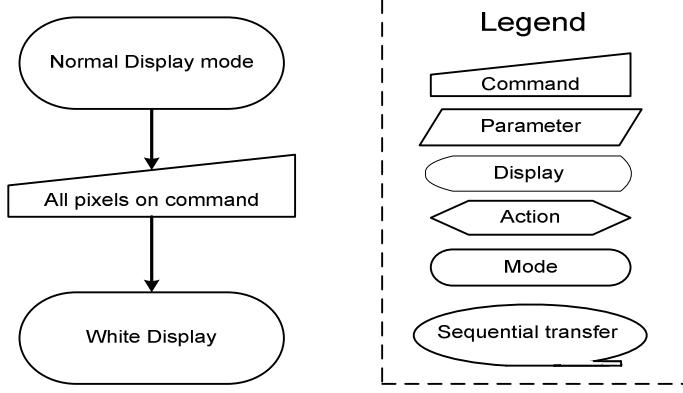
5.2.17. Display Inversion ON (21h)

| 21h | | INVON (Display Inversion ON) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-----------------------|---|-----------------------|---|-----------------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used to enter the Display Inversion mode.</p> <p>This command makes no change of the content of the frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command does not change any other status.</p> <p>To exit Display Inversion mode, the Display inversion OFF command (20h) should be written.</p>  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Inversion On mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display Inversion OFF</td></tr> <tr> <td>SW Reset</td><td>Display Inversion OFF</td></tr> <tr> <td>HW Reset</td><td>Display Inversion OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display Inversion OFF | SW Reset | Display Inversion OFF | HW Reset | Display Inversion OFF | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display Inversion OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

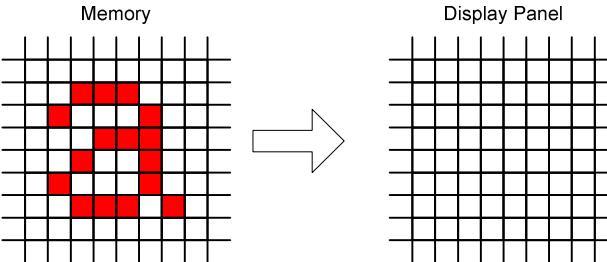
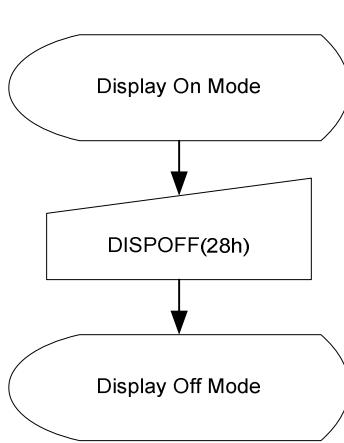
5.2.18. All Pixels OFF (22h)

| 22h | | ALLPOFF (All pixels off) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-------------|---|-------------|---|-------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command turns the display panel black in the Sleep Out mode, and the status of the Display On/Off register can be On or Off. This command makes no change to the contents of the Frame Memory. This command does not change any other status.</p>  <p>The diagram illustrates the state change. On the left, labeled 'Memory', there is a 6x6 grid of red squares representing pixels. An arrow points to the right, labeled 'Display Panel', where the same grid is shown as a solid black rectangle, indicating that all pixels are turned off.</p> <p>To exit this mode, All Pixels On, Normal Display Mode On or Partial Mode On commands can be used. The display panel shows the content of the Frame Memory after applying Normal Display Mode On and Partial Mode On commands.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Display Inversion On mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display OFF</td></tr> <tr> <td>SW Reset</td><td>Display OFF</td></tr> <tr> <td>HW Reset</td><td>Display OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display OFF | SW Reset | Display OFF | HW Reset | Display OFF | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <pre> graph TD A([Normal Display mode]) --> B[All pixels off command] B --> C([Black Display]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

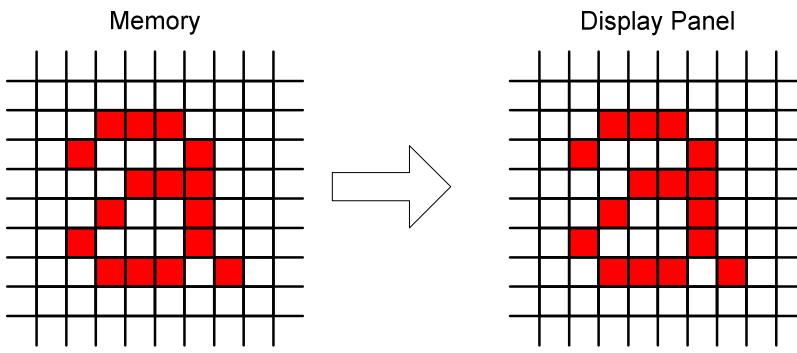
5.2.19. All Pixels ON (23h)

| 23h | ALLPON (All pixels on) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----|----|-----|--------|---------------|--|-------------|---|-------------|---|-------------|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command turns the display panel white in the Sleep Out mode, and the status of the Display On/Off register can be On or Off. This command makes no change to the contents of the Frame Memory. This command does not change any other status.</p>  <p>To exit this mode, All Pixels Off, Normal Display Mode On or Partial Mode On commands can be used. The display shows the content of the Frame Memory after applying Normal Display Mode On and Partial Mode On commands.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Inversion On mode. | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display OFF | SW Reset | Display OFF | HW Reset | Display OFF | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <pre> graph TD A([Normal Display mode]) --> B[All pixels on command] B --> C([White Display]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.20. Display OFF (28h)

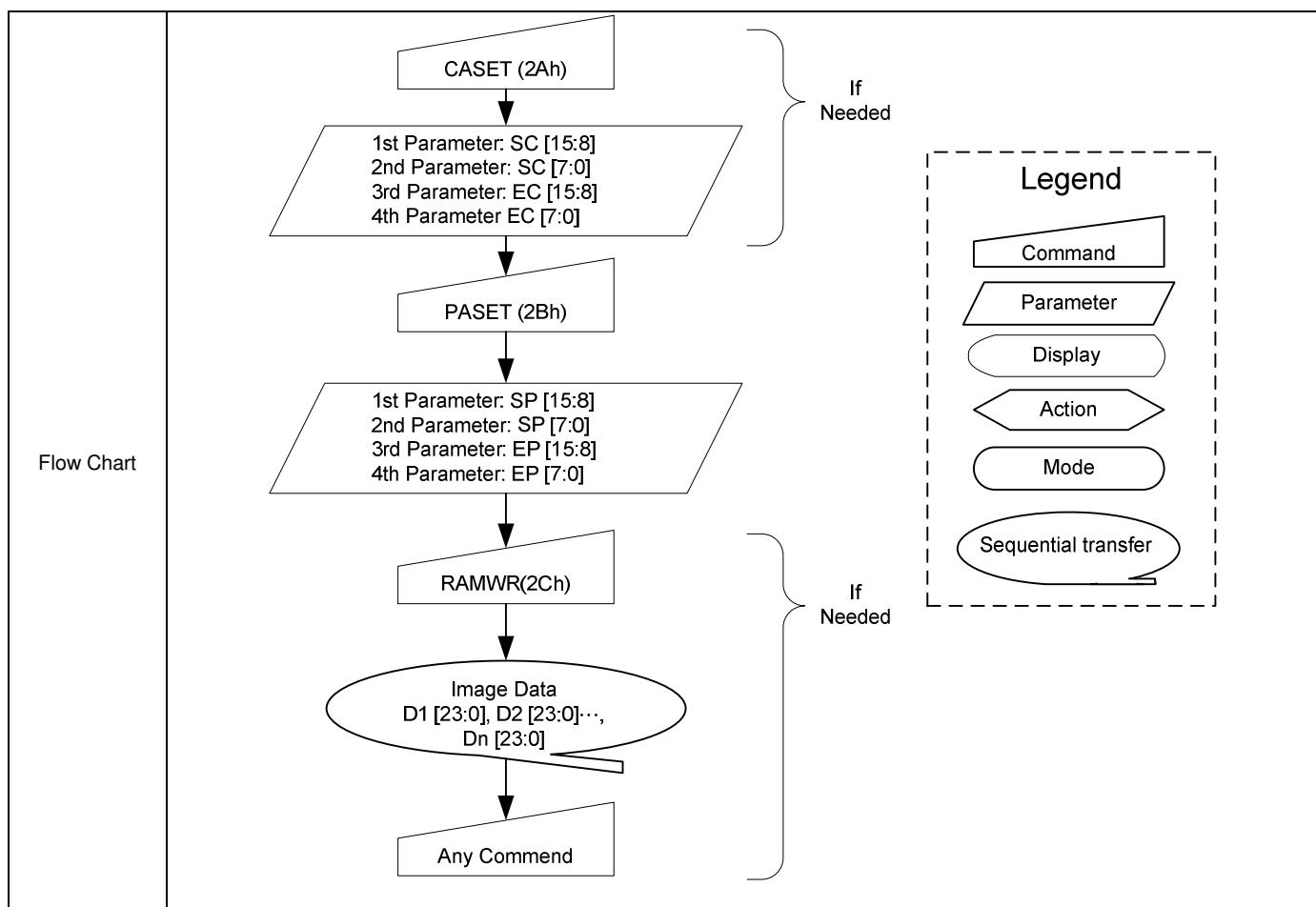
| 28h | | DISOFF (Display OFF) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|----------------------|-----|----------|----|----|----|----|----|----|----|----|-----|--------|---------------|--|-------------|---|-------------|---|-------------|--|-----|----------|-----|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28h | | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command causes the ILI9488 to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p>  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Display Off mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display OFF</td></tr> <tr> <td>SW Reset</td><td>Display OFF</td></tr> <tr> <td>HW Reset</td><td>Display OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display OFF | SW Reset | Display OFF | HW Reset | Display OFF | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.21. Display ON (29h)

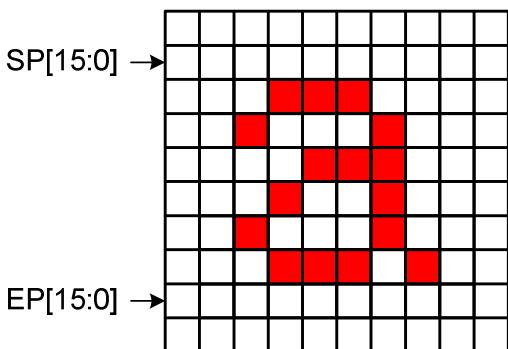
| 29h | DISON (Display ON) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----|----|-----|--|--------|---------------|--|-------------|---|-------------|---|-------------|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h | | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command causes the ILI9488 to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p>  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is already in the Display On mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Display OFF | SW Reset | Display OFF | HW Reset | Display OFF | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Display OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD A([Display Off Mode]) --> B[DISPON (29h)] B --> C([Display On Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

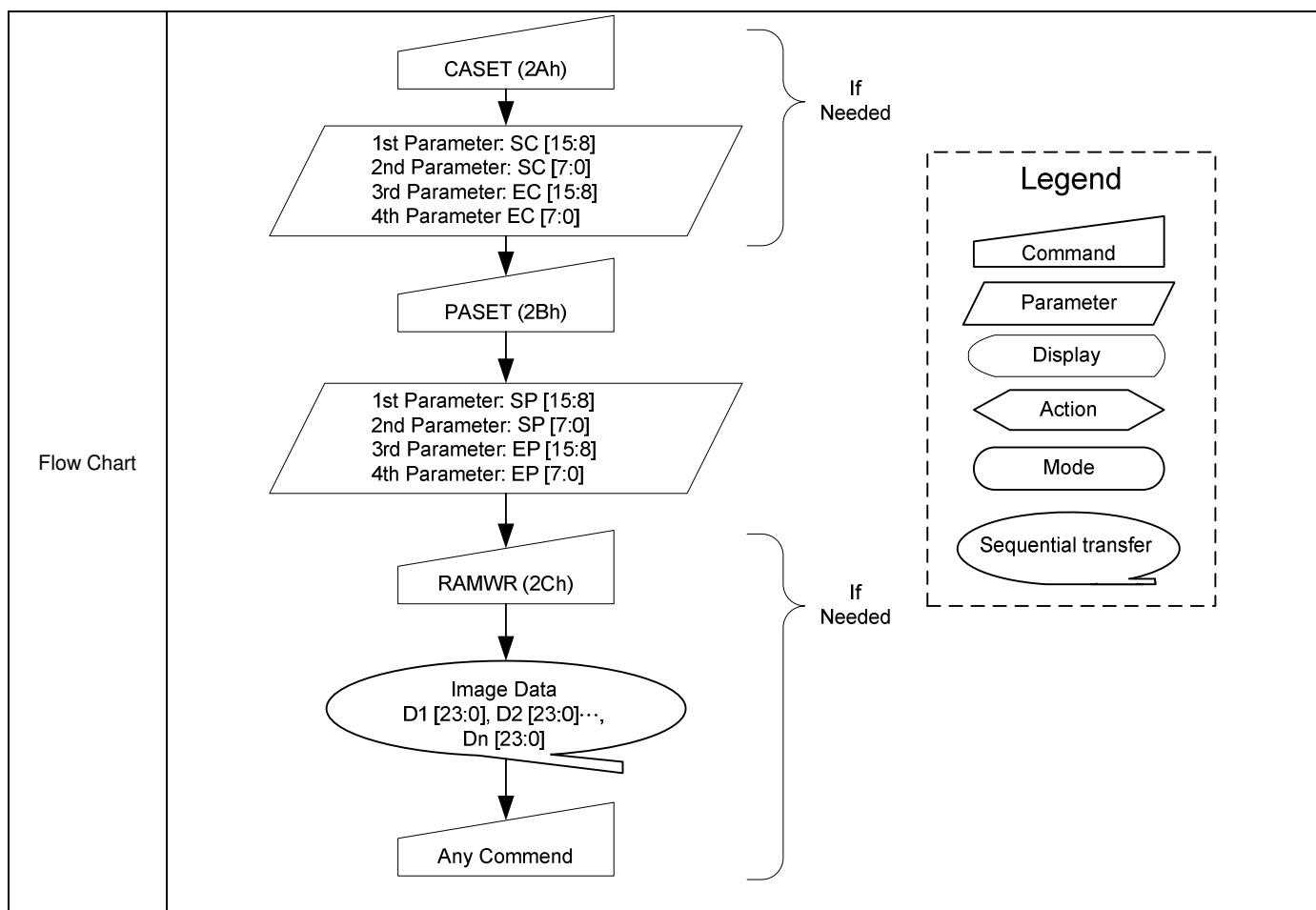
5.2.22. Column Address Set (2Ah)

| 2Ah | | CASET (Column Address Set) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|--------|---------------|--|-------------------|---|-------------------|---|-------------------|--|----------|-------------------|-------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2Ah | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | SC [15:8] | | | | | | | | | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | SC [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | EC [15:8] | | | | | | | | | XX | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | EC [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| Description | This command is used to define the area of the frame memory that the MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command is applied. Each value represents one column line in the Frame Memory. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | SC [15:0] must always be equal to or less than EC [15:0]. Note: When SC [15:0] or EC [15:0] is greater than 013Fh (when MADCTL's D5 = 0) or 01DFh (when MADCTL's D5 = 1), data out of range will be ignored. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SC [15:0] = 0000h</td> <td>EC [15:0] = 00EFh</td> </tr> <tr> <td>SW Reset</td> <td>SC [15:0] = 0000h</td> <td>If MADCTL's D5 = 0: EC [15:0] = 013Fh If MADCTL's D5 = 1: EC [15:0] = 01DFh</td> </tr> <tr> <td>HW Reset</td> <td>SC [15:0] = 0000h</td> <td>EC [15:0] = 013Fh</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | | Power On Sequence | SC [15:0] = 0000h | EC [15:0] = 00EFh | SW Reset | SC [15:0] = 0000h | If MADCTL's D5 = 0: EC [15:0] = 013Fh If MADCTL's D5 = 1: EC [15:0] = 01DFh | HW Reset | SC [15:0] = 0000h | EC [15:0] = 013Fh |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | SC [15:0] = 0000h | EC [15:0] = 00EFh | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | SC [15:0] = 0000h | If MADCTL's D5 = 0: EC [15:0] = 013Fh If MADCTL's D5 = 1: EC [15:0] = 01DFh | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | SC [15:0] = 0000h | EC [15:0] = 013Fh | | | | | | | | | | | | | | | | | | | | | | | | |



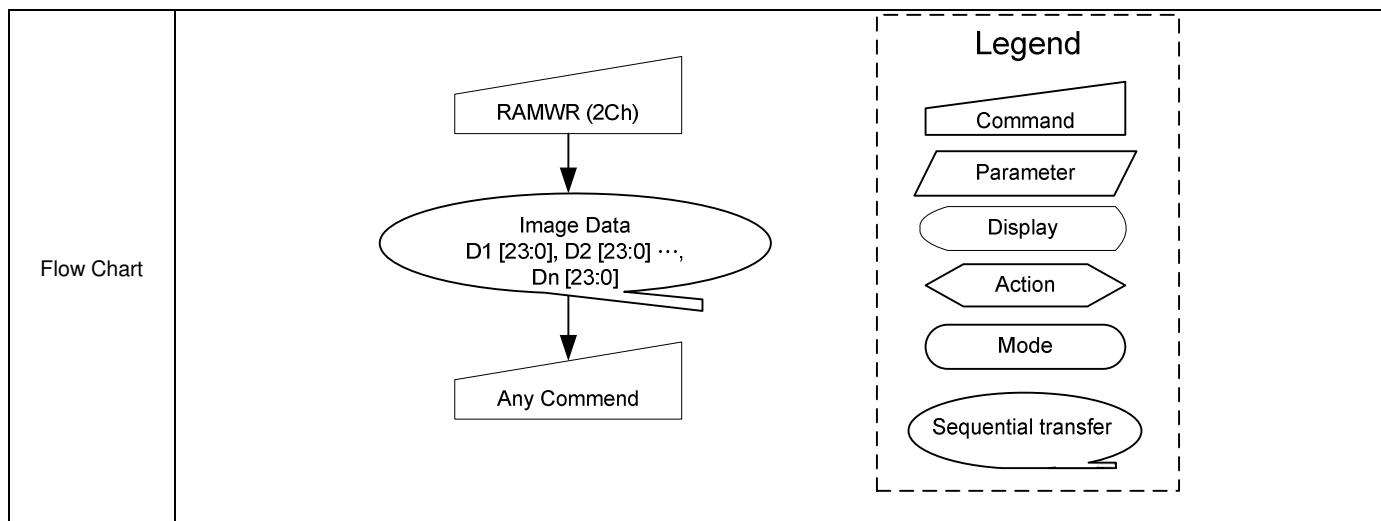
5.2.23. Page Address Set (2Bh)

| 2Bh | | PASET (Page Address Set) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|--|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|--------|---------------|--|-------------------|---|-------------------|---|-------------------|--|----------|-------------------|-------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2Bh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | SP [15:8] | | | | | | | | | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | SP [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | EP [15:8] | | | | | | | | | XX | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | EP [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| Description | This command is used to define the area of the frame memory that the MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command is applied. Each value represents one Page line in the Frame Memory. | | | | | | | | | | | | | | | | | | | | | | | | | |
| |  X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | SP [15:0] must always be equal to or less than EP [15:0] When SP [15:0] or EP [15:0] is greater than 01DFh (when MADCTL's D5 = 0) or 013Fh (when MADCTL's D5 = 1), data out of range will be ignored. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SP [15:0] = 0000h</td> <td>EP [15:0] = 013Fh</td> </tr> <tr> <td>SW Reset</td> <td>SP [15:0] = 0000h</td> <td>If MADCTL's D5 = 0: EP [15:0] = 01DFh If MADCTL's D5 = 1: EP [15:0] = 013Fh</td> </tr> <tr> <td>HW Reset</td> <td>SP [15:0] = 0000h</td> <td>EP [15:0] = 01EFh</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | | Power On Sequence | SP [15:0] = 0000h | EP [15:0] = 013Fh | SW Reset | SP [15:0] = 0000h | If MADCTL's D5 = 0: EP [15:0] = 01DFh If MADCTL's D5 = 1: EP [15:0] = 013Fh | HW Reset | SP [15:0] = 0000h | EP [15:0] = 01EFh |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | SP [15:0] = 0000h | EP [15:0] = 013Fh | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | SP [15:0] = 0000h | If MADCTL's D5 = 0: EP [15:0] = 01DFh If MADCTL's D5 = 1: EP [15:0] = 013Fh | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | SP [15:0] = 0000h | EP [15:0] = 01EFh | | | | | | | | | | | | | | | | | | | | | | | | |



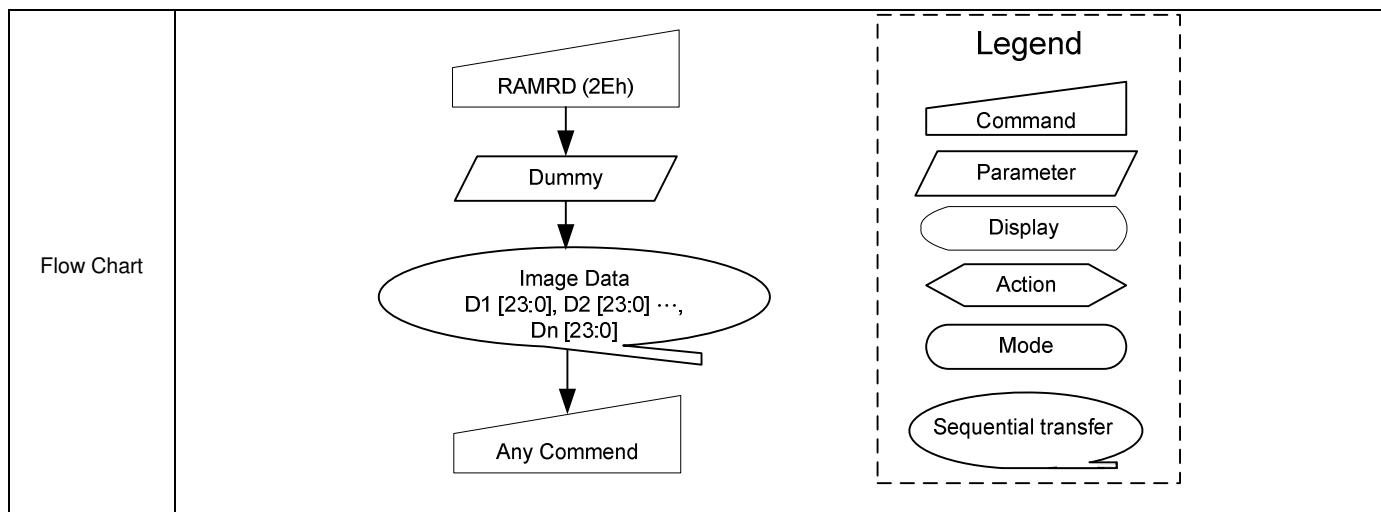
5.2.24. Memory Write (2Ch)

| 2Ch | | RAMWR (Memory Write) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|----------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|--|--------|---------------|--|------------------------------------|---|------------------------------------|---|------------------------------------|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | | D1 [23:0] | | | | | | | | XX | | | | | | | | | | | | | |
| : | 1 | 1 | ↑ | | Dx [23:0] | | | | | | | | XX | | | | | | | | | | | | | |
| N th Parameter | 1 | 1 | ↑ | | Dn [23:0] | | | | | | | | XX | | | | | | | | | | | | | |
| Description | <p>This command transfers image data from the host processor to the ILI9488's frame memory starting at the pixel location specified by Column Address Set (2Ah) and Page Address Set (2Bh) commands.</p> <p>If Memory Access Control (36h) D5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in the frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$, the extra pixels are ignored.</p> <p>If Memory Access control (36h) D5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in the frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$, the extra pixels are ignored.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | There is no restriction on the length of parameters. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is set randomly</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is set randomly</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Contents of memory is set randomly | SW Reset | Contents of memory is set randomly | HW Reset | Contents of memory is set randomly | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |

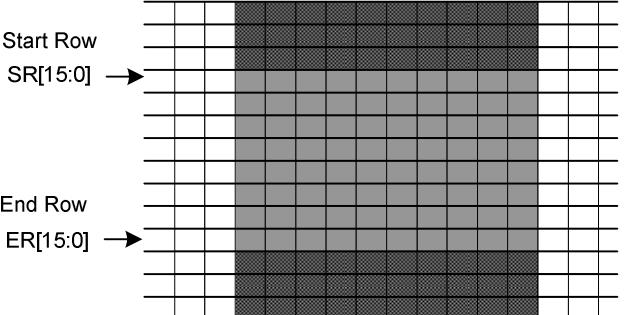
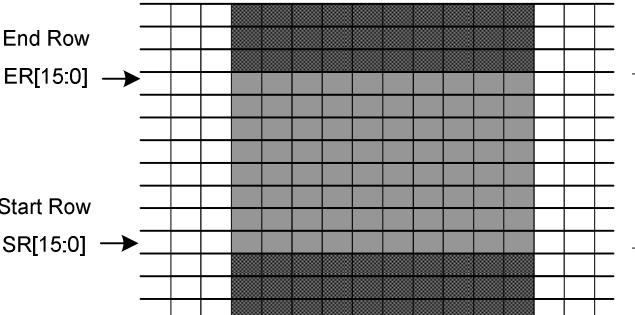
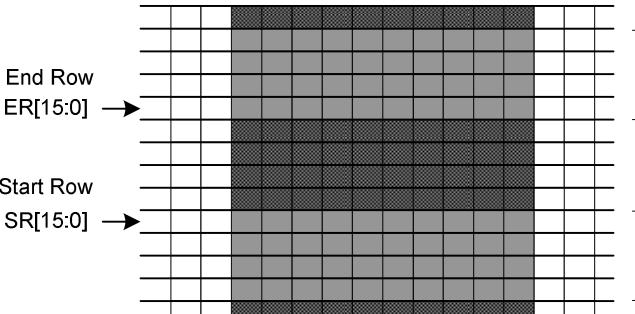


5.2.25. Memory Read (2Eh)

| 2Eh | | RAMRD (Memory Read) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------|-----|-----|----------|-----------|----|----|----|----|----|----|----|-----|--------|---------------|--|------------------------------------|---|------------------------------------|---|------------------------------------|--|-----|----------|-----|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | | XX | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2Eh | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | | | D1 [23:0] | | | | | | | | XX | | | | | | | | | | | | |
| : | 1 | ↑ | 1 | | | Dx [23:0] | | | | | | | | XX | | | | | | | | | | | | |
| (N+1) th Parameter | 1 | ↑ | 1 | | | Dn [23:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This command transfers image data from the ILI9488's frame memory to the host processor starting at the pixel location specified by set_column_address and set_page_address commands.</p> <p>If Memory Access control (36h) D5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from the frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If Memory Access Control (36h) D5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from the frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | There is no restriction on the length of parameters. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is set randomly</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is set randomly</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Contents of memory is set randomly | SW Reset | Contents of memory is set randomly | HW Reset | Contents of memory is set randomly | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | |

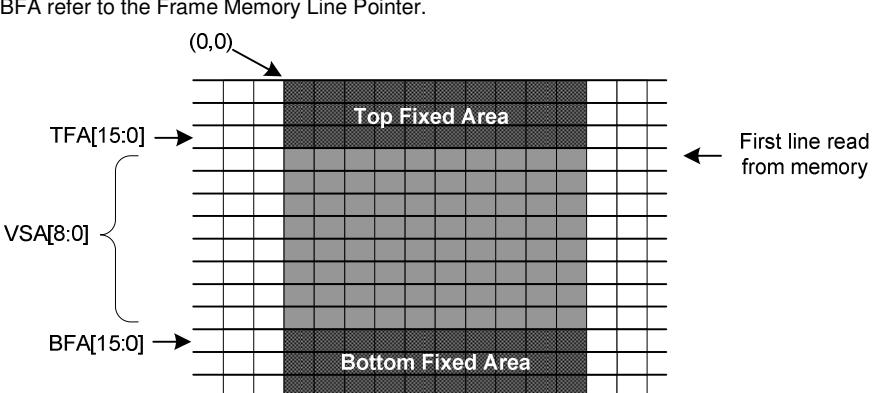


5.2.26. Partial Area (30h)

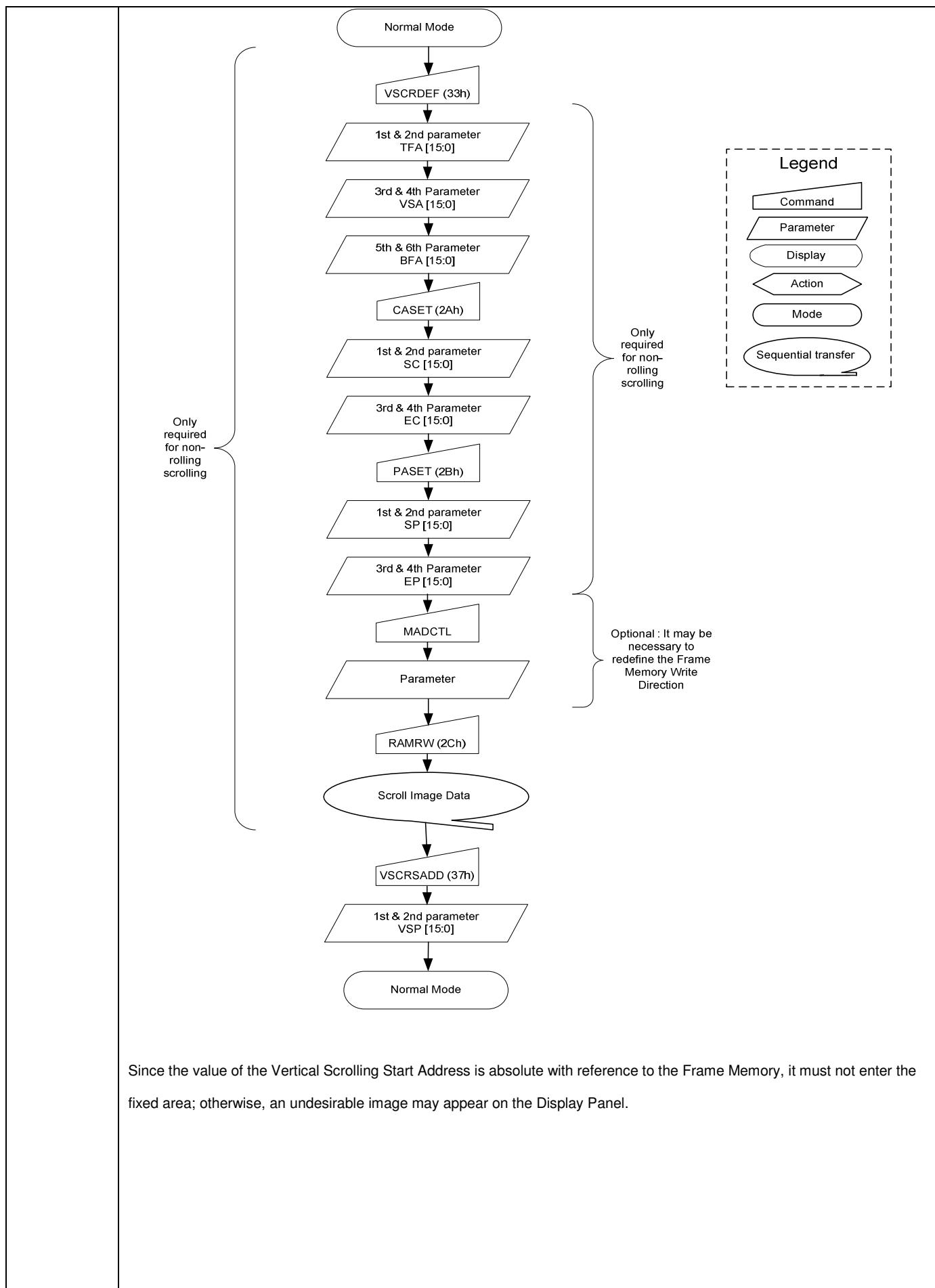
| PLTAR (Partial Area) | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|---|-----|-----|----------|-----------|----|----|----|----|----|----|----|-----|--|--|--|--|--|--|--|--|
| 30h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | SR [15:8] | | | | | | | | XX | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | SR [7:0] | | | | | | | | XX | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | ER [15:8] | | | | | | | | XX | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | ER [7:0] | | | | | | | | XX | | | | | | | | |
| Description | <p>This command defines the Partial Display mode's display area. There are two parameters associated with this command: the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory</p> <p>If End Row > Start Row when MADCTL (36h) D4 = 0:</p>  <p>If End Row > Start Row when MADCTL (36h) D4 = 1:</p>  <p>If End Row < Start Row when MADCTL (36h) D4 = 0:</p>  <p>If End Row = Start Row, then the Partial Area will be one row deep.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | |
| Restriction | SR [15:0] and ER [15:0] cannot be 0000h or exceed the last vertical line number (01EFh). | | | | | | | | | | | | | | | | | | | | |

| Register Availability | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Status</th><th style="text-align: center; padding: 5px;">Availability</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Normal Mode On, Idle Mode Off, Sleep Out</td><td style="padding: 5px;">Yes</td></tr> <tr> <td style="padding: 5px;">Normal Mode On, Idle Mode On, Sleep Out</td><td style="padding: 5px;">Yes</td></tr> <tr> <td style="padding: 5px;">Partial Mode On, Idle Mode Off, Sleep Out</td><td style="padding: 5px;">Yes</td></tr> <tr> <td style="padding: 5px;">Partial Mode On, Idle Mode On, Sleep Out</td><td style="padding: 5px;">Yes</td></tr> <tr> <td style="padding: 5px; text-align: center;">Sleep In</td><td style="padding: 5px;">Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
|---|---|---------------------------------|---------------|--|-------------------|---|---------------------------------|---|---------------------------------|--|----------|---------------------------------|---------------------------------|
| Status | Availability | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | |
| Default | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Status</th><th colspan="2" style="text-align: center; padding: 5px;">Default Value</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Power On Sequence</td><td style="padding: 5px;">SR [15:0] = 0000_{HEX}</td><td style="padding: 5px;">ER [15:0] = 01DF_{HEX}</td></tr> <tr> <td style="padding: 5px;">SW Reset</td><td style="padding: 5px;">SR [15:0] = 0000_{HEX}</td><td style="padding: 5px;">ER [15:0] = 01DF_{HEX}</td></tr> <tr> <td style="padding: 5px;">HW Reset</td><td style="padding: 5px;">SR [15:0] = 0000_{HEX}</td><td style="padding: 5px;">ER [15:0] = 01DF_{HEX}</td></tr> </tbody> </table> | Status | Default Value | | Power On Sequence | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} | SW Reset | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} | HW Reset | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} |
| Status | Default Value | | | | | | | | | | | | |
| Power On Sequence | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} | | | | | | | | | | | |
| SW Reset | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} | | | | | | | | | | | |
| HW Reset | SR [15:0] = 0000 _{HEX} | ER [15:0] = 01DF _{HEX} | | | | | | | | | | | |
| Flow Chart | <p>1. To Enter Partial Mode</p> <pre> graph TD PLTAR[PLTAR(30h)] --> S1_1[1st Parameter: SR [15:8]] --> S1_2[2nd Parameter: SR [7:0]] S1_1 --- S1_2 S1_2 --> S2_1[3rd Parameter: ER [15:8]] --> S2_2[4th Parameter: ER [7:0]] S2_1 --- S2_2 S2_2 --> PTION[PTION (12h)] PTION --> PM[Partial Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>2. To Leave Partial Mode</p> <pre> graph TD PM[Partial Mode] --> DISPOFF[DISPOFF (28h)] DISPOFF --> NORON[NORON (13h)] NORON --> PMOFF[Partial Mode OFF] PMOFF --> RAMRW[RAMRW (2Ch)] RAMRW --> ID[Image Data D1 [23:0], D2 [23:0] ..., Dn [23:0]] ID --> DISPON[DISPON(29h)] </pre> <p>(Option) To prevent Tearing Effect Image displayed</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | |

5.2.27. Vertical Scrolling Definition (33h)

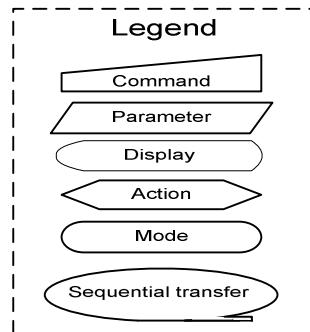
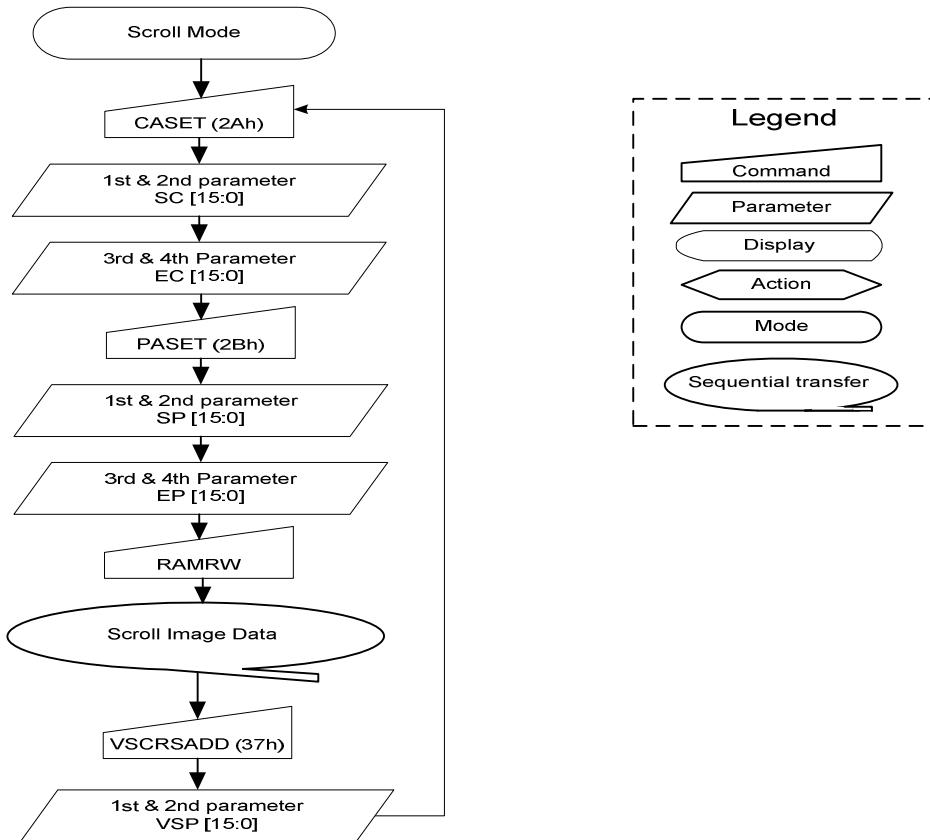
| 33h | | VSCRDEF (Vertical Scrolling Definition) | | | | | | | | | | | | | | | | | | | | |
|---------------------------|---|---|-----|-----|----------|------------|----|----|----|----|----|----|----|-----|--|--|--|--|--|--|--|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33h | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | | XX | TFA [15:8] | | | | | | | | XX | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | | XX | TFA [7:0] | | | | | | | | XX | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | | XX | VSA [15:8] | | | | | | | | XX | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | | XX | VSA [7:0] | | | | | | | | XX | | | | | | | | |
| 5 th Parameter | 1 | 1 | ↑ | | XX | BFA [15:8] | | | | | | | | XX | | | | | | | | |
| 6 th Parameter | 1 | 1 | ↑ | | XX | BFA [7:0] | | | | | | | | XX | | | | | | | | |
| Description | <p>This command defines the display vertical scrolling area.</p> <p>Memory Access Control (36h) D4 = 0: The 1st and 2nd parameter, TFA [8:0], describe the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd and 4th parameter, VSA [8:0], describe the height of the Vertical Scrolling Area in number of lines of the frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.</p> <p>The 5th and 6th parameter, BFA [8:0], describe the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.</p> <p>TFA, VSA, and BFA refer to the Frame Memory Line Pointer.</p>  | | | | | | | | | | | | | | | | | | | | | |
| | <p>Memory Access Control (36h) D4 = 1: The 1st and 2nd parameter, TFA [8:0], describe the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.</p> <p>The 3rd and 4th parameter, VSA [8:0], describe the height of the Vertical Scrolling Area in number of lines of the frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.</p> <p>The 5th and 6th parameter, BFA [8:0], describe the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.</p> <p>TFA, VSA, and BFA refer to the Frame Memory Line Pointer.</p> | | | | | | | | | | | | | | | | | | | | | |

| | <p>X = void</p> <p>First line read from memory</p> | | | | | | | | | | | | | | | | |
|---|--|----------------------------------|----------------------------------|--|-----|---|----------------------------------|---|----------------------------------|--|----------------------------------|----------------------------------|----------------------------------|----------|----------------------------------|----------------------------------|----------------------------------|
| Restriction | The sum of TFA, VSA, and BFA must equal the number of the display device's horizontal lines (pages); otherwise, the Scrolling mode is undefined. In the Vertical Scroll Mode, set_address_mode B5 should be set to 0 – this only affects the Frame Memory Write. | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | | |
| Status | Availability | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th colspan="3">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = 01E0_{HEX}</td><td>BFA [15:0] = 0000_{HEX}</td></tr> <tr> <td>SW Reset</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = 01E0_{HEX}</td><td>BFA [15:0] = 0000_{HEX}</td></tr> <tr> <td>HW Reset</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = 01E0_{HEX}</td><td>BFA [15:0] = 0000_{HEX}</td></tr> </tbody> </table> | Status | Default Value | | | Power On Sequence | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} | SW Reset | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} | HW Reset | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} |
| Status | Default Value | | | | | | | | | | | | | | | | |
| Power On Sequence | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} | | | | | | | | | | | | | | |
| SW Reset | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} | | | | | | | | | | | | | | |
| HW Reset | TFA [15:0] = 0000 _{HEX} | VSA [15:0] = 01E0 _{HEX} | BFA [15:0] = 0000 _{HEX} | | | | | | | | | | | | | | |
| Flow Chart | <ol style="list-style-type: none"> To enter the Vertical Scroll Mode: | | | | | | | | | | | | | | | | |

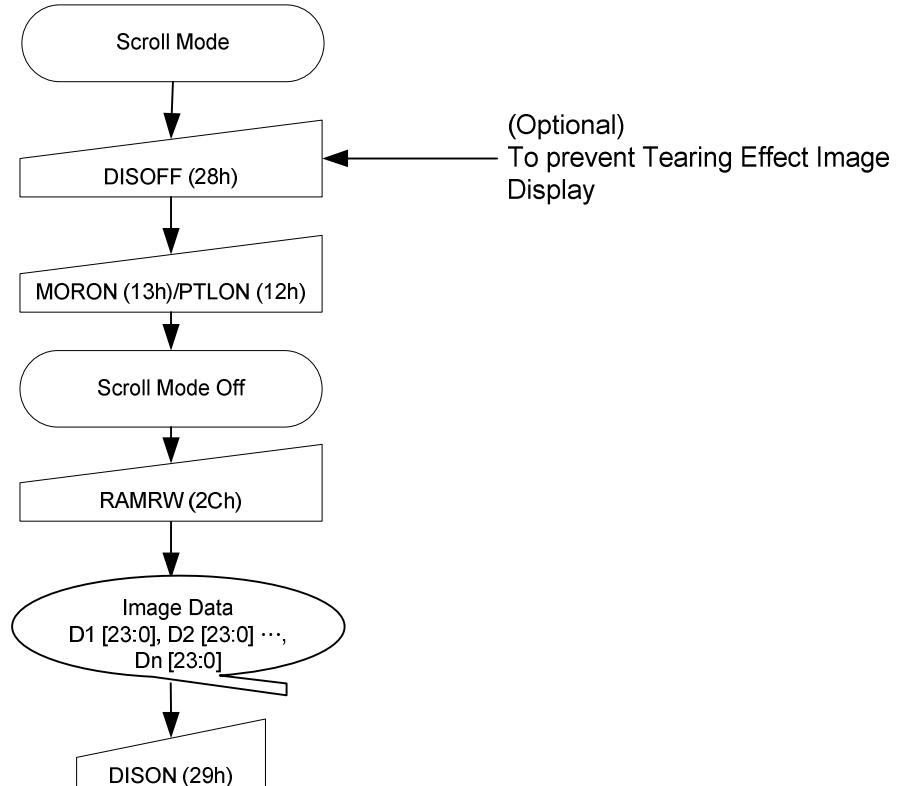


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise, an undesirable image may appear on the Display Panel.

2. Continuous Scroll:

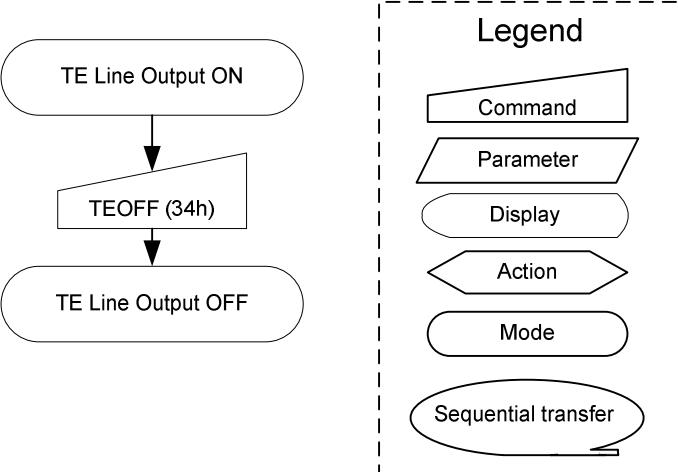


3. To Leave the Vertical Scroll Mode:

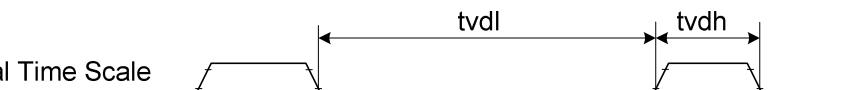
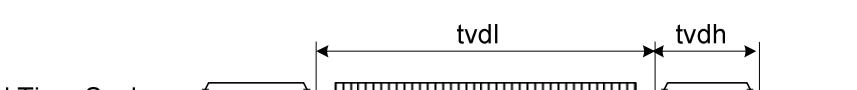


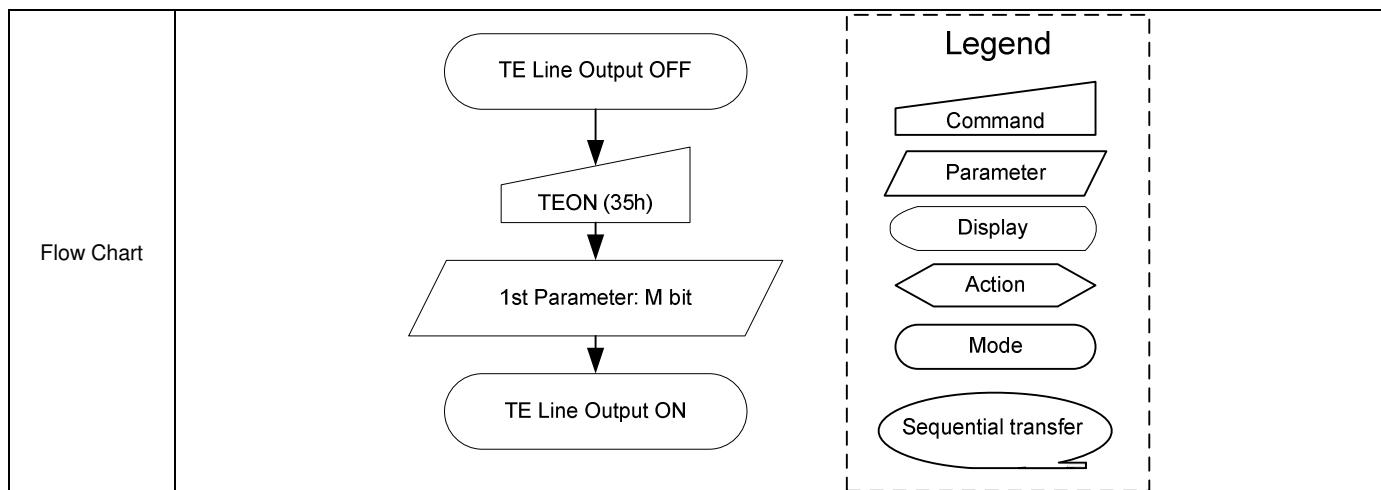
Note: To exit the Scroll Mode, both Normal Display Mode On (13h) and Partial Mode On (12h) commands can be used.

5.2.28. Tearing Effect Line OFF (34h)

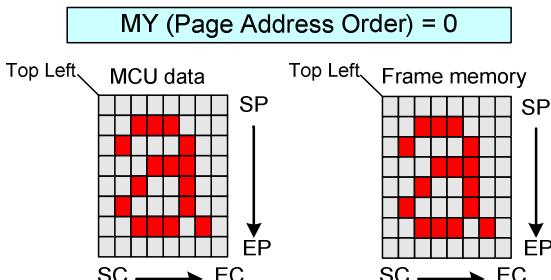
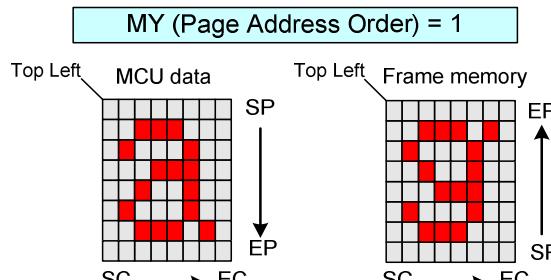
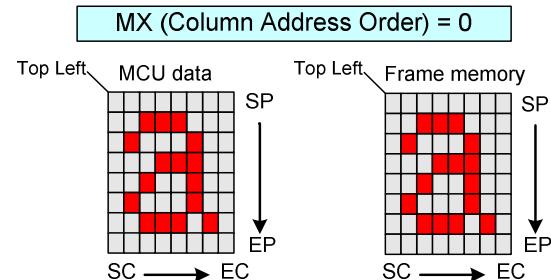
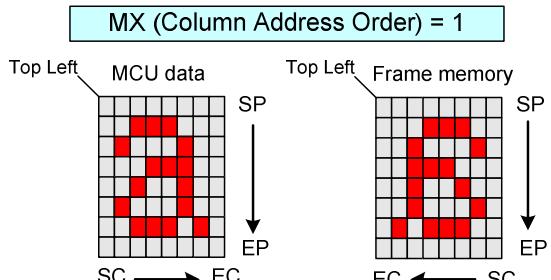
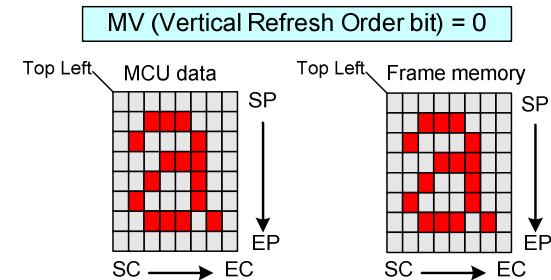
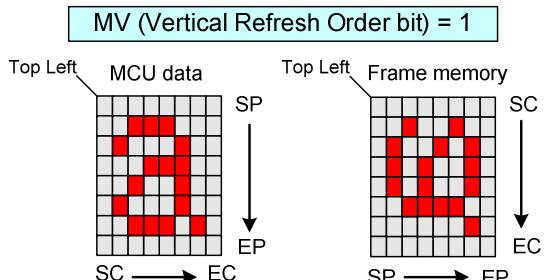
| 34h | | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command turns off the ILI9488's Tearing Effect output signal on the TE signal line.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the Tearing Effect output is already Off. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>OFF</td></tr> <tr> <td>SW Reset</td><td>OFF</td></tr> <tr> <td>HW Reset</td><td>OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | OFF | SW Reset | OFF | HW Reset | OFF | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <pre> graph TD A([TE Line Output ON]) --> B[TEOFF (34h)] B --> C([TE Line Output OFF]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.29. Tearing Effect Line ON (35h)

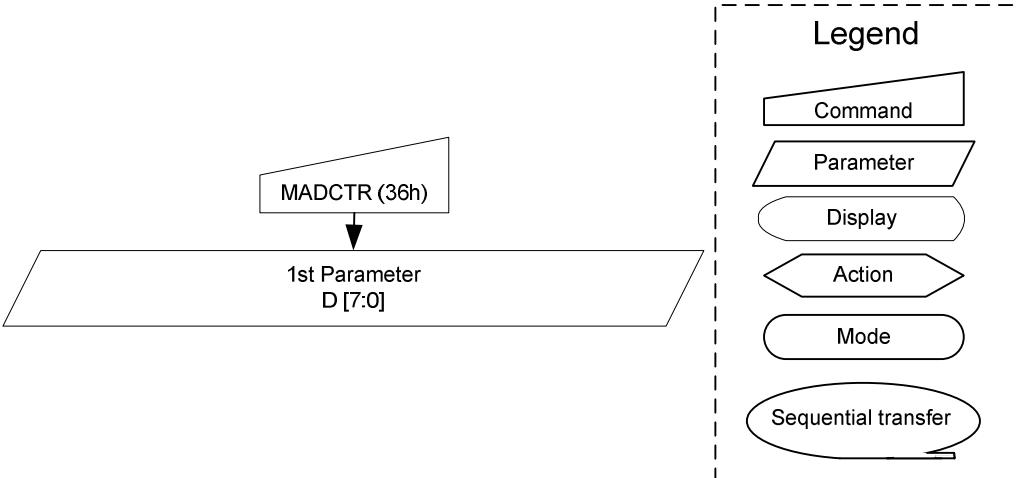
| 35h | | TEOFF (Tearing Effect Line ON) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------|-----|----------|----|----|----|----|----|----|----|----|-----|--|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | M | XX | | | | | | | | | | | | | |
| Description | <p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. Changing the MADCTL bit D4 will not affect this output. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.</p> <p>When M = 0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>Vertical Time Scale</p> <p>tvdl</p> <p>tvdh</p> <p>When M = 1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information :</p>  <p>Vertical Time Scale</p> <p>tvdl</p> <p>tvdh</p> <p>Note: During the Sleep In Mode with the Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the Tearing Effect output is already off. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>OFF</td></tr> <tr> <td>SW Reset</td><td>OFF</td></tr> <tr> <td>HW Reset</td><td>OFF</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | OFF | SW Reset | OFF | HW Reset | OFF | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | OFF | | | | | | | | | | | | | | | | | | | | | | | | | |



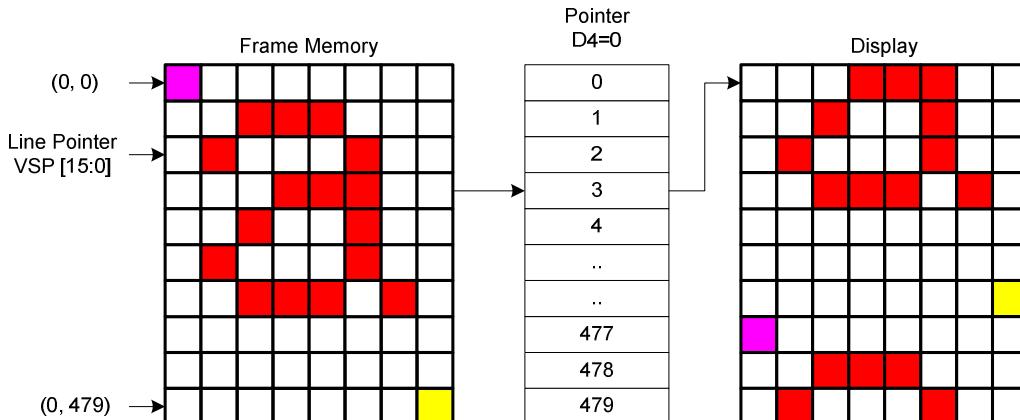
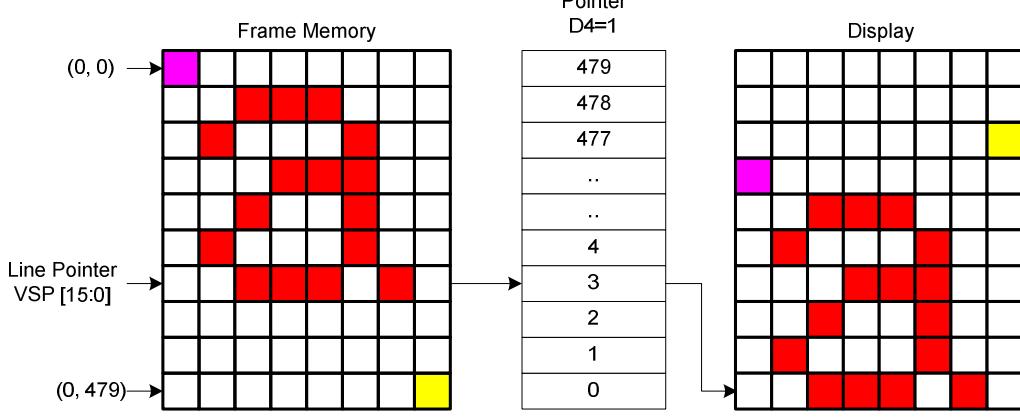
5.2.30. Memory Access Control (36h)

| 36h | | MADCTL (Memory Access Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|--|---|---|----------|----|----|----|----|-----|----|----|----|-----|--|-----|--------|------|-------------|----|----|-------------------|---|----|----|----------------------|----|----|---------------------|----|----|------------------------|---|----|-----|---------------|---|----|----|--------------------------|--|----|---|----------|----------|----|---|----------|----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | MY | MX | MV | ML | BGR | MH | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | This command defines read/write scanning direction of the frame memory. This command makes no change on other driver status. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <table border="1"> <thead> <tr> <th>Bit</th><th>Symbol</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>D7</td><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control the direction from the MPU to memory write/read.</td></tr> <tr> <td>D6</td><td>MX</td><td>Column Address Order</td></tr> <tr> <td>D5</td><td>MV</td><td>Row/Column Exchange</td></tr> <tr> <td>D4</td><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr> <tr> <td>D3</td><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel)</td></tr> <tr> <td>D2</td><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr> <tr> <td>D1</td><td>X</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>D0</td><td>X</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> | | | | | | | | | | | | | | Bit | Symbol | Name | Description | D7 | MY | Row Address Order | These 3 bits control the direction from the MPU to memory write/read. | D6 | MX | Column Address Order | D5 | MV | Row/Column Exchange | D4 | ML | Vertical Refresh Order | LCD vertical refresh direction control. | D3 | BGR | RGB-BGR Order | Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel) | D2 | MH | Horizontal Refresh ORDER | LCD horizontal refreshing direction control. | D1 | X | Reserved | Reserved | D0 | X | Reserved | Reserved |
| Bit | Symbol | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | MY | Row Address Order | These 3 bits control the direction from the MPU to memory write/read. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | MX | Column Address Order | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | MV | Row/Column Exchange | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | ML | Vertical Refresh Order | LCD vertical refresh direction control. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | BGR | RGB-BGR Order | Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | MH | Horizontal Refresh ORDER | LCD horizontal refreshing direction control. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D1 | X | Reserved | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D0 | X | Reserved | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | |
|-------------|---|---|
| | ML (Vertical refresh order bit) = 0 | ML (Vertical refresh order bit) = 1 |
| | | |
| | BGR (RGB-BGR Order control bit) = 0 | BGR (RGB-BGR Order control bit) = 1 |
| | | |
| | MH (Horizontal refresh order control bit) = 0 | MH (Horizontal refresh order control bit) = 1 |
| | | |
| Restriction | <p>Note: Top-Left (0,0) represents the physical memory location.</p> <p>X = void</p> | |

| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
|---|---|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Status | Availability | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>00h</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 00h | SW Reset | 00h | HW Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | |
| Power On Sequence | 00h | | | | | | | | | | | | |
| SW Reset | 00h | | | | | | | | | | | | |
| HW Reset | 00h | | | | | | | | | | | | |
| Flow Chart |  <p>The flowchart illustrates the structure of a command. It starts with a rectangular box labeled "MADCTR (36h)" with an arrow pointing down to a trapezoidal box labeled "1st Parameter D [7:0]". To the right of the flowchart is a legend enclosed in a dashed box, mapping symbols to command types:</p> <ul style="list-style-type: none"> Command: Triangular symbol Parameter: Rectangle Display: Oval Action: Diamond Mode: Horizontal oval Sequential transfer: Oval with a trailing arrow | | | | | | | | | | | | |

5.2.31. Vertical Scrolling Start Address (37h)

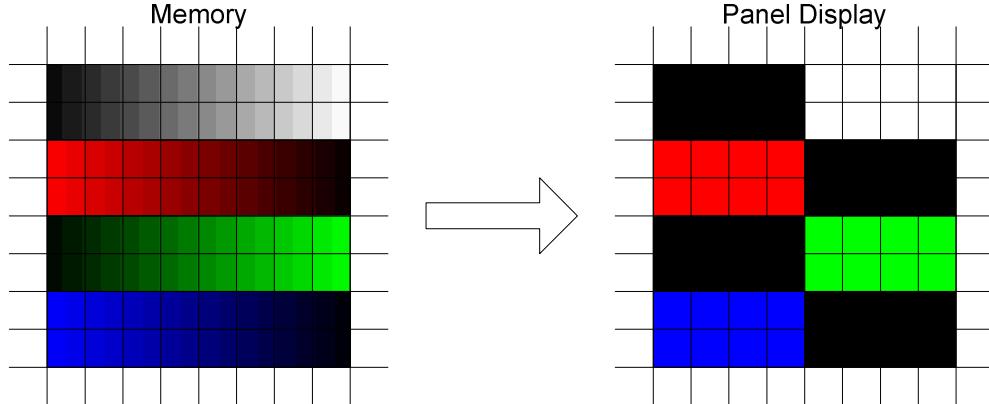
| 37h | VSCRSADD (Vertical Scrolling Start Address) | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|---|-----|-----|----------|------------|----|----|----|----|----|----|----|-----|--|--|--|--|--|--|--|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37h | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | VSP [15:8] | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | VSP [7:0] | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display, as illustrated below:</p> <p>When MADCTL(36h) D4 = 0</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480, and VSP = 3</p>  <p>When MADCTL(36h) D4 = 1</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480, and VSP = 3</p>  <p>Note: When the new Pointer position and Picture Data are sent, the result on the display will appear at the next Panel Scan to avoid tearing effect.</p> <p>VSP refers to the Frame Memory line Pointer.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | |
| Restriction | Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)). Otherwise, undesirable image will occur on the Panel. | | | | | | | | | | | | | | | | | | | | | |

| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
|---|--|--------|---------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Status | Availability | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>00h</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </tbody> </table> | Status | Default Value | Power On Sequence | 00h | SW Reset | 00h | HW Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | |
| Power On Sequence | 00h | | | | | | | | | | | | |
| SW Reset | 00h | | | | | | | | | | | | |
| HW Reset | 00h | | | | | | | | | | | | |
| Flow Chart | See Vertical Scrolling Definition (33h) description. | | | | | | | | | | | | |

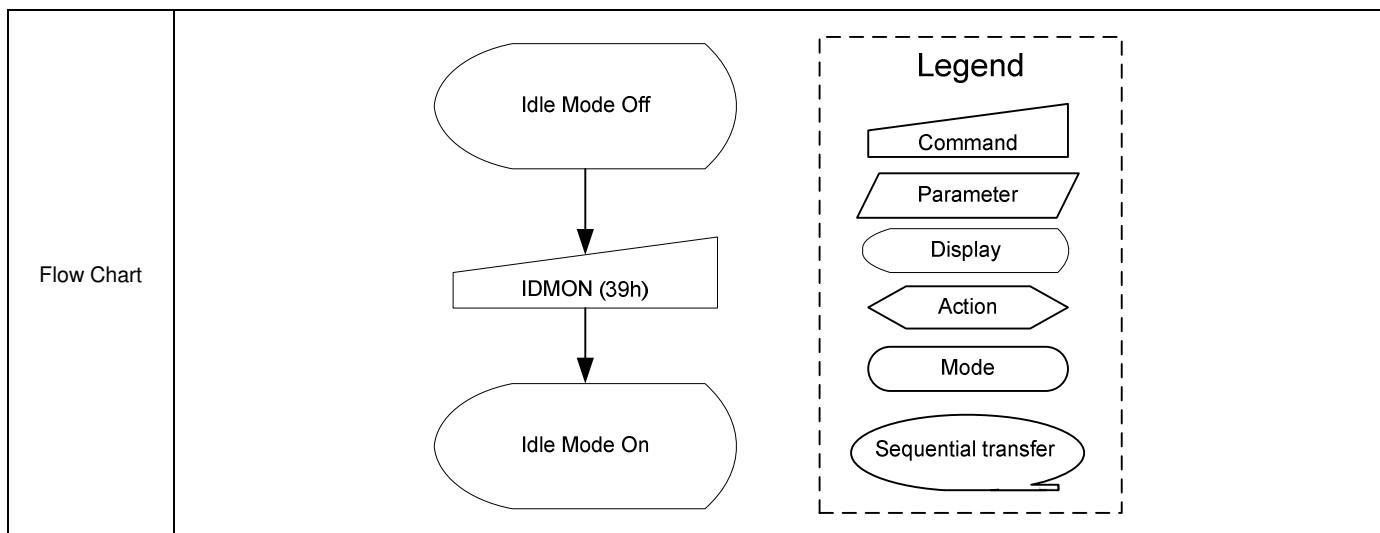
5.2.32. Idle Mode OFF (38h)

| 38h | | IDMOFF (Idle Mode OFF) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|--------|---------------|--|---------------|---|---------------|---|---------------|--|-----|----------|-----|--|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command causes the ILI9488 to exit the Idle mode. In the Idle Mode OFF, the display panel can display a maximum of 262,144 colors.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the ILI9488 is not in the Idle mode. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Idle Mode Off</td></tr> <tr> <td>SW Reset</td><td>Idle Mode Off</td></tr> <tr> <td>HW Reset</td><td>Idle Mode Off</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Idle Mode Off | SW Reset | Idle Mode Off | HW Reset | Idle Mode Off | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Idle Mode Off | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Idle Mode Off | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Idle Mode Off | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD A([Idle mode on]) --> B[/IDMOFF (38h)] B --> C([Idle mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.33. Idle Mode ON (39h)

| 39h | IDMON (Idle Mode ON) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------------------------|--|----------------|---|---------------|---|---------------|--|-----|----------|-----|--|--|--|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|-----|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|---------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|-------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|-------|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | No parameter | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used to enter the Idle Mode On.</p> <p>In the Idle Mode On, color expression is reduced. The first bits of R, G, and B in the Frame Memory will determine the display color, as shown in the table below.</p>  <table border="1"> <thead> <tr> <th colspan="14">Memory Contents vs. Display Color</th> </tr> <tr> <th></th> <th>R₅</th> <th>R₄</th> <th>R₃</th> <th>R₂</th> <th>R₁</th> <th>R₀</th> <th>G₅</th> <th>G₄</th> <th>G₃</th> <th>G₂</th> <th>G₁</th> <th>G₀</th> <th>B₅</th> <th>B₄</th> <th>B₃</th> <th>B₂</th> <th>B₁</th> <th>B₀</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | | Memory Contents vs. Display Color | | | | | | | | | | | | | | | R ₅ | R ₄ | R ₃ | R ₂ | R ₁ | R ₀ | G ₅ | G ₄ | G ₃ | G ₂ | G ₁ | G ₀ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | Black | 0XXXXX | | | | | | 0XXXXX | | | | | | 0XXXXX | | | | | | Blue | 0XXXXX | | | | | | 0XXXXX | | | | | | 1XXXXX | | | | | | Red | 1XXXXX | | | | | | 0XXXXX | | | | | | 0XXXXX | | | | | | Magenta | 1XXXXX | | | | | | 0XXXXX | | | | | | 1XXXXX | | | | | | Green | 0XXXXX | | | | | | 1XXXXX | | | | | | 0XXXXX | | | | | | Cyan | 0XXXXX | | | | | | 1XXXXX | | | | | | 1XXXXX | | | | | | Yellow | 1XXXXX | | | | | | 1XXXXX | | | | | | 0XXXXX | | | | | | White | 1XXXXX | | | | | | 1XXXXX | | | | | | 1XXXXX | | | | | |
| Memory Contents vs. Display Color | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | R ₅ | R ₄ | R ₃ | R ₂ | R ₁ | R ₀ | G ₅ | G ₄ | G ₃ | G ₂ | G ₁ | G ₀ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Black | 0XXXXX | | | | | | 0XXXXX | | | | | | 0XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Blue | 0XXXXX | | | | | | 0XXXXX | | | | | | 1XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Red | 1XXXXX | | | | | | 0XXXXX | | | | | | 0XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Magenta | 1XXXXX | | | | | | 0XXXXX | | | | | | 1XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Green | 0XXXXX | | | | | | 1XXXXX | | | | | | 0XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Cyan | 0XXXXX | | | | | | 1XXXXX | | | | | | 1XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Yellow | 1XXXXX | | | | | | 1XXXXX | | | | | | 0XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| White | 1XXXXX | | | | | | 1XXXXX | | | | | | 1XXXXX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the module is already in the Idle Off mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle mode OFF</td> </tr> <tr> <td>SW Reset</td> <td>Idle mode OFF</td> </tr> <tr> <td>HW Reset</td> <td>Idle mode OFF</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Idle mode OFF | SW Reset | Idle mode OFF | HW Reset | Idle mode OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Idle mode OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Idle mode OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Idle mode OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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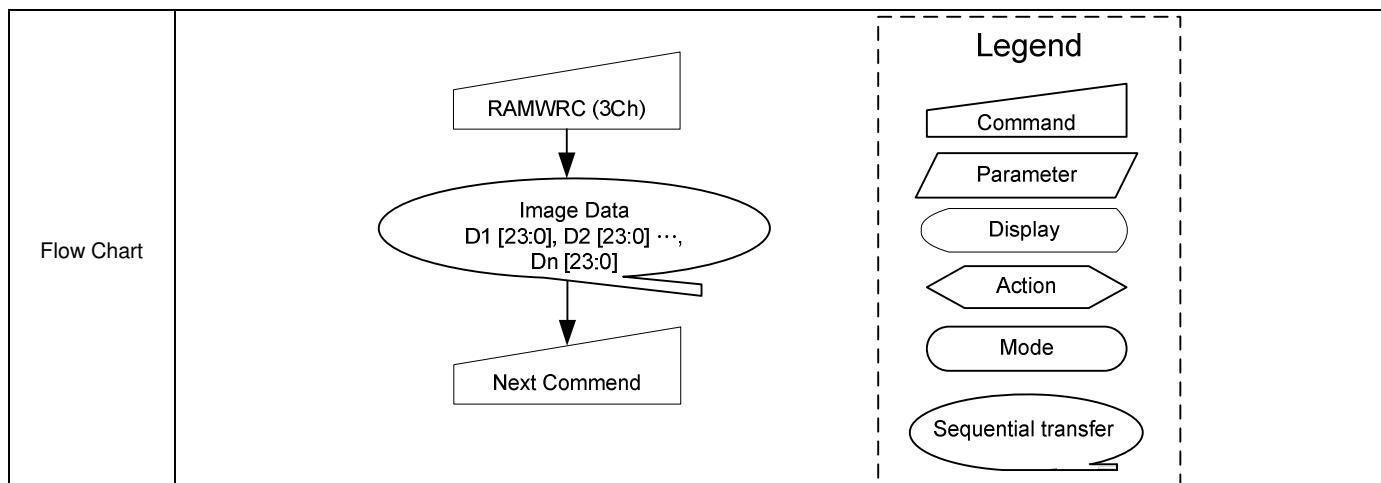


5.2.34. Interface Pixel Format (3Ah)

| 3Ah | | COLMOD (Interface Pixel Format) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------------------|----------------------|-----------|----|-----------|------------------------|----|----|-----------|----|----|-----|--|-----------|---------------|--|----------------------|---|-----|---|----------------------|--|-----|----------|-----|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|------------------------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|---------------|---|---|---|-----------------|---|---|---|---------------|---|---|---|-----------------|---|---|---|---------------|---|---|---|-----------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3Ah | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | X | DPI [2:0] | | | X | DBI [2:0] | | | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format selector of the RGB interface, and DBI [2:0] is the pixel format of the MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="3">DPI [2:0]</th> <th>RGB Interface Format</th> <th colspan="3">DBI [2:0]</th> <th colspan="3">MCU Interface Format</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>Reserved</td> <td>0</td><td>0</td><td>0</td><td>Reserved</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>Reserved</td> <td>0</td><td>0</td><td>1</td><td>3 bits/pixel (8 color)</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>Reserved</td> <td>0</td><td>1</td><td>0</td><td>Reserved</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>Reserved</td> <td>0</td><td>1</td><td>1</td><td>Reserved</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>Reserved</td> <td>1</td><td>0</td><td>0</td><td>Reserved</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>16 bits/pixel</td> <td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td> </tr> <tr> <td>1</td><td>1</td><td>0</td><td>18 bits/pixel</td> <td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>24 bits/pixel</td> <td>1</td><td>1</td><td>1</td><td>24 bits / pixel</td> </tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | | DPI [2:0] | | | RGB Interface Format | DBI [2:0] | | | MCU Interface Format | | | 0 | 0 | 0 | Reserved | 0 | 0 | 0 | Reserved | 0 | 0 | 1 | Reserved | 0 | 0 | 1 | 3 bits/pixel (8 color) | 0 | 1 | 0 | Reserved | 0 | 1 | 0 | Reserved | 0 | 1 | 1 | Reserved | 0 | 1 | 1 | Reserved | 1 | 0 | 0 | Reserved | 1 | 0 | 0 | Reserved | 1 | 0 | 1 | 16 bits/pixel | 1 | 0 | 1 | 16 bits / pixel | 1 | 1 | 0 | 18 bits/pixel | 1 | 1 | 0 | 18 bits / pixel | 1 | 1 | 1 | 24 bits/pixel | 1 | 1 | 1 | 24 bits / pixel |
| DPI [2:0] | | | RGB Interface Format | DBI [2:0] | | | MCU Interface Format | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | Reserved | 0 | 0 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | Reserved | 0 | 0 | 1 | 3 bits/pixel (8 color) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | Reserved | 0 | 1 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | Reserved | 0 | 1 | 1 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | Reserved | 1 | 0 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 16 bits/pixel | 1 | 0 | 1 | 16 bits / pixel | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 18 bits/pixel | 1 | 1 | 0 | 18 bits / pixel | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 24 bits/pixel | 1 | 1 | 1 | 24 bits / pixel | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>06h</td> </tr> <tr> <td>SW Reset</td> <td>06h</td> </tr> <tr> <td>HW Reset</td> <td>06h</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 06h | SW Reset | 06h | HW Reset | 06h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 06h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 06h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 06h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>Example :</p> <pre> graph TD A([18 bit/pixel Mode]) --> B[/ COLMOD(3Ah) DBI: 111 /] B --> C([24 bit/pixel Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

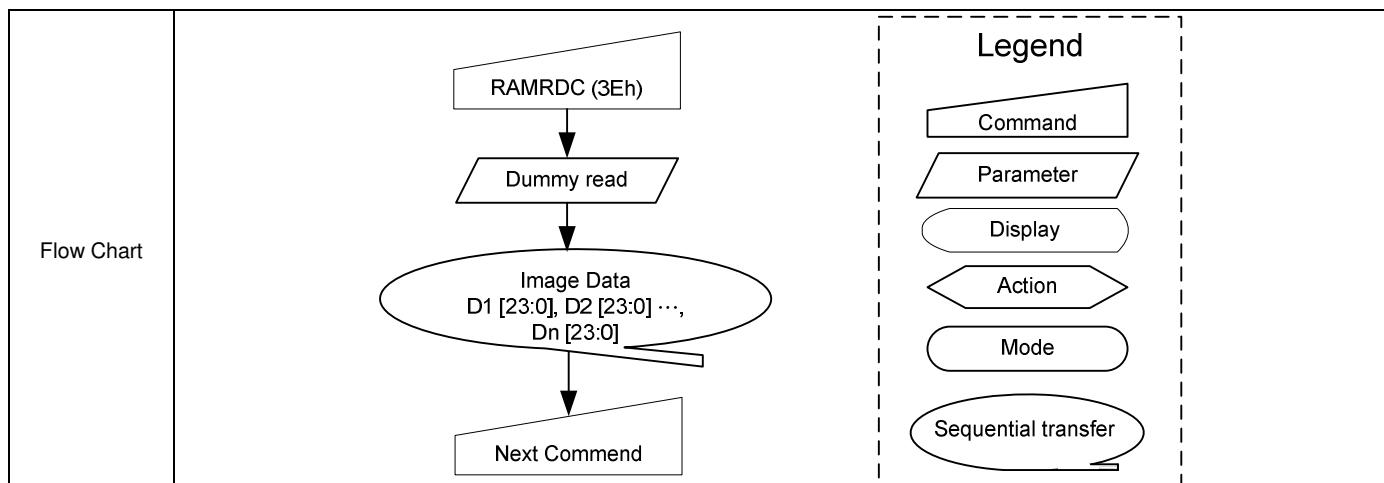
5.2.35. Memory Write Continue (3Ch)

| 3Ch | 13 | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | |
|---|---|----------------------|-----|-----|-----------|----|----|----|----|----|----|----|-----|-----------|----------------|--|--------------------------------------|---|------------------------------------|---|------------------------------------|--|---|------------------------|------------------|---|------------------------|----------------------|
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3Ch | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | | D1 [23:0] | | | | | | | | XX | | | | | | | | | | | | | | | |
| : | 1 | 1 | ↑ | | Dx [23:0] | | | | | | | | XX | | | | | | | | | | | | | | | |
| N th Parameter | 1 | 1 | ↑ | | Dn [23:0] | | | | | | | | XX | | | | | | | | | | | | | | | |
| Description | <p>This command is used to transfer data from the MCU to the frame memory if the frame memory wants to continue memory write after the "Memory Write (2Ch)" command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions as it has been done by the "Memory Write (2Ch)" command.</p> <p>Then D [23:0] is stored in the frame memory and the column register and the page register incremented as the table below:</p> <p>Column and Page Counter Control.</p> <table border="1"> <thead> <tr> <th>Condition</th><th>Column counter</th><th>Page Counter</th></tr> </thead> <tbody> <tr> <td>When RAMWR/RAMRD command is accepted</td><td>Return to Start Column</td><td>Return to Start Page</td></tr> <tr> <td>Complete Pixel Read/Write action</td><td>Incremented by 1</td><td>No change</td></tr> <tr> <td>The Column counter value is large than the End Column</td><td>Return to Start Column</td><td>Incremented by 1</td></tr> <tr> <td>The Page counter value is large than the End Page</td><td>Return to Start Column</td><td>Return to Start Page</td></tr> </tbody> </table> <p>Sending any other command can stop the Frame Write.</p> <p>X = void</p> | | | | | | | | | | | | | Condition | Column counter | Page Counter | When RAMWR/RAMRD command is accepted | Return to Start Column | Return to Start Page | Complete Pixel Read/Write action | Incremented by 1 | No change | The Column counter value is large than the End Column | Return to Start Column | Incremented by 1 | The Page counter value is large than the End Page | Return to Start Column | Return to Start Page |
| Condition | Column counter | Page Counter | | | | | | | | | | | | | | | | | | | | | | | | | | |
| When RAMWR/RAMRD command is accepted | Return to Start Column | Return to Start Page | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Complete Pixel Read/Write action | Incremented by 1 | No change | | | | | | | | | | | | | | | | | | | | | | | | | | |
| The Column counter value is large than the End Column | Return to Start Column | Incremented by 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| The Page counter value is large than the End Page | Return to Start Column | Return to Start Page | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>There is no restriction on the length of parameters.</p> <p>No access to the frame memory in the Sleep In mode.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is set randomly</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is set randomly</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Contents of memory is set randomly | SW Reset | Contents of memory is set randomly | HW Reset | Contents of memory is set randomly | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | |

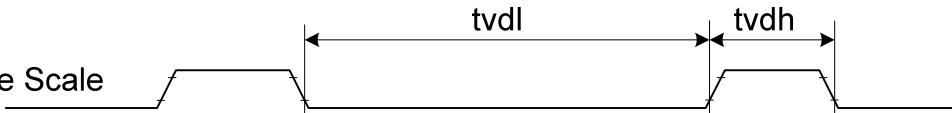
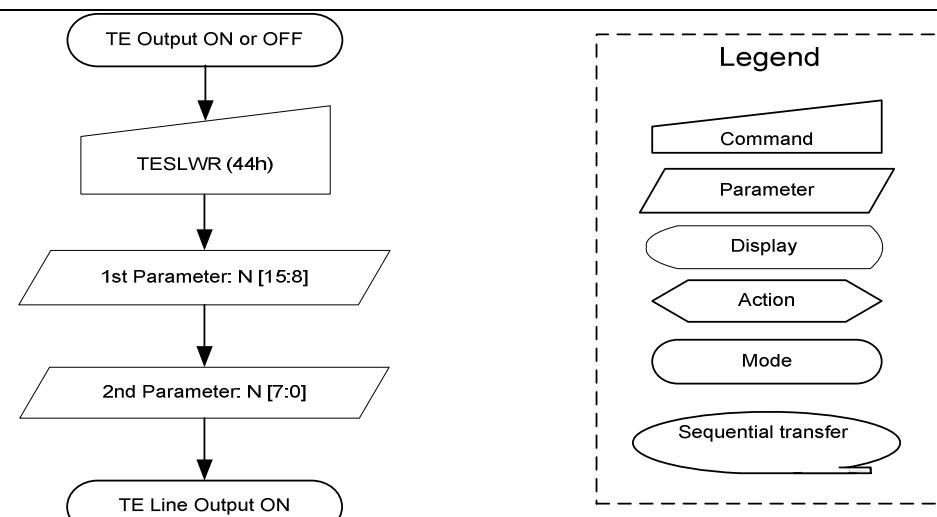


5.2.36. Memory Read Continue (3Eh)

| RAMRDRC (Memory Read Continue) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|-----------|----------------|--|--------------------------------------|---|------------------------------------|---|------------------------------------|--|---|--------------------------|----------------|---|--------------------------|------------------------|
| 3Eh | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3Eh | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | | D1 [23:0] | | | | | | | | | XX | | | | | | | | | | | | | | | |
| : | 1 | ↑ | 1 | | Dx [23:0] | | | | | | | | | XX | | | | | | | | | | | | | | | |
| N th Parameter | 1 | ↑ | 1 | | Dn [23:0] | | | | | | | | | XX | | | | | | | | | | | | | | | |
| Description | <p>This command is used to transfer data from the frame memory to the MCU, if the MCU wants to continue memory read after "Memory Read (2Eh)" command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions as it has been done by the "Memory Read (2Eh)" command.</p> <p>Then D [23:0] is read back from the frame memory, and the column register and the page register are incremented as shown in the table below: Column and Page Counter Control.</p> <table border="1"> <thead> <tr> <th>Condition</th> <th>Column counter</th> <th>Page Counter</th> </tr> </thead> <tbody> <tr> <td>When RAMWR/RAMRD command is accepted</td> <td>Return to "Start Column"</td> <td>Return to "Start Page"</td> </tr> <tr> <td>Complete Pixel Read/Write action</td> <td>Increment by 1</td> <td>No change</td> </tr> <tr> <td>The Column counter value is large than "End Column"</td> <td>Return to "Start Column"</td> <td>Increment by 1</td> </tr> <tr> <td>The Page counter value is large than "End Page"</td> <td>Return to "Start Column"</td> <td>Return to "Start Page"</td> </tr> </tbody> </table> <p>Frame Read can be stopped by sending any other command.</p> <p>X = void</p> | | | | | | | | | | | | | | Condition | Column counter | Page Counter | When RAMWR/RAMRD command is accepted | Return to "Start Column" | Return to "Start Page" | Complete Pixel Read/Write action | Increment by 1 | No change | The Column counter value is large than "End Column" | Return to "Start Column" | Increment by 1 | The Page counter value is large than "End Page" | Return to "Start Column" | Return to "Start Page" |
| Condition | Column counter | Page Counter | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| When RAMWR/RAMRD command is accepted | Return to "Start Column" | Return to "Start Page" | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Complete Pixel Read/Write action | Increment by 1 | No change | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| The Column counter value is large than "End Column" | Return to "Start Column" | Increment by 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| The Page counter value is large than "End Page" | Return to "Start Column" | Return to "Start Page" | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>There is no restriction on the length of parameters.</p> <p>No access to the frame memory in the Sleep In mode.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | Contents of memory is set randomly | SW Reset | Contents of memory is set randomly | HW Reset | Contents of memory is set randomly | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | Contents of memory is set randomly | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



5.2.37. Write Tear Scan Line (44h)

| TESLWR (Write Tear Scan Line) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|-----|----------|----------|----|----|----|----|----|----|----|-----|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| 44h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44h | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | N [15:8] | | | | | | | | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | N [7:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. Changing Memory Access Control (36h) D4 will not affect the TE signal. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>Note that set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0. The Tearing Effect Output line shall be active low when the ILI9488 is in the Sleep mode. X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | This command has no effect when the Tearing Effect output is already ON. | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>00h</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 00h | SW Reset | No change | HW Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No change | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <pre> graph TD A([TE Output ON or OFF]) --> B[TESLWR (44h)] B --> C{1st Parameter: N [15:8]} C --> D{2nd Parameter: N [7:0]} D --> E([TE Line Output ON]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.38. Read Scan Line (45h)

| 45h | | TESLRD (Read Tear Scan Line) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------------|-----|----------|----------|----|----|----|----|----|----|----|-----|--|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | N [15:8] | | | | | | | | | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | ↑ | 1 | XX | N [7:0] | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>The display reads the current scan line N, used to update the display device. The total number of scan lines on a display device is defined as: V_Low + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.</p> <p>When in the Sleep Mode, the value returned by Read Scan Line command is undefined.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | None | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 00h | SW Reset | No change | HW Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No change | | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | | | | | | | | | | | | | | |

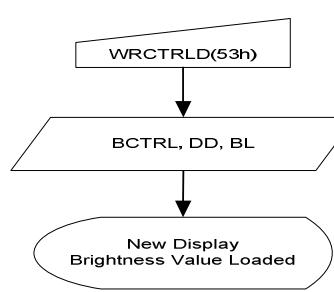
5.2.39. Write Display Brightness Value (51h)

| 51h | | WRDISBV (Write Display Brightness) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | DBV [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This command is used to adjust the brightness value of the display.</p> <p>DBV [7:0]: 8 bit, for display brightness of the manual brightness setting and the CABC in the ILI9488. PWM output signal and PWM_OUT pin control the LED driver IC in order to control the display brightness.</p> <p>In principle, 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD A[WRDISBV (51h)] --> B[DBV [7:0]] B --> C("New Display Brightness Value Loaded") </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command (triangular box) Parameter (trapezoid) Display (oval) Action (diamond) Mode (horizontal bar) Sequential transfer (oval with arrow) | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.40. Read Display Brightness Value (52h)

| 52h | | RDDISBV (Read Display Brightness Value) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|-----|-----|----------|-----------|----|----|----|----|----|----|----|-----|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52h | | | | | | | | | | | | |
| 1 st Parameter | | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | | 1 | ↑ | 1 | XX | DBV [7:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This command is used to return the brightness value of the display.</p> <p>DBV [7:0] is reset when the display is in the Sleep In mode.</p> <p>DBV [7:0] is 0 when the bit BCTRL of Write CTRL Display (53h) command is 0.</p> <p>DBV [7:0] is the manual set brightness specified by the Write CTRL Display (53h) command when the BCTRL bit is 1.</p> <p>When the bit BCTRL of Write CTRL Display (53h) command is 1 and C1/C0 bit of Write Content Adaptive Brightness Control (55h) command are 0, DBV [7:0] output is the brightness value specified by the Write Display Brightness (51h) command.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.41. Write CTRL Display Value (53h)

| 53h | WRCTRLD (Write Control Display) | | | | | | | | | | | | | | | | | | | | | | | | |
|--|---|-----|-----|----------|----|----|-------|----|----|----|----|----|-------|-------------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53h | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | XX | | | | | | | | | | | | |
| This command is used to control the display brightness. | | | | | | | | | | | | | | | | | | | | | | | | | |
| BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BCTRL</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Brightness Control Block OFF (DBV [7:0] = 00h)</td></tr> <tr> <td>1</td><td>Brightness Control Block ON (DBV [7:0] is active)</td></tr> </tbody> </table> | | | | | | | | | | | | | BCTRL | Description | 0 | Brightness Control Block OFF (DBV [7:0] = 00h) | 1 | Brightness Control Block ON (DBV [7:0] is active) | | | | | | | |
| BCTRL | Description | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Brightness Control Block OFF (DBV [7:0] = 00h) | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Brightness Control Block ON (DBV [7:0] is active) | | | | | | | | | | | | | | | | | | | | | | | | |
| DD: Display Dimming Control. This function is only for the manual brightness setting. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DD</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Display Dimming OFF</td></tr> <tr> <td>1</td><td>Display Dimming ON</td></tr> </tbody> </table> | | | | | | | | | | | | | DD | Description | 0 | Display Dimming OFF | 1 | Display Dimming ON | | | | | | | |
| DD | Description | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Display Dimming OFF | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Display Dimming ON | | | | | | | | | | | | | | | | | | | | | | | | |
| BL: Backlight Control On/Off <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BL</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Backlight Control OFF</td></tr> <tr> <td>1</td><td>Backlight Control ON</td></tr> </tbody> </table> | | | | | | | | | | | | | BL | Description | 0 | Backlight Control OFF | 1 | Backlight Control ON | | | | | | | |
| BL | Description | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Backlight Control OFF | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Backlight Control ON | | | | | | | | | | | | | | | | | | | | | | | | |
| Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD = 1, e.g. BCTRL: 0 -> 1 or 1-> 0. When the BL bit changes from On to Off, backlight is turned off without gradual dimming, even if dimming-on (DD = 1) are selected. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart |  <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.42. Read CTRL Display Value (54h)

| 54h | RDCTRLD (Read Control Display Value) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|-----|----------|----|----|-------|----|----|----|----|----|-----|--|--------|---------------|--|--|---|---|---|-------------|--|---------------------|----------|--------------------|----|-------------|---|-----------------------|---|----------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54h | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | XX | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used to control the display brightness.</p> <p>BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.</p> <table border="1"> <thead> <tr> <th>BCTRL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Brightness Control Block OFF (DBV [7:0] = 00h)</td> </tr> <tr> <td>1</td> <td>Brightness Control Block ON (DBV [7:0] is active)</td> </tr> </tbody> </table> <p>DD: Display Dimming Control. This function is only for the manual brightness setting.</p> <table border="1"> <thead> <tr> <th>DD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Display Dimming OFF</td> </tr> <tr> <td>1</td> <td>Display Dimming ON</td> </tr> </tbody> </table> <p>BL: Backlight Control On/Off</p> <table border="1"> <thead> <tr> <th>BL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Backlight Control OFF</td> </tr> <tr> <td>1</td> <td>Backlight Control ON</td> </tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | | BCTRL | Description | 0 | Brightness Control Block OFF (DBV [7:0] = 00h) | 1 | Brightness Control Block ON (DBV [7:0] is active) | DD | Description | 0 | Display Dimming OFF | 1 | Display Dimming ON | BL | Description | 0 | Backlight Control OFF | 1 | Backlight Control ON |
| BCTRL | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Brightness Control Block OFF (DBV [7:0] = 00h) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Brightness Control Block ON (DBV [7:0] is active) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DD | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Display Dimming OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Display Dimming ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BL | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Backlight Control OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Backlight Control ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD RDCTRLD[RDCTRLD(54h)] --> HostDriver[Host Driver] HostDriver --> Parameters[1st Parameter: Dummy Read 2nd Parameter: Control Display Value Read] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.43. Write Content Adaptive Brightness Control Value (55h)

| 55h | | WRCABC (Write Content Adaptive Brightness Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|--|-----|----------|---------|----|----|-------------|----------------------|-------|----|----|-----|--|---------|---------------|--|-----|---|-----------|---|-----|--|----------------|----------|-----|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|---|---|----------------------|---|---|---|---|---|---|---|---|---|---|---------------|---|---|---|---|---|---|---|---|---|---|--------------|---|---|---|---|---|---|---|---|---|---|-----------------|-------|---|---|---|---|---|---|---|---|---|--------------------|-------|---|---|---|---|---|---|---|---|---|------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | C [7:0] | | | | | | | | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command is used to set parameters of image content based on the adaptive brightness control functionality. The first 4 different modes are for content adaptive image functionality, which are defined in the table below. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="8">C [7:0]</th> <th>Description</th> <th>CE Ratio Range</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>OFF</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>User Interface Image</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Still Picture</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Moving Image</td><td>-</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Low enhancement</td><td>1.250</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Medium enhancement</td><td>1.750</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>High enhancement</td><td>2.250</td></tr> </tbody> </table> | | | | | | | | | | | | | | C [7:0] | | | | | | | | Description | CE Ratio Range | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | User Interface Image | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Still Picture | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Moving Image | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Low enhancement | 1.250 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Medium enhancement | 1.750 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | High enhancement |
| C [7:0] | | | | | | | | Description | CE Ratio Range | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | User Interface Image | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Still Picture | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Moving Image | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Low enhancement | 1.250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Medium enhancement | 1.750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | High enhancement | 2.250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>The flowchart illustrates the process of setting a new adaptive image mode. It begins with the command "WRCABC(55h)", which then points to the "1st Parameter: C [1:0]". This parameter selection leads to the final outcome, "New Adaptive Image Mode". To the right of the flowchart is a legend defining the symbols used:</p> <ul style="list-style-type: none"> Command (triangular box) Parameter (trapezoid) Display (oval) Action (parallelogram) Mode (diamond) Sequential transfer (oval with a curved arrow) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.44. Read Content Adaptive Brightness Control Value (56h)

| 56h | | RDCABC (Read Content Adaptive Brightness Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | C [7:0] | | | | | | | | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | This command is used to read the settings of image content based on the adaptive brightness control functionality. The first 4 different modes are for the content adaptive image functionality, which are defined in the table below. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="9">C [7:0]</th> <th>Description</th> <th>CE Ratio Range</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>OFF</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>User Interface Image</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Still Picture</td><td>-</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Moving Image</td><td>-</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Low enhancment</td><td>1.250</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Medium enhancement</td><td>1.750</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>High enhancement</td><td>2.250</td></tr> </tbody> </table> | | | | | | | | | | | | | | C [7:0] | | | | | | | | | Description | CE Ratio Range | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | User Interface Image | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Still Picture | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Moving Image | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Low enhancment | 1.250 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Medium enhancement | 1.750 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | High enhancement | 2.250 |
| C [7:0] | | | | | | | | | Description | CE Ratio Range | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | User Interface Image | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Still Picture | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Moving Image | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Low enhancment | 1.250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Medium enhancement | 1.750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | High enhancement | 2.250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD RDCABC[\"RDCABC (56h)\"] --> Host[\"Host\"] Host --> Driver[\"Driver\"] Driver --> Parameters[\"1st Parameter: Dummy Read\n2nd Parameter: CABC Value Read\"]</pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.45. Write CABC Minimum Brightness (5Eh)

| 5Eh | | WRCABCMB (Write CABC Minimum Brightness) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5Eh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | CMB [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This command is used to set the minimum brightness value of the display for the CABC function.</p> <p>CMB [7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.</p> <p>When the CABC is active, it cannot reduce the display brightness to less than the CABC minimum brightness setting. Image processing function works normally, even if the brightness cannot be changed.</p> <p>This manual brightness setting does not affect other functions. Manual brightness can set the display brightness to less than the CABC minimum brightness. Smooth transition and dimming function can work normally.</p> <p>When display brightness is turned off (BCTRL = 0 of Write CTRL Display (53h)), the CABC minimum brightness setting is ignored.</p> <p>In principle, 00h value means the lowest brightness for CABC, and FFh value means the highest brightness for CABC.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD A[WRCABCMB (5Eh)] --> B{1st Parameter: CMB [7:0]} B --> C([New Display Luminance Value Loaded]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command (triangular box) Parameter (rectangle) Display (oval) Action (diamond) Mode (trapezoid) Sequential transfer (elliptical arrow) | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.46. Read CABC Minimum Brightness (5Fh)

| 5Fh | | RDCABCMB (Read CABC Minimum Brightness) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---|-----|----------|-----------|----|----|----|----|----|----|----|-----|-----|--------|---------------|--|-----|---|-----------|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 5Fh | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | CMB [7:0] | | | | | | | | XX | | | | | | | | | | | | | |
| Description | This command reads the minimum brightness value of the CABC function. In principle, 00h value means the lowest brightness and FFh value means the highest brightness. CMB [7:0] is the CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value | Power ON Sequence | 00h | SW Reset | No Change | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power ON Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | No Change | | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>The flowchart illustrates the command sequence. It starts with a rectangular box labeled "RDCABCMB (5Fh)". An arrow points from this box down to a trapezoidal box labeled "1st Parameter: Dummy Read" and "2nd Parameter: CABC minimum Brightness Read". Above this trapezoid is the word "Host", and below it is the word "Driver". To the right of the trapezoid is a legend box titled "Legend". Inside the legend box are six items: "Command" (represented by a rectangle), "Parameter" (represented by a rectangle), "Display" (represented by an oval), "Action" (represented by a diamond), "Mode" (represented by an oval), and "Sequential transfer" (represented by an oval).</p> | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.47. Read Automatic Brightness Control Self-diagnostic Result (68h)

| 68h | RDABCSDR (Read automatic brightness control self-diagnostic result) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|--|-----|----------|---------|----|----|----|----|----|----|----|-----|--------|---------------|--|-----|---|--|---|-------------------------|---|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68h | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | D [7:6] | | 0 | 0 | 0 | 0 | 0 | 0 | XX | | | | | | | | | | | | |
| Description | This command indicates the status of the display self-diagnostic results for automatic brightness control after the Sleep Out command, as described in the table below. | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Action</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Register Loading Detection</td><td>Invert the D7 bit if register values loading work properly</td></tr> <tr> <td>D6</td><td>Functionality Detection</td><td>Invert the D6 bit if the display is working</td></tr> </tbody> </table> | | | | | | | | | | | | | Bit | Description | Action | D7 | Register Loading Detection | Invert the D7 bit if register values loading work properly | D6 | Functionality Detection | Invert the D6 bit if the display is working | | | |
| Bit | Description | Action | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | Register Loading Detection | Invert the D7 bit if register values loading work properly | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | Functionality Detection | Invert the D6 bit if the display is working | | | | | | | | | | | | | | | | | | | | | | | |
| | Bit D7 – Register Loading Detection, see the section “Register loading Detection”. Bit D6 – Functionality Detection, see the section “Functionality Detection”. Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to 0. X = void | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value | Power On Sequence | 00h | S/W Reset | 00h | H/W Reset | 00h | | | | |
| Status | Default Value | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| S/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| H/W Reset | 00h | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>The flowchart illustrates the communication sequence. It begins with a rectangular box labeled "Read RDABCSDR (68h)" above a dashed line, representing the "Host" side. An arrow points down to a trapezoidal box labeled "1st Parameter: Dummy Read Send the 2nd Parameter" below the dashed line, representing the "Driver" side. To the right of the dashed line is a legend box titled "Legend" containing six items: "Command" (arrow pointing right), "Parameter" (arrow pointing down), "Display" (arrow pointing left), "Action" (arrow pointing up), "Mode" (horizontal arrow), and "Sequential transfer" (oval).</p> | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.48. Read ID1 (DAh)

| DAh | RDID1 (Read ID1) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|----|--------|---------------------------------------|--|-------------------|---|-----------|---|-----|--|----------|----------|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | | XX | | | | | | | | | | | | |
| Description | This read byte identifies the LCD module's manufacturer ID and it is specified by users. The 1 st parameter is a dummy data. The 2 nd parameter is the LCD module's manufacturer ID. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | The ILI9488 sends the 2 nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>54h</td><td>OTP value</td></tr> <tr> <td>SW Reset</td><td>54h</td><td>OTP value</td></tr> <tr> <td>HW Reset</td><td>54h</td><td>OTP value</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value (Before OTP program) | Default Value (After OTP program) | Power On Sequence | 54h | OTP value | SW Reset | 54h | OTP value | HW Reset | 54h | OTP value |
| Status | Default Value (Before OTP program) | Default Value (After OTP program) | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 54h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 54h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 54h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD RDID1[RDID1 (DAh)] --> HostDriver[Host Driver] HostDriver --> 1stParameter[1st Parameter: Dummy Read] 1stParameter --> 2ndParameter[2nd Parameter: Send ID1 [7:0]] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.49. Read ID2 (DBh)

| DBh | RDID2 (Read ID2) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|-----|--------|---------------------------------------|--|-------------------|---|-----------|---|-----|--|----------|----------|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | DBh | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | ID2 [7:0] | | | | | | | | XX | | | | | | | | | | | | | |
| Description | <p>This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter is the LCD module/driver version ID, and the ID parameter range is from 80h to FFh.</p> <p>The ID2 can be programmed by the OTP function.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>80h</td><td>OTP value</td></tr> <tr> <td>SW Reset</td><td>80h</td><td>OTP value</td></tr> <tr> <td>HW Reset</td><td>80h</td><td>OTP value</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Default Value (Before OTP program) | Default Value (After OTP program) | Power On Sequence | 80h | OTP value | SW Reset | 80h | OTP value | HW Reset | 80h | OTP value |
| Status | Default Value (Before OTP program) | Default Value (After OTP program) | | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 80h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 80h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 80h | OTP value | | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <pre> graph TD RDID2[RDID2 (DBh)] --> HostDriver[Host Driver] HostDriver --> 1stParameter[1st Parameter: Dummy Read] 1stParameter --> 2ndParameter[2nd Parameter: Send ID2 [7:0]] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer | | | | | | | | | | | | | | | | | | | | | | | | | |

5.2.50. Read ID3 (DCh)

| DCh | RDID3 (Read ID3) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------------------------------|-----|----------|-----------|----|----|----|----|----|----|----|-----|--------|---------------------------------------|--|-------------------|---|-----------|---|-----|--|----------|----------|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCh | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | XX | | | | | | | | | | | | |
| Description | <p>This read byte identifies the LCD module/driver, and It is specified by users.</p> <p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter is the LCD module/driver ID.</p> <p>The ID3 can be programmed by the OTP function.</p> <p>X = Void.</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | <p>The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p> | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes | Normal Mode On, Idle Mode On, Sleep Out | Yes | Partial Mode On, Idle Mode Off, Sleep Out | Yes | Partial Mode On, Idle Mode On, Sleep Out | Yes | Sleep In | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep In | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | <table border="1"> <thead> <tr> <th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>66h</td><td>OTP value</td></tr> <tr> <td>SW Reset</td><td>66h</td><td>OTP value</td></tr> <tr> <td>HW Reset</td><td>66h</td><td>OTP value</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Default Value (Before OTP program) | Default Value (After OTP program) | Power On Sequence | 66h | OTP value | SW Reset | 66h | OTP value | HW Reset | 66h | OTP value |
| Status | Default Value (Before OTP program) | Default Value (After OTP program) | | | | | | | | | | | | | | | | | | | | | | | |
| Power On Sequence | 66h | OTP value | | | | | | | | | | | | | | | | | | | | | | | |
| SW Reset | 66h | OTP value | | | | | | | | | | | | | | | | | | | | | | | |
| HW Reset | 66h | OTP value | | | | | | | | | | | | | | | | | | | | | | | |
| Flow Chart | <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <pre> graph TD RDID3[DCh] --> HostDriver[Host Driver] HostDriver --> 1stParam[1st Parameter: Dummy Read] 1stParam --> 2ndParam[2nd Parameter: Send ID3 [7:0]] </pre> | | | | | | | | | | | | | | | | | | | | | | | | |

5.3. Extend Command (EXTC) Description

5.3.1. Interface Mode Control (B0h)

| IFMODE (Interface Mode Control) | | | | | | | | | | | | | |
|---------------------------------|--|-----|-----|----------|--------|----|----|----|------|------|-----|-----|-----|
| B0h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h |
| 1 st Parameter | 1 | 1 | ↑ | XX | SDA_EN | 0 | 0 | 0 | VSPL | HSPL | DPL | EPL | 00h |
| Description | Set the operation status of the display interface. The setting becomes effective as soon as the command is received. EPL: ENABLE polarity (0 = High enable for RGB interface, 1 = Low enable for RGB interface) DPL: DOTCLK polarity set (0 = data fetched at the rising time, 1 = data fetched at the falling time) HSPL: HSYNC polarity (0 = Low level sync clock, 1 = High level sync clock) VSPL: VSYNC polarity (0 = Low level sync clock, 1 = High level sync clock) SDA_EN: 3/4 wire serial interface selection SDA_EN = 0, DIN and SDO pins are used for 3/4 wire serial interface. SDA_EN = 1, DIN/SDA pin is used for 3/4 wire serial interface and SDO pin is not used. X = void | | | | | | | | | | | | |

| Restriction | | | | | | | | | | | | | |
|---|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

5.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

| B1h | FRMCTR1 (Frame Rate Control (In Normal Mode/Full colors)) | | | | | | | | | | | | | | | | | | | | | | |
|--|--|-----|-----|------------|--|----|----|------------|--|----|------------|-----|-----|------------|----------------|-----|------|-----|--------|-----|--------|-----|---------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1h | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | FRS [3:0] | | | | 0 | 0 | DIVA [1:0] | | B0h | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNA [4:0] | | | | 11h | | | | | | | | | | | |
| Description | DIVA [1:0]: division ratio for internal clocks when Normal mode. <table border="1"> <thead> <tr> <th>DIVA [1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>Fosc</td> </tr> <tr> <td>0 1</td> <td>Fosc/2</td> </tr> <tr> <td>1 0</td> <td>Fosc/4</td> </tr> <tr> <td>1 1</td> <td>Ffosc/8</td> </tr> </tbody> </table> FRS [3:0]: Set the frame frequency of full color normal mode. Set the division ratio for internal clocks of the Normal Display Mode On | | | | | | | | | | | | | DIVA [1:0] | Division Ratio | 0 0 | Fosc | 0 1 | Fosc/2 | 1 0 | Fosc/4 | 1 1 | Ffosc/8 |
| DIVA [1:0] | Division Ratio | | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | Fosc | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | Fosc/2 | | | | | | | | | | | | | | | | | | | | | | |
| 1 0 | Fosc/4 | | | | | | | | | | | | | | | | | | | | | | |
| 1 1 | Ffosc/8 | | | | | | | | | | | | | | | | | | | | | | |
| $\text{Frame Rate} = \frac{\text{Fosc}}{\text{DIVA} \times ((\text{CNT}+1) \times 2) \times \text{RTNA} \times (\text{Display Line}+\text{VBP}+\text{VFP})}$ | | | | | | | | | | | | | | | | | | | | | | | |
| Fosc: Internal oscillator frequency | | | | | | | | | | | | | | | | | | | | | | | |
| CNT: Frame rate setting | | | | | | | | | | | | | | | | | | | | | | | |
| DIVA: Division Ratio | | | | | | | | | | | | | | | | | | | | | | | |
| RTNA: Clocks per line | | | | | | | | | | | | | | | | | | | | | | | |
| Display Line: Total driving line number | | | | | | | | | | | | | | | | | | | | | | | |
| VBP: Back porch line number | | | | | | | | | | | | | | | | | | | | | | | |
| VFP: Front porch line number | | | | | | | | | | | | | | | | | | | | | | | |
| FRS [3:0] | | | | CNT | Frame rate(Hz) Tearing Effect Line OFF(R34h) | | | | Frame rate(Hz) Tearing Effect Line ON(R35h) VBP+VFP <24 | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 37 | 28.78 | | | | 27.64 | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 35 | 30.38 | | | | 29.17 | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 33 | 32.17 | | | | 30.89 | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 31 | 34.18 | | | | 32.82 | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 29 | 36.46 | | | | 35.01 | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 27 | 39.06 | | | | 37.51 | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 25 | 42.07 | | | | 40.40 | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 23 | 45.57 | | | | 43.76 | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 21 | 49.71 | | | | 47.74 | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 19 | 54.69 | | | | 52.52 | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 17 | 60.76 | | | | 58.35 | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 15 | 68.36 | | | | 65.65 | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 13 | 78.13 | | | | 75.03 | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 11 | 91.15 | | | | 87.53 | | | | | | | | | | | | | | |

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Case 1 Tearing Effect Line OFF(R34h)

Example1: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=2 lines.

Following the formula, the frame rate = 60.76Hz.

Case 2 Tearing Effect Line ON(R35h)

(1) Example1: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=2 lines.

If VBP+VFP less than 24, the VBP+VFP will be set to 24. The frame rate = 58.35Hz

(2) Example2: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=14 lines.

VBP+VFP greater than 24, the original setting is kept. The frame rate = 57.89Hz.

RTNA [4:0]: RTNA [4:0] is used to set 1H (line) period of the Normal mode at the MCU interface.

| RTNA [4:0] | | | | | Clock per Line |
|------------|---|---|---|---|--------------------|
| 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | Setting prohibited |
| 0 | 0 | 0 | 1 | 0 | Setting prohibited |
| 0 | 0 | 0 | 1 | 1 | Setting prohibited |
| 0 | 0 | 1 | 0 | 0 | Setting prohibited |
| 0 | 0 | 1 | 0 | 1 | Setting prohibited |
| 0 | 0 | 1 | 1 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 1 | Setting prohibited |
| 0 | 1 | 0 | 1 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 1 | Setting prohibited |
| 0 | 1 | 0 | 1 | 1 | Setting prohibited |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited |
| 1 | 0 | 0 | 0 | 0 | 16 clocks |
| 1 | 0 | 0 | 0 | 1 | 17 clocks |
| 1 | 0 | 0 | 1 | 0 | 18 clocks |
| 1 | 0 | 0 | 1 | 1 | 19 clocks |
| 1 | 0 | 1 | 0 | 0 | 20 clocks |
| 1 | 0 | 1 | 0 | 1 | 21 clocks |

| RTNA [4:0] | | | | | Clock per Line |
|------------|---|---|---|---|--------------------|
| 0 | 1 | 0 | 1 | 1 | Setting prohibited |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited |
| 1 | 0 | 0 | 0 | 0 | 16 clocks |
| 1 | 0 | 0 | 0 | 1 | 17 clocks |
| 1 | 0 | 0 | 1 | 0 | 18 clocks |
| 1 | 0 | 0 | 1 | 1 | 19 clocks |
| 1 | 0 | 1 | 0 | 0 | 20 clocks |
| 1 | 0 | 1 | 0 | 1 | 21 clocks |

| RTNA [4:0] | | | | | Clock per Line |
|------------|---|---|---|---|----------------|
| 1 | 0 | 1 | 1 | 0 | 22 clocks |
| 1 | 0 | 1 | 1 | 1 | 23 clocks |
| 1 | 1 | 0 | 0 | 0 | 24 clocks |
| 1 | 1 | 0 | 0 | 1 | 25 clocks |
| 1 | 1 | 0 | 1 | 0 | 26 clocks |
| 1 | 1 | 0 | 1 | 1 | 27 clocks |
| 1 | 1 | 1 | 0 | 0 | 28 clocks |
| 1 | 1 | 1 | 0 | 1 | 29 clocks |
| 1 | 1 | 1 | 1 | 0 | 30 clocks |
| 1 | 1 | 1 | 1 | 1 | 31 clocks |

X = void

Restriction

| Status | Availability |
|---|--------------|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Register Availability

5.3.3. Frame Rate Control (In Idle Mode/8 Colors) (B2h)

| B2h | FRMCTR2 (Frame Rate Control (In Idle Mode/8 colors)) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------|--------------|--|--------------------|---|-----|---|-----|--|----------------|----------|-----|------------|----------------|-----|--------------------|-----|--------|-----|--------|-----|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|--|--|--|--|--|------------|--|--|--|--|----------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|----------------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVB [1:0] | | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 11h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | Set the division ratio for internal clocks of the Idle Mode ON. DIVB [1:0]: division ratio for internal clocks when in the Idle mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>DIVB [1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>fosc</td> </tr> <tr> <td>0 1</td> <td>fosc/2</td> </tr> <tr> <td>1 0</td> <td>fosc/4</td> </tr> <tr> <td>1 1</td> <td>fosc/8</td> </tr> </tbody> </table> | | | | | | | | | | | | | DIVB [1:0] | Division Ratio | 0 0 | fosc | 0 1 | fosc/2 | 1 0 | fosc/4 | 1 1 | fosc/8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIVB [1:0] | Division Ratio | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | fosc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | fosc/2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 0 | fosc/4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 1 | fosc/8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RTNB [4:0]: RTNB [4:0] is used to set 1H (line) period of the Idle Mode ON. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| RTNB [4:0] | | | | | Clock per Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 0 | 1 | 1 | 0 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RTNB [4:0] | | | | | Clock per Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 16 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 1 | 17 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 18 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 1 | 19 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 20 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 21 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RTNB [4:0] | | | | | Clock per Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 0 | 22 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 1 | 23 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 24 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 1 | 25 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 0 | 26 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 1 | 27 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 28 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 1 | 29 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 30 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 31 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.4. Frame Rate Control (In Partial Mode/Full Colors) (B3h)

| B3h | FRMCTR3 (Frame Rate Control (In Partial Mode/Full colors)) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|--------------------|----|----|----|----|----|------------|-----|-----|------------|--------------|--|-----|---|----------------|---|-----|--|-----|----------|--------------------|---|---|---|---|----------------|--------------------|---|---|---|---|--------------------|--------------------|---|---|---|---|--------------------|--------------------|---|---|---|---|--------------------|--------------------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|-----------|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|--------------------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|---|---|---|---|---|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVC [1:0] | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | RTNC [4:0] | | 11h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Set the division ratio for internal clocks of the Partial mode ON (Idle mode off). DIVC [1:0]: division ratio for internal clocks when in the Partial mode. <table border="1"> <thead> <tr> <th>DIVC [1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>fosc</td> </tr> <tr> <td>0 1</td> <td>fosc/2</td> </tr> <tr> <td>1 0</td> <td>fosc/4</td> </tr> <tr> <td>1 1</td> <td>fosc/8</td> </tr> </tbody> </table> RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of the Partial mode ON. <table border="1"> <thead> <tr> <th colspan="5">RTNC [4:0]</th> <th>Clock per Line</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>0</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td> <td>16 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>1</td> <td>17 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td> <td>18 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>1</td> <td>19 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>0</td> <td>20 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td> <td>21 clocks</td> </tr> </tbody> </table> X = void | | | | | | | | | | | | | | DIVC [1:0] | Division Ratio | 0 0 | fosc | 0 1 | fosc/2 | 1 0 | fosc/4 | 1 1 | fosc/8 | RTNC [4:0] | | | | | Clock per Line | 0 | 0 | 0 | 0 | 0 | Setting prohibited | 0 | 0 | 0 | 0 | 1 | Setting prohibited | 0 | 0 | 0 | 1 | 0 | Setting prohibited | 0 | 0 | 0 | 1 | 1 | Setting prohibited | 0 | 0 | 1 | 0 | 0 | Setting prohibited | 0 | 0 | 1 | 0 | 1 | Setting prohibited | 0 | 0 | 1 | 1 | 0 | Setting prohibited | 0 | 0 | 1 | 1 | 1 | Setting prohibited | 0 | 1 | 0 | 0 | 0 | Setting prohibited | 0 | 1 | 0 | 0 | 1 | Setting prohibited | 0 | 1 | 0 | 1 | 0 | Setting prohibited | 0 | 1 | 0 | 1 | 1 | Setting prohibited | 0 | 1 | 1 | 0 | 0 | Setting prohibited | 0 | 1 | 1 | 0 | 1 | Setting prohibited | 0 | 1 | 1 | 1 | 0 | Setting prohibited | 0 | 1 | 1 | 1 | 1 | Setting prohibited | 1 | 0 | 0 | 0 | 0 | 16 clocks | 1 | 0 | 0 | 0 | 1 | 17 clocks | 1 | 0 | 0 | 1 | 0 | 18 clocks | 1 | 0 | 0 | 1 | 1 | 19 clocks | 1 | 0 | 1 | 0 | 0 | 20 clocks | 1 | 0 | 1 | 0 | 1 | 21 clocks |
| DIVC [1:0] | Division Ratio | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 0 1 | fosc/2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 0 | fosc/4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 1 | fosc/8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RTNC [4:0] | | | | | Clock per Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 0 | 0 | 1 | 0 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 1 | 0 | 0 | 0 | 0 | 16 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 1 | 17 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 18 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 1 | 19 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 20 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 21 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <table border="1"> <thead> <tr> <th colspan="5">RTNC [4:0]</th> <th>Clock per Line</th> </tr> </thead> <tbody> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>0</td> <td>Setting prohibited</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>1</td> <td>Setting prohibited</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td> <td>16 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>1</td> <td>17 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td> <td>18 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>1</td> <td>19 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>0</td> <td>20 clocks</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td> <td>21 clocks</td> </tr> </tbody> </table> | | | | | | | | | | | | | RTNC [4:0] | | | | | Clock per Line | 0 | 1 | 0 | 1 | 1 | Setting prohibited | 0 | 1 | 1 | 0 | 0 | Setting prohibited | 0 | 1 | 1 | 0 | 1 | Setting prohibited | 0 | 1 | 1 | 1 | 0 | Setting prohibited | 0 | 1 | 1 | 1 | 1 | Setting prohibited | 1 | 0 | 0 | 0 | 0 | 16 clocks | 1 | 0 | 0 | 0 | 1 | 17 clocks | 1 | 0 | 0 | 1 | 0 | 18 clocks | 1 | 0 | 0 | 1 | 1 | 19 clocks | 1 | 0 | 1 | 0 | 0 | 20 clocks | 1 | 0 | 1 | 0 | 1 | 21 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RTNC [4:0] | | | | | Clock per Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 16 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 1 | 17 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 18 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 1 | 19 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 20 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 21 clocks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.5. Display Inversion Control (B4h)

| B4h | INVTR (Display Inversion Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|--------------------|----------|----|-----------|----|----|--------|------------|----|----|-----|------------|--------------|--|-----------|---|-----|---|------------------|--|-----|----------|-----------------|---|---|---|-----------------|-------|--|--|--------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4h | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | DINV [2:0] | | | 02h | | | | | | | | | | | | | | | | | | | | |
| DINV: set the Display Inversion mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <table border="1"> <thead> <tr> <th colspan="3">DINV [2:0]</th> <th>Inversion</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>Column inversion</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>1 dot inversion</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>2 dot inversion</td> </tr> <tr> <td colspan="3">other</td><td>Setting prohibited</td> </tr> </tbody> </table> | | | | | | | | | | | | | DINV [2:0] | | | Inversion | 0 | 0 | 0 | Column inversion | 0 | 0 | 1 | 1 dot inversion | 0 | 1 | 0 | 2 dot inversion | other | | | Setting prohibited |
| DINV [2:0] | | | Inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | Column inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 dot inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 dot inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| other | | | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Column Inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1st frame | | | | | | 2nd frame | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 line | + | - | + | - | + | - | + | - | 1 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 2 line | + | - | + | - | + | - | + | - | 2 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 3 line | + | - | + | - | + | - | + | - | 3 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 4 line | + | - | + | - | + | - | + | - | 4 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 1-Dot Inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1st frame | | | | | | 2nd frame | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 line | + | - | + | - | + | - | + | - | 1 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 2 line | - | + | - | + | - | + | - | + | 2 line | + | - | + | | | | | | | | | | | | | | | | | | | | | |
| 3 line | + | - | + | - | + | - | + | - | 3 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 4 line | - | + | - | + | - | + | - | + | 4 line | + | - | + | | | | | | | | | | | | | | | | | | | | | |
| 2-Dot Inversion | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1st frame | | | | | | 2nd frame | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 line | + | - | + | - | + | - | + | - | 1 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 2 line | + | - | + | - | + | - | + | - | 2 line | - | + | - | | | | | | | | | | | | | | | | | | | | | |
| 3 line | - | + | - | + | - | + | - | + | 3 line | + | - | + | | | | | | | | | | | | | | | | | | | | | |
| 4 line | - | + | - | + | - | + | - | + | 4 line | + | - | + | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td> </tr> <tr> <td>Sleep IN</td><td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.6. Blanking Porch Control (B5h)

| B5h | PRCTR (Blanking Porch) | | | | | | | | | | | | | |
|---------------------------|------------------------|-----|-----|----------|----|----|----|----|----|----|----|----|-----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5h | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | VFP [4:0] | 02h |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | VBP [4:0] | 02h |
| 3 rd Parameter | 1 | 1 | ↑ | XX | | | | | | | | | HFP [7:0] | 0Ah |
| 4 th Parameter | 1 | 1 | ↑ | XX | | | | | | | | | HBP [7:0] | 04h |

VFP [4:0]/VBP [4:0]: The VFP [4:0] and VBP [4:0] bits specify the line number of vertical front and back porch period respectively.

| VFP [4:0] | Number of lines of front porch |
|-----------|--------------------------------|
| 00000 | Setting prohibited |
| 00001 | Setting prohibited |
| 00010 | 2 |
| 00011 | 3 |
| : | : |
| 11100 | 28 |
| 11101 | 29 |
| 11110 | 30 |
| 11111 | 31 |

| VBP [4:0] | Number of lines of back porch |
|-----------|-------------------------------|
| 00000 | Setting prohibited |
| 00001 | Setting prohibited |
| 00010 | 2 |
| 00011 | 3 |
| : | : |
| 11100 | 28 |
| 11101 | 29 |
| 11110 | 30 |
| 11111 | 31 |

Notes:

1. VBP + VFP ≤ 32
2. Recommendation: The porch number of VBP + VFP must be even.

Description

HFP [7:0]: The HFP [7:0] bits specify the dotclk number of horizontal front porch period.

| HFP [7:0] | Number of dotclk of front porch |
|-----------|---------------------------------|
| 00000000 | Setting prohibited |
| 00000001 | Setting prohibited |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111100 | 252 |
| 11111101 | 253 |
| 11111110 | 254 |
| 11111111 | 255 |

HBP [7:0]: The HBP [7:0] bits specify the dotclk number of horizontal back porch period.

| HBP [7:0] | Number of dotclk of back porch |
|------------------|---------------------------------------|
| 00000000 | Setting prohibited |
| 00000001 | Setting prohibited |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111100 | 252 |
| 11111101 | 253 |
| 11111110 | 254 |
| 11111111 | 255 |

X = void

| Restriction | | | | | | | | | | | | | |
|---|--|---------------|---------------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

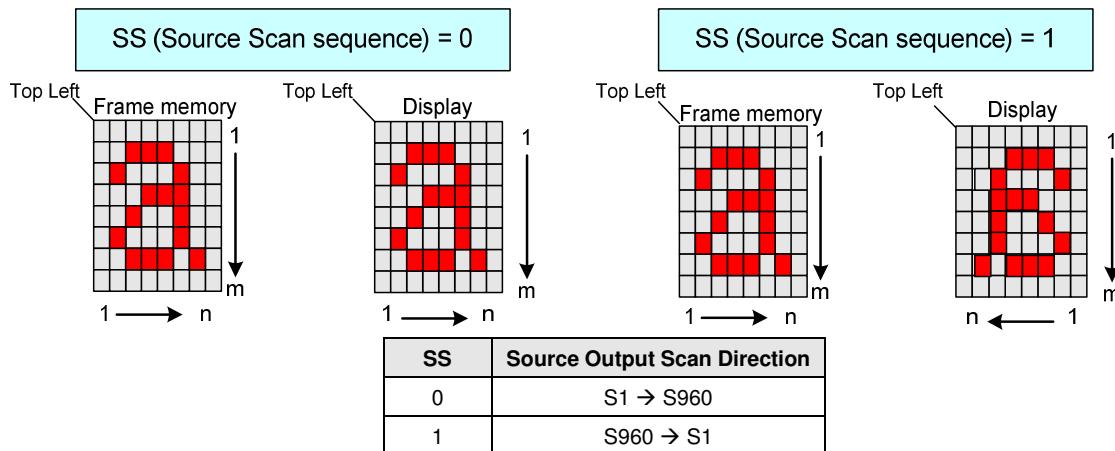
5.3.7. Display Function Control (B6h)

| B6h | DISCTRL (Display Function Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|------------------------------------|--------------------------------------|--|--|-----|----|----|-----------|-----------|----|----|--------|--------------------------|----------------|------------------------------------|--------------------------------------|--------------------------|-----------------------|-------------|----------------------------|---|---|--------------------|-----|---|---|---------------|----------------------------|---|---|--------------------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6h | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | BYPASS | RCM | RM | DM | PTG [1:0] | PT [1:0] | | | 02h | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | GS | SS | SM | ISC [3:0] | ISC [3:0] | | | 02h | | | | | | | | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | NL [5:0] | NL [5:0] | | | 3Bh | | | | | | | | | | | | | | | | | | | | |
| Description | DM: Select the display operation mode. | | | | <table border="1"> <thead> <tr> <th>DM</th> <th>Interface Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Internal system clock</td> </tr> <tr> <td>1</td> <td>RGB interface(DOTCLK)</td> </tr> </tbody> </table> | | | | | | | | | DM | Interface Mode | 0 | Internal system clock | 1 | RGB interface(DOTCLK) | | | | | | | | | | | | | | |
| DM | Interface Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Internal system clock | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | RGB interface(DOTCLK) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RM: Select the interface to access the GRAM. When RM = 0, the driver will write display data to the GRAM via the system interface, and the driver will write display data to the GRAM via the RGB interface when RM = 1. | | | | <table border="1"> <thead> <tr> <th>RM</th> <th>Interface for RAM access</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>System interface</td> </tr> <tr> <td>1</td> <td>RGB interface</td> </tr> </tbody> </table> | | | | | | | | | RM | Interface for RAM access | 0 | System interface | 1 | RGB interface | | | | | | | | | | | | | | | |
| RM | Interface for RAM access | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | System interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | RGB interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RCM: RGB interface selection (refer to the RGB interface section). | | | | <table border="1"> <thead> <tr> <th>RCM</th> <th>RGB transfer mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DE Mode</td> </tr> <tr> <td>1</td> <td>SYNC Mode</td> </tr> </tbody> </table> | | | | | | | | | RCM | RGB transfer mode | 0 | DE Mode | 1 | SYNC Mode | | | | | | | | | | | | | | | |
| RCM | RGB transfer mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | DE Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | SYNC Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BYPASS: Select the display data path (memory or direct to shift register) when the RGB interface is used. | | | | <table border="1"> <thead> <tr> <th>BYPASS</th> <th>Display data path</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Memory</td> </tr> <tr> <td>1</td> <td>Direct to shift register</td> </tr> </tbody> </table> | | | | | | | | | BYPASS | Display data path | 0 | Memory | 1 | Direct to shift register | | | | | | | | | | | | | | | |
| BYPASS | Display data path | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Memory | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Direct to shift register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Note: The RGB input signal, when set to the BYPASS mode, the Hsync low \geq 3, HBP \geq 3, HFP \geq 10. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PTG [1:0]: Set the scan mode in a non-display area. | | | | <table border="1"> <thead> <tr> <th>PTG1</th> <th>PTG0</th> <th>Gate outputs in a non-display area</th> <th>Source outputs in a non-display area</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal scan</td> <td>Set with the PT [2:0] bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>Setting prohibited</td> <td>---</td> </tr> <tr> <td>1</td> <td>0</td> <td>Interval scan</td> <td>Set with the PT [2:0] bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting prohibited</td> <td>---</td> </tr> </tbody> </table> | | | | | | | | | | PTG1 | PTG0 | Gate outputs in a non-display area | Source outputs in a non-display area | 0 | 0 | Normal scan | Set with the PT [2:0] bits | 0 | 1 | Setting prohibited | --- | 1 | 0 | Interval scan | Set with the PT [2:0] bits | 1 | 1 | Setting prohibited | --- |
| PTG1 | PTG0 | Gate outputs in a non-display area | Source outputs in a non-display area | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Normal scan | Set with the PT [2:0] bits | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Setting prohibited | --- | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Interval scan | Set with the PT [2:0] bits | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Setting prohibited | --- | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

| PT [1:0] | | Source output in a non-display area |
|----------|---|-------------------------------------|
| 0 | 0 | V63 |
| 0 | 1 | V0 |
| 1 | 0 | AGND |
| 1 | 1 | Hi-Z |

SS: Select the shift direction of outputs from the source driver.



In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

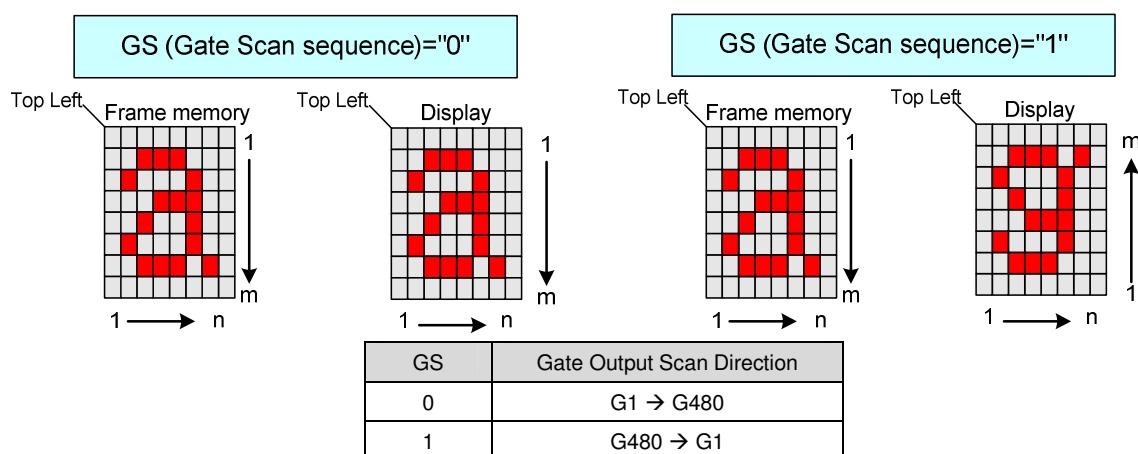
To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

ISC [3:0]: Set the scan cycle when the PTG selects interval scan in a non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

| ISC [3:0] | Scan cycle | (f _{FRAME})=60Hz |
|-----------|-------------------|----------------------------|
| 4'h0 | Setting inhibited | - |
| 4'h1 | 3 frames | 50ms |
| 4'h2 | 5 frames | 84ms |
| 4'h3 | 7 frames | 117ms |
| 4'h4 | 9 frames | 150ms |
| 4'h5 | 11 frames | 184ms |
| 4'h6 | 13 frames | 217ms |
| 4'h7 | 15 frames | 251ms |
| 4'h8 | 17 frames | 284ms |
| 4'h9 | 19 frames | 317ms |
| 4'hA | 21 frames | 351ms |
| 4'hB | 23 frames | 384ms |
| 4'hC | 25 frames | 418ms |
| 4'hD | 27 frames | 451ms |
| 4'hE | 29 frames | 484ms |
| 4'hF | 31 frames | 518ms |

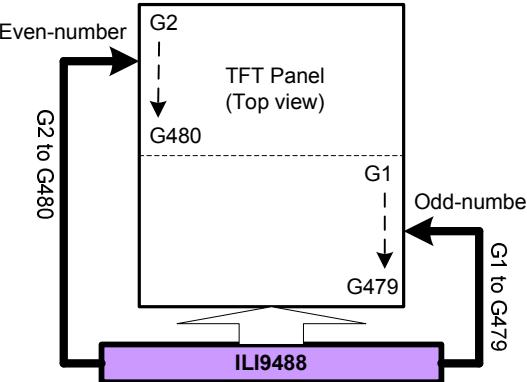
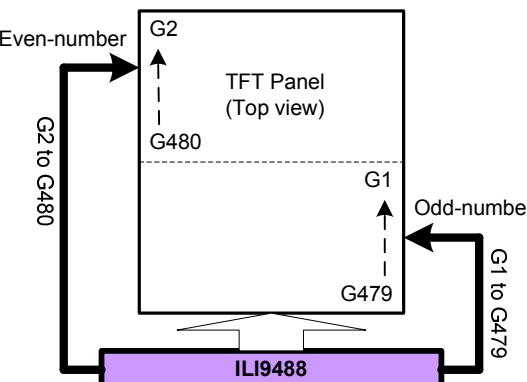
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GS: Set the direction of scan by the gate driver.

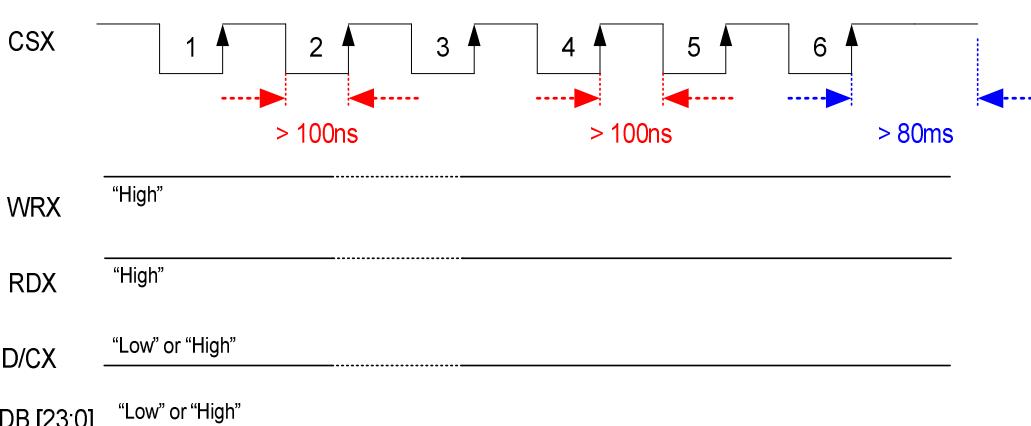


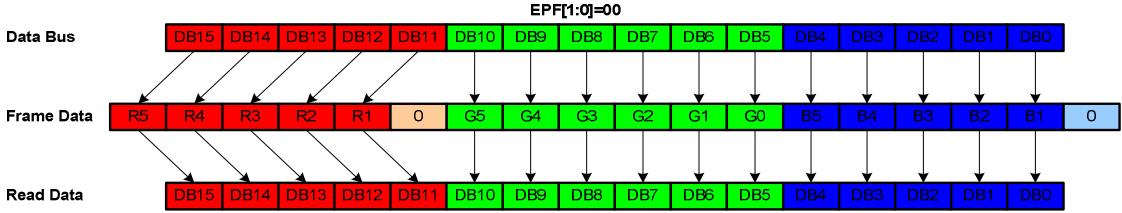
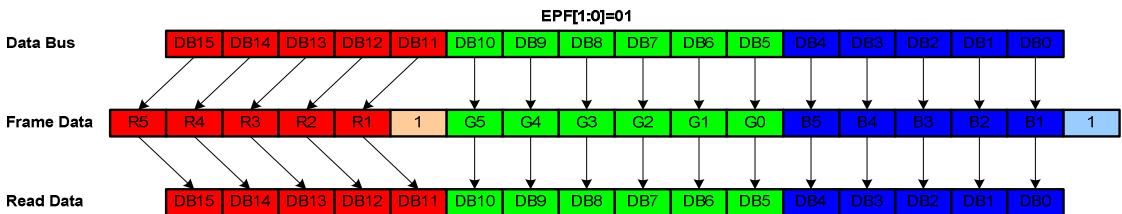
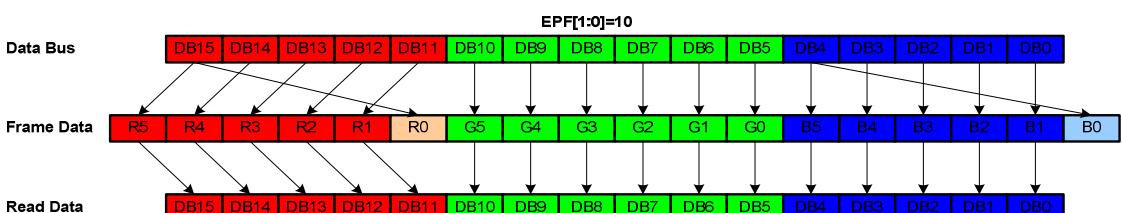
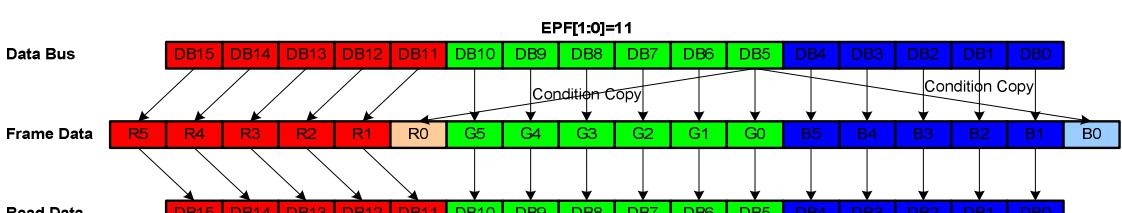
SM: Set the gate driver pin arrangement in combination with the GS bit (RB6h) to select the optimal scan mode for the module.

| SM | GS | Scan Direction | Gate Output Sequence |
|----|----|---|--|
| 0 | 0 | TFT Panel (Top view) G2, G4, G1, G3 G478, G480, G477, G479 | G1 → G2 → G3 → G4 → G477 → G478 → G479 → G480 |
| 0 | 1 | TFT Panel (Top view) G2, G4, G1, G3 G478, G480, G477, G479 | G480 → G479 → G478 → G477 → → G4 → G3 → G2 → G1 |

| 1 | 0 |  <p>Even-number G2 to G480</p> <p>G2 TFT Panel (Top view) G480 G1 G479 Odd-number G1 to G479</p> <p>ILI9488</p> | <p>G1→G3→.....→G477→G479→ G2→G4→.....→G478→G480</p> | | | | | | | | | | | | |
|---|------------------------|--|---|----------------|--|------------------------|---|-------------------|---|-----|--|-----|----------|-----|--|
| 1 | 1 |  <p>Even-number G2 to G480</p> <p>G2 TFT Panel (Top view) G480 G1 G479 Odd-number G1 to G479</p> <p>ILI9488</p> | <p>G480→G478→.....→G4→G2→ G479→G477→.....→G3→G1</p> | | | | | | | | | | | | |
| | | <p>NL [5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same as or more than the number of lines necessary for the size of the liquid crystal panel.</p> <table border="1"> <thead> <tr> <th>NL [5:0]</th> <th>LCD Drive Line</th> </tr> </thead> <tbody> <tr> <td>6'h00 ~ 6'h3B</td> <td>8 * (NL [5:0]+1) lines</td> </tr> <tr> <td>Others</td> <td>Setting inhibited</td> </tr> </tbody> </table> | NL [5:0] | LCD Drive Line | 6'h00 ~ 6'h3B | 8 * (NL [5:0]+1) lines | Others | Setting inhibited | | | | | | | |
| NL [5:0] | LCD Drive Line | | | | | | | | | | | | | | |
| 6'h00 ~ 6'h3B | 8 * (NL [5:0]+1) lines | | | | | | | | | | | | | | |
| Others | Setting inhibited | | | | | | | | | | | | | | |
| | | X = void | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | |
| Register Availability | | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | |
| Status | Availability | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | |

5.3.8. Entry Mode Set (B7h)

| B7h | ETMOD (Entry Mode Set) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|--|---------------------|-----------------------|----------|-----------|----|--------|----|---------|-----|-----|---------------------|-----|---|-----|---|---|-----|---|---|-----|---|---|----------------|--|--|--|--|--|--|--|--|--|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7h | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | EPF [1:0] | | 0 | 0 | DSTB | GON | DTE | GAS | 06h | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>DSTB: The ILI9488 driver enters the Deep Standby Mode when the DSTB is set to high (= 1). In the Deep Standby mode, both internal logic power and SRAM power are turned off, the display data are stored in the Frame Memory, and the instructions are not saved. Rewrite Frame Memory content and instructions after exiting the Deep Standby Mode.</p> <p>Note: The ILI9488 provides two ways to exit the Deep Standby Mode:</p> <ul style="list-style-type: none"> (1) Exit Deep Standby Mode by pull down CSX to low (= 0) 6 times. (2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.  <p>CSX 1 ↑ 2 ↑ 3 ↑ 4 ↑ 5 ↑ 6 ↑ > 80ms</p> <p>WRX "High"</p> <p>RDX "High"</p> <p>D/CX "Low" or "High"</p> <p>DB [23:0] "Low" or "High"</p> <p>GAS: Low voltage detection control</p> <table border="1"> <thead> <tr> <th>GAS</th> <th>Low voltage detection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Enable</td> </tr> <tr> <td>1</td> <td>Disable</td> </tr> </tbody> </table> <p>GON/DTE: Set the output level of the gate driver G1 ~ G320 as follows:</p> <table border="1"> <thead> <tr> <th>GON</th> <th>DTE</th> <th>G1~G320 Gate Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>VGH</td> </tr> <tr> <td>0</td> <td>1</td> <td>VGH</td> </tr> <tr> <td>1</td> <td>0</td> <td>VGL</td> </tr> <tr> <td>1</td> <td>1</td> <td>Normal display</td> </tr> </tbody> </table> <p>EPF [1:0]: Set the data format when 16bbp (R, G, B) to 18 bbp (R, G, B) is stored in the internal GRAM</p> | GAS | Low voltage detection | 0 | | | Enable | 1 | Disable | GON | DTE | G1~G320 Gate Output | 0 | 0 | VGH | 0 | 1 | VGH | 1 | 0 | VGL | 1 | 1 | Normal display | | | | | | | | | | | |
| GAS | Low voltage detection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GON | DTE | G1~G320 Gate Output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | VGH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | VGH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | VGL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Normal display | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| |  <p>EPF[1:0]=00</p> <p>Data Bus: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> <p>Frame Data: R5, R4, R3, R2, R1, 0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, 0</p> <p>Read Data: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> | | | | | | | | | | | | |
|---|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| |  <p>EPF[1:0]=01</p> <p>Data Bus: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> <p>Frame Data: R5, R4, R3, R2, R1, 1, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, 1</p> <p>Read Data: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> | | | | | | | | | | | | |
| |  <p>EPF[1:0]=10</p> <p>Data Bus: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> <p>Frame Data: R5, R4, R3, R2, R1, R0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, B0</p> <p>Read Data: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> | | | | | | | | | | | | |
| |  <p>EPF[1:0]=11</p> <p>Data Bus: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> <p>Frame Data: R5, R4, R3, R2, R1, R0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, B0</p> <p>Read Data: DB15, DB14, DB13, DB12, DB11, DB10, DB9, DB8, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0</p> <p>Condition Copy logic:</p> <pre> graph TD Input[Input data] --> Green{Green Data} Green -- "Green data = odd" --> RB{R/B Data} RB -- "R=B" --> RB_G0[G0 is copied to R0/B0] RB -- "R!=B" --> ByPass((By-pass)) Green -- "Green data = even" --> ByPass </pre> | | | | | | | | | | | | |
| | X = void | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

5.3.9. Color Enhancement Control 1 (B9h)

| B9h | | CECTRL1 (Color Enhancement Control 1) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------------------------|-----|---------|----|----|----|----|----|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D[23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9h | | | | | | | | | | | | | |
| 1 st parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 2 nd parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 3 rd parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 4 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 5 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 6 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 7 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 8 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 9 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 10 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 11 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| 12 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | | | | | 04h | | | | | | | | | | | | | |
| Description | Each parameter is a base value 40h, the localization saturation ratio is calculated: $\text{Saturation Ratio} = \frac{\text{Axis setting value}}{64}$ Axis setting value= 0~255 (00h~FFh, default = 40h) Saturation Ratio = 0~3.98 (default = 1) See chapter “ 9 Color Enhancement Function” for these parameters operation. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.10. Color Enhancement Control 2 (BAh)

| BAh | | CECTRL2 (Color Enhancement Control 2) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------------------------|-----|---------|----|----|----|----|---------------------|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D[23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BAh | | | | | | | | | | | | | |
| 1 st parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fourth_Axis 1 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 2 nd parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fourth_Axis 2 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 3 rd parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fourth_Axis 3 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 4 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fourth_Axis 4 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 5 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fifth_Axis 1 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 6 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fifth_Axis 2 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 7 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fifth_Axis 3 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 8 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Fifth_Axis 4 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 9 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Sixth_Axis 1 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 10 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Sixth_Axis 2 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 11 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Sixth_Axis 3 [4:0] | | | | 04h | | | | | | | | | | | | | |
| 12 th parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | Sixth_Axis 4 [4:0] | | | | 04h | | | | | | | | | | | | | |
| Description | Each parameter is a base value 40h, the localization saturation ratio is calculated: $\text{Saturation Ratio} = \frac{\text{Axis setting value}}{64}$ Axis setting value= 0~255 (00h~FFh, default = 40h) Saturation Ratio = 0~3.98 (default = 1) See chapter "9 Color Enhancement Function" for these parameters operation. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.11. HS Lanes Control (BEh)

| BEh | HSLCTRL (HS Lanes Control) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------|------------|----------|---------|----------|--------|----|----|--------|----|----|-----|--------|--------------|--|------------|---|-----|---|-------|--|-----|----------|---------|--------|--------|-------|---|---|--------|--------|---------|---------|-------|---|---|---------|---------|--------|--------|-------|---|---|--------|--------|---------|---------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BEh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | D/C_Swap | PN_Inv | 0 | 0 | BT OTP | 0 | 0 | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>BT OTP: When the BT_FROM OTP of 1Ah in the NV Memory Write (D0h) command is set to 1, then this BT OTP will become 1 as well.</p> <p>D/C Swap: Swap the DATA/CLOCK of DSI Lanes.</p> <p>PN Inv: Swap the positive/negitive of the polarity of HS Lanes.</p> <table border="1"> <thead> <tr> <th>Type</th><th>D/C_Swap</th><th>PN_Inv</th><th colspan="4">Pin define</th></tr> </thead> <tbody> <tr> <td>Type1</td><td>0</td><td>0</td><td>CLOCK_P</td><td>CLOCK_N</td><td>DATA_P</td><td>DATA_N</td></tr> <tr> <td>Type2</td><td>1</td><td>0</td><td>DATA_P</td><td>DATA_N</td><td>CLOCK_P</td><td>CLOCK_N</td></tr> <tr> <td>Type3</td><td>0</td><td>1</td><td>CLOCK_N</td><td>CLOCK_P</td><td>DATA_N</td><td>DATA_P</td></tr> <tr> <td>Type4</td><td>1</td><td>1</td><td>DATA_N</td><td>DATA_P</td><td>CLOCK_N</td><td>CLOCK_P</td></tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | Type | D/C_Swap | PN_Inv | Pin define | | | | Type1 | 0 | 0 | CLOCK_P | CLOCK_N | DATA_P | DATA_N | Type2 | 1 | 0 | DATA_P | DATA_N | CLOCK_P | CLOCK_N | Type3 | 0 | 1 | CLOCK_N | CLOCK_P | DATA_N | DATA_P | Type4 | 1 | 1 | DATA_N | DATA_P | CLOCK_N | CLOCK_P |
| Type | D/C_Swap | PN_Inv | Pin define | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Type1 | 0 | 0 | CLOCK_P | CLOCK_N | DATA_P | DATA_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Type2 | 1 | 0 | DATA_P | DATA_N | CLOCK_P | CLOCK_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Type3 | 0 | 1 | CLOCK_N | CLOCK_P | DATA_N | DATA_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Type4 | 1 | 1 | DATA_N | DATA_P | CLOCK_N | CLOCK_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.12. Power Control 1 (C0h)

| C0h | PWCTRL 1 (Power Control 1) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|------------|------------------------|----------|----|----|----|----|------------|----|----|----|------------|------------|------------|------------|----------|-----------------------|-----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|----------------------|------------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | VRH1 [4:0] | | | | 0Eh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | | VRH2 [4:0] | | | | 0Eh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | VRH1 [4:0]: Set the VREG1OUT voltage for positive gamma | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>VRH1 [4:0]</th> <th>VREG1OUT</th> <th>VRH1 [4:0]</th> <th>VREG1OUT</th> </tr> </thead> <tbody> <tr><td>5'h00</td><td>Halt (Vreg1out = Hiz)</td><td>5'h10</td><td>1.25 x 3.65 = 4.5625</td></tr> <tr><td>5'h01</td><td>1.25 x 2.90 = 3.6250</td><td>5'h11</td><td>1.25 x 3.70 = 4.6250</td></tr> <tr><td>5'h02</td><td>1.25 x 2.95 = 3.6875</td><td>5'h12</td><td>1.25 x 3.75 = 4.6875</td></tr> <tr><td>5'h03</td><td>1.25 x 3.00 = 3.7500</td><td>5'h13</td><td>1.25 x 3.80 = 4.7500</td></tr> <tr><td>5'h04</td><td>1.25 x 3.05 = 3.8125</td><td>5'h14</td><td>1.25 x 3.85 = 4.8125</td></tr> <tr><td>5'h05</td><td>1.25 x 3.10 = 3.8750</td><td>5'h15</td><td>1.25 x 3.90 = 4.8750</td></tr> <tr><td>5'h06</td><td>1.25 x 3.15 = 3.9375</td><td>5'h16</td><td>1.25 x 3.95 = 4.9375</td></tr> <tr><td>5'h07</td><td>1.25 x 3.20 = 4.0000</td><td>5'h17</td><td>1.25 x 4.00 = 5.0000</td></tr> <tr><td>5'h08</td><td>1.25 x 3.25 = 4.0625</td><td>5'h18</td><td>1.25 x 4.05 = 5.0625</td></tr> <tr><td>5'h09</td><td>1.25 x 3.30 = 4.1250</td><td>5'h19</td><td>1.25 x 4.10 = 5.1250</td></tr> <tr><td>5'h0A</td><td>1.25 x 3.35 = 4.1875</td><td>5'h1A</td><td>1.25 x 4.15 = 5.1875</td></tr> <tr><td>5'h0B</td><td>1.25 x 3.40 = 4.2500</td><td>5'h1B</td><td>1.25 x 4.20 = 5.2500</td></tr> <tr><td>5'h0C</td><td>1.25 x 3.45 = 4.3125</td><td>5'h1C</td><td>1.25 x 4.25 = 5.3125</td></tr> <tr><td>5'h0D</td><td>1.25 x 3.50 = 4.3750</td><td>5'h1D</td><td>1.25 x 4.30 = 5.3750</td></tr> <tr><td>5'h0E</td><td>1.25 x 3.55 = 4.4375</td><td>5'h1E</td><td>1.25 x 4.35 = 5.4375</td></tr> <tr><td>5'h0F</td><td>1.25 x 3.60 = 4.5000</td><td>5'h1F</td><td>1.25 x 4.40 = 5.5000</td></tr> </tbody> </table> | | | | | | | | | | | | | VRH1 [4:0] | VREG1OUT | VRH1 [4:0] | VREG1OUT | 5'h00 | Halt (Vreg1out = Hiz) | 5'h10 | 1.25 x 3.65 = 4.5625 | 5'h01 | 1.25 x 2.90 = 3.6250 | 5'h11 | 1.25 x 3.70 = 4.6250 | 5'h02 | 1.25 x 2.95 = 3.6875 | 5'h12 | 1.25 x 3.75 = 4.6875 | 5'h03 | 1.25 x 3.00 = 3.7500 | 5'h13 | 1.25 x 3.80 = 4.7500 | 5'h04 | 1.25 x 3.05 = 3.8125 | 5'h14 | 1.25 x 3.85 = 4.8125 | 5'h05 | 1.25 x 3.10 = 3.8750 | 5'h15 | 1.25 x 3.90 = 4.8750 | 5'h06 | 1.25 x 3.15 = 3.9375 | 5'h16 | 1.25 x 3.95 = 4.9375 | 5'h07 | 1.25 x 3.20 = 4.0000 | 5'h17 | 1.25 x 4.00 = 5.0000 | 5'h08 | 1.25 x 3.25 = 4.0625 | 5'h18 | 1.25 x 4.05 = 5.0625 | 5'h09 | 1.25 x 3.30 = 4.1250 | 5'h19 | 1.25 x 4.10 = 5.1250 | 5'h0A | 1.25 x 3.35 = 4.1875 | 5'h1A | 1.25 x 4.15 = 5.1875 | 5'h0B | 1.25 x 3.40 = 4.2500 | 5'h1B | 1.25 x 4.20 = 5.2500 | 5'h0C | 1.25 x 3.45 = 4.3125 | 5'h1C | 1.25 x 4.25 = 5.3125 | 5'h0D | 1.25 x 3.50 = 4.3750 | 5'h1D | 1.25 x 4.30 = 5.3750 | 5'h0E | 1.25 x 3.55 = 4.4375 | 5'h1E | 1.25 x 4.35 = 5.4375 | 5'h0F | 1.25 x 3.60 = 4.5000 | 5'h1F |
| VRH1 [4:0] | VREG1OUT | VRH1 [4:0] | VREG1OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h00 | Halt (Vreg1out = Hiz) | 5'h10 | 1.25 x 3.65 = 4.5625 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h01 | 1.25 x 2.90 = 3.6250 | 5'h11 | 1.25 x 3.70 = 4.6250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h02 | 1.25 x 2.95 = 3.6875 | 5'h12 | 1.25 x 3.75 = 4.6875 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h03 | 1.25 x 3.00 = 3.7500 | 5'h13 | 1.25 x 3.80 = 4.7500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h04 | 1.25 x 3.05 = 3.8125 | 5'h14 | 1.25 x 3.85 = 4.8125 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h05 | 1.25 x 3.10 = 3.8750 | 5'h15 | 1.25 x 3.90 = 4.8750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h06 | 1.25 x 3.15 = 3.9375 | 5'h16 | 1.25 x 3.95 = 4.9375 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h07 | 1.25 x 3.20 = 4.0000 | 5'h17 | 1.25 x 4.00 = 5.0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h08 | 1.25 x 3.25 = 4.0625 | 5'h18 | 1.25 x 4.05 = 5.0625 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h09 | 1.25 x 3.30 = 4.1250 | 5'h19 | 1.25 x 4.10 = 5.1250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0A | 1.25 x 3.35 = 4.1875 | 5'h1A | 1.25 x 4.15 = 5.1875 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0B | 1.25 x 3.40 = 4.2500 | 5'h1B | 1.25 x 4.20 = 5.2500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0C | 1.25 x 3.45 = 4.3125 | 5'h1C | 1.25 x 4.25 = 5.3125 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0D | 1.25 x 3.50 = 4.3750 | 5'h1D | 1.25 x 4.30 = 5.3750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0E | 1.25 x 3.55 = 4.4375 | 5'h1E | 1.25 x 4.35 = 5.4375 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0F | 1.25 x 3.60 = 4.5000 | 5'h1F | 1.25 x 4.40 = 5.5000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VRH2 [4:0]: Set the VREG2OUT voltage for negative gammas | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <thead> <tr> <th>VRH2 [4:0]</th> <th>VREG2OUT</th> <th>VRH2 [4:0]</th> <th>VREG2OUT</th> </tr> </thead> <tbody> <tr><td>5'h00</td><td>Halt (Vreg2out = Hiz)</td><td>5'h10</td><td>-1.25 x 3.65 = -4.5625</td></tr> <tr><td>5'h01</td><td>-1.25 x 2.90 = -3.6250</td><td>5'h11</td><td>-1.25 x 3.70 = -4.6250</td></tr> <tr><td>5'h02</td><td>-1.25 x 2.95 = -3.6875</td><td>5'h12</td><td>-1.25 x 3.75 = -4.6875</td></tr> <tr><td>5'h03</td><td>-1.25 x 3.00 = -3.7500</td><td>5'h13</td><td>-1.25 x 3.80 = -4.7500</td></tr> <tr><td>5'h04</td><td>-1.25 x 3.05 = -3.8125</td><td>5'h14</td><td>-1.25 x 3.85 = -4.8125</td></tr> <tr><td>5'h05</td><td>-1.25 x 3.10 = -3.8750</td><td>5'h15</td><td>-1.25 x 3.90 = -4.8750</td></tr> <tr><td>5'h06</td><td>-1.25 x 3.15 = -3.9375</td><td>5'h16</td><td>-1.25 x 3.95 = -4.9375</td></tr> <tr><td>5'h07</td><td>-1.25 x 3.20 = -4.0000</td><td>5'h17</td><td>-1.25 x 4.00 = -5.0000</td></tr> <tr><td>5'h08</td><td>-1.25 x 3.25 = -4.0625</td><td>5'h18</td><td>-1.25 x 4.05 = -5.0625</td></tr> <tr><td>5'h09</td><td>-1.25 x 3.30 = -4.1250</td><td>5'h19</td><td>-1.25 x 4.10 = -5.1250</td></tr> <tr><td>5'h0A</td><td>-1.25 x 3.35 = -4.1875</td><td>5'h1A</td><td>-1.25 x 4.15 = -5.1875</td></tr> <tr><td>5'h0B</td><td>-1.25 x 3.40 = -4.2500</td><td>5'h1B</td><td>-1.25 x 4.20 = -5.2500</td></tr> <tr><td>5'h0C</td><td>-1.25 x 3.45 = -4.3125</td><td>5'h1C</td><td>-1.25 x 4.25 = -5.3125</td></tr> <tr><td>5'h0D</td><td>-1.25 x 3.50 = -4.3750</td><td>5'h1D</td><td>-1.25 x 4.30 = -5.3750</td></tr> <tr><td>5'h0E</td><td>-1.25 x 3.55 = -4.4375</td><td>5'h1E</td><td>-1.25 x 4.35 = -5.4375</td></tr> <tr><td>5'h0F</td><td>-1.25 x 3.60 = -4.5000</td><td>5'h1F</td><td>-1.25 x 4.40 = -5.5000</td></tr> </tbody> </table> | | | | | | | | | | | | | VRH2 [4:0] | VREG2OUT | VRH2 [4:0] | VREG2OUT | 5'h00 | Halt (Vreg2out = Hiz) | 5'h10 | -1.25 x 3.65 = -4.5625 | 5'h01 | -1.25 x 2.90 = -3.6250 | 5'h11 | -1.25 x 3.70 = -4.6250 | 5'h02 | -1.25 x 2.95 = -3.6875 | 5'h12 | -1.25 x 3.75 = -4.6875 | 5'h03 | -1.25 x 3.00 = -3.7500 | 5'h13 | -1.25 x 3.80 = -4.7500 | 5'h04 | -1.25 x 3.05 = -3.8125 | 5'h14 | -1.25 x 3.85 = -4.8125 | 5'h05 | -1.25 x 3.10 = -3.8750 | 5'h15 | -1.25 x 3.90 = -4.8750 | 5'h06 | -1.25 x 3.15 = -3.9375 | 5'h16 | -1.25 x 3.95 = -4.9375 | 5'h07 | -1.25 x 3.20 = -4.0000 | 5'h17 | -1.25 x 4.00 = -5.0000 | 5'h08 | -1.25 x 3.25 = -4.0625 | 5'h18 | -1.25 x 4.05 = -5.0625 | 5'h09 | -1.25 x 3.30 = -4.1250 | 5'h19 | -1.25 x 4.10 = -5.1250 | 5'h0A | -1.25 x 3.35 = -4.1875 | 5'h1A | -1.25 x 4.15 = -5.1875 | 5'h0B | -1.25 x 3.40 = -4.2500 | 5'h1B | -1.25 x 4.20 = -5.2500 | 5'h0C | -1.25 x 3.45 = -4.3125 | 5'h1C | -1.25 x 4.25 = -5.3125 | 5'h0D | -1.25 x 3.50 = -4.3750 | 5'h1D | -1.25 x 4.30 = -5.3750 | 5'h0E | -1.25 x 3.55 = -4.4375 | 5'h1E | -1.25 x 4.35 = -5.4375 | 5'h0F | -1.25 x 3.60 = -4.5000 | 5'h1F | -1.25 x 4.40 = -5.5000 |
| VRH2 [4:0] | VREG2OUT | VRH2 [4:0] | VREG2OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h00 | Halt (Vreg2out = Hiz) | 5'h10 | -1.25 x 3.65 = -4.5625 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h01 | -1.25 x 2.90 = -3.6250 | 5'h11 | -1.25 x 3.70 = -4.6250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h02 | -1.25 x 2.95 = -3.6875 | 5'h12 | -1.25 x 3.75 = -4.6875 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h03 | -1.25 x 3.00 = -3.7500 | 5'h13 | -1.25 x 3.80 = -4.7500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h04 | -1.25 x 3.05 = -3.8125 | 5'h14 | -1.25 x 3.85 = -4.8125 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h05 | -1.25 x 3.10 = -3.8750 | 5'h15 | -1.25 x 3.90 = -4.8750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h06 | -1.25 x 3.15 = -3.9375 | 5'h16 | -1.25 x 3.95 = -4.9375 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h07 | -1.25 x 3.20 = -4.0000 | 5'h17 | -1.25 x 4.00 = -5.0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h08 | -1.25 x 3.25 = -4.0625 | 5'h18 | -1.25 x 4.05 = -5.0625 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h09 | -1.25 x 3.30 = -4.1250 | 5'h19 | -1.25 x 4.10 = -5.1250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0A | -1.25 x 3.35 = -4.1875 | 5'h1A | -1.25 x 4.15 = -5.1875 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0B | -1.25 x 3.40 = -4.2500 | 5'h1B | -1.25 x 4.20 = -5.2500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0C | -1.25 x 3.45 = -4.3125 | 5'h1C | -1.25 x 4.25 = -5.3125 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0D | -1.25 x 3.50 = -4.3750 | 5'h1D | -1.25 x 4.30 = -5.3750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0E | -1.25 x 3.55 = -4.4375 | 5'h1E | -1.25 x 4.35 = -5.4375 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5'h0F | -1.25 x 3.60 = -4.5000 | 5'h1F | -1.25 x 4.40 = -5.5000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Note 1: The setting of DDVDH and VRH1 should be: VREG1OUT \leq (DDVDH - 0.5) V. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Note 2: The setting of DDVDL and VRH2 should be VREG2OUT \geq (DDVDL + 0.5) V. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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| | X = void | | | | | | | | | | | | |
|---|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Restriction | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

5.3.13. Power Control 2 (C1h)

| C1h | PWCTRL 2 (Power Control 2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--------------|--------------|------------|------------|------------|----|----|----|----------|----|----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|--|--|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1h | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | BT [2:0] | | | 43h | | | | | | | | | | | | | | | | |
| BT [2:0]: Set the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | BT [2:0] | DDVDH | DDVDL | VCL | VGH | VGL | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h0 | VCI x 2 | -(VCI x 2) | - VCI | VCI x 6 | - VCI x 5 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h1 | | | | | - VCI x 4 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h2 | | | | Inhibited | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h3 | | | | VCI x 5 | - VCI x 5 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h4 | | | | | - VCI x 4 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h5 | | | | | - VCI x 3 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h6 | | | | | - VCI x 4 | | | | | | | | | | | | | | | | | | | | | | | |
| | 3'h7 | | | | | - VCI x 3 | | | | | | | | | | | | | | | | | | | | | | | |
| Notes: <ol style="list-style-type: none"> 1. DDVDH setting restriction: DDVDH ≤ 6.0 V. 2. To prevent the device damage, please keep VGH – VGL ≤ 32V. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.14. Power Control 3 (For Normal Mode) (C2h)

| C2h | PWCTRL 3 (Power Control 3) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|---|----------|----|------------|----|----|----|------------|----|----|-----|------------|--------------|--|---|---|-----|---|-----|--|-------|----------|-----|---|---|---|-------|--|--|---|---|---|-------|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|------------|--|--|---------------------------------------|--|--|---|---|---|-------|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | DCA1 [2:0] | | | 0 | DCA0 [2:0] | | | 33h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>DCA0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.</p> <p>DCA1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption..</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="3">DCA0 [2:0]</th> <th colspan="3">Step-up cycle for step-up circuit 1/4/5</th> </tr> <tr> <td>0</td><td>0</td><td>0</td> <td colspan="3">1/8 H</td> </tr> <tr> <td>0</td><td>0</td><td>1</td> <td colspan="3">1/4 H</td> </tr> <tr> <td>0</td><td>1</td><td>0</td> <td colspan="3">1/2 H</td> </tr> <tr> <td>0</td><td>1</td><td>1</td> <td colspan="3">1 H</td> </tr> <tr> <td>1</td><td>0</td><td>0</td> <td colspan="3">2 H</td> </tr> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="3">DCA1 [2:0]</th> <th colspan="3">Step-up cycle for step-up circuit 2/3</th> </tr> <tr> <td>0</td><td>0</td><td>0</td> <td colspan="3">1/2 H</td> </tr> <tr> <td>0</td><td>0</td><td>1</td> <td colspan="3">1 H</td> </tr> <tr> <td>0</td><td>1</td><td>0</td> <td colspan="3">2 H</td> </tr> <tr> <td>0</td><td>1</td><td>1</td> <td colspan="3">4 H</td> </tr> <tr> <td>1</td><td>0</td><td>0</td> <td colspan="3">8 H</td> </tr> </table> <p>X = void</p> | | | | | | | | | | | | | DCA0 [2:0] | | | Step-up cycle for step-up circuit 1/4/5 | | | 0 | 0 | 0 | 1/8 H | | | 0 | 0 | 1 | 1/4 H | | | 0 | 1 | 0 | 1/2 H | | | 0 | 1 | 1 | 1 H | | | 1 | 0 | 0 | 2 H | | | DCA1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | | | 0 | 0 | 0 | 1/2 H | | | 0 | 0 | 1 | 1 H | | | 0 | 1 | 0 | 2 H | | | 0 | 1 | 1 | 4 H | | | 1 | 0 | 0 | 8 H | | |
| DCA0 [2:0] | | | Step-up cycle for step-up circuit 1/4/5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1/4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DCA1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.15. Power Control 4 (For Idle Mode) (C3h)

| C3h | PWCTRL 4 (Power Control 4) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|---|----------|----|------------|------------|----|----|------------|----|----|---|--------|--------------|--|-------|---|-----|---|-------|--|-----|----------|-------|---|---|---|-----|---|---|---|-----|--|--|--|--|--|--|--|--|--|------------|--|--|---------------------------------------|---|---|---|-------|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | DCB1 [2:0] | | | 0 | DCB0 [2:0] | | | 33h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | DCB0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption. DCB1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="3">DCB0 [2:0]</th> <th>Step-up cycle for step-up circuit 1/4/5</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>1/8 H</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1/4 H</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1/2 H</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1 H</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>2 H</td></tr> </tbody> </table> | | | | | | DCB0 [2:0] | | | | | | Step-up cycle for step-up circuit 1/4/5 | 0 | 0 | 0 | 1/8 H | 0 | 0 | 1 | 1/4 H | 0 | 1 | 0 | 1/2 H | 0 | 1 | 1 | 1 H | 1 | 0 | 0 | 2 H | <table border="1"> <thead> <tr> <th colspan="3">DCB1 [2:0]</th> <th>Step-up cycle for step-up circuit 2/3</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>1/2 H</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1 H</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>2 H</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>4 H</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>8 H</td></tr> </tbody> </table> | | | | | | | | | DCB1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | 0 | 0 | 0 | 1/2 H | 0 | 0 | 1 | 1 H | 0 | 1 | 0 | 2 H | 0 | 1 | 1 | 4 H | 1 |
| DCB0 [2:0] | | | Step-up cycle for step-up circuit 1/4/5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1/4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DCB1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.16. Power Control 5 (For Partial Mode) (C4h)

| C4h | PWCTRL 5 (Power Control 5) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|---|----------|----|------------|----|----|----|------------|----|----|-----|------------|--------------|--|---|---|-----|---|-----|--|-------|----------|-----|---|---|---|-------|--|--|---|---|---|-------|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|------------|--|--|---------------------------------------|--|--|---|---|---|-------|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|---|---|---|-----|--|--|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | DCC1 [2:0] | | | 0 | DCC0 [2:0] | | | 33h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>DCC0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.</p> <p>DCC1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="3">DCC0 [2:0]</th> <th colspan="3">Step-up cycle for step-up circuit 1/4/5</th> </tr> <tr> <td>0</td><td>0</td><td>0</td> <td colspan="3">1/8 H</td> </tr> <tr> <td>0</td><td>0</td><td>1</td> <td colspan="3">1/4 H</td> </tr> <tr> <td>0</td><td>1</td><td>0</td> <td colspan="3">1/2 H</td> </tr> <tr> <td>0</td><td>1</td><td>1</td> <td colspan="3">1 H</td> </tr> <tr> <td>1</td><td>0</td><td>0</td> <td colspan="3">2 H</td> </tr> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="3">DCC1 [2:0]</th> <th colspan="3">Step-up cycle for step-up circuit 2/3</th> </tr> <tr> <td>0</td><td>0</td><td>0</td> <td colspan="3">1/2 H</td> </tr> <tr> <td>0</td><td>0</td><td>1</td> <td colspan="3">1 H</td> </tr> <tr> <td>0</td><td>1</td><td>0</td> <td colspan="3">2 H</td> </tr> <tr> <td>0</td><td>1</td><td>1</td> <td colspan="3">4 H</td> </tr> <tr> <td>1</td><td>0</td><td>0</td> <td colspan="3">8 H</td> </tr> </table> <p>X = void</p> | | | | | | | | | | | | | DCC0 [2:0] | | | Step-up cycle for step-up circuit 1/4/5 | | | 0 | 0 | 0 | 1/8 H | | | 0 | 0 | 1 | 1/4 H | | | 0 | 1 | 0 | 1/2 H | | | 0 | 1 | 1 | 1 H | | | 1 | 0 | 0 | 2 H | | | DCC1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | | | 0 | 0 | 0 | 1/2 H | | | 0 | 0 | 1 | 1 H | | | 0 | 1 | 0 | 2 H | | | 0 | 1 | 1 | 4 H | | | 1 | 0 | 0 | 8 H | | |
| DCC0 [2:0] | | | Step-up cycle for step-up circuit 1/4/5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1/4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DCC1 [2:0] | | | Step-up cycle for step-up circuit 2/3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1/2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 8 H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.17. VCOM Control (C5h)

| C5h | VMCTRL (VCOM Control) | | | | | | | | | | | | | |
|---------------------------|-----------------------|-----|-----|----------|---------------|----|----|----|----|----|----|-----|-----|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5h | |
| 1 st Parameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | nVM | 00h | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | VCM_REG [7:0] | | | | | | | | | 40h |
| 3 rd Parameter | 1 | 1 | ↑ | XX | VCM_REG_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | |
| 4 th Parameter | 1 | ↑ | 1 | XX | VCM_OUT [7:0] | | | | | | | | | 40h |

nVM: When the NV memory is programmed, the nVM will be set to 1 automatically.

- 0: NV memory is not programmed
- 1: NV memory is programmed

VCM_REG [7:0] is used to set the factor to generate VCOM voltage from the reference voltage VREG2OUT.

| VCM_REG [7:0] | | | | | | | | VCOM |
|---------------|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1.98438 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -1.96875 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | -1.95313 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | -1.9375 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | -1.92188 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | -1.90625 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | -1.89063 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | -1.875 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | -1.85938 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | -1.84375 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | -1.82813 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | -1.8125 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | -1.79688 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | -1.78125 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -1.76563 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | -1.75 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | -1.73438 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | -1.71875 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | -1.70313 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | -1.6875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | -1.67188 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -1.65625 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | -1.64063 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | -1.625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | -1.60938 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | -1.59375 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | -1.57813 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | -1.5625 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | -1.54688 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | -1.53125 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | -1.51563 |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|----------|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | -1.5 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | -1.48438 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | -1.46875 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | -1.45313 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | -1.4375 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | -1.42188 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | -1.40625 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | -1.39063 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | -1.375 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | -1.35938 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -1.34375 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | -1.32813 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | -1.3125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | -1.29688 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | -1.28125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | -1.26563 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | -1.25 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | -1.23438 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | -1.21875 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -1.20313 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | -1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | -1.17188 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | -1.15625 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | -1.14063 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | -1.125 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | -1.10938 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | -1.09375 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | -1.07813 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | -1.0625 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | -1.04688 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | -1.03125 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -1.01563 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | -1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | -0.98438 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | -0.96875 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | -0.95313 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | -0.9375 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | -0.92188 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | -0.90625 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | -0.89063 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | -0.875 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | -0.85938 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | -0.84375 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | -0.82813 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | -0.8125 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | -0.79688 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | -0.78125 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | -0.76563 |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|----------|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | -0.75 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | -0.73438 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -0.71875 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | -0.70313 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | -0.6875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | -0.67188 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -0.65625 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | -0.64063 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | -0.625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | -0.60938 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | -0.59375 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | -0.57813 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | -0.5625 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | -0.54688 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | -0.53125 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | -0.51563 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | -0.5 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | -0.48438 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | -0.46875 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | -0.45313 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | -0.4375 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | -0.42188 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -0.40625 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | -0.39063 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | -0.375 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | -0.35938 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | -0.34375 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | -0.32813 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | -0.3125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | -0.29688 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | -0.28125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | -0.26563 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -0.25 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | -0.23438 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -0.21875 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | -0.20313 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -0.1875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | -0.17188 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | -0.15625 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | -0.14063 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | -0.125 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | -0.10938 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | -0.09375 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | -0.07813 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | -0.0625 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -0.04688 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -0.03125 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -0.01563 |

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| | | <table border="1"> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td colspan="9">10000001~11111110</td><td>Inhibit</td></tr> <tr><td colspan="9">11111111</td><td>Halt</td></tr> </table> | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10000001~11111110 | | | | | | | | | Inhibit | 11111111 | | | | | | | | | Halt | |
|---|--------------|---|--------|--------------|--|-----|---|-----|---|-----|--|-----|-------------------|-----|--|--|--|--|--|--|--|---------|----------|--|--|--|--|--|--|--|--|------|--|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| 10000001~11111110 | | | | | | | | | Inhibit | | | | | | | | | | | | | | | | | | | | | | | | |
| 11111111 | | | | | | | | | Halt | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <p>VCM_REG_EN: Select the Vcom value from VCM_REG [7:0] or NV memory.</p> <p>0: VCOM value from NV memory. 1: VCOM value from VCM_REG [7:0].</p> <p>VCM_OUT [7:0]: NV memory programmed value.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.18. CABC Control 1 (C6h)

| C6h | CABCCTRL1 (CABC Control 1) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-----|----------|-----------------|----|----|----|----|----|---------|--------------------|------------------|-----|--|-----------------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|--------------|-----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--------------------|---|---|---|---|---|---|---|---|---|---|---|--------|---|---|---|---|---|---|---|---|---|---|---|---------|---|---|---|---|---|---|---|---|---|---|---|---------|---|---|---|---|---|---|---|---|---|---|---|---------|---|--|--|--|--|--|--|--|--|--|--|---|-----------|---|--|--|--|--|--|--|--|--|--|--|---|-----------|---|--|--|--|--|--|--|--|--|--|--|---|-----------|---|--|--|--|--|--|--|--|--|--|--|---|-----------|--------|--|--|--|--|--|--|--|--|--|--|--|--------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | SCD_VLINE [7:0] | | | | | | | | | E0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SCD_VLINE [10:8] | 01h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | SCD_VLINE [10:0]: This parameter is used to set the display line per frame while the partial mode is ON. <table border="1"> <thead> <tr> <th colspan="12">SCD_VLINE [8:0]</th> <th rowspan="2">Display line</th> </tr> <tr> <th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1 line</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>4 lines</td> </tr> <tr> <td colspan="11">:</td><td>:</td><td>477 lines</td> </tr> <tr> <td colspan="11">:</td><td>:</td><td>478 lines</td> </tr> <tr> <td colspan="11">0</td><td>1</td><td>479 lines</td> </tr> <tr> <td colspan="11">0</td><td>0</td><td>480 lines</td> </tr> <tr> <td colspan="12">Others</td><td>Setting prohibited</td> </tr> </tbody> </table> | | | | | | | | | | | | | | | SCD_VLINE [8:0] | | | | | | | | | | | | Display line | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Setting prohibited | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 line | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 lines | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 lines | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4 lines | : | | | | | | | | | | | : | 477 lines | : | | | | | | | | | | | : | 478 lines | 0 | | | | | | | | | | | 1 | 479 lines | 0 | | | | | | | | | | | 0 | 480 lines | Others | | | | | | | | | | | | Setting prohibited |
| SCD_VLINE [8:0] | | | | | | | | | | | | Display line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | | | | | | | | | | | : | 477 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | | | | | | | | | | | : | 478 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | | | | | | | | | | 1 | 479 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | | | | | | | | | | 0 | 480 lines | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Others | | | | | | | | | | | | Setting prohibited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.19. CABC Control 2 (C8h)

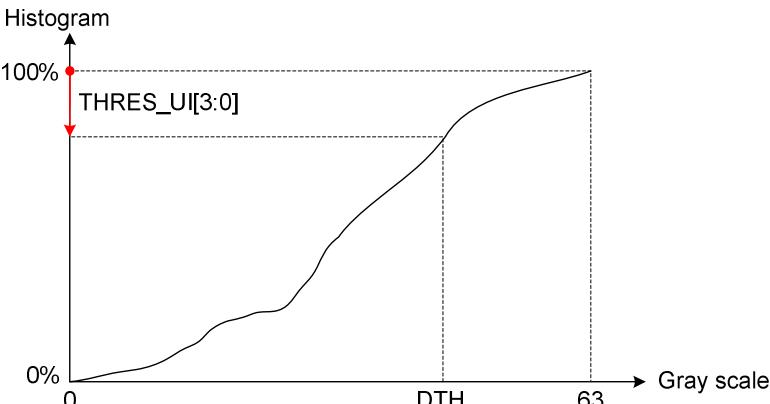
| C8h | CABCCTRL2 (CABC Control 2) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------------------------|-----|----------|----|----|----|----|----|----|----|---------|-----|--------|--------------|--|-----|---|------------|---|-----|--|-----|----------|---------------------------------|---|---|---------------------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8h | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | PWM POL | B0h | | | | | | | | | | | | | | | |
| Description | PWM POL: The bit is used to define the polarity of the CABC_PWM signal. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BL</th><th>LEDPWM POL</th><th>CABC_PWM pin</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Always low</td></tr> <tr> <td>0</td><td>1</td><td>Always high</td></tr> <tr> <td>1</td><td>0</td><td>Original polarity of PWM signal</td></tr> <tr> <td>1</td><td>1</td><td>Inversed polarity of PWM signal</td></tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | BL | LEDPWM POL | CABC_PWM pin | 0 | 0 | Always low | 0 | 1 | Always high | 1 | 0 | Original polarity of PWM signal | 1 | 1 | Inversed polarity of PWM signal |
| BL | LEDPWM POL | CABC_PWM pin | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Always low | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Always high | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Original polarity of PWM signal | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Inversed polarity of PWM signal | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.20. CABC Control 3 (C9h)

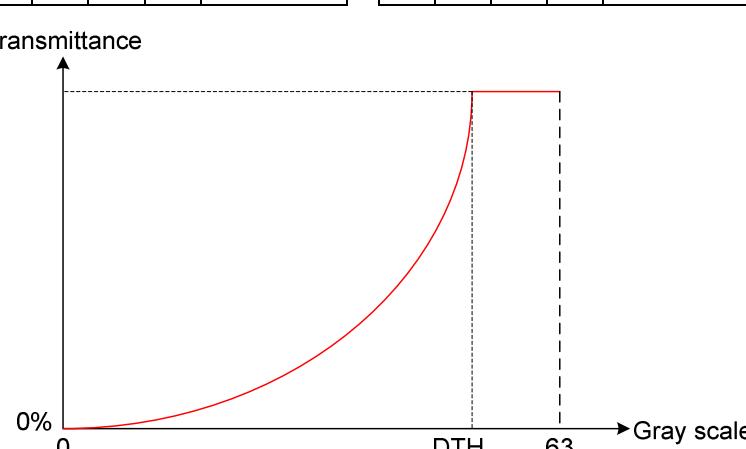
| C9h | CABCCTRL3 (CABC Control 3) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|-----|-------------------|-----------------|----|----|-------------|-------------------|----|----|----|-----|---|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|---|---|--|--|-------------------|-----------------|--|--|-------------|-------------|----|----|----|----|---|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | THRES_MOV [3:0] | | | | THRES_STILL [3:0] | | | | BBh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the MOVING image mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="4">THRES_MOV [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr> </tbody> </table> | | | | THRES_MOV [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 0 | 0 | 0 | 0 | 99 % | 0 | 0 | 0 | 1 | 98 % | 0 | 0 | 1 | 0 | 96 % | 0 | 0 | 1 | 1 | 94 % | 0 | 1 | 0 | 0 | 92 % | 0 | 1 | 0 | 1 | 90 % | 0 | 1 | 1 | 0 | 88 % | 0 | 1 | 1 | 1 | 86 % | <table border="1"> <thead> <tr> <th colspan="4">THRES_MOV [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr> </tbody> </table> | | | | THRES_MOV [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 1 | 0 | 0 | 0 | 84 % | 1 | 0 | 0 | 1 | 82 % | 1 | 0 | 1 | 0 | 80 % | 1 | 0 | 1 | 1 | 78 % | 1 | 1 | 0 | 0 | 76 % | 1 | 1 | 0 | 1 | 74 % | 1 | 1 | 1 | 0 | 72 % | 1 | 1 | 1 | 1 |
| THRES_MOV [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 99 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 98 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 96 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 94 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 92 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 90 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 88 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 86 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| THRES_MOV [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 84 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 82 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 80 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 78 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 76 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 74 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 72 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 70 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the STILL mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <thead> <tr> <th colspan="4">THRES_STILL [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr> </tbody> </table> | | | | THRES_STILL [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 0 | 0 | 0 | 0 | 99 % | 0 | 0 | 0 | 1 | 98 % | 0 | 0 | 1 | 0 | 96 % | 0 | 0 | 1 | 1 | 94 % | 0 | 1 | 0 | 0 | 92 % | 0 | 1 | 0 | 1 | 90 % | 0 | 1 | 1 | 0 | 88 % | 0 | 1 | 1 | 1 | 86 % | <table border="1"> <thead> <tr> <th colspan="4">THRES_STILL [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr> </tbody> </table> | | | | THRES_STILL [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 1 | 0 | 0 | 0 | 84 % | 1 | 0 | 0 | 1 | 82 % | 1 | 0 | 1 | 0 | 80 % | 1 | 0 | 1 | 1 | 78 % | 1 | 1 | 0 | 0 | 76 % | 1 | 1 | 0 | 1 | 74 % | 1 | 1 | 1 | 0 | 72 % | 1 | 1 | 1 | 1 | 70 % |
| THRES_STILL [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 99 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 98 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 96 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 94 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 92 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 90 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 88 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 86 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| THRES_STILL [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 84 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 82 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 80 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 78 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 76 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 74 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 72 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 70 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| | <p>Histogram</p> <p>100%</p> <p>THRES_MOV [3:0]/THRES_STILL [3:0]</p> <p>0%</p> <p>DTH</p> <p>63</p> <p>Gray scale</p> <p>X = Void</p> | | | | | | | | | | | | |
|---|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Restriction | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

5.3.21. CABC Control 4 (CAh)

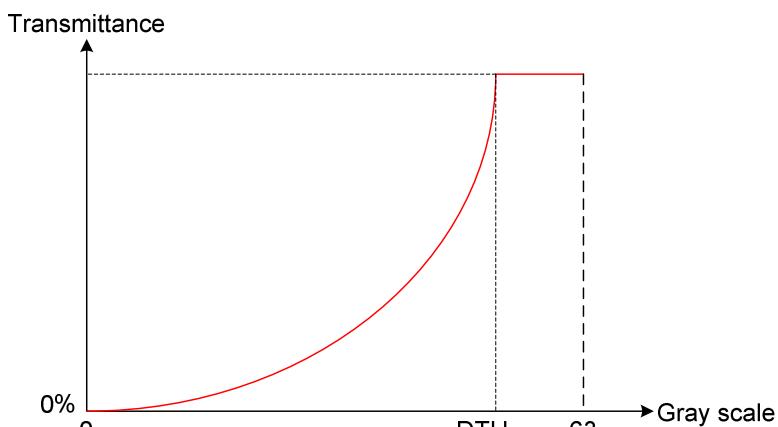
| CAh | CABCCTRL4 (CABC Control 4) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|----------------|-------------|----|----|-------------|----|----------------|----|----|----|-----|--------|--------------|--|-----|---|-----|---|------|--|-----|----------|-----|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|----------------|--|--|--|-------------|----|----|----|----|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CAh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | THRES_UI [3:0] | | | | 0Bh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.</p> <table border="1"> <thead> <tr> <th colspan="4">THRES_UI [3:0]</th> <th rowspan="2">Description</th> </tr> <tr> <th>D3</th> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="4">THRES_UI [3:0]</th> <th rowspan="2">Description</th> </tr> <tr> <th>D3</th> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr> </tbody> </table>  <p>X = Void.</p> | | THRES_UI [3:0] | | | | Description | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 | 99 % | 0 | 0 | 0 | 1 | 98 % | 0 | 0 | 1 | 0 | 96 % | 0 | 0 | 1 | 1 | 94 % | 0 | 1 | 0 | 0 | 92 % | 0 | 1 | 0 | 1 | 90 % | 0 | 1 | 1 | 0 | 88 % | 0 | 1 | 1 | 1 | 86 % | THRES_UI [3:0] | | | | Description | D3 | D2 | D1 | D0 | 1 | 0 | 0 | 0 | 84 % | 1 | 0 | 0 | 1 | 82 % | 1 | 0 | 1 | 0 | 80 % | 1 | 0 | 1 | 1 | 78 % | 1 | 1 | 0 | 0 | 76 % | 1 | 1 | 0 | 1 | 74 % | 1 | 1 | 1 | 0 | 72 % | 1 | 1 | 1 | 1 | 70 % |
| THRES_UI [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 99 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 98 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 96 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 94 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 92 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 90 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 88 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 86 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| THRES_UI [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 84 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 82 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 80 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 78 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 76 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 74 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 72 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 70 % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.22. CABC Control 5 (CBh)

| CBh | CABCCTRL5 (CABC Control 5) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|--|-----|-----|-------------|------------------|----|----|----|-----------------|----|----|----|-----|--|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|--|--|--|-----------------|--|--|--|-------------|----|----|----|----|--|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CBh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | DTH_MOV [3:0] | | | | DTH_STILL [3:0] | | | | A8h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | DTH_MOV [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the MOVING image mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="4">DTH_MOV [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>224</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>220</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>216</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>212</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>208</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>204</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>200</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>196</td></tr> </tbody> </table> | | | | DTH_MOV [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 0 | 0 | 0 | 0 | 224 | 0 | 0 | 0 | 1 | 220 | 0 | 0 | 1 | 0 | 216 | 0 | 0 | 1 | 1 | 212 | 0 | 1 | 0 | 0 | 208 | 0 | 1 | 0 | 1 | 204 | 0 | 1 | 1 | 0 | 200 | 0 | 1 | 1 | 1 | 196 | <table border="1"> <thead> <tr> <th colspan="4">DTH_MOV [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>192</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>188</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>184</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>180</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>176</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>172</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>168</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>164</td></tr> </tbody> </table> | | | | DTH_MOV [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 1 | 0 | 0 | 0 | 192 | 1 | 0 | 0 | 1 | 188 | 1 | 0 | 1 | 0 | 184 | 1 | 0 | 1 | 1 | 180 | 1 | 1 | 0 | 0 | 176 | 1 | 1 | 0 | 1 | 172 | 1 | 1 | 1 | 0 | 168 | 1 | 1 | 1 | 1 |
| DTH_MOV [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 224 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 216 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 212 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 208 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 204 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 196 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DTH_MOV [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 192 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 188 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 184 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 172 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 168 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 164 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | DTH_OPT [2:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the STILL image mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="4">DTH_STILLI [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>224</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>220</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>216</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>212</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>208</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>204</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>200</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>196</td></tr> </tbody> </table> | | | | DTH_STILLI [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 0 | 0 | 0 | 0 | 224 | 0 | 0 | 0 | 1 | 220 | 0 | 0 | 1 | 0 | 216 | 0 | 0 | 1 | 1 | 212 | 0 | 1 | 0 | 0 | 208 | 0 | 1 | 0 | 1 | 204 | 0 | 1 | 1 | 0 | 200 | 0 | 1 | 1 | 1 | 196 | <table border="1"> <thead> <tr> <th colspan="4">DTH_STILL [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>192</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>188</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>184</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>180</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>176</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>172</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>168</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>164</td></tr> </tbody> </table> | | | | DTH_STILL [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 1 | 0 | 0 | 0 | 192 | 1 | 0 | 0 | 1 | 188 | 1 | 0 | 1 | 0 | 184 | 1 | 0 | 1 | 1 | 180 | 1 | 1 | 0 | 0 | 176 | 1 | 1 | 0 | 1 | 172 | 1 | 1 | 1 | 0 | 168 | 1 | 1 | 1 | 1 |
| DTH_STILLI [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 224 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 216 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 212 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 208 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 204 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 196 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DTH_STILL [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 192 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 188 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 184 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 172 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 168 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 164 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction |  <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Register Availability | Status | Availability |
|-----------------------|---|--------------|
| | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| | Sleep IN | Yes |

5.3.23. CABC Control 6 (CCh)

| CCh | CABCCTRL6 (CABC Control 6) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|--|-----|-----|-------------|--------------|----|----|----|--------------|----|----|----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|--|--|--|--|--------------|--|--|--|-------------|----|----|----|----|--|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|---|---|---|---|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CCh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | DTH_UI [3:0] | | | | 03h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | DTH_UI [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the USER INTERFACE mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <table border="1"> <thead> <tr> <th colspan="4">DTH_UI [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>252</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>248</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>244</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>240</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>236</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>232</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>228</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>224</td></tr> </tbody> </table> | | | | DTH_UI [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 0 | 0 | 0 | 0 | 252 | 0 | 0 | 0 | 1 | 248 | 0 | 0 | 1 | 0 | 244 | 0 | 0 | 1 | 1 | 240 | 0 | 1 | 0 | 0 | 236 | 0 | 1 | 0 | 1 | 232 | 0 | 1 | 1 | 0 | 228 | 0 | 1 | 1 | 1 | 224 | <table border="1"> <thead> <tr> <th colspan="4">DTH_UI [3:0]</th> <th>Description</th> </tr> <tr> <th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>220</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>216</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>212</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>208</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>204</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>200</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>196</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>192</td></tr> </tbody> </table> | | | | DTH_UI [3:0] | | | | Description | D3 | D2 | D1 | D0 | | 1 | 0 | 0 | 0 | 220 | 1 | 0 | 0 | 1 | 216 | 1 | 0 | 1 | 0 | 212 | 1 | 0 | 1 | 1 | 208 | 1 | 1 | 0 | 0 | 204 | 1 | 1 | 0 | 1 | 200 | 1 | 1 | 1 | 0 | 196 | 1 | 1 | 1 | 1 | 192 |
| DTH_UI [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 252 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 248 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 244 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 240 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 236 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 232 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 228 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 224 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DTH_UI [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 216 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 212 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 208 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 204 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 196 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 192 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.24. CABC Control 7 (CDh)

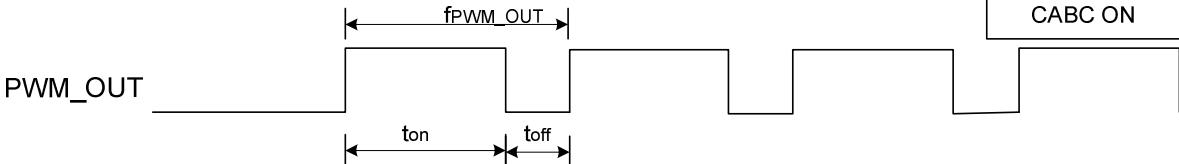
| CDh | CABCCTRL7 (CABC Control 7) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-------------|----------|----|---------------|----|----|----|-----------------|----|----|-----|-------------------------------|--------------|--|-------------|---|-----|---|-----|--|-----|----------|-----|---|---|---------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CDh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | DIM_MOV [2:0] | | | 0 | DIM_STILL [2:0] | | | 43h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | DIM_STILL [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Still mode. DIM_MOV [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Still mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th colspan="3">DIM_MOV [2:0]/DIM_STILL [2:0]</th> <th rowspan="2">Description</th> </tr> <tr> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 frames</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>4 frames</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>8 frames</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>16 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>32 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>64 frames</td> </tr> </tbody> </table> <p>X = void</p> <p>Note: In the above picture, DIM1 [2:0] means DIM_MOV [2:0], DIM_STILL [2:0], and DIM_UI [2:0] are in different modes.</p> | | | | | | | | | | | | | DIM_MOV [2:0]/DIM_STILL [2:0] | | | Description | D2 | D1 | D0 | 0 | 0 | 0 | 1 frame | 0 | 0 | 1 | 1 frame | 0 | 1 | 0 | 2 frames | 0 | 1 | 1 | 4 frames | 1 | 0 | 0 | 8 frames | 1 | 0 | 1 | 16 frames | 1 | 1 | 0 | 32 frames | 1 | 1 | 1 | 64 frames |
| DIM_MOV [2:0]/DIM_STILL [2:0] | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 frame | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 frame | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 8 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 16 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 32 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 64 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.25. CABC Control 8 (CEh)

| CEh | CABCCTRL8 (CABC Control 8) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|----------------------------|-----|-------------|----------|---------------|----|----|----|----|--------------|----|----|-----|-------------------------------|--|--|-------------|----|----|----|---|---|---|---------|---|---|---|---------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CEh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | DIM_MIN [3:0] | | | | 0 | DIM_UI [2:0] | | | 02h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIM_UI [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the UI mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <thead> <tr> <th colspan="3">DIM_MOV [2:0]/DIM_STILL [2:0]</th> <th rowspan="2">Description</th> </tr> <tr> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 frames</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>4 frames</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>8 frames</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>16 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>32 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>64 frames</td> </tr> </tbody> </table> <p>The graph illustrates the brightness transition over time. It starts at a baseline labeled 'Brightness=A'. A vertical double-headed arrow indicates the range of the brightness change, labeled 'DIM2[3:0]'. The curve rises during a period labeled 'Transition time' to a peak labeled 'Brightness=B'. From 'Brightness=B', the curve falls during another 'Transition time' to a lower level labeled 'Brightness=C'. A vertical double-headed arrow from 'Brightness=B' to 'Brightness=C' is labeled 'DIM1[2:0]'. The horizontal axis is labeled 'Time'.</p> | | | | | | | | | | | | | | DIM_MOV [2:0]/DIM_STILL [2:0] | | | Description | D2 | D1 | D0 | 0 | 0 | 0 | 1 frame | 0 | 0 | 1 | 1 frame | 0 | 1 | 0 | 2 frames | 0 | 1 | 1 | 4 frames | 1 | 0 | 0 | 8 frames | 1 | 0 | 1 | 16 frames | 1 | 1 | 0 | 32 frames | 1 | 1 | 1 | 64 frames |
| DIM_MOV [2:0]/DIM_STILL [2:0] | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 frame | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 frame | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 2 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 8 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 16 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 32 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 64 frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIM_MIN [3:0]: The parameter is used to set the limitation of the minimum brightness change. If the parameter is larger than the difference between the target brightness and the current brightness, then the brightness will not be changed. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Notes: <ol style="list-style-type: none"> In the above picture, DIM1 [2:0] means DIM_MOV [2:0], DIM_STILL [2:0], and DIM_UI [2:0] are in different modes. In the above picture, DIM2 [3:0] means DIM_MIN [3:0]. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Register Availability | Status | | Availability |
|-----------------------|---|-----|--------------|
| | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | |
| | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | |
| | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | |
| | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | |
| | Sleep IN | Yes | |

5.3.26. CABC Control 9 (CFh)

| CFh | CABCCTRL9 (CABC Control 9) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|---------------|-----|----------|---------------|----|----|-----------------------|----|----|----|----|-----|--|-----------------------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|---|---|---|---|---|-----------|---|---|---|---|---|---|---|---|-----------|---|---|---|---|---|---|---|---|-----------|---|---|---|---|---|---|---|---|-----------|---|---|---|---|---|---|---|---|-----------|---|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---------|---|---|---|---|---|---|---|---|----------|---|---|---|---|---|---|---|---|----------|---|---|---|---|---|---|---|---|----------|---|---|---|---|---|---|---|---|----------|--|--|--|--|--|--|--|--|--|
| | DCX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | CFh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | PWM_DIV [7:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | PWM_DIV [7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period can be calculated using the equation below: $f_{\text{PWM_OUT}} = \frac{18\text{MHz}}{(\text{PWM_DIV}[7:0]+1) \times 255}$ <table border="1"> <thead> <tr> <th colspan="8">PWM_DIV [7:0]</th> <th rowspan="2">$f_{\text{PWM_OUT}}$</th> </tr> <tr> <th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70.58 KHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>35.29 KHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>23.53 KHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>17.64 KHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>14.11 KHz</td></tr> <tr><td colspan="8">:</td><td>:</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>280.0Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>279.0 Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>277.9 Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>276.8 Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>275.8 Hz</td></tr> </tbody> </table>  <p>X = void</p> <p>Note: The output frequency tolerance of the internal frequency divider in the CABC is ±10%.</p> | PWM_DIV [7:0] | | | | | | | | | | | | | $f_{\text{PWM_OUT}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 70.58 KHz | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 35.29 KHz | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 23.53 KHz | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 17.64 KHz | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 14.11 KHz | : | | | | | | | | : | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 280.0Hz | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 279.0 Hz | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 277.9 Hz | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 276.8 Hz | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 275.8 Hz | | | | | | | | | |
| PWM_DIV [7:0] | | | | | | | | $f_{\text{PWM_OUT}}$ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 70.58 KHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 35.29 KHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 23.53 KHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 17.64 KHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 14.11 KHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | | | | | | | | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 280.0Hz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 279.0 Hz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 277.9 Hz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 276.8 Hz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 275.8 Hz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr><td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.27. NV Memory Write (D0h)

| D0h | | NVMWR (NV Memory Write) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-------------------------|-----|------------|----------------|----------|----|----|--------------------------------|----|----|----|-----|-----|---------------|----------------|--|-----|---|-----|---|-----|--|--------------------------------|----------|-----|--|--|--|--|--|--|--|-----------------|-----|-----|--|--|--|--|--|--|--|-----------------|-----|-----|--|--|--|--|--|--|--|-----------------|-----|----------|--|--|--|--|--|--|--|----------------------|-----|---|---|---|------------|--|--|--|--|------------------|-----|---|---|---|------------|--|--|--|--|------------------|-----|-----|-----|----|----|---|---|---|---|--------------------|-----|---|---|---|---|-------------|----------|--|--|----------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | PGM_ADR [7:0] | | | | | | | | | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | PGM_DATA [7:0] | | | | | | | | | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | <p>This command is used to program the NV memory data. After a successful OTP operation, the information of PGM_DATA [7:0] will be programmed to the NV memory.</p> <p>PGM_ADR [7:0]: The select bits of ID1, ID2, ID3, VMF [6:0], VRH1, VRH2, BT and MADCTL programming.</p> <p>PGM_DATA [7:0]: The programmed data.</p> <table border="1"> <thead> <tr> <th>PGM_ADR [7:0]</th> <th colspan="8">PGM_DATA [7:0]</th> <th>Programmed NV Memory Selection</th> </tr> </thead> <tbody> <tr> <td>03h</td> <td colspan="8">ID1</td> <td>ID1 programming</td> </tr> <tr> <td>07h</td> <td colspan="8">ID2</td> <td>ID2 programming</td> </tr> <tr> <td>0Bh</td> <td colspan="8">ID3</td> <td>ID3 programming</td> </tr> <tr> <td>0Fh</td> <td colspan="8">VMF[7:0]</td> <td>VMF[6:0] programming</td> </tr> <tr> <td>16h</td> <td>0</td><td>0</td><td>0</td> <td colspan="5">VRH1 [4:0]</td> <td>VRH1 programming</td> </tr> <tr> <td>17h</td> <td>0</td><td>0</td><td>0</td> <td colspan="5">VRH2 [4:0]</td> <td>VRH2 programming</td> </tr> <tr> <td>19h</td> <td>BGR</td><td>REV</td><td>MX</td> <td>MY</td> <td>0</td><td>0</td><td>0</td><td>0</td> <td>MADCTL programming</td> </tr> <tr> <td>1Ah</td> <td>0</td><td>0</td><td>0</td> <td>0</td> <td>BT_FROM_OTP</td> <td colspan="3">BT [2:0]</td> <td>BT programming</td> </tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | | PGM_ADR [7:0] | PGM_DATA [7:0] | | | | | | | | Programmed NV Memory Selection | 03h | ID1 | | | | | | | | ID1 programming | 07h | ID2 | | | | | | | | ID2 programming | 0Bh | ID3 | | | | | | | | ID3 programming | 0Fh | VMF[7:0] | | | | | | | | VMF[6:0] programming | 16h | 0 | 0 | 0 | VRH1 [4:0] | | | | | VRH1 programming | 17h | 0 | 0 | 0 | VRH2 [4:0] | | | | | VRH2 programming | 19h | BGR | REV | MX | MY | 0 | 0 | 0 | 0 | MADCTL programming | 1Ah | 0 | 0 | 0 | 0 | BT_FROM_OTP | BT [2:0] | | | BT programming |
| PGM_ADR [7:0] | PGM_DATA [7:0] | | | | | | | | Programmed NV Memory Selection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03h | ID1 | | | | | | | | ID1 programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07h | ID2 | | | | | | | | ID2 programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Bh | ID3 | | | | | | | | ID3 programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Fh | VMF[7:0] | | | | | | | | VMF[6:0] programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16h | 0 | 0 | 0 | VRH1 [4:0] | | | | | VRH1 programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 17h | 0 | 0 | 0 | VRH2 [4:0] | | | | | VRH2 programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 19h | BGR | REV | MX | MY | 0 | 0 | 0 | 0 | MADCTL programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1Ah | 0 | 0 | 0 | 0 | BT_FROM_OTP | BT [2:0] | | | BT programming | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.28. NV Memory Protection Key (D1h)

| D1h | | NVMPKEY (NV Memory Protection Key) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------------------|-----|----------|-------------|----|----|----|----|----|----|----|-----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | KEY [23:16] | | | | | | | | | 55h | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | KEY [15:8] | | | | | | | | | AAh | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | KEY [7:0] | | | | | | | | | 66h | | | | | | | | | | | | |
| Description | <p>KEY [23:0]: NV memory programming protection key. When writing OTP data to D0h, this register must be set to 0x55AA66h to enable the OTP programming. If the D1h register is not written with 0x55AA66h, then the NV memory programming will be aborted.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.29. NV Memory Status Read (D2h)

| D2h | 13x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|--------------------|---------------|----|----|----|---------------|----|----|----|-----|---|--------------|--|-----|---|-----|---|-----|--|---------------|----------|-----|---|---|-------------------|---|---|---|---|--------------------|---|---|---|---|--------------------|---|---|---|---|--------------------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | ID2_CNT [3:0] | | | | ID1_CNT [3:0] | | | | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | ↑ | 1 | XX | VMF_CNT [3:0] | | | | ID3_CNT [3:0] | | | | 00h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description | PGM_CNT [1:0]: NV memory program record. The bits will increase “+1” automatically after writing NV_VMF [5:0] to the NV memory. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="4">ID1_CNT [3:0]/ID2_CNT [3:0]/ID3_CNT [3:0]/ VMF_CNT [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>No Programmed</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>Programmed 1 time</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>Programmed 2 times</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>Programmed 3 times</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>Programmed 4 times</td></tr> </tbody> </table> | | | | | | | | | | | | | ID1_CNT [3:0]/ID2_CNT [3:0]/ID3_CNT [3:0]/ VMF_CNT [3:0] | | | | Description | 0 | 0 | 0 | 0 | No Programmed | 0 | 0 | 0 | 1 | Programmed 1 time | 0 | 0 | 1 | 1 | Programmed 2 times | 0 | 1 | 1 | 1 | Programmed 3 times | 1 | 1 | 1 | 1 | Programmed 4 times |
| ID1_CNT [3:0]/ID2_CNT [3:0]/ID3_CNT [3:0]/ VMF_CNT [3:0] | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | No Programmed | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | Programmed 1 time | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | Programmed 2 times | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Programmed 3 times | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | Programmed 4 times | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | | | | | | | | | | | | | | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.30. Read ID4 (D3h)

| D3h | RDID4 (Read ID4) | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | ↑ | 1 | XX | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 94h | | | | | | | | | | | | | |
| 4 th Parameter | 1 | ↑ | 1 | XX | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 88h | | | | | | | | | | | | | |
| Description | This command is used to read the IC device code. The 1 st parameter shows the dummy read period. The 2 nd and 3 rd parameter mean the IC model name. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.31. Adjust Control 1 (D7h)

| D7h | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | |
|---|---|-------------|-----|----------|----|----|--------------------|--------------------------|----|----|----|----|-----|--------------------------|--------------|--|-----|---|--------|---|-----|--|-----|----------|----------|---|---|----------|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D7h | | | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | Chopper_op_clk_opt | Chopper_op_clk_sel [1:0] | 0 | 1 | 1 | 1 | 03h | | | | | | | | | | | | | | | |
| Description | <p>Chopper_op_clk_opt: Source Op-amp chopper function option (0 or 1) 0 (default) = refer to the table of Chopper_sel [1:0] in F2h 1 = refer to the table of Chopper_op_clk_sel below</p> <p>Chopper_op_clk_sel[1:0]: Source Op-amp chopper function option</p> <table border="1"> <thead> <tr> <th colspan="2">Chopper_op_clk_sel [1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>op_clk</td> </tr> <tr> <td>1</td><td>0</td><td>op_clk/2</td> </tr> <tr> <td>0</td><td>1</td><td>op_clk/4</td> </tr> <tr> <td>1</td><td>1</td><td>op_clk/8</td> </tr> </tbody> </table> <p>X = void</p> | | | | | | | | | | | | | Chopper_op_clk_sel [1:0] | | Description | 0 | 0 | op_clk | 1 | 0 | op_clk/2 | 0 | 1 | op_clk/4 | 1 | 1 | op_clk/8 |
| Chopper_op_clk_sel [1:0] | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | op_clk | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | op_clk/2 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | op_clk/4 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | op_clk/8 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes | | | |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.32. PGAMCTRL (Positive Gamma Control) (E0h)

| E0h | | PGAMCTRL (Positive Gamma Control) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----------------------------------|-----|----------|------------|------------|------------|------------|------------|------------|----|-----|-----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP0 [3:0] | | | | 0Fh | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VP1 [5:0] | | | | | | 1Fh | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VP2 [5:0] | | | | | | 1Ch | | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP4 [3:0] | | | | 0Bh | | | | | | | | | | | | | |
| 5 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VP6 [4:0] | | | | 0Eh | | | | | | | | | | | | | | |
| 6 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP13 [3:0] | | | | 09h | | | | | | | | | | | | | |
| 7 th Parameter | 1 | 1 | ↑ | XX | 0 | VP20 [6:0] | | | | | | | | 48h | | | | | | | | | | | | |
| 8 th Parameter | 1 | 1 | ↑ | XX | VP36 [3:0] | | | | | VP27 [3:0] | | | | 99h | | | | | | | | | | | | |
| 9 th Parameter | 1 | 1 | ↑ | XX | 0 | VP43 [6:0] | | | | | | | | 38h | | | | | | | | | | | | |
| 10 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP50 [3:0] | | | | 0Ah | | | | | | | | | | | | | |
| 11 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VP57 [4:0] | | | | 14h | | | | | | | | | | | | | | |
| 12 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP59 [3:0] | | | | 06h | | | | | | | | | | | | | |
| 13 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VP61 [5:0] | | | | | | 11h | | | | | | | | | | | | | |
| 14 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VP62 [5:0] | | | | | | 09h | | | | | | | | | | | | | |
| 15 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP63 [3:0] | | | | 00h | | | | | | | | | | | | | |
| Description | Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.33. NGAMCTRL (Negative Gamma Control) (E1h)

| E1h | | NGAMCTRL (Negative Gamma Control) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----------------------------------|-----|----------|------------|------------|------------|------------|------------|------------|----|-----|-----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN0 [3:0] | | | | 0Fh | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VN1 [5:0] | | | | | | 36h | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VN2 [5:0] | | | | | | 2Eh | | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN4 [3:0] | | | | 09h | | | | | | | | | | | | | |
| 5 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RVN6 [4:0] | | | | 0Ah | | | | | | | | | | | | | | |
| 6 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN13 [3:0] | | | | 04h | | | | | | | | | | | | | |
| 7 th Parameter | 1 | 1 | ↑ | XX | 0 | VN20 [6:0] | | | | | | | | 46h | | | | | | | | | | | | |
| 8 th Parameter | 1 | 1 | ↑ | XX | VN36 [3:0] | | | | | VN27 [3:0] | | | | 66h | | | | | | | | | | | | |
| 9 th Parameter | 1 | 1 | ↑ | XX | 0 | VN43 [6:0] | | | | | | | | 37h | | | | | | | | | | | | |
| 10 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN50 [3:0] | | | | 06h | | | | | | | | | | | | | |
| 11 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VN57 [4:0] | | | | 10h | | | | | | | | | | | | | | |
| 12 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN59 [3:0] | | | | 04h | | | | | | | | | | | | | |
| 13 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VN61 [5:0] | | | | | | 24h | | | | | | | | | | | | | |
| 14 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VN62 [5:0] | | | | | | 20h | | | | | | | | | | | | | |
| 15 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN63 [3:0] | | | | 00h | | | | | | | | | | | | | |
| Description | Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.34. Digital Gamma Control 1 (E2h)

| E2h | | DGAMCTRL (Digital Gamma Control 1) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|------------------------------------|-----|-----|-------------|----|----|----|-------------|----|----|----|-----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | RCA0 [3:0] | | | | BCA0 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | RCA1 [3:0] | | | | BCA1 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | RCA2 [3:0] | | | | BCA2 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | RCA3 [3:0] | | | | BCA3 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 5 th Parameter | 1 | 1 | ↑ | XX | RCA4 [3:0] | | | | BCA4 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 6 th Parameter | 1 | 1 | ↑ | XX | RCA5 [3:0] | | | | BCA5 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 7 th Parameter | 1 | 1 | ↑ | XX | RCA6 [3:0] | | | | BCA6 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 8 th Parameter | 1 | 1 | ↑ | XX | RCA7 [3:0] | | | | BCA7 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 9 th Parameter | 1 | 1 | ↑ | XX | RCA8 [3:0] | | | | BCA8 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 10 th Parameter | 1 | 1 | ↑ | XX | RCA9 [3:0] | | | | BCA9 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 11 th Parameter | 1 | 1 | ↑ | XX | RCA10 [3:0] | | | | BCA10 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 12 th Parameter | 1 | 1 | ↑ | XX | RCA11 [3:0] | | | | BCA11 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 13 th Parameter | 1 | 1 | ↑ | XX | RCA12 [3:0] | | | | BCA12 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 14 th Parameter | 1 | 1 | ↑ | XX | RCA13 [3:0] | | | | BCA13 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 15 th Parameter | 1 | 1 | ↑ | XX | RCA14 [3:0] | | | | BCA14 [3:0] | | | | 00h | | | | | | | | | | | | | |
| 16 th Parameter | 1 | 1 | ↑ | XX | RCA15 [3:0] | | | | BCA15 [3:0] | | | | 00h | | | | | | | | | | | | | |
| Description | RCA0 [3:0] ~ RCA15 [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCA0 [3:0] ~ BCA15 [3:0]: Gamma Macro-adjustment registers for blue gamma curve. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.35. Digital Gamma Control 2 (E3h)

| E3h | DGAMCTRL (Digital Gamma Control 2) | | | | | | | | | | | | |
|----------------------------|------------------------------------|-----|-----|----------|-------------|----|----|----|-------------|----|----|----|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3h |
| 1 st Parameter | 1 | 1 | ↑ | XX | RFA0 [3:0] | | | | BFA0 [3:0] | | | | 00h |
| 2 nd Parameter | 1 | 1 | ↑ | XX | RFA1 [3:0] | | | | BFA1 [3:0] | | | | 00h |
| 3 rd Parameter | 1 | 1 | ↑ | XX | RFA2 [3:0] | | | | BFA2 [3:0] | | | | 00h |
| 4 th Parameter | 1 | 1 | ↑ | XX | RFA3 [3:0] | | | | BFA3 [3:0] | | | | 00h |
| 5 th Parameter | 1 | 1 | ↑ | XX | RFA4 [3:0] | | | | BFA4 [3:0] | | | | 00h |
| 6 th Parameter | 1 | 1 | ↑ | XX | RFA5 [3:0] | | | | BFA5 [3:0] | | | | 00h |
| 7 th Parameter | 1 | 1 | ↑ | XX | RFA6 [3:0] | | | | BFA6 [3:0] | | | | 00h |
| 8 th Parameter | 1 | 1 | ↑ | XX | RFA7 [3:0] | | | | BFA7 [3:0] | | | | 00h |
| 9 th Parameter | 1 | 1 | ↑ | XX | RFA8 [3:0] | | | | BFA8 [3:0] | | | | 00h |
| 10 th Parameter | 1 | 1 | ↑ | XX | RFA9 [3:0] | | | | BFA9 [3:0] | | | | 00h |
| 11 th Parameter | 1 | 1 | ↑ | XX | RFA10 [3:0] | | | | BFA10 [3:0] | | | | 00h |
| 12 th Parameter | 1 | 1 | ↑ | XX | RFA11 [3:0] | | | | BFA11 [3:0] | | | | 00h |
| 13 th Parameter | 1 | 1 | ↑ | XX | RFA12 [3:0] | | | | BFA12 [3:0] | | | | 00h |
| 14 th Parameter | 1 | 1 | ↑ | XX | RFA13 [3:0] | | | | BFA13 [3:0] | | | | 00h |
| 15 th Parameter | 1 | 1 | ↑ | XX | RFA14 [3:0] | | | | BFA14 [3:0] | | | | 00h |
| 16 th Parameter | 1 | 1 | ↑ | XX | RFA15 [3:0] | | | | BFA15 [3:0] | | | | 00h |
| 17 th Parameter | 1 | 1 | ↑ | XX | RFA16 [3:0] | | | | BFA16 [3:0] | | | | 00h |
| 18 th Parameter | 1 | 1 | ↑ | XX | RFA17 [3:0] | | | | BFA17 [3:0] | | | | 00h |
| 19 th Parameter | 1 | 1 | ↑ | XX | RFA18 [3:0] | | | | BFA18 [3:0] | | | | 00h |
| 20 th Parameter | 1 | 1 | ↑ | XX | RFA19 [3:0] | | | | BFA19 [3:0] | | | | 00h |
| 21 th Parameter | 1 | 1 | ↑ | XX | RFA20 [3:0] | | | | BFA20 [3:0] | | | | 00h |
| 22 th Parameter | 1 | 1 | ↑ | XX | RFA21 [3:0] | | | | BFA21 [3:0] | | | | 00h |
| 23 th Parameter | 1 | 1 | ↑ | XX | RFA22 [3:0] | | | | BFA22 [3:0] | | | | 00h |
| 24 th Parameter | 1 | 1 | ↑ | XX | RFA23 [3:0] | | | | BFA23 [3:0] | | | | 00h |
| 25 th Parameter | 1 | 1 | ↑ | XX | RFA24 [3:0] | | | | BFA24 [3:0] | | | | 00h |
| 26 th Parameter | 1 | 1 | ↑ | XX | RFA25 [3:0] | | | | BFA25 [3:0] | | | | 00h |
| 27 th Parameter | 1 | 1 | ↑ | XX | RFA26 [3:0] | | | | BFA26 [3:0] | | | | 00h |
| 28 th Parameter | 1 | 1 | ↑ | XX | RFA27 [3:0] | | | | BFA27 [3:0] | | | | 00h |
| 29 th Parameter | 1 | 1 | ↑ | XX | RFA28 [3:0] | | | | BFA28 [3:0] | | | | 00h |
| 30 th Parameter | 1 | 1 | ↑ | XX | RFA29 [3:0] | | | | BFA29 [3:0] | | | | 00h |
| 31 th Parameter | 1 | 1 | ↑ | XX | RFA30 [3:0] | | | | BFA30 [3:0] | | | | 00h |
| 32 th Parameter | 1 | 1 | ↑ | XX | RFA31 [3:0] | | | | BFA31 [3:0] | | | | 00h |

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| | | | | | | | |
|----------------------------|---|---|---|----|-------------|-------------|-----|
| 33 th Parameter | 1 | 1 | ↑ | XX | RFA32 [3:0] | BFA32 [3:0] | 00h |
| 34 th Parameter | 1 | 1 | ↑ | XX | RFA33 [3:0] | BFA33 [3:0] | 00h |
| 35 th Parameter | 1 | 1 | ↑ | XX | RFA34 [3:0] | BFA34 [3:0] | 00h |
| 36 th Parameter | 1 | 1 | ↑ | XX | RFA35 [3:0] | BFA35 [3:0] | 00h |
| 37 th Parameter | 1 | 1 | ↑ | XX | RFA36 [3:0] | BFA36 [3:0] | 00h |
| 38 th Parameter | 1 | 1 | ↑ | XX | RFA37 [3:0] | BFA37 [3:0] | 00h |
| 39 th Parameter | 1 | 1 | ↑ | XX | RFA38 [3:0] | BFA38 [3:0] | 00h |
| 40 th Parameter | 1 | 1 | ↑ | XX | RFA39 [3:0] | BFA39 [3:0] | 00h |
| 41 th Parameter | 1 | 1 | ↑ | XX | RFA40 [3:0] | BFA40 [3:0] | 00h |
| 42 th Parameter | 1 | 1 | ↑ | XX | RFA41 [3:0] | BFA41 [3:0] | 00h |
| 43 th Parameter | 1 | 1 | ↑ | XX | RFA42 [3:0] | BFA42 [3:0] | 00h |
| 44 th Parameter | 1 | 1 | ↑ | XX | RFA43 [3:0] | BFA43 [3:0] | 00h |
| 45 th Parameter | 1 | 1 | ↑ | XX | RFA44 [3:0] | BFA44 [3:0] | 00h |
| 46 th Parameter | 1 | 1 | ↑ | XX | RFA45 [3:0] | BFA45 [3:0] | 00h |
| 47 th Parameter | 1 | 1 | ↑ | XX | RFA46 [3:0] | BFA46 [3:0] | 00h |
| 48 th Parameter | 1 | 1 | ↑ | XX | RFA47 [3:0] | BFA47 [3:0] | 00h |
| 49 th Parameter | 1 | 1 | ↑ | XX | RFA48 [3:0] | BFA48 [3:0] | 00h |
| 50 th Parameter | 1 | 1 | ↑ | XX | RFA49 [3:0] | BFA49 [3:0] | 00h |
| 51 th Parameter | 1 | 1 | ↑ | XX | RFA50 [3:0] | BFA50 [3:0] | 00h |
| 52 th Parameter | 1 | 1 | ↑ | XX | RFA51 [3:0] | BFA51 [3:0] | 00h |
| 53 th Parameter | 1 | 1 | ↑ | XX | RFA52 [3:0] | BFA52 [3:0] | 00h |
| 54 th Parameter | 1 | 1 | ↑ | XX | RFA53 [3:0] | BFA53 [3:0] | 00h |
| 55 th Parameter | 1 | 1 | ↑ | XX | RFA54 [3:0] | BFA54 [3:0] | 00h |
| 56 th Parameter | 1 | 1 | ↑ | XX | RFA55 [3:0] | BFA55 [3:0] | 00h |
| 57 th Parameter | 1 | 1 | ↑ | XX | RFA56 [3:0] | BFA56 [3:0] | 00h |
| 58 th Parameter | 1 | 1 | ↑ | XX | RFA57 [3:0] | BFA57 [3:0] | 00h |
| 59 th Parameter | 1 | 1 | ↑ | XX | RFA58 [3:0] | BFA58 [3:0] | 00h |
| 60 th Parameter | 1 | 1 | ↑ | XX | RFA59 [3:0] | BFA59 [3:0] | 00h |
| 61 th Parameter | 1 | 1 | ↑ | XX | RFA60 [3:0] | BFA60 [3:0] | 00h |
| 62 th Parameter | 1 | 1 | ↑ | XX | RFA61 [3:0] | BFA61 [3:0] | 00h |
| 63 th Parameter | 1 | 1 | ↑ | XX | RFA62 [3:0] | BFA62 [3:0] | 00h |
| 64 th Paramete | 1 | 1 | ↑ | XX | RFA63 [3:0] | BFA63 [3:0] | 00h |
| Description | RFA0 [3:0] ~ RFA63 [3:0]: Gamma Micro-adjustment register for red gamma curve. BFA0 [3:0] ~ BFA63 [3:0]: Gamma Micro-adjustment register for blue gamma curve. X = void | | | | | | |
| Restriction | | | | | | | |

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| Register Availability | Status | Availability |
|-----------------------|---|--------------|
| | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| | Sleep IN | Yes |

5.3.36. Set Image Function (E9h)

| E9h | | SETIMAGE (Set Image Function) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-------------------------------|-----|-----|----------|----|----|----|----|----|----|----|-------|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9h | | | | | | | | | | | | |
| 1 st Parameter | | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | DB_EN | 00h | | | | | | | | | | | | |
| Description | DB_EN: Enable 24-bits Data Bus; users can use DB23~DB0 as 24-bits data input. X = void | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.37. Adjust Control 2 (F2h)

| F2h | Adjust Control 2 | | | | | | | | | | | | |
|----------------------------|------------------|-----|-----|----------|------------------|--------------|----|----|---------------|----|----|-------------------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2h |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Chopper_delay_opt | 58h |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | GSW_TG1[5:0] | | | | | | 0 | 04h |
| 3 rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |
| 4 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02h |
| 5 th Parameter | 1 | 1 | ↑ | XX | 0 | EQTI[2:0] | | | 0 | 0 | 1 | 0 | 22h |
| 6 th Parameter | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42h |
| 7 th Parameter | 1 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFh |
| 8 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah |
| 9 th Parameter | 1 | 1 | ↑ | XX | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90h |
| 10 th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | GSW_Mode[1:0] | | 0 | 0 | 14h |
| 11 th Parameter | 1 | 1 | ↑ | XX | Chopper_sel[1:0] | | 0 | 0 | 1 | 0 | 0 | 0 | 88h |

Chopper_delay_opt: Source Op-amp chopper function option.

| Chopper_delay_opt | Description |
|-------------------|------------------------|
| 0 | Original Chopper |
| 1 | Chopper delay one line |

Chopper_sel [1:0]: Source Op-amp chopper function option.

| Chopper_opt | Chopper_sel[1:0] | Description |
|-------------|------------------|---|
| 1 | 0 0 | Close chopper |
| 1 | 0 1 | 1 frame chopper |
| 1 | 1 0 | 2 frame chopper |
| 1 | 1 1 | 3 frame chopper |
| 0 | 0 0 | 1-line(1 frame chopper polarity change) |
| 0 | 0 1 | 2-line(1 frame chopper polarity change) |
| 0 | 1 0 | 1-line(2 frame chopper polarity change) |
| 0 | 1 1 | 2-line(2 frame chopper polarity change) |

Eqrti [2:0]: Source EQ internal timing adjustment. The timing can be adjusted from 0 to 7 time scales. (time scal: op_clk)

| Eqrti [2:0] | | | Description |
|-------------|---|---|---------------|
| 0 | 0 | 0 | 1 unit op_clk |
| 0 | 0 | 1 | 2 unit op_clk |
| 0 | 1 | 0 | 3 unit op_clk |
| 0 | 1 | 1 | 4 unit op_clk |
| 1 | 0 | 0 | 5 unit op_clk |
| 1 | 0 | 1 | 6 unit op_clk |
| 1 | 1 | 0 | 7 unit op_clk |
| 1 | 1 | 1 | 8 unit op_clk |

GSW_Mode[1:0]: Slope function setting.

| GSW_Mode[1:0] | | Description |
|---------------|---|--------------|
| 0 | 0 | Sharp slope |
| 0 | 1 | Normal slope |
| 1 | 0 | Gently slope |
| 1 | 1 | GSW off |

GSW_TG1[5:0]: Gate modulation timing control. The timing can be adjusted:

| Gsw_tg1[5:0] | | | | | | Description |
|--------------|---|---|---|---|---|------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 40 unit Osc_clk |
| 0 | 0 | 0 | 0 | 0 | 1 | 44 unit Osc_clk |
| 0 | 0 | 0 | 0 | 1 | 0 | 48 unit Osc_clk |
| 0 | 0 | 0 | 0 | 1 | 1 | 52 unit Osc_clk |
| 0 | 0 | 0 | 1 | 0 | 0 | 56 unit Osc_clk |
| 0 | 0 | 0 | 1 | 0 | 1 | 60 unit Osc_clk |
| 0 | 0 | 0 | 1 | 1 | 0 | 64 unit Osc_clk |
| 0 | 0 | 0 | 1 | 1 | 1 | 68 unit Osc_clk |
| 0 | 0 | 1 | 0 | 0 | 0 | 72 unit Osc_clk |
| 0 | 0 | 1 | 0 | 0 | 1 | 76 unit Osc_clk |
| 0 | 0 | 1 | 0 | 1 | 0 | 80 unit Osc_clk |
| 0 | 0 | 1 | 0 | 1 | 1 | 84 unit Osc_clk |
| 0 | 0 | 1 | 1 | 0 | 0 | 88 unit Osc_clk |
| 0 | 0 | 1 | 1 | 0 | 1 | 92 unit Osc_clk |
| 0 | 0 | 1 | 1 | 1 | 0 | 96 unit Osc_clk |
| 0 | 0 | 1 | 1 | 1 | 1 | 100 unit Osc_clk |
| 0 | 1 | 0 | 0 | 0 | 0 | 104 unit Osc_clk |
| 0 | 1 | 0 | 0 | 0 | 1 | 108 unit Osc_clk |
| 0 | 1 | 0 | 0 | 1 | 0 | 112 unit Osc_clk |

| | | | | | | |
|---|---|---|---|---|---|------------------|
| 0 | 1 | 0 | 0 | 1 | 1 | 116 unit Osc_clk |
| 0 | 1 | 0 | 1 | 0 | 0 | 120 unit Osc_clk |
| 0 | 1 | 0 | 1 | 0 | 1 | 124 unit Osc_clk |
| 0 | 1 | 0 | 1 | 1 | 0 | 128 unit Osc_clk |
| 0 | 1 | 0 | 1 | 1 | 1 | 132 unit Osc_clk |
| 0 | 1 | 1 | 0 | 0 | 0 | 136 unit Osc_clk |
| 0 | 1 | 1 | 0 | 0 | 1 | 140 unit Osc_clk |
| 0 | 1 | 1 | 0 | 1 | 0 | 144 unit Osc_clk |
| 0 | 1 | 1 | 0 | 1 | 1 | 148 unit Osc_clk |
| 0 | 1 | 1 | 1 | 0 | 0 | 152 unit Osc_clk |
| 0 | 1 | 1 | 1 | 0 | 1 | 156 unit Osc_clk |
| 0 | 1 | 1 | 1 | 1 | 0 | 160 unit Osc_clk |
| 0 | 1 | 1 | 1 | 1 | 1 | 164 unit Osc_clk |
| 1 | 0 | 0 | 0 | 0 | 0 | 168 unit Osc_clk |
| 1 | 0 | 0 | 0 | 0 | 1 | 172 unit Osc_clk |
| 1 | 0 | 0 | 0 | 1 | 0 | 176 unit Osc_clk |
| 1 | 0 | 0 | 0 | 1 | 1 | 180 unit Osc_clk |
| 1 | 0 | 0 | 1 | 0 | 0 | 184 unit Osc_clk |
| 1 | 0 | 0 | 1 | 0 | 1 | 188 unit Osc_clk |
| 1 | 0 | 0 | 1 | 1 | 0 | 192 unit Osc_clk |
| 1 | 0 | 0 | 1 | 1 | 1 | 196 unit Osc_clk |
| 1 | 0 | 1 | 0 | 0 | 0 | 200 unit Osc_clk |
| 1 | 0 | 1 | 0 | 0 | 1 | 204 unit Osc_clk |
| 1 | 0 | 1 | 0 | 1 | 0 | 208 unit Osc_clk |
| 1 | 0 | 1 | 0 | 1 | 1 | 212 unit Osc_clk |
| 1 | 0 | 1 | 1 | 0 | 0 | 216 unit Osc_clk |
| 1 | 0 | 1 | 1 | 0 | 1 | 220 unit Osc_clk |
| 1 | 0 | 1 | 1 | 1 | 0 | 224 unit Osc_clk |
| 1 | 0 | 1 | 1 | 1 | 1 | 228 unit Osc_clk |
| 1 | 1 | 0 | 0 | 0 | 0 | 232 unit Osc_clk |
| 1 | 1 | 0 | 0 | 0 | 1 | 236 unit Osc_clk |
| 1 | 1 | 0 | 0 | 1 | 0 | 240 unit Osc_clk |
| 1 | 1 | 0 | 0 | 1 | 1 | 244 unit Osc_clk |
| 1 | 1 | 0 | 1 | 0 | 0 | 248 unit Osc_clk |
| 1 | 1 | 0 | 1 | 0 | 1 | 252 unit Osc_clk |
| 1 | 1 | 0 | 1 | 1 | 0 | 256 unit Osc_clk |
| 1 | 1 | 0 | 1 | 1 | 1 | 260 unit Osc_clk |
| 1 | 1 | 1 | 0 | 0 | 0 | 264 unit Osc_clk |
| 1 | 1 | 1 | 0 | 0 | 1 | 268 unit Osc_clk |
| 1 | 1 | 1 | 0 | 1 | 0 | 272 unit Osc_clk |
| 1 | 1 | 1 | 0 | 1 | 1 | 276 unit Osc_clk |
| 1 | 1 | 1 | 1 | 0 | 0 | 280 unit Osc_clk |
| 1 | 1 | 1 | 1 | 0 | 1 | 284 unit Osc_clk |
| 1 | 1 | 1 | 1 | 1 | 0 | 288 unit Osc_clk |
| 1 | 1 | 1 | 1 | 1 | 1 | 292 unit Osc_clk |

| | X = void | | | | | | | | | | | | |
|---|---|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| Restriction | | | | | | | | | | | | | |
| Register Availability | <table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></tbody></table> | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | |

5.3.38. Adjust Control 3 (F7h)

| Adjust Control 3 | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|---------------|----|----|----|----|----|----|----|-----|-----|---------------|--------------|--|--|---|---|---|-----|--|-----|----------|-----|
| F7h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | F7h | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | A9h | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 51h | | | | | | | | | | | | |
| 3 rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 2Ch | | | | | | | | | | | | |
| 4 th Parameter | 1 | 1 | ↑ | XX | DSI_18_option | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 82h | | | | | | | | | | | | |
| Description | DSI_18_option: DSI 18bit option | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>DSI_18_option</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>DSI write DCS command, use stream packet RGB 666</td></tr> <tr> <td>1</td><td>DSI write DCS command, use loose packet RGB 666</td></tr> </tbody> </table> | | | | | | | | | | | | | | DSI_18_option | Description | 0 | DSI write DCS command, use stream packet RGB 666 | 1 | DSI write DCS command, use loose packet RGB 666 | | | | | | |
| DSI_18_option | Description | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | DSI write DCS command, use stream packet RGB 666 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | DSI write DCS command, use loose packet RGB 666 | | | | | | | | | | | | | | | | | | | | | | | | | |
| X = void | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.39. Adjust Control 4 (F8h)

| Adjust Control 4 | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|----|----|----------------|---------------|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| F8h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8h | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 3-Gamma_Enable | Dither_Enable | 04h | | | | | | | | | | | | | |
| Description | <p>3-Gamma_Enable: 3-Gamma function enable.</p> <p>Dither_Enable: Dither function enable.</p> <p>X = void</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.40. Adjust Control 5(F9h)

| Adjust Control 5 | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|-----|-----|----------|----|----|----|----|-------------|----|----|----|-----|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| F9h | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9h | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | Chopper_opt | 0 | 0 | 0 | 00h | | | | | | | | | | | | |
| Description | Chopper_opt: Source Op-amp chopper function option. Please refer to F2h (Section 5.3.37) for more information. X = void | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.41. SPI Read Command Setting (FBh)

| FBh | Read EXTC command is SPI mode | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----|-----|----------|-------------|----|----|----|---------------|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FBh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | SPI_READ_EN | 0 | 0 | 0 | SPI_CNT [3:0] | | | | 00h | | | | | | | | | | | | | |
| Description | SPI_READ_EN: SPI read enable (see Note) SPI_CNT [3:0]: SPI read parameter number (see Note) | | | | | | | | | | | | | | | | | | | | | | | | | |
| | <pre> graph TD START([START]) --> READ[Read the Extended command in SPI operation mode Example: read Register XXh, Nth parameter] READ --> SET_FB[Set Register FBh 1. Enable SPI read (SPI_READ_EN=1) 2. Nth parameter to be read out (SPI_CNT[3:0])] SET_FB --> SET_XX[Set Register XXh command And read out the Nth Parameter] SET_XX --> END([END SPI read]) END --> SET_DISABLE[Set Register FBh Disable SPI read (SPI_READ_EN=0) (Enable SPI write)] </pre> <p>The flowchart illustrates the process of reading an extended command via SPI. It begins with a START state, followed by reading the extended command in SPI mode (e.g., reading Register XXh, Nth parameter). This leads to setting Register FBh with two specific configurations: enabling SPI read (SPI_READ_EN=1) and specifying the Nth parameter to be read out (SPI_CNT[3:0]). Subsequently, the Register XXh command is set, and the Nth parameter is read out. Finally, the process concludes with an END SPI read state, followed by disabling SPI read (SPI_READ_EN=0) and enabling SPI write.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table> | | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

5.3.42. Adjust Control 6 (FCh)

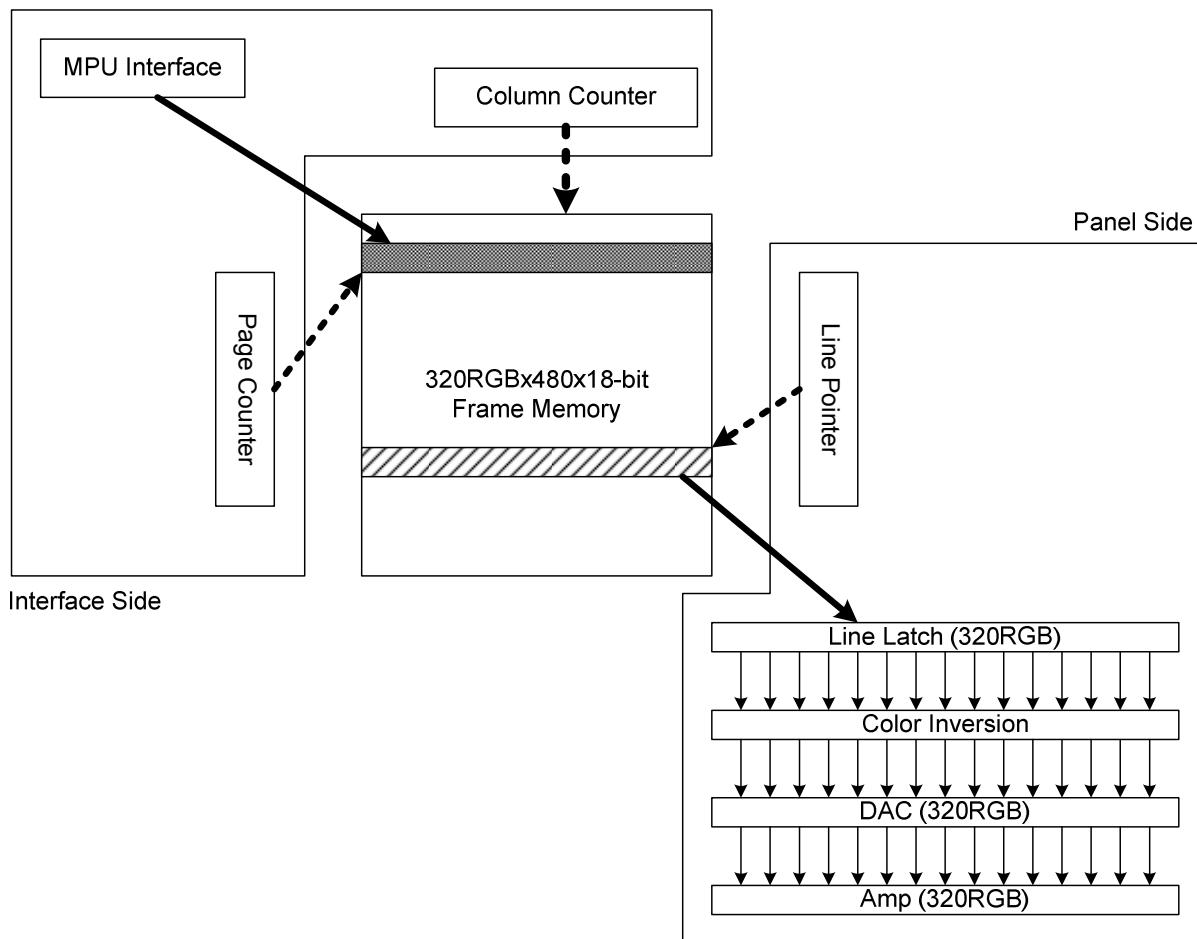
| FCh | Adjust Control 6 | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-----|----------|----|----------------|----|------------|----|----|----|----|-----|--|--------|--------------|--|-----|---|-----|---|-----|--|-----|----------|-----|
| | D/CX | RDX | WRX | D [23:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX | | | | | | | | | | | | | |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FCh | | | | | | | | | | | | | |
| 1 st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | | | | | | | | | | | | | |
| 2 nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | NOWI [4:0] | | | | | 05h | | | | | | | | | | | | | |
| Description | NOWI [4:0]:Gate driver non-overlap timing control. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | NOWI [4:0] | | | | | Description | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 0 | 0 | 1 | 1 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 0 | 1 | 0 | 2 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 0 | 1 | 1 | 3 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | 0 | 0 | 4 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | 0 | 1 | 5 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | 1 | 0 | 6 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | 1 | 1 | 7 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | 0 | 0 | 8 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | 0 | 1 | 9 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | 1 | 0 | 10 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | 1 | 1 | 11 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | 0 | 0 | 12 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | 0 | 1 | 13 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | 1 | 0 | 14 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | 1 | 1 | 15 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| | 1 | 0 | 0 | 0 | 0 | 16 unit op_clk | | | | | | | | | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | <table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table> | | | | | | | | | | | | | Status | Availability | Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | Sleep IN | Yes |
| Status | Availability | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |
| Sleep IN | Yes | | | | | | | | | | | | | | | | | | | | | | | | | |

6. Display Data RAM

6.1. Configuration

The 320 x 480 x 18-bit graphic type static RAM has a 345,600-byte memory allowing the storage of a 320 (RGB) x 480 image with the 18-bit resolution.

Panel Read and Interface Read (or Interface Write) can occur simultaneously with the Frame Memory. This process will not cause any visible effects on the display.

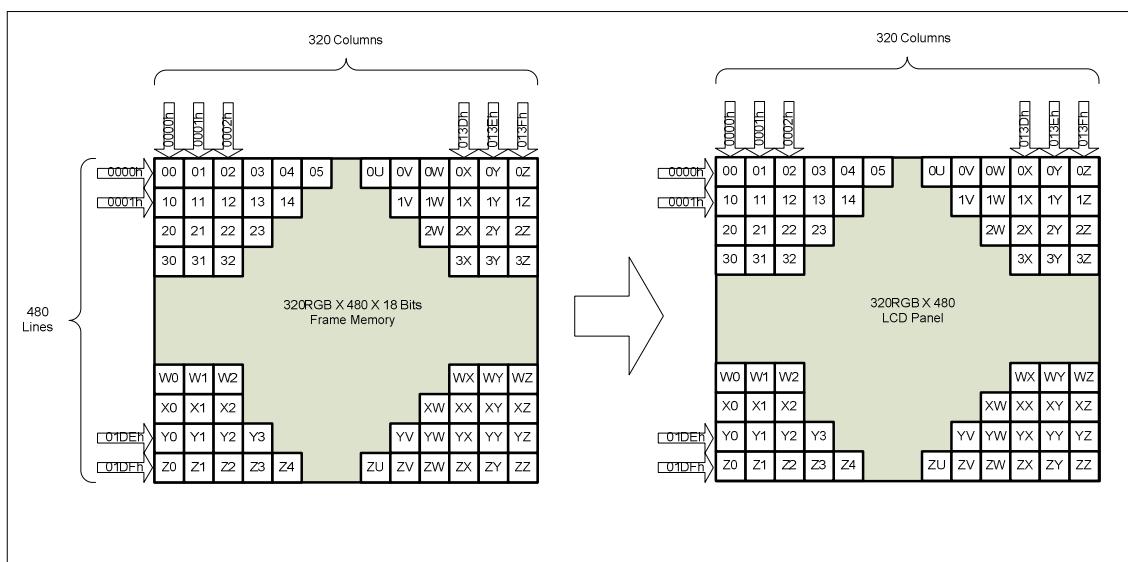


6.2. Memory to Display Address Mapping

6.2.1. Fully Display

Example: 320 (RGB) x 480 dot display mode

- (1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.
- (2) NORON (Normal Display Mode On) instruction (R13h).
- (3) SC = 0 x 0000h, EC = 0 x 013Fh (R2Ah) and SP = 0 x 0000h, EP = 0 x 01DFh (R2Bh), ML = 0.



6.2.2. Vertical Scrolling Display

The Vertical Scrolling Mode is determined by Vertical Scrolling Definition (33h) and Vertical Scrolling Start Address (37h) commands. The Vertical Scroll Mode function is explained by the examples of (TFA + VSA + BFA) = 480 in Figure 128.

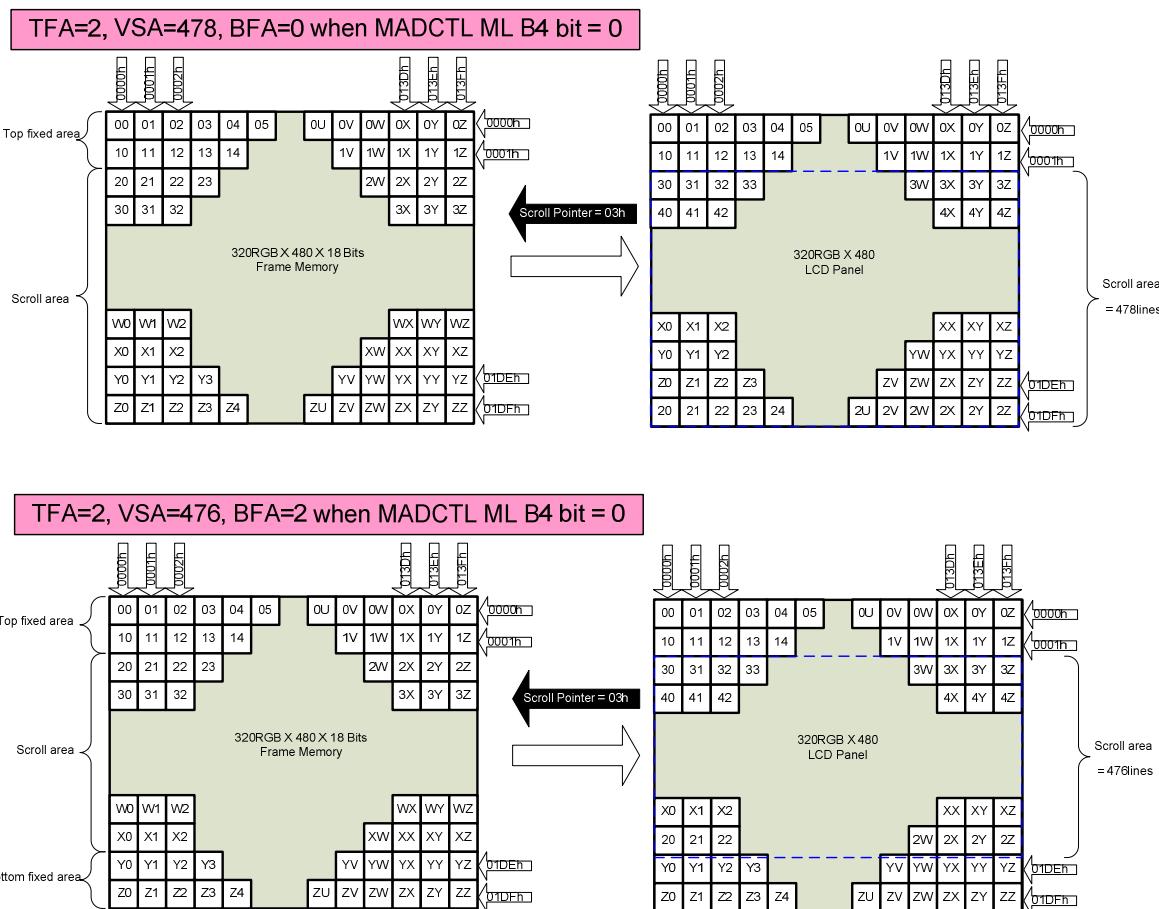


Figure 128: Vertical Scrolling Mode Function

Note: When Vertical Scrolling Definition Parameters ($TFA + VSA + BFA \neq 480$), the Scrolling Mode is undefined.

6.2.3. Vertical Scrolling 320 (RGB) (H) x 480 (V) Example

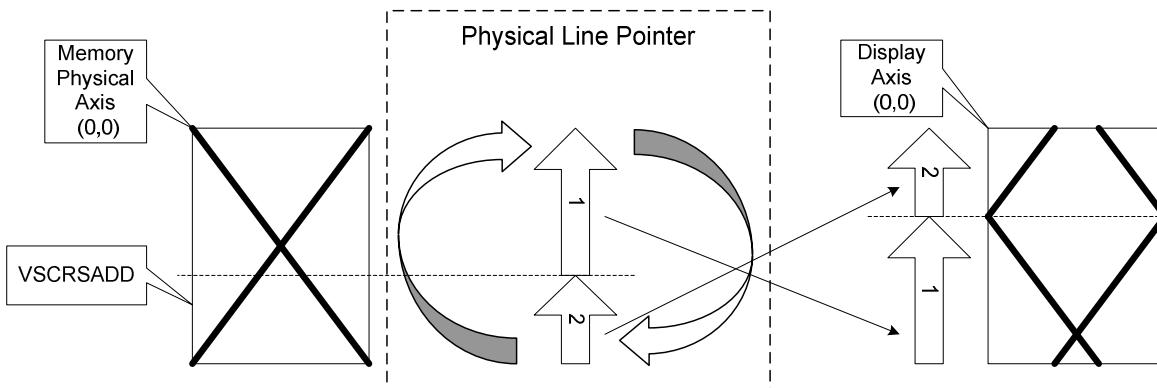
6.2.3.1. Case 1: $TFA + VSA + BFA \neq 480$

This setting is prohibited because it will cause a display output error.

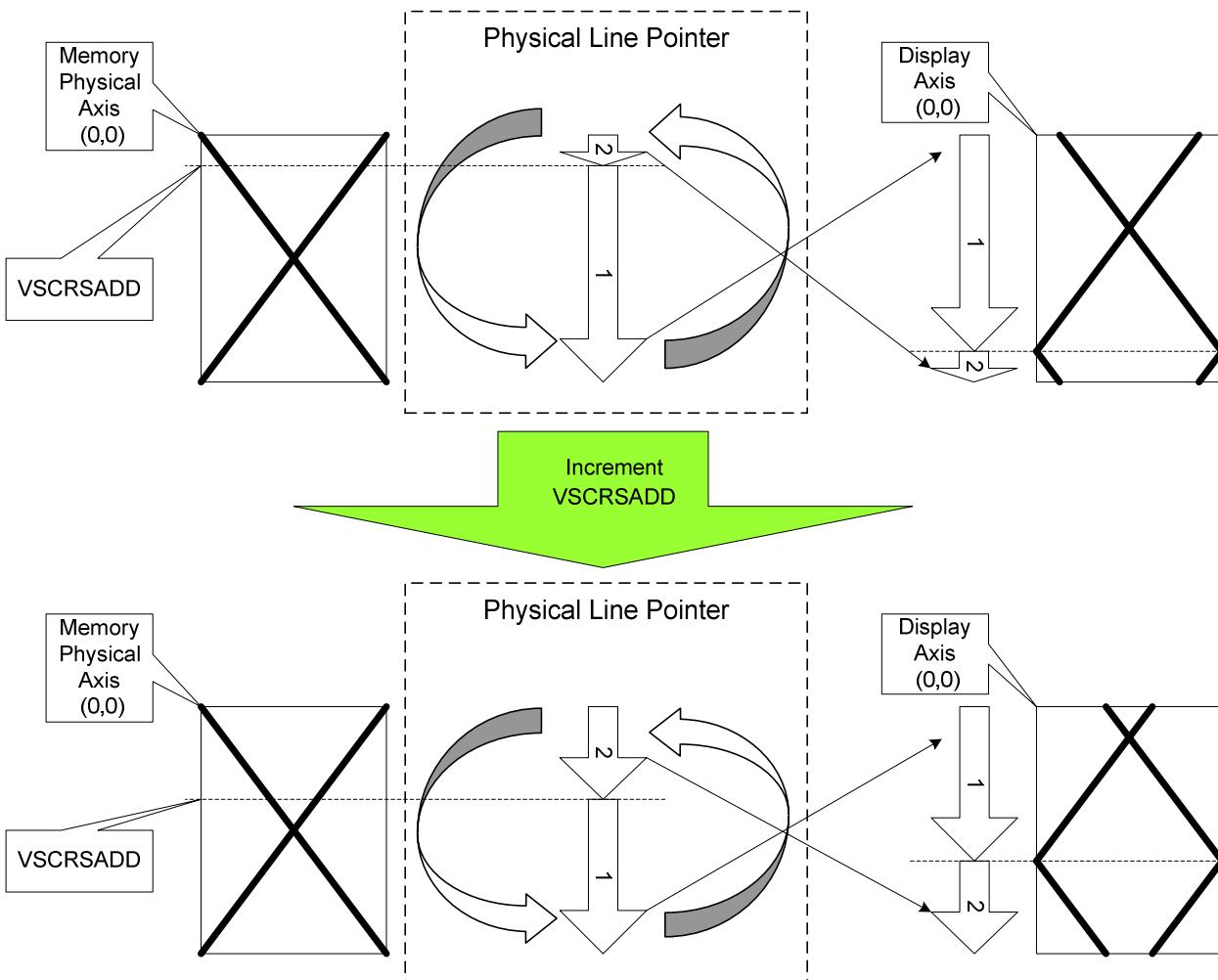
6.2.3.2. Case 2: $TFA + VSA + BFA = 480$

The operations of the Rolling Scrolling are explained by those examples below.

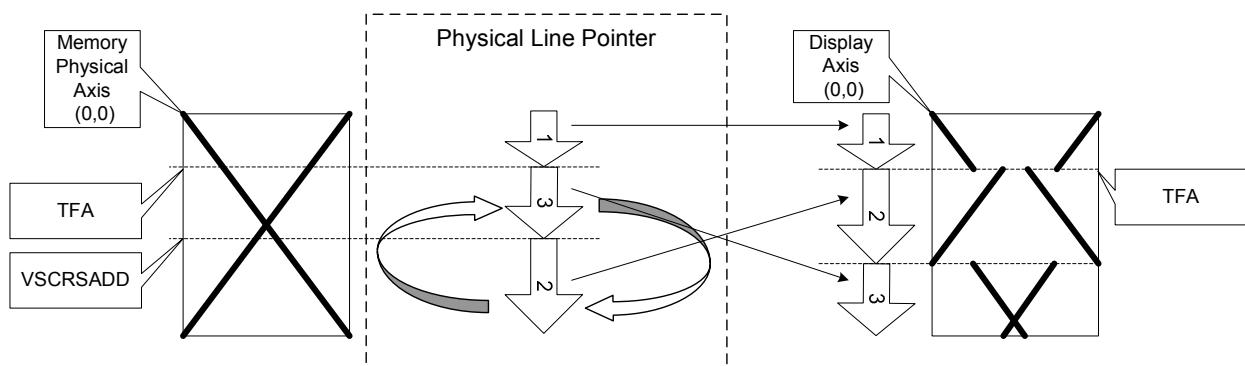
When $TFA=0$, $VSA=480$, $BFA=0$, $VSCRSADD=40$ and $MADCTL$ ML B4 bit = 1



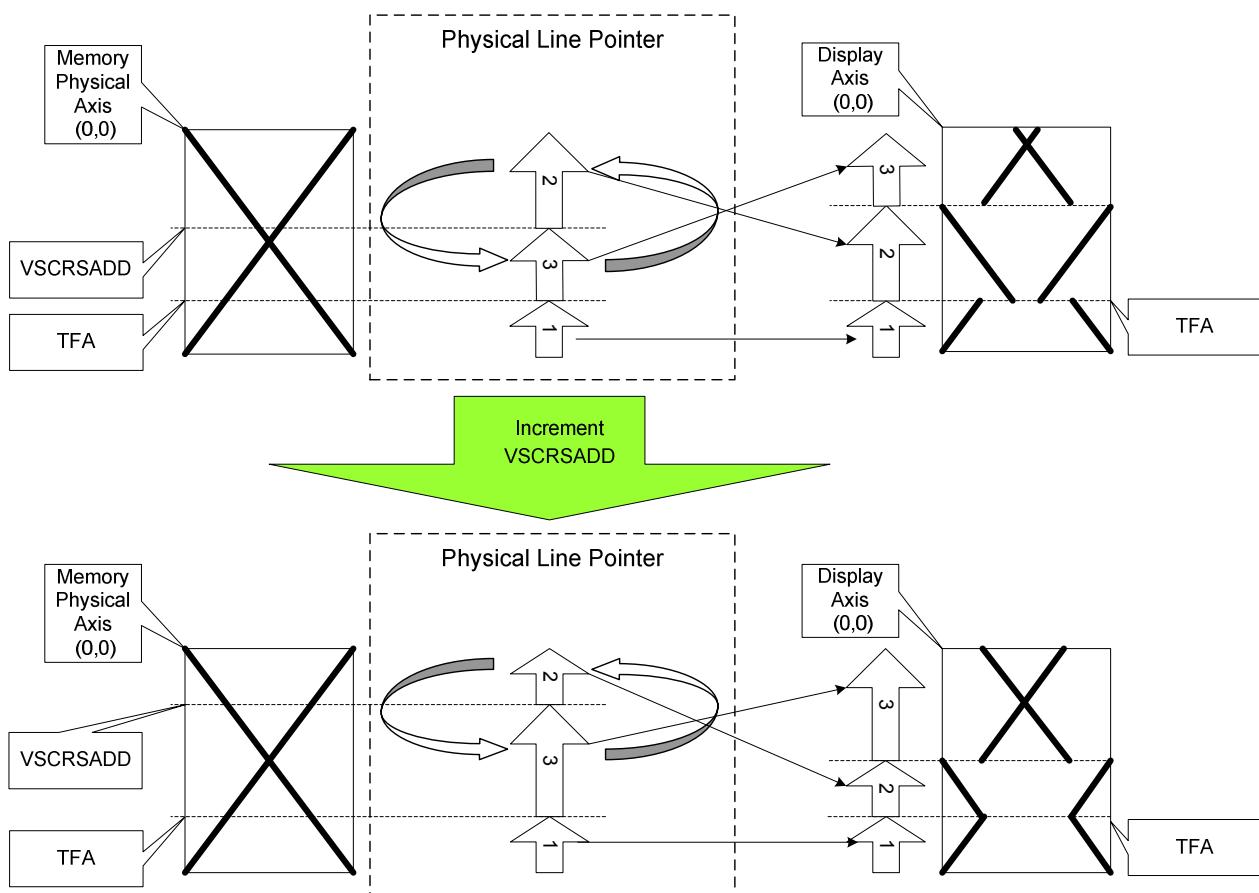
When TFA=0, VSA=480, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



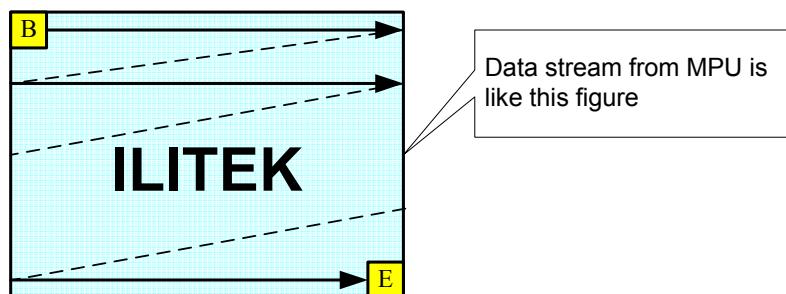
When TFA=30, VSA=450, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



When TFA=30, VSA=450, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



6.3. MCU to Memory Write/Read Direction



The data is written in the order illustrated above. The Counter, indicating where in the physical memory the data is to be written, is controlled by the Memory Data Access Control Command, Bits D7, D6, and D5, as described below.

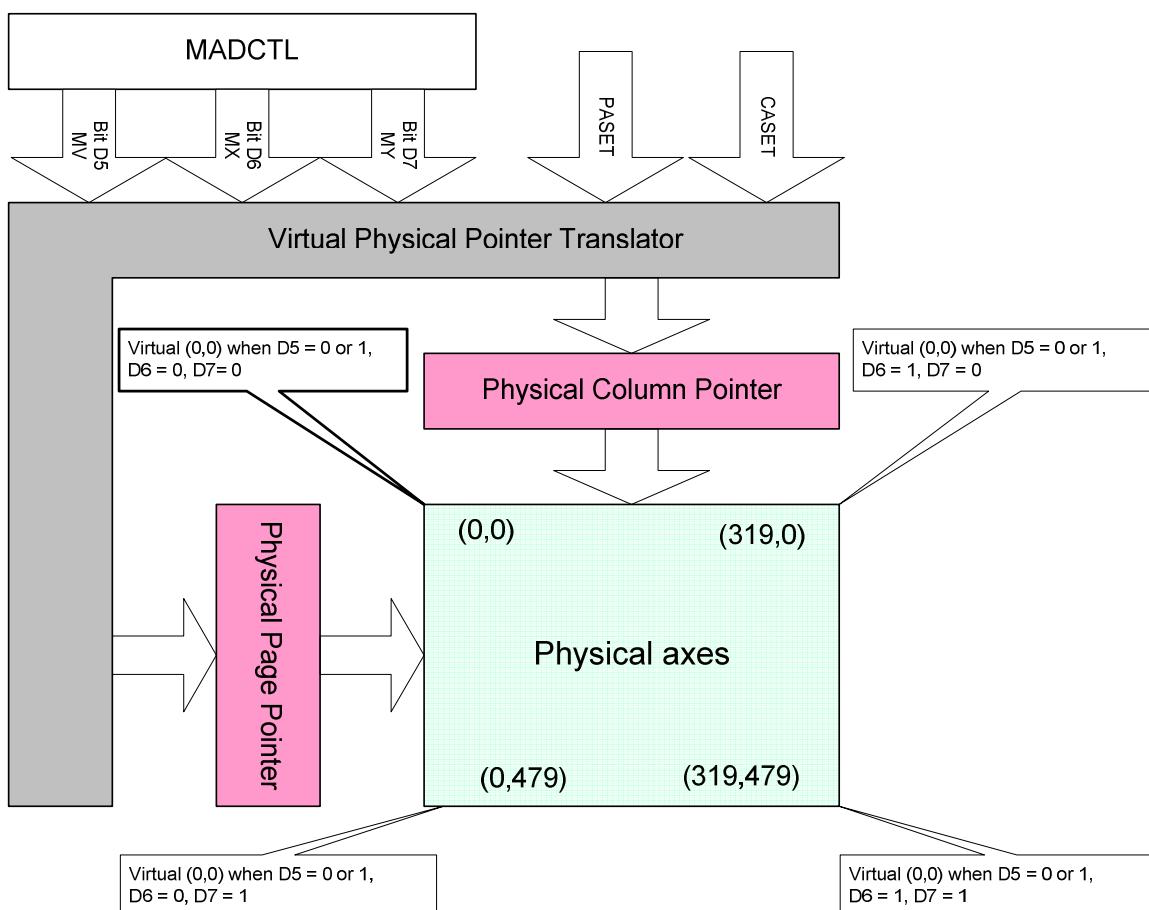


Figure 129: MV, MX, MY Setting (320 (RGB) x 480)

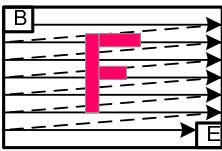
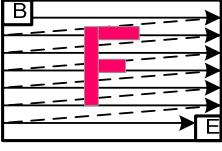
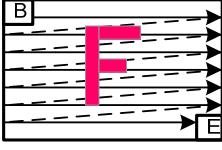
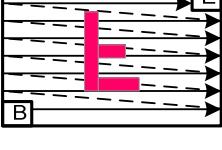
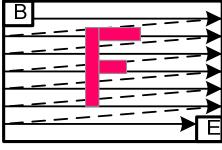
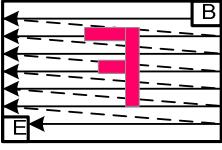
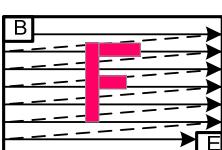
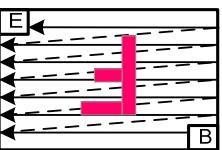
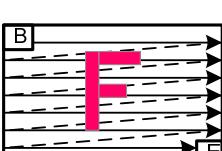
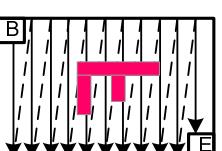
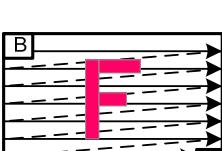
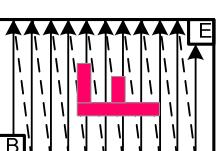
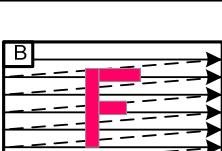
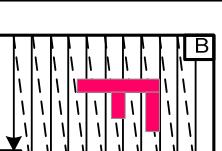
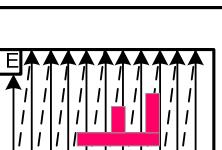
| D5 | D6 | D7 | CASET | PASET |
|----|----|----|---|---------------------------------------|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Page Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (479-Physical Page Pointer) |
| 0 | 1 | 0 | Direct to (319-Physical Column Pointer) | Direct to Physical Page Pointer |
| 0 | 1 | 1 | Direct to (319-Physical Column Pointer) | Direct to (479-Physical Page Pointer) |
| 1 | 0 | 0 | Direct to Physical Page Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (479-Physical Page Pointer) | Direct to Physical Column Pointer |

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| | | | | |
|---|---|---|---------------------------------------|---|
| 1 | 1 | 0 | Direct to Physical Page Pointer | Direct to (319-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (479-Physical Page Pointer) | Direct to (319-Physical Column Pointer) |

| Condition | Column Counter | Page counter |
|---|------------------------|----------------------|
| When RAMWR/RAMRD command is accepted | Return to Start column | Return to Start Page |
| Complete Pixel Read/Write action | Incremented by 1 | No change |
| The Column values are large than End Column | Return to Start column | Incremented by 1 |
| The Page counter are large than End Page | Return to Start column | Return to Start Page |

Note: One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

| Display Data Direction | MADCTR Parameter | | | Image in the Memory (MCU) | Image in the Driver (Frame Memory) |
|--------------------------------|------------------|----|----|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 |  |  |
| X-Y Exchange X-Mirror | 1 | 1 | 0 |  |  |
| X-Y Exchange X-Mirror Y-Mirror | 1 | 1 | 1 |  |  |

7. Tearing Effect Information

The Tearing Effect Line (TE) signal supplies panel synchronization information to the MCU. The TE signal determines the position for refreshing GRAM data for the display panel; the MCU can reference the TE to decide when to send image data in order to avoid abnormal visual effect on the display panel. The TE signal is enabled or disabled by the Tearing Effect Line ON or OFF commands. The TE Line output mode is defined by the parameter of the “Tearing Effect Line ON” command.

Tearing Effect information is sent in two different ways:

- ❖ Separated Line, which is the Tearing Effect Line (TE)
- ❖ Tearing Effect Bus Trigger (TEE): the ILI9488 sends a trigger to inform the MCU.

The TE is used in the MCU parallel interface, and can also be used in the DSI if the Tearing Effect Bus Trigger (TEE) is not possible to be used. However, the Tearing Effect (TEE) Bus Trigger can only be used in the DSI.

7.1. Tearing Effect Line

7.1.1. Tearing Effect Line Modes

Mode 1, illustrated in Figure 130, the Tearing Effect output signal consists of V-Sync information only:

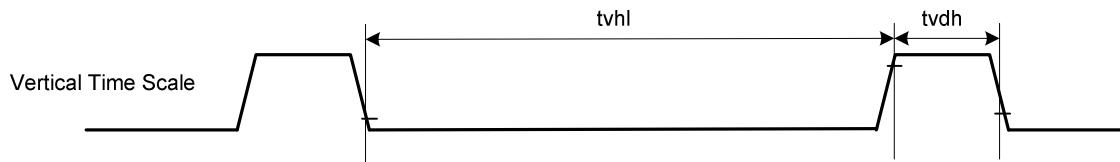


Figure 130: Tearing Effect Line Mode 1

tvdh = The LCD display is not updated from the Frame Memory.

tvhl = The LCD display is updated from the Frame Memory (except the Invisible Line – see the figure above).

Mode 2, illustrated in Figure 131, the Tearing Effect output signal consists of V-Sync and H-Sync information; there is one V-sync and “N” H-sync pulses per field. The resolution is 320 (RGB) x 480, and N = 480.

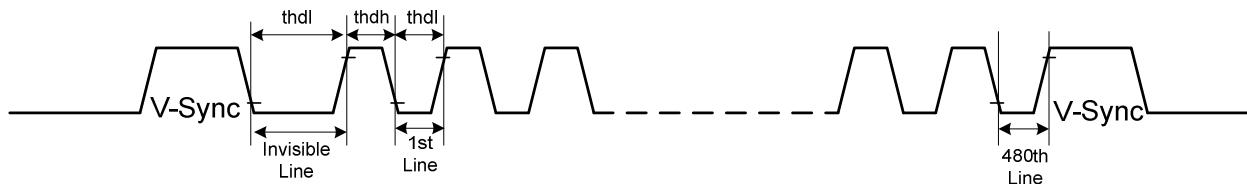
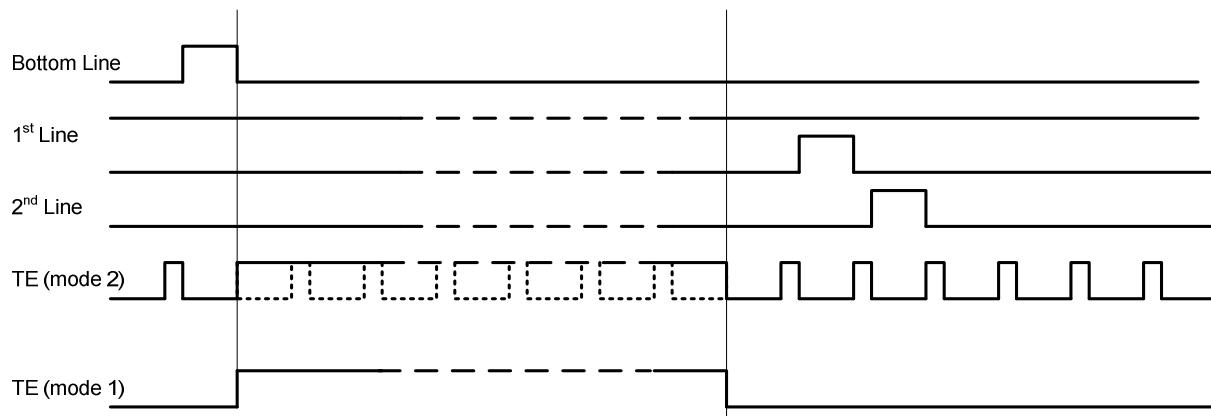


Figure 131: Tearing Effect Line Mode 2

thdh = The LCD display is not updated from the Frame Memory.

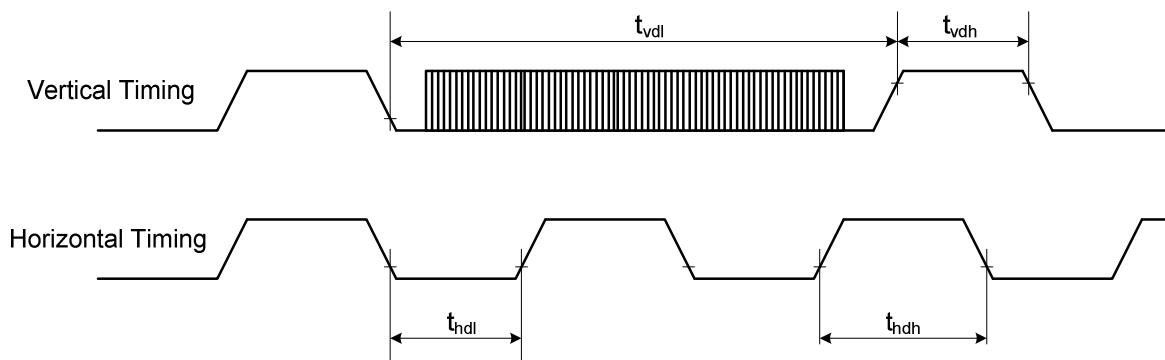
thdl = The LCD display is updated from the Frame Memory (except the Invisible Line – see the figure above).



Note: During the Sleep In Mode, the Tearing Effect Output Pin is active Low.

7.1.2. Tearing Effect Line Timing

The tearing effect signal is described below:



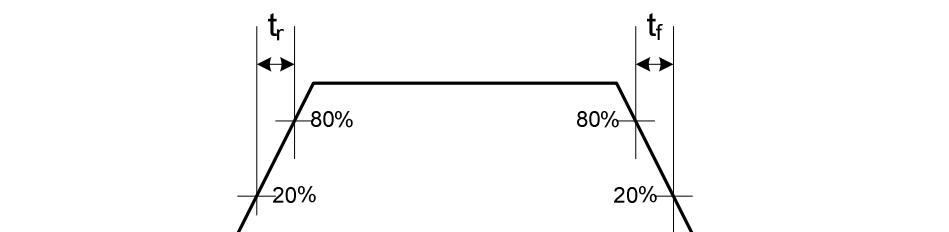
The AC characteristic of the Tearing Effect Signal is: 320 (RGB) x 480 Resolution.

Table 36: Tearing Effect Line Timing

| Symbol | Parameter | Min. | Max. | Unit | Description |
|-----------|---------------------------------|------|------|------|-------------|
| t_{vdl} | Vertical timing low duration | 10 | 40 | ms | |
| t_{vdh} | Vertical timing high duration | 500 | 2000 | us | |
| t_{hdl} | Horizontal timing low duration | 15 | 75 | us | |
| t_{hdh} | Horizontal timing high duration | 1 | 5 | us | |

Notes:

1. The timings in Table 36 are applied when MADCTL D4 = 0 and D4 = 1.
2. The signal's rising and falling times (t_f , t_r) are stipulated to be equal to or less than 15ns.



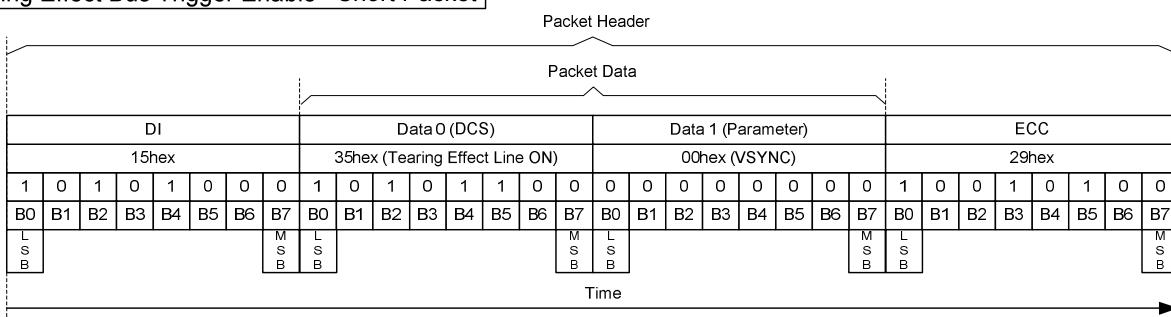
The Tearing Effect Output Line is fed back to the MCU and should be used to avoid the Tearing Effect.

7.2. Tearing Effect Bus Trigger

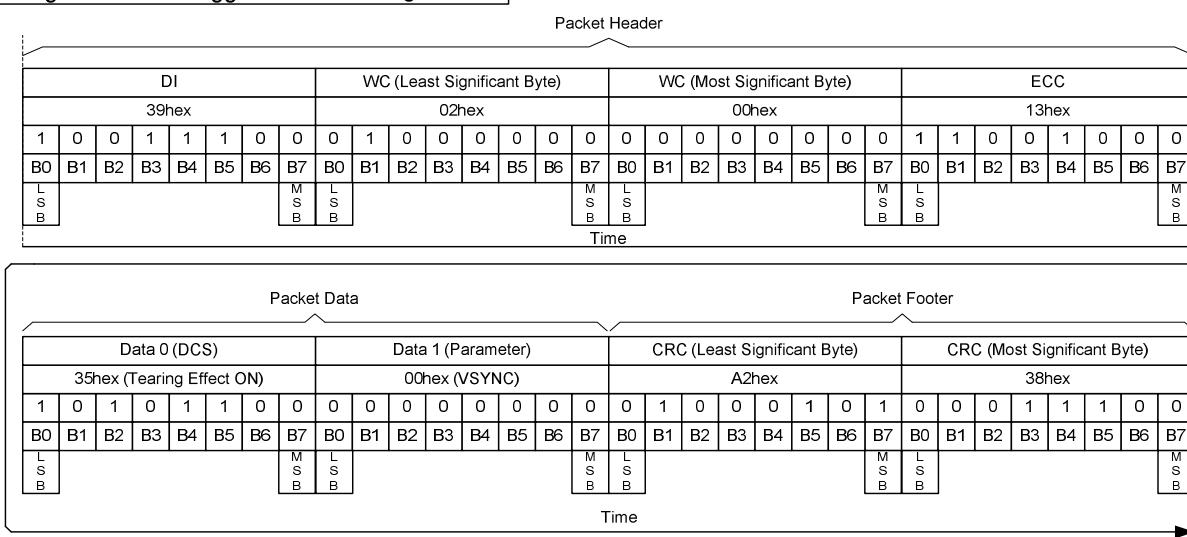
Tearing Effect Bus Trigger information supplies a Panel synchronization trigger to the MCU and this Tearing Effect Bus Trigger information can be enabled or disabled by Tearing Effect Line Off (34h) and Tearing Effect Line On (35h) commands when the only mode of the Tearing Effect Signal is VSYNC information. The ILI9488 sends this trigger information in the Escape Mode after the Bus Turnaround (BTA) and the Tearing Effect Bus Trigger can only be used in the DSI without the TE line.

7.2.1. Tearing Effect Bus Trigger Enable

Tearing Effect Bus Trigger Enable - Short Packet



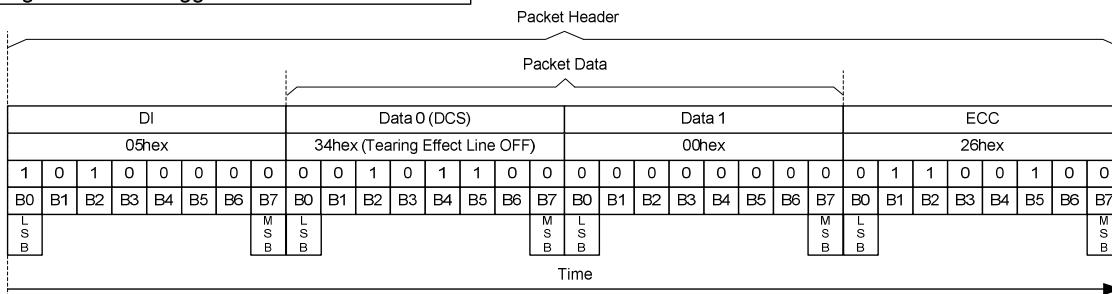
Tearing Effect Bus Trigger Enable - Long Packet



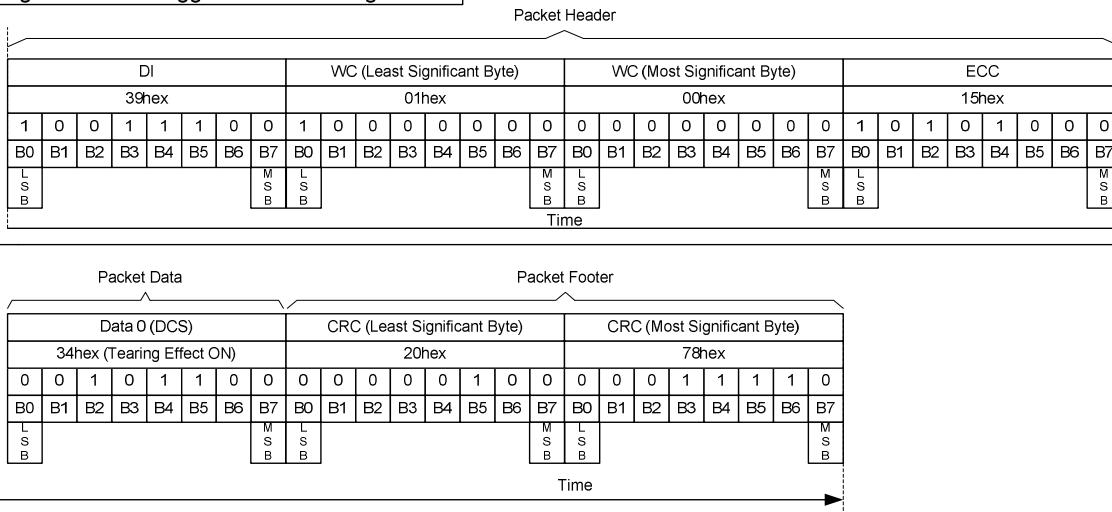
7.2.2. Tearing Effect Bus Trigger Disable

The MCU can disable the Tearing Effect Bus Trigger on the ILI9488 in 2 different ways: when a Short Packet (SPa) or Long Packet (LPa) is used. These both possibilities are illustrated below.

Tearing Effect Bus Trigger Disable - Short Packet



Tearing Effect Bus Trigger Disable - Long Packet



7.2.3. Tearing Effect Bus Trigger Sequences

| Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and HSDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (LPa) | HSDT | → | - | - | Tearing Effect Bus Trigger Enable |
| 3 | - | LP-11 | → | - | - | |
| 4 | - | BTA | ↔ | BTA | - | Interface Control Change from the MCU to the display module (ILI9488) |
| 5 | - | - | ← | LP-11 | - | If No Error, then go to Line 7 If Error occurs, then go to Line 12 |
| 6 | | | | | | |
| 7 | - | - | ← | TEE | - | TE (Escape Trigger) on the next VSYNC |
| 8 | - | - | ← | LP-11 | - | |
| 9 | - | BTA | ↔ | BTA | - | Interface Control Change from the display module (ILI9488) to MCU |
| 10 | - | LP-11 | → | - | - | End |

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| | | | | | | |
|----|---|-------|---|------|--------------------------|--------------|
| 11 | | | | | | |
| 12 | - | - | ← | LPDT | Acknowledge Error Report | Error Report |
| 13 | - | - | ← | LP-1 | - | |
| 14 | - | BTA | ↔ | BTA | - | |
| 15 | - | LP-11 | → | - | - | End |

| Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and LPDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|--------------------------|---|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (LPa) | LPDT | → | - | - | Tearing Effect Bus Trigger Enable |
| 3 | - | LP-11 | → | - | - | |
| 4 | - | BTA | ↔ | BTA | - | Interface Control Change from the MCU to the display module (ILI9488) |
| 5 | - | - | ← | LP-11 | - | If No Error, then go to Line 7 If Error occurs, then go to Line 12 |
| 6 | | | | | | |
| 7 | - | - | ← | TEE | - | TE (Escape Trigger) on the next VSYNC |
| 8 | - | - | ← | LP-11 | - | |
| 9 | - | BTA | ↔ | BTA | - | Interface Control Change from the display module (ILI9488) to MCU |
| 10 | - | LP-11 | → | - | - | End |
| 11 | | | | | | |
| 12 | - | - | ← | LPDT | Acknowledge Error Report | Error Report |
| 13 | - | - | ← | LP-1 | - | |
| 14 | - | BTA | ↔ | BTA | - | |
| 15 | - | LP-11 | → | - | - | End |

| Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and HSDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|---------------|---|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (SPa) | HSDT | → | - | - | Tearing Effect Bus Trigger Enable |
| 3 | - | LP-11 | → | - | - | |
| 4 | - | BTA | ↔ | BTA | - | Interface Control Change from the MCU to the display module (ILI9488) |
| 5 | - | - | ← | LP-11 | - | If No Error, then go to Line 7 If Error occurs, then go to Line 12 |
| 6 | | | | | | |
| 7 | - | - | ← | TEE | - | TE (Escape Trigger) on the next VSYNC |
| 8 | - | - | ← | LP-11 | - | |
| 9 | - | BTA | ↔ | BTA | - | Interface Control Change from the display module (ILI9488) to MCU |
| 10 | - | LP-11 | → | - | - | End |

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| | | | | | | |
|----|---|-------|---|------|--------------------------|--------------|
| 11 | | | | | | |
| 12 | - | - | ← | LPDT | Acknowledge Error Report | Error Report |
| 13 | - | - | ← | LP-1 | - | |
| 14 | - | BTA | ↔ | BTA | - | |
| 15 | - | LP-11 | → | - | - | End |

| Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and LPDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|--------------------------|---|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (SPa) | LPDT | → | - | - | Tearing Effect Bus Trigger Enable |
| 3 | - | LP-11 | → | - | - | |
| 4 | - | BTA | ↔ | BTA | - | Interface Control Change from the MCU to the display module (ILI9488) |
| 5 | - | - | ← | LP-11 | - | If No Error, then go to Line 7 If Error occurs, then go to Line 12 |
| 6 | | | | | | |
| 7 | - | - | ← | TEE | - | TE (Escape Trigger) on the next VSYNC |
| 8 | - | - | ← | LP-11 | - | |
| 9 | - | BTA | ↔ | BTA | - | Interface Control Change from the display module (ILI9488) to MCU |
| 10 | - | LP-11 | → | - | - | End |
| 11 | | | | | | |
| 12 | - | - | ← | LPDT | Acknowledge Error Report | Error Report |
| 13 | - | - | ← | LP-1 | - | |
| 14 | - | BTA | ↔ | BTA | - | |
| 15 | - | LP-11 | → | - | - | End |

| Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and LPDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|---------------|------------------------------------|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (SPa) | LPDT | → | - | - | Tearing Effect Bus Trigger Disable |
| 3 | - | LP-11 | → | - | - | End |

| Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and HSDT | | | | | | |
|---|-----------------|------------------------|-----------------------|------------------------|---------------|------------------------------------|
| Line | MCU | | Information Direction | Display Module | | Comment |
| | Packet Sender | Interface Mode Control | | Interface Mode Control | Packet Sender | |
| 1 | - | LP-11 | → | - | - | Start |
| 2 | DCS Write (SPa) | HSDT | → | - | - | Tearing Effect Bus Trigger Disable |
| 3 | - | LP-11 | → | - | - | End |

8. CABC (Content Adaptive Brightness Control)

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The ILI9488 refers the gray scale content of display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

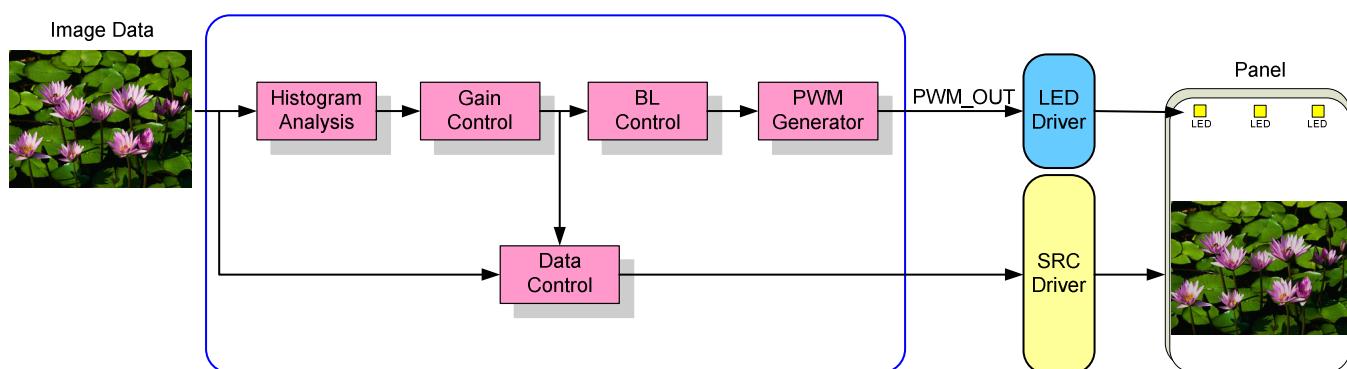


Figure 132: CABC Block Diagram

The ILI9488 can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via PWM_OUT pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{\text{pwm_out}} = \frac{12.5\text{MHz}}{(\text{PWM_DIV}[7:0]+1) \times 255}$$

Figure 133 is the basic timing diagram which is applied from the ILI9488 line order to control a LED driver.

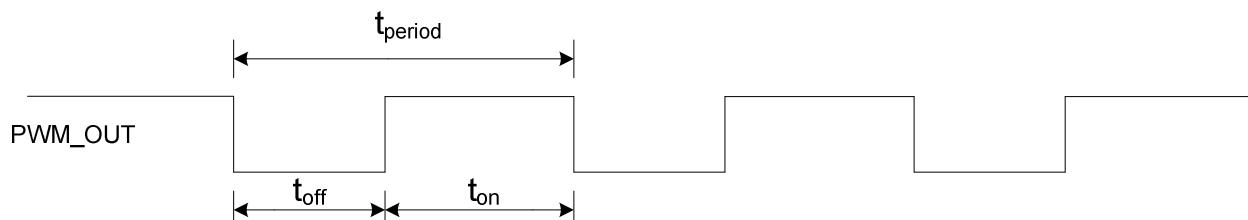


Figure 133: PWM OUT On/Off Period

9. Color Enhancement Function

The Color Enhancement Function enhances saturation by calculating image data of the display on the liquid crystal panel. The saturation enhancement coefficients of red, yellow, green, cyan, blue, magenta, are set independently. The function enhances color and makes pixel colors more vivid.

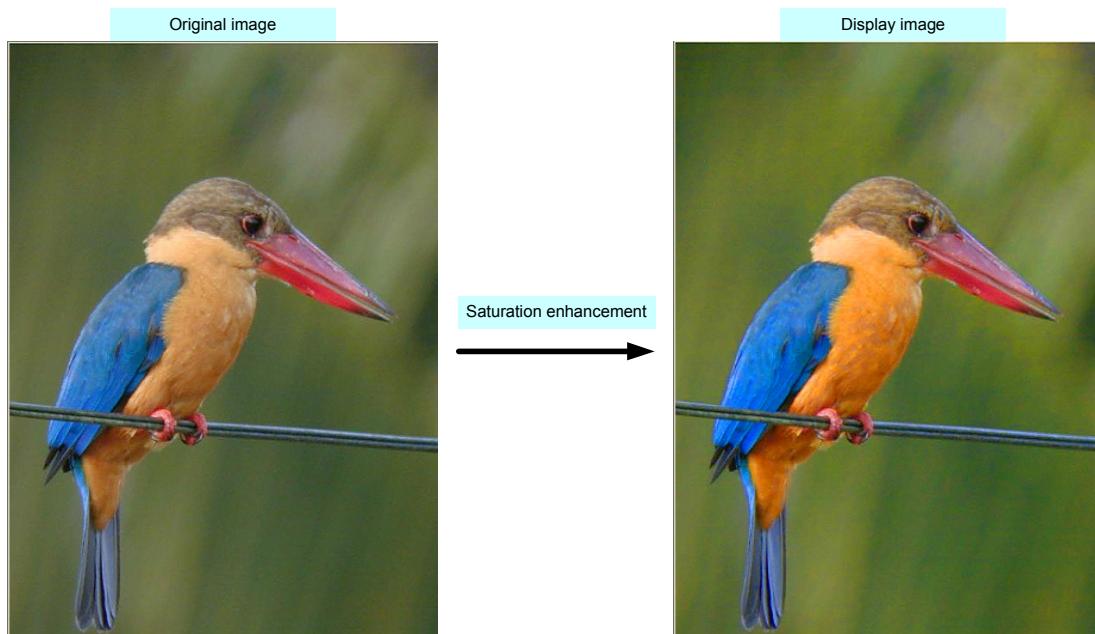


Figure 134: Saturation Enhancement Image

The displayed image with color enhanced is generated when the saturation enhancement coefficients of the input image are 1.0 or more. See the saturation diagram Figure 135. The colors of the input image are enhanced. Both green and magenta colors keep the original gray value without enhanced.

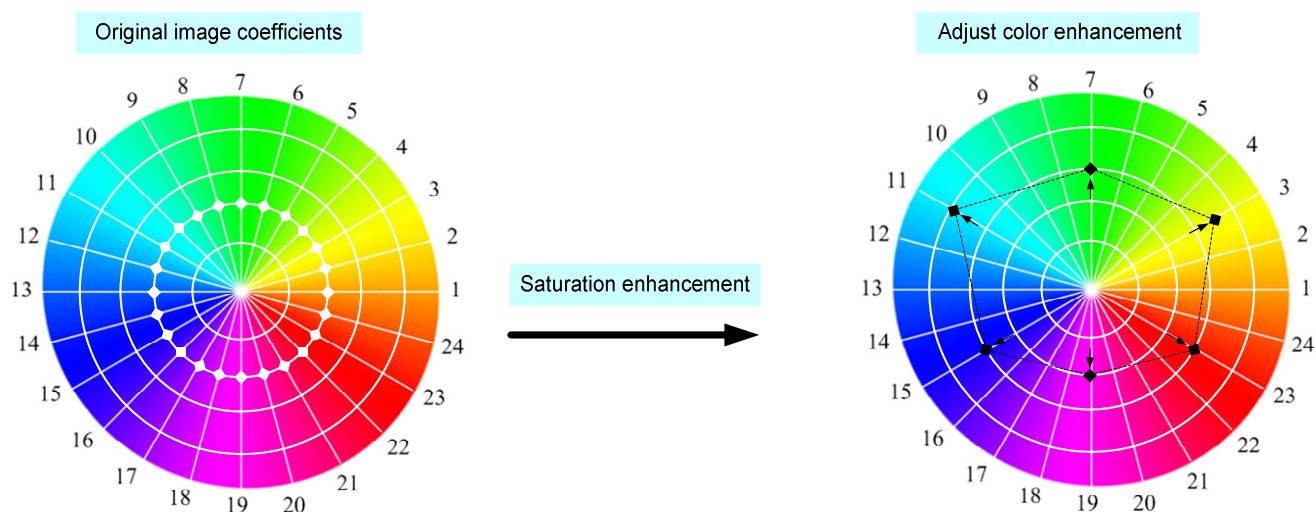


Figure 135: 6-axis Color Enhancement

10. Sleep Out Command and Self-Diagnostic Functions

10.1. Register Loading Detection

The Sleep Out command (Sleep Out (11h)) is a trigger for an internal function of the ILI9488, which indicates if the ILI9488 loading function of factory default values from EEPROM (or similar devices) to registers of the display controller works properly. Factory values of the EEPROM and register values of the display controller are compared by the display controller (1st step: compare register and EEPROM values, 2nd step: load the EEPROM value to register). If those two values (EEPROM and register values) are the same, the bit D7 is inverted (= increased by 1), which is defined in the command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those two values are not the same, this bit (D7) is not inverted (= not increased by 1), and the used TE-line is set to low (registers will keep their current values) and can only be reactivated by the “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is:

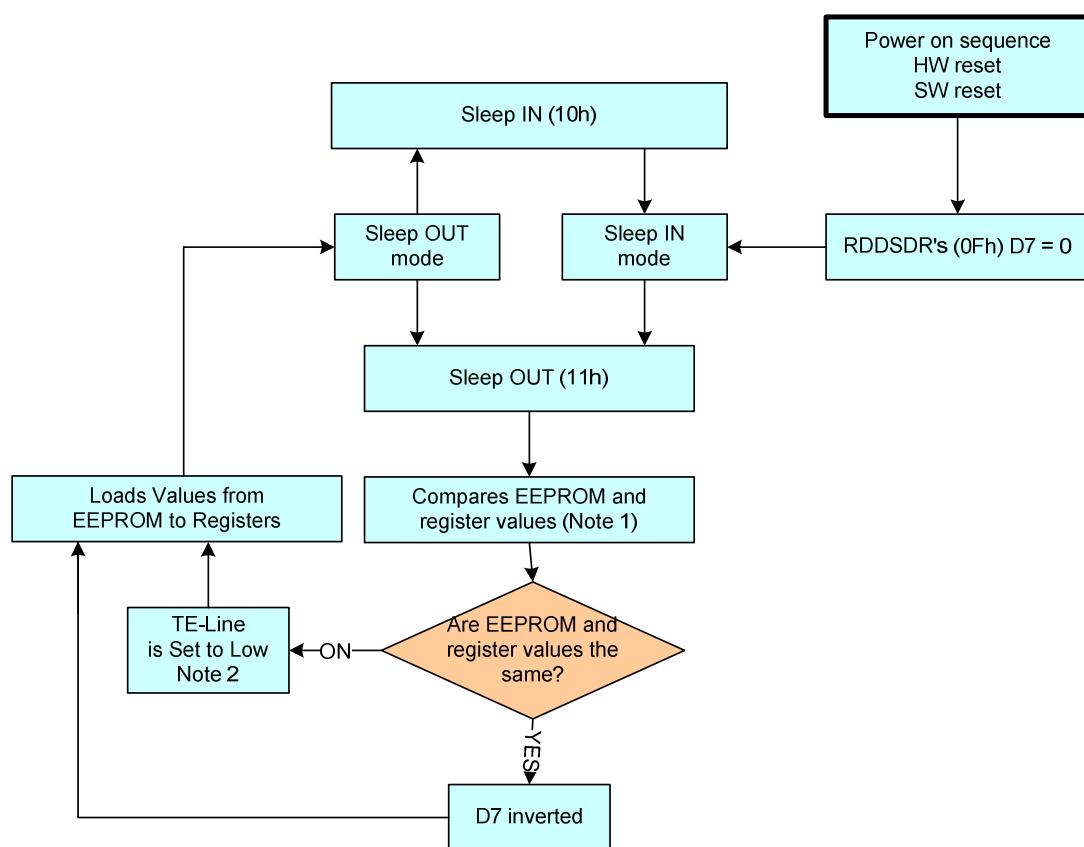


Figure 136: Register Loading Detection

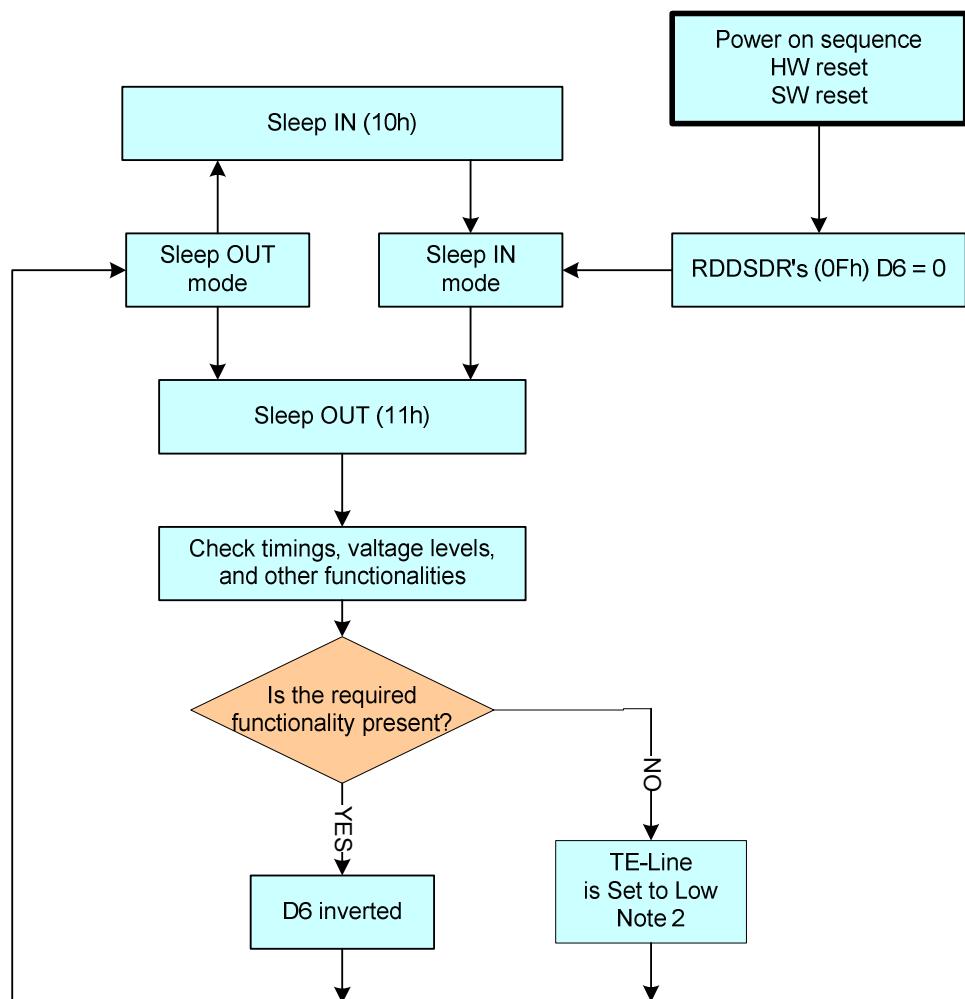
Notes:

1. If the EEPROM and register values are not compared and loaded, they can be changed by commands 00h to AFh and DAh to DDh.
2. This information is only used when the TE line is used.

10.2. Functionality Detection

The Sleep Out command (Command “Sleep Out (11h)”) is a trigger for an internal function of the ILI9488, which indicates if the ILI9488 is still running and meets functionality requirements. The internal function (the display controller) is compared if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (increased by 1), defined in the command “Read Display Self-Diagnostic Result (0Fh)” (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (not increased by 1) and the used TE-line is set to low (registers will keep their current values) and can only be reactivated by the Tearing Effect Line On (35h) command.

The flow chart for this internal function is:



Notes:

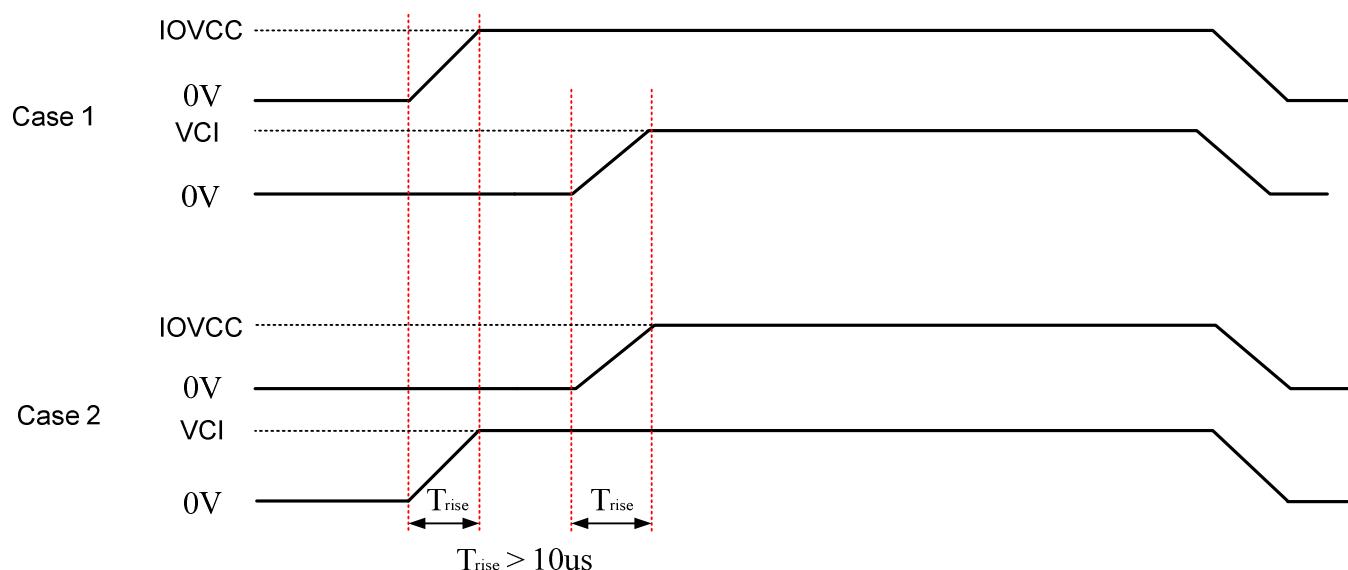
- When changing from the Sleep In mode to the Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and the value of RDDSDR’s D6 is valid. Otherwise, there will be 5msec delay for the D6’s value to be valid when the Sleep Out command is sent in the Sleep Out mode.
- This function is only used when the TE-line is used.

11. Power ON/OFF Sequence

IOVCC and VCI can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with a minimum of 120msec. If the LCD is in the Sleep In mode, VCI and IOVCC can be powered down with a minimum of 0msec after the RESX has been released. CSX can be applied at any time or can be permanently grounded. RESX has high priority over CSX.

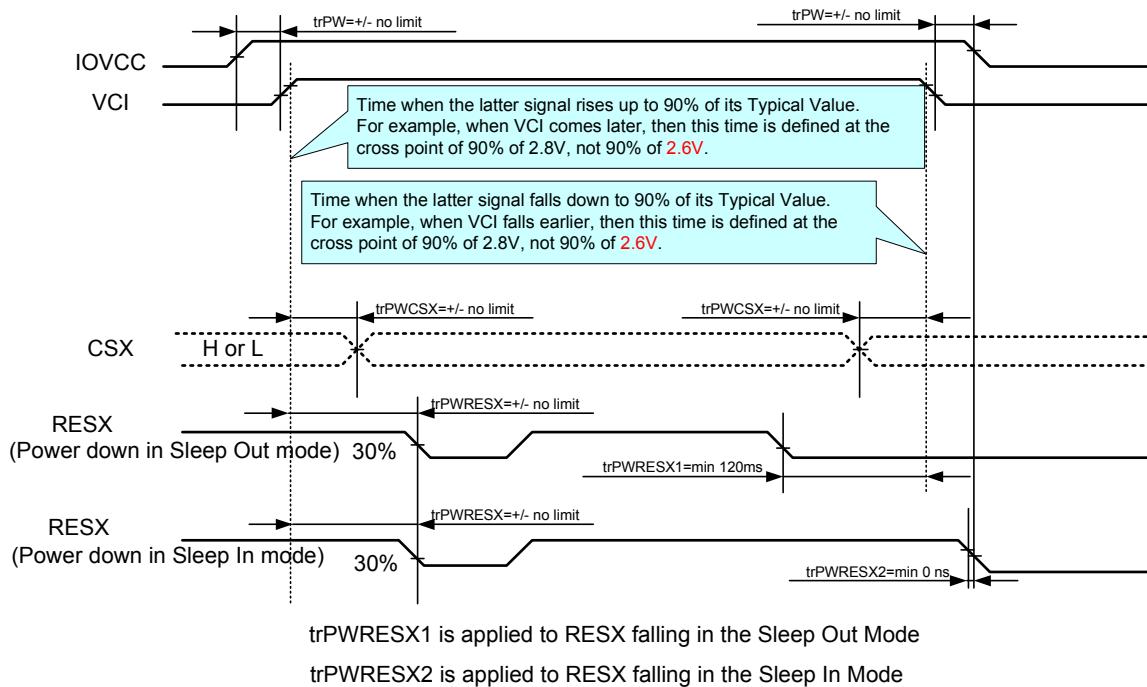
Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing(T_{rise}) must be greater than 10us.



11.1. Case 1 – RESX Line is Held High or Unstable by Host at Power ON

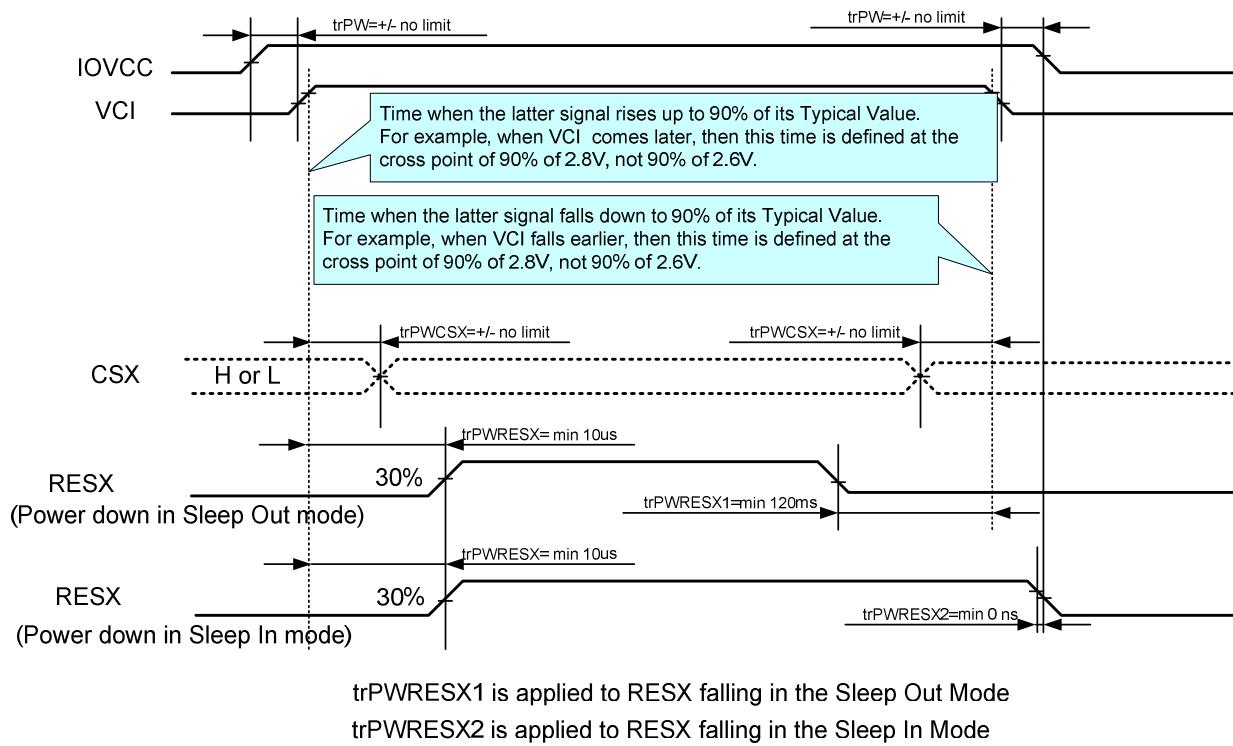
If the RESX line is held High or unstable by the host during Power On, then Hardware Reset must be applied after both VCI and IOVCC have been applied. Otherwise, the correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

11.2. Case 2 – RESX Line is Held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for a minimum of 10 μ sec after both VCI and IOVCC have been applied.



Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

11.3. Uncontrolled Power Off

The Uncontrolled Power Off means the situation when a battery is removed without the controlled power off sequence. There will not be any damages on the display module, or the display module will not cause any damages on the host or lines of the interface. At an uncontrolled power off event, the ILI9488 will force the display to become blank and will not cause any abnormal visible effects within 1 second on the display and remains blank until "Power On Sequence" powers it up.

12. Power Level Definition

12.1. Power Levels

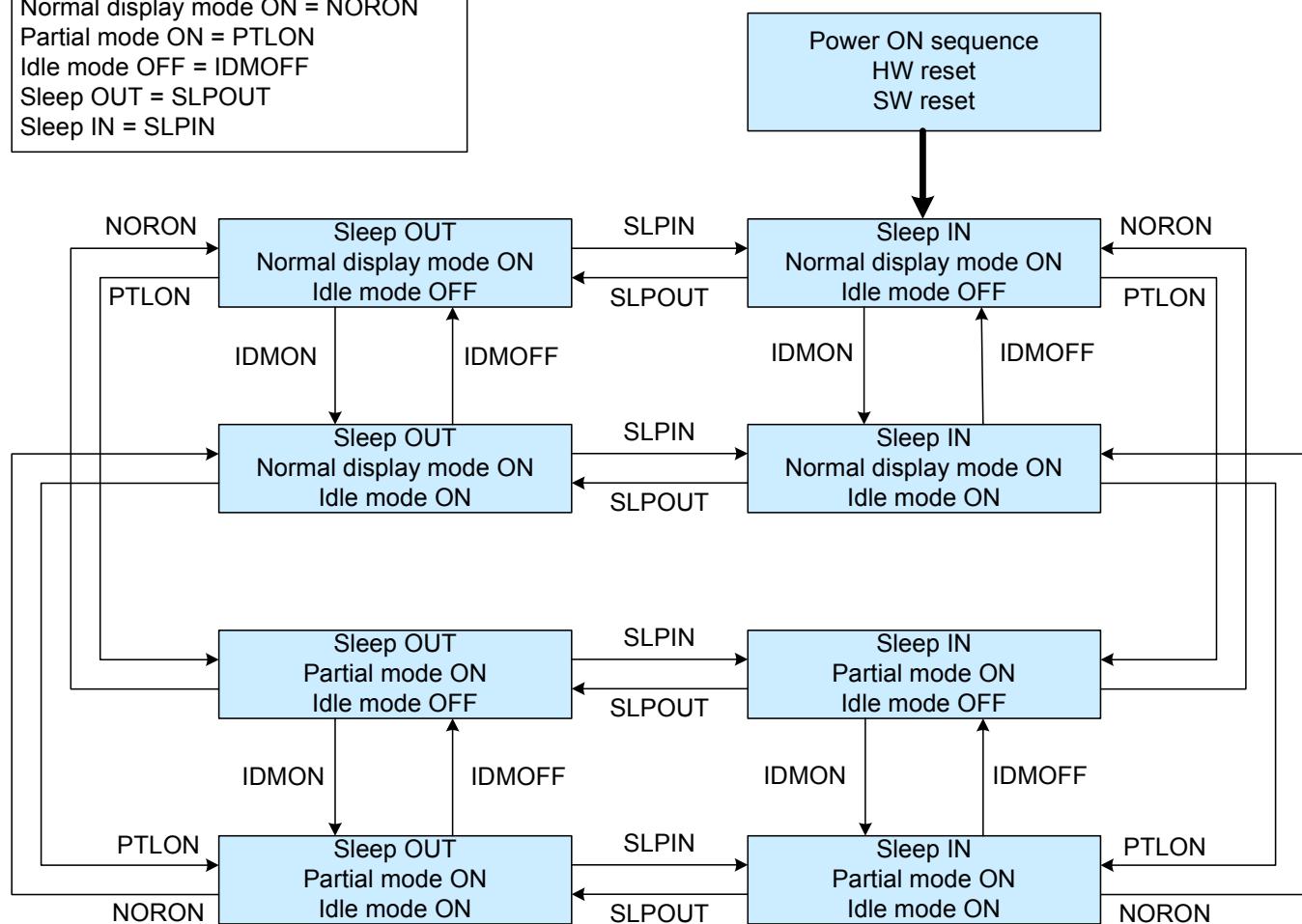
6 level modes are defined in order from Maximum to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
In this mode, the display is able to show a maximum of 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
In this mode, part of the display is used with a maximum of 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
In this mode, part of the display is used with 8 colors.
5. Sleep In Mode
In this mode, the DC/DC converter, internal oscillator, and panel driver circuit are stopped. Only the MCU interface and memory can work with the VCI power supply. Contents of the memory are safe and cannot be changed.
6. Power Off Mode
In this mode, both VCI and IOVCC are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Only when both Power supplies are removed can Mode 6 be entered.

12.2. Power Flow Chart

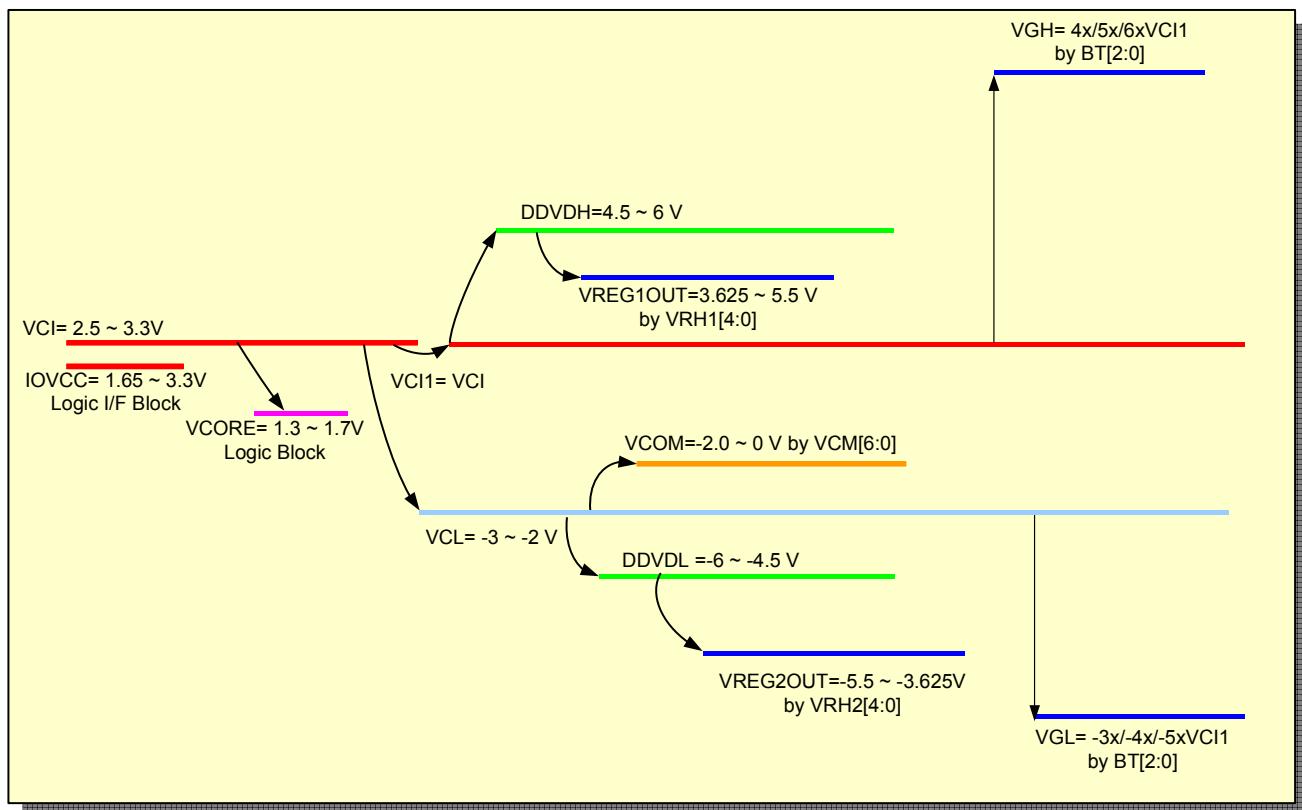
Normal display mode ON = NORON
 Partial mode ON = PTLON
 Idle mode OFF = IDMOFF
 Sleep OUT = SLPOUT
 Sleep IN = SLPIN



Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

12.3. LCM Voltage Generation



Note: The DDVDH, DDVDL, VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to the current consumption at respective outputs.

13. Reset

13.1. Registers

The initialized values of registers are listed in Table 37.

Table 37: Initial Values of Registers

| Register | After Powered ON | After Hardware Reset | After Software Reset |
|----------------------------|--------------------------|--------------------------|--------------------------|
| Frame Memory | Random | Random | Random |
| Sleep | In | In | In |
| Display Mode | Normal | Normal | Normal |
| Display Status | Display Off | Display Off | Display Off |
| Idle Mode | Off | Off | Off |
| All Pixels Off | Off | Off | Off |
| All Pixels On | Off | Off | Off |
| Column Start Address (2Ah) | 0000 h | 0000 h | 0000 h |
| Column End Address (2Ah) | 013F h | 013F h | 013F h |
| Page Start Address (2Bh) | 0000 h | 0000 h | 0000 h |
| Page End Address (2Bh) | 01DF h | 01DF h | 01DF h |
| Gamma Setting | GC0 | GC0 | GC0 |
| Partial Area Start (30h) | 0000 h | 0000 h | 0000 h |
| Partial Area End (30h) | 01DF h | 01DF h | 01DF h |
| MADCTL (36h) | 00 h | 00 h | 00h |
| RDNUMED (05h) | 00 h | 00 h | 00h |
| RDDPM (0Ah) | 08 h | 08 h | 08 h |
| RDDMADCTL (0Bh) | 00 h | 00 h | 00 h |
| RDDCOLMOD (0Ch) | 06 h | 06 h | 06 h |
| RDDIM (0Dh) | 00 h | 00 h | 00 h |
| RDDSM (0Eh) | 00 h | 00 h | 00 h |
| RDDSDR (0Fh) | 00 h | 00 h | 00 h |
| Color Pixel Format (3Ah) | 18 Bit/Pixel | 18 Bit/Pixel | 18 Bit/Pixel |
| TE Output Line (35h) | Off | Off | Off |
| TE Line Mode (35h) | Mode 1 ^{Note 2} | Mode 1 ^{Note 2} | Mode 1 ^{Note 2} |
| RDDISBV (52h) | 00 h | 00 h | No charge |
| RDCTRLD (54h) | 00 h | 00 h | No charge |
| RDCABC (56h) | 00 h | 00 h | No charge |
| RDCABCMB (5Fh) | 00 h | 00 h | No charge |

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

13.2. Output Pins, I/O Pins

Table 38: Output and I/O Pins

| Pin/Line | After Power ON | After Hardware Reset | After Software Reset |
|-----------------------------|-----------------|----------------------|----------------------|
| DB [23:0] | Hi-Z (Inactive) | Hi-Z (Inactive) | Hi-Z (Inactive) |
| SDA (Output direction), SDO | Hi-Z (Inactive) | Hi-Z (Inactive) | Hi-Z (Inactive) |
| MIPI_DATA_P | Hi-Z (Inactive) | Hi-Z (Inactive) | Hi-Z (Inactive) |
| MIPI_DATA_N | Hi-Z (Inactive) | Hi-Z (Inactive) | Hi-Z (Inactive) |
| CABC_PWM_OUT | Low | Low | Low |
| TE | Low | Low | Low |

Note: There will be no output from DB [23:0], SDA, SDO, CABC_PWM_OUT, TE, MIPI_DATA_P, and MIPI_DATA_N, during the Power ON/OFF sequence, hardware reset, and software reset.

13.3. Input Pins

| Pin/Line | During Power ON Process | After Power ON | After Hardware Reset | After Software Reset | During Power OFF Process |
|--------------|-------------------------|----------------|----------------------|----------------------|--------------------------|
| RESX | <i>See Chapter 11</i> | Input valid | Input valid | Input valid | <i>See Chapter 11</i> |
| CSX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| D/CX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| WRX/SCL | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| RDX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| VSYNC | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| HSYNC | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| ENABLE | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| DOTCLK | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| DB [23:0] | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| MIPI_CLOCK_P | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| MIPI_CLOCK_N | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| MIPI_DATA_P | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| MIPI_DATA_N | Input invalid | Input valid | Input valid | Input valid | Input invalid |

13.4. Reset Timing

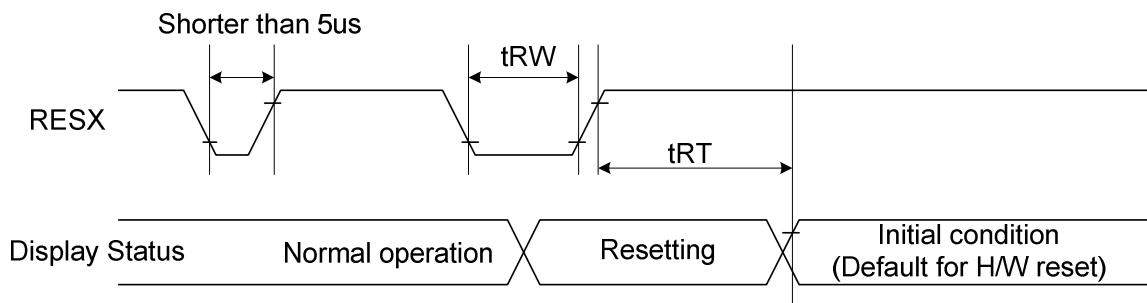


Table 39: Reset Timing

| Signal | Symbol | Parameter | Min | Max | Unit |
|--------|--------|----------------------|-----|----------------------------------|------|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) 120 (note 1,6,7) | mS |

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

| RESX Pulse | Action |
|---------------------|----------------|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

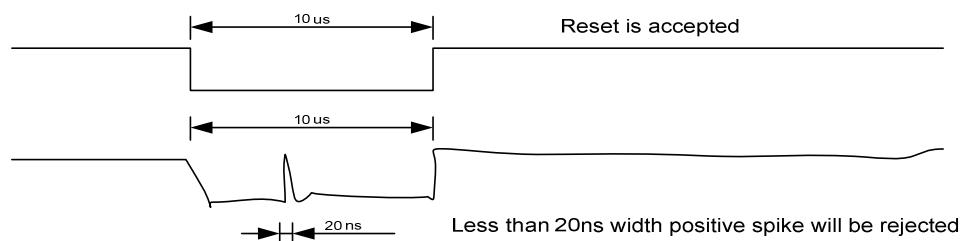
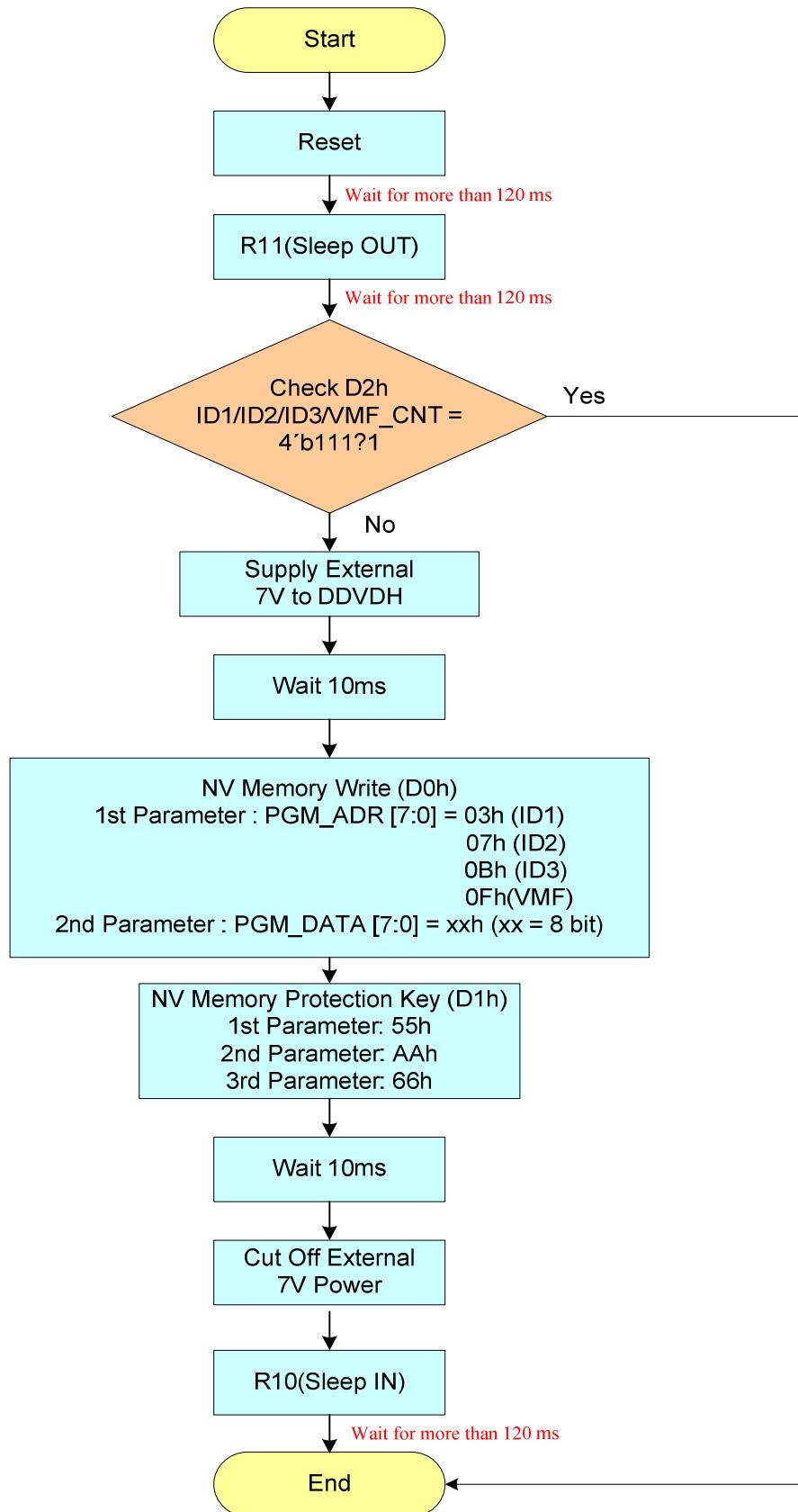


Figure 137: Positive Noise Pulse during Reset Low

5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

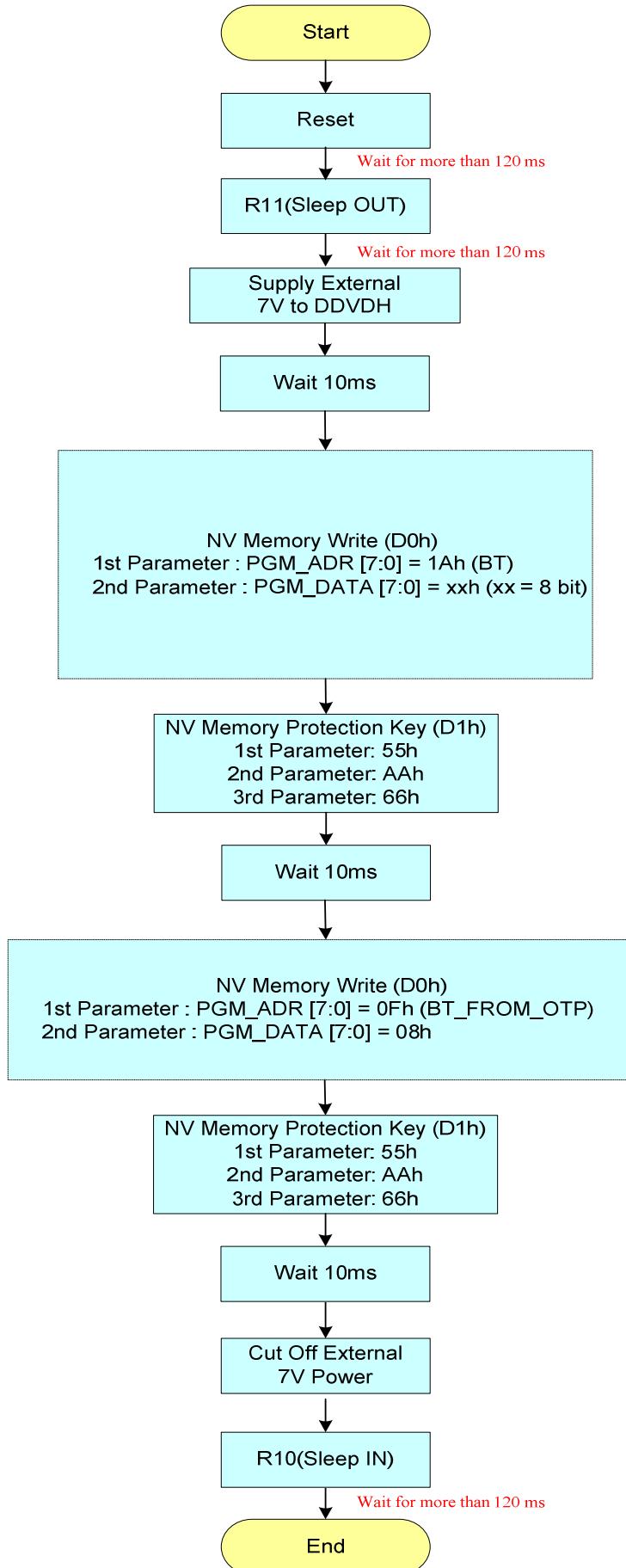
14. NV Memory Programming Flow

14.1. ID1/ID2/ID3 and VCOM Programming Flow

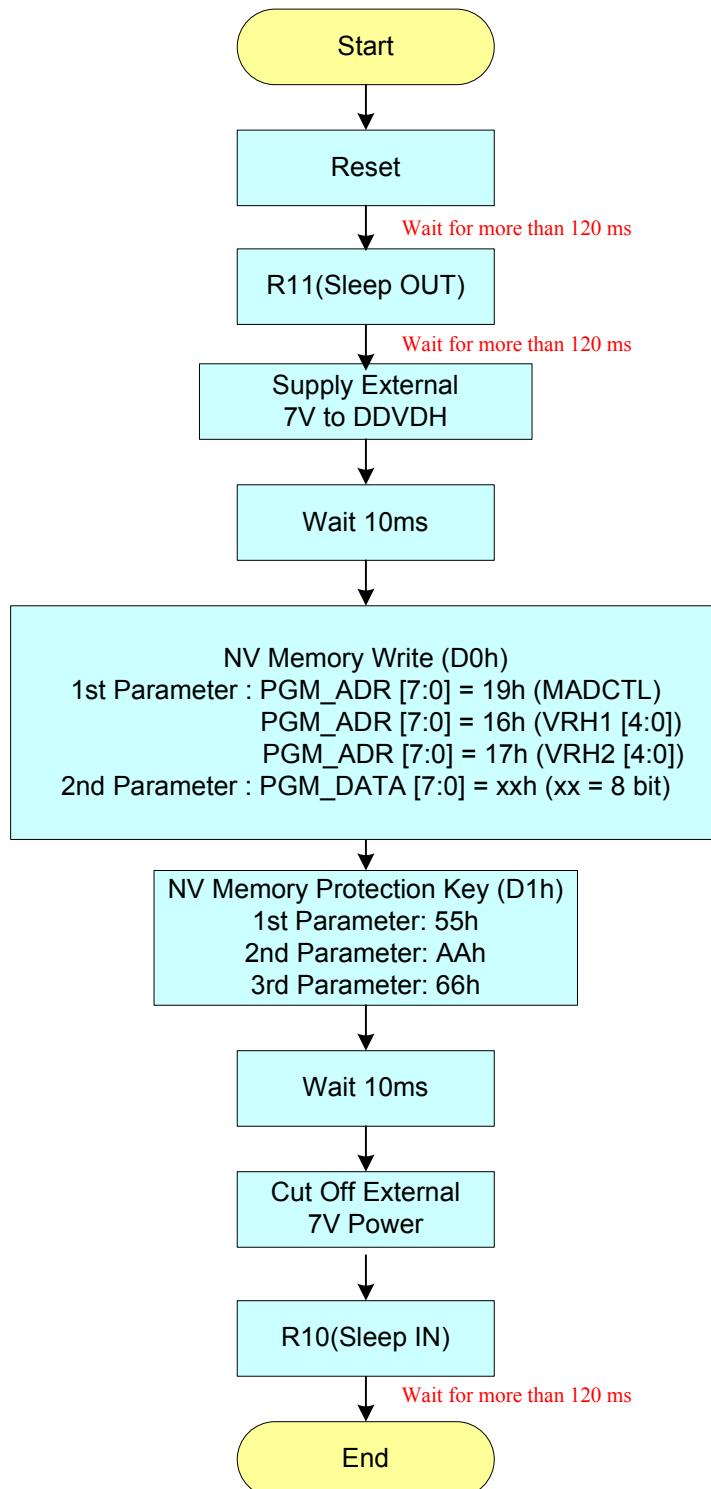


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14.2. BT Programming Flow



14.3. VRH1, VRH2 and MADCTL Programming Flow

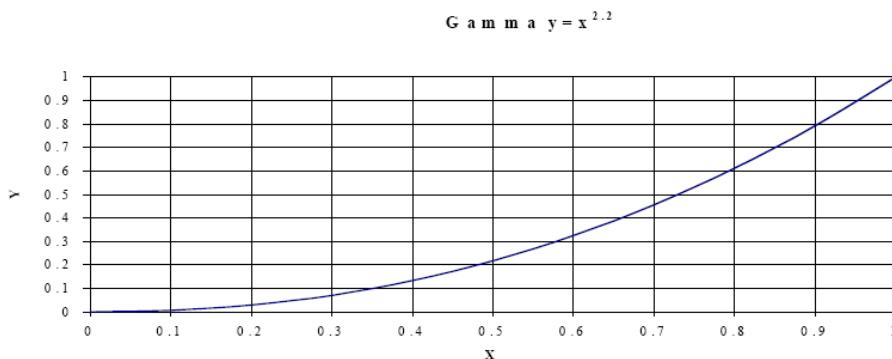


15. GAMMA Correction

The ILI9488 provides one gamma curve (Gamma2.2).

15.1. Gamma Curve

15.1.1. Gamma Curve (GC0), applies the function $y = x^{2.2}$



15.2. Gamma Default Values

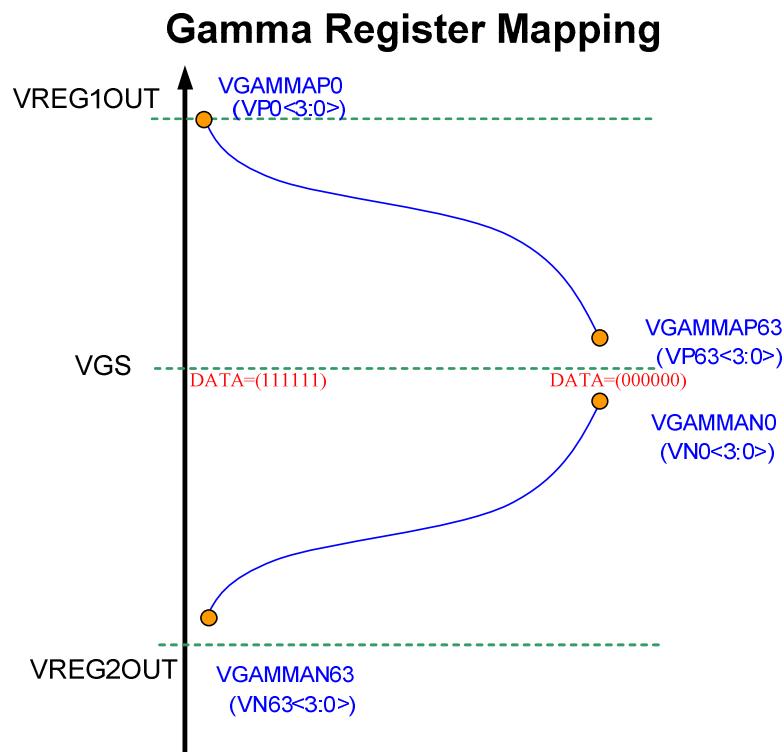


Figure 138:Gamma Register Mapping

15.2.1. Positive Gamma Control (E0h)

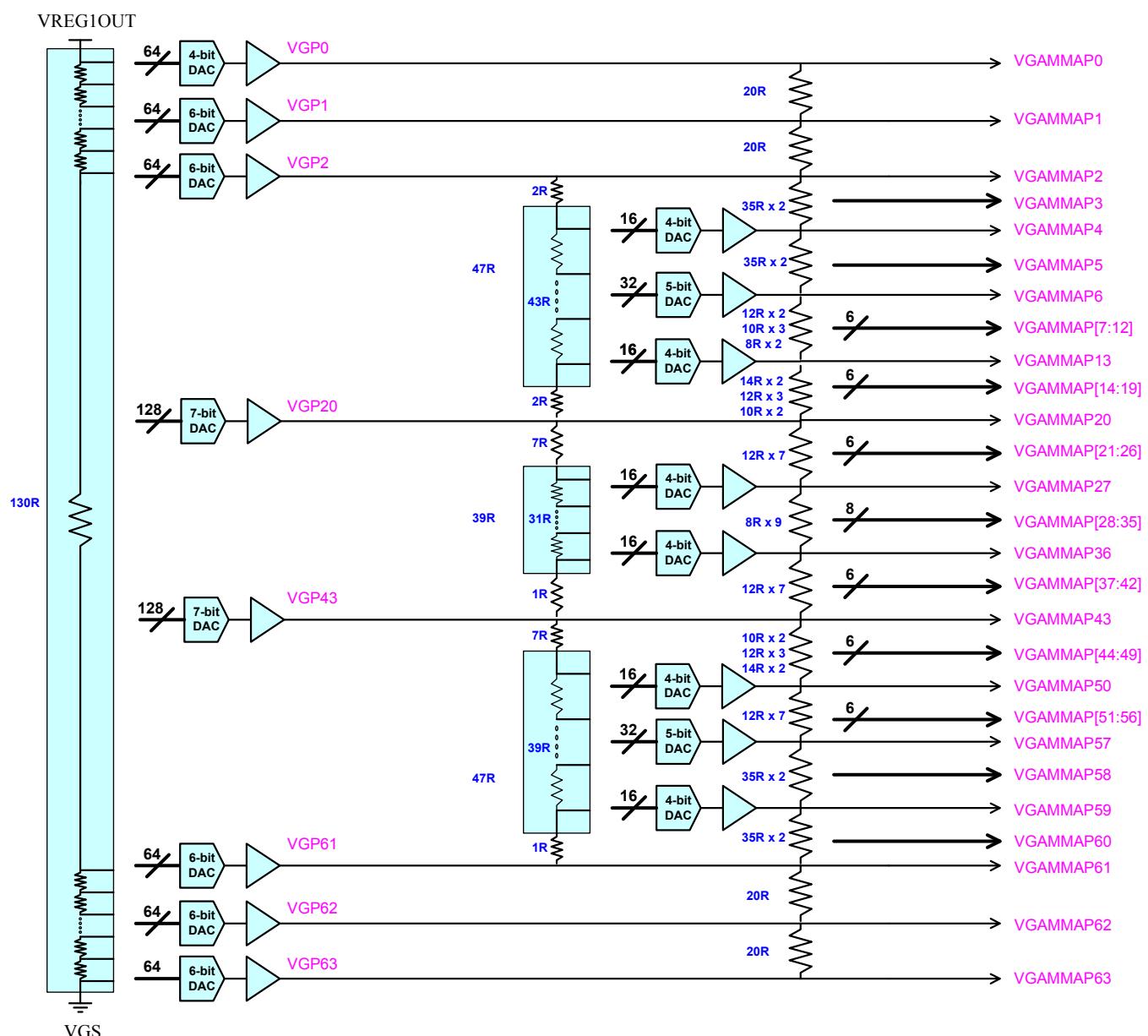


Figure 139: Positive Gamma Control (E0h)

15.2.2. Negative Gamma Control (E1h)

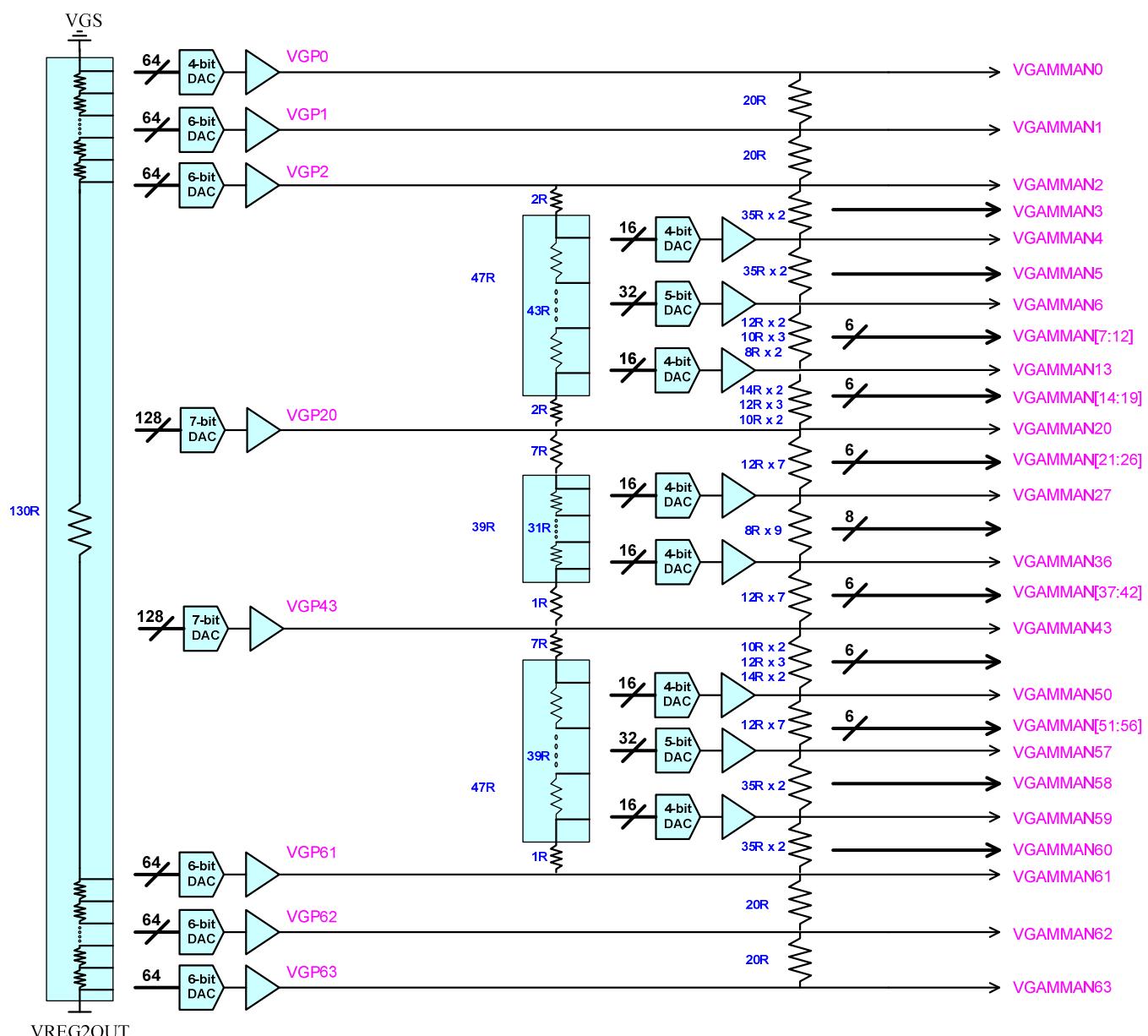


Figure 140: Negative Gamma Control (E1h)

| Positive polarity | Resister stream | Gamma 64 grayscale voltage calculation formula |
|-------------------|-----------------|--|
| VGMMAP0 | | $VGSP + \Delta VDHP(130R - 1R * VP0 [3:0]) / 130R$ |
| VGMMAP1 | | $VGSP + \Delta VDHP(130R - 1R * VP0 [5:0]) / 130R$ |
| VGMMAP2 | 3.5R | $VGSP + \Delta VDHP(130R - 1R * VP0 [5:0]) / 130R$ |
| VGMMAP3 | 3.5R | $VGAMMAP4 + (VGAMMP2 - VGAMMAP4) * (3.5R) / (7R)$ |
| VGMMAP4 | 3.5R | $VGAMMAP20 + (VGAMMAP2 - VGAMMAP20) * ((40R - 1R * VP4 [3:0]) / 47R)$ |
| VGMMAP5 | 3.5R | $VGAMMAP6 + (VGAMMP4 - VGAMMAP6) * (3.5R) / (7R)$ |
| VGMMAP6 | 1.2R | $VGAMMAP20 + (VGAMMAP2 - VGAMMAP20) * ((45R - 1R * VP6 [4:0]) / 47R)$ |
| VGMMAP7 | 1.2R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (5.8R) / (7R)$ |
| VGMMAP8 | 1R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (4.6R) / (7R)$ |
| VGMMAP9 | 1R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (3.6R) / (7R)$ |
| VGMMAP10 | 1R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (2.6R) / (7R)$ |
| VGMMAP11 | 0.8R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (1.6R) / (7R)$ |
| VGMMAP12 | 0.8R | $VGAMMAP13 + (VGAMMP6 - VGAMMAP13) * (0.8R) / (7R)$ |
| VGMMAP13 | 1.4R | $VGAMMAP20 + (VGAMMAP2 - VGAMMAP20) * ((17R - 1R * VP13 [3:0]) / 47R)$ |
| VGMMAP14 | 1.4R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (7R) / (8.4R)$ |
| VGMMAP15 | 1.2R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (5.6R) / (8.4R)$ |
| VGMMAP16 | 1.2R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (4.4R) / (8.4R)$ |
| VGMMAP17 | 1.2R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (3.2R) / (8.4R)$ |
| VGMMAP18 | 1R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (2R) / (8.4R)$ |
| VGMMAP19 | 1R | $VGAMMAP20 + (VGAMMP13 - VGAMMAP20) * (1R) / (8.4R)$ |
| VGMMAP20 | 1.2R | $VGSP + \Delta VDHP(130R - 1R * VP20 [6:0]) / 130R : VP20 [6:0] = 0 \sim 63$ $VGSP + \Delta VDHP(129R - 1R * VP20 [6:0]) / 130R : VP20 [6:0] = 64 \sim 127$ |
| VGMMAP21 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (7.2R) / (8.4R)$ |
| VGMMAP22 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (6R) / (8.4R)$ |
| VGMMAP23 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (4.8R) / (8.4R)$ |
| VGMMAP24 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (3.6R) / (8.4R)$ |
| VGMMAP25 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (2.4R) / (8.4R)$ |
| VGMMAP26 | 1.2R | $VGAMMAP27 + (VGAMMP20 - VGAMMAP27) * (1.2R) / (8.4R)$ |
| VGMMAP27 | 1.2R | $VGAMMAP43 + (VGAMMAP20 - VGAMMAP43) * ((32R - 1R * VP27 [3:0]) / 39R)$ |
| VGMMAP28 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (9.6R) / (10.8R)$ |
| VGMMAP29 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (8.4R) / (10.8R)$ |
| VGMMAP30 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (7.2R) / (10.8R)$ |
| VGMMAP31 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (6R) / (10.8R)$ |
| VGMMAP32 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (4.8R) / (10.8R)$ |
| VGMMAP33 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (3.6R) / (10.8R)$ |
| VGMMAP34 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (2.4R) / (10.8R)$ |
| VGMMAP35 | 1.2R | $VGAMMAP36 + (VGAMMP27 - VGAMMAP36) * (1.2R) / (10.8R)$ |

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| | | |
|----------|------|--|
| VGMMAP36 | 1.2R | VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((16R-1R*VP36 [3:0])/39R) |
| VGMMAP37 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(7.2R)/(8.4R) |
| VGMMAP38 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(6R)/(8.4R) |
| VGMMAP39 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(4.8R)/(8.4R) |
| VGMMAP40 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(3.6R)/(8.4R) |
| VGMMAP41 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(2.4R)/(8.4R) |
| VGMMAP42 | 1.2R | VGAMMAP43+(VGAMMP36-VGAMMAP43)*(1.2R)/(8.4R) |
| VGMMAP43 | 1R | VGSP+ΔVDHP(130R-1R*VP43 [6:0])/130R : VP43 [6:0] = 0~63 VGSP+ΔVDHP(129R-1R*VP43 [6:0])/130R : VP43 [6:0] = 64~127 |
| VGMMAP44 | 1R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(7.4R)/(8.4R) |
| VGMMAP45 | 1.2R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(6.4R)/(8.4R) |
| VGMMAP46 | 1.2R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(5.2R)/(8.4R) |
| VGMMAP47 | 1.2R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(4R)/(8.4R) |
| VGMMAP48 | 1.4R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(2.8R)/(8.4R) |
| VGMMAP49 | 1.4R | VGAMMAP50+(VGAMMP43-VGAMMAP50)*(1.4R)/(8.4R) |
| VGMMAP50 | 0.8R | VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((40R-1R*VP50 [3:0])/47R) |
| VGMMAP51 | 0.8R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(6.2R)/(7R) |
| VGMMAP52 | 1R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(5.4R)/(7R) |
| VGMMAP53 | 1R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(4.4R)/(7R) |
| VGMMAP54 | 1R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(3.4R)/(7R) |
| VGMMAP55 | 1.2R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(2.4R)/(7R) |
| VGMMAP56 | 1.2R | VGAMMAP57+(VGAMMP50-VGAMMAP57)*(1.2R)/(7R) |
| VGMMAP57 | 3.5R | VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((31R-1R*VP57 [3:0])/47R) |
| VGMMAP58 | 3.5R | VGAMMAP59+(VGAMMP57-VGAMMAP59)*(3.5R)/(7R) |
| VGMMAP59 | 3.5R | VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((21R-1R*VP59 [3:0])/47R) |
| VGMMAP60 | 3.5R | VGAMMAP61+(VGAMMP59-VGAMMAP61)*(3.5R)/(7R) |
| VGMMAP61 | | VGSP+ΔVDHP(65R-1R*VP61 [5:0])/130R |
| VGMMAP62 | | VGSP+ΔVDHP(65R-1R*VP62 [5:0])/130R |
| VGMMAP63 | | VGSP+ΔVDHP(23R-1R*VP63 [3:0])/130R |

| Negative polarity | Resister stream | Gamma 64 grayscale voltage calculation formula |
|-------------------|-----------------|--|
| VGMMAN63 | | $VREG2OUT + \Delta VDHN(23R-1R*VN63 [3:0])/130R$ |
| VGMMAN62 | | $VREG2OUT + \Delta VDHN(65R-1R*VN62 [5:0])/130R$ |
| VGMMAN61 | | $VREG2OUT + \Delta VDHN(65R-1R*VN61 [5:0])/130R$ |
| VGMMAN60 | 3.5R | $VGAMMAN61 + (VGAMMP59 - VGAMMAN61)*(3.5R)/(7R)$ |
| VGMMAN59 | 3.5R | $VGAMMAN61 + (VGAMMAN43 - VGAMMAN61)*((21R-1R*VN59 [3:0])/47R)$ |
| VGMMAN58 | 3.5R | $VGAMMAN59 + (VGAMMP57 - VGAMMAN59)*(3.5R)/(7R)$ |
| VGMMAN57 | 3.5R | $VGAMMAN61 + (VGAMMAN43 - VGAMMAN61)*((31R-1R*VN57 [3:0])/47R)$ |
| VGMMAN56 | 1.2R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(1.2R)/(7R)$ |
| VGMMAN55 | 1.2R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(2.4R)/(7R)$ |
| VGMMAN54 | 1R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(3.4R)/(7R)$ |
| VGMMAN53 | 1R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(4.4R)/(7R)$ |
| VGMMAN52 | 1R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(5.4R)/(7R)$ |
| VGMMAN51 | 0.8R | $VGAMMAN57 + (VGAMMP50 - VGAMMAN57)*(6.2R)/(7R)$ |
| VGMMAN50 | 0.8R | $VGAMMAN61 + (VGAMMAN43 - VGAMMAN61)*((40R-1R*VN50 [3:0])/47R)$ |
| VGMMAN49 | 1.4R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(1.4R)/(8.4R)$ |
| VGMMAN48 | 1.4R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(2.8R)/(8.4R)$ |
| VGMMAN47 | 1.2R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(4R)/(8.4R)$ |
| VGMMAN46 | 1.2R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(5.2R)/(8.4R)$ |
| VGMMAN45 | 1.2R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(6.4R)/(8.4R)$ |
| VGMMAN44 | 1R | $VGAMMAN50 + (VGAMMP43 - VGAMMAN50)*(7.4R)/(8.4R)$ |
| VGMMAN43 | 1R | $VREG2OUT + \Delta VDHN(130R-1R*VN43 [5:0])/130R : VN43 [5:0] = 0\sim63$ $VREG2OUT + \Delta VDHN(129R-1R*VN43 [5:0])/130R : VN43 [5:0] = 64\sim127$ |
| VGMMAN42 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(1.2R)/(8.4R)$ |
| VGMMAN41 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(2.4R)/(8.4R)$ |
| VGMMAN40 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(3.6R)/(8.4R)$ |
| VGMMAN39 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(4.8R)/(8.4R)$ |
| VGMMAN38 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(6R)/(8.4R)$ |
| VGMMAN37 | 1.2R | $VGAMMAN43 + (VGAMMP36 - VGAMMAN43)*(7.2R)/(8.4R)$ |
| VGMMAN36 | 1.2R | $VGAMMAN43 + (VGAMMAN20 - VGAMMAN43)*((16R-1R*VN36 [3:0])/39R)$ |
| VGMMAN35 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(1.2R)/(10.8R)$ |
| VGMMAN34 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(2.4R)/(10.8R)$ |
| VGMMAN33 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(3.6R)/(10.8R)$ |
| VGMMAN32 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(4.8R)/(10.8R)$ |
| VGMMAN31 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(6R)/(10.8R)$ |
| VGMMAN30 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(7.2R)/(10.8R)$ |
| VGMMAN29 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(8.4R)/(10.8R)$ |
| VGMMAN28 | 1.2R | $VGAMMAN36 + (VGAMMP27 - VGAMMAN36)*(9.6R)/(10.8R)$ |

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| | | |
|----------|------|--|
| VGMMAN27 | 1.2R | VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((32R-1R*VN27 [3:0])/39R) |
| VGMMAN26 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(1.2R)/(8.4R) |
| VGMMAN25 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(2.4R)/(8.4R) |
| VGMMAN24 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(3.6R)/(8.4R) |
| VGMMAN23 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(4.8R)/(8.4R) |
| VGMMAN22 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(6R)/(8.4R) |
| VGMMAN21 | 1.2R | VGAMMAN27+(VGAMMP20-VGAMMAN27)*(7.2R)/(8.4R) |
| VGMMAN20 | 1.2R | VREG2OUT+ Δ VDHN(130R-1R*VN20 [5:0])/130R : VN20 [5:0] = 0~63 VREG2OUT+ Δ VDHN(129R-1R*VN20 [5:0])/130R : VN20 [5:0] = 64~127 |
| VGMMAN19 | 1R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(1R)/(8.4R) |
| VGMMAN18 | 1R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(2R)/(8.4R) |
| VGMMAN17 | 1.2R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(3.2R)/(8.4R) |
| VGMMAN16 | 1.2R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(4.4R)/(8.4R) |
| VGMMAN15 | 1.2R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(5.6R)/(8.4R) |
| VGMMAN14 | 1.4R | VGAMMAN20+(VGAMMP13-VGAMMAN20)*(7R)/(8.4R) |
| VGMMAN13 | 1.4R | VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((17R-1R*VN13 [3:0])/47R) |
| VGMMAN12 | 0.8R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(0.8R)/(7R) |
| VGMMAN11 | 0.8R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(1.6R)/(7R) |
| VGMMAN10 | 1R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(2.6R)/(7R) |
| VGMMAN9 | 1R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(3.6R)/(7R) |
| VGMMAN8 | 1R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(4.6R)/(7R) |
| VGMMAN7 | 1.2R | VGAMMAN13+(VGAMMP6-VGAMMAN13)*(5.8R)/(7R) |
| VGMMAN6 | 1.2R | VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((45R-1R*VN6 [4:0])/47R) |
| VGMMAN5 | 3.5R | VGAMMAN6+(VGAMMP4-VGAMMAN6)*(3.5R)/(7R) |
| VGMMAN4 | 3.5R | VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((40R-1R*VN4 [3:0])/47R) |
| VGMMAN3 | 3.5R | VGAMMAN4+(VGAMMP2-VGAMMAN4)*(3.5R)/(7R) |
| VGMMAN2 | 3.5R | VREG2OUT+ Δ VDHN(130R-1R*VN2 [5:0])/130R |
| VGMMAN1 | | VREG2OUT+ Δ VDHN(130R-1R*VN1 [5:0])/130R |
| VGMMAN0 | | VREG2OUT+ Δ VDHN(130R-1R*VN0 [3:0])/130R |

16. Deep Standby Mode Setting

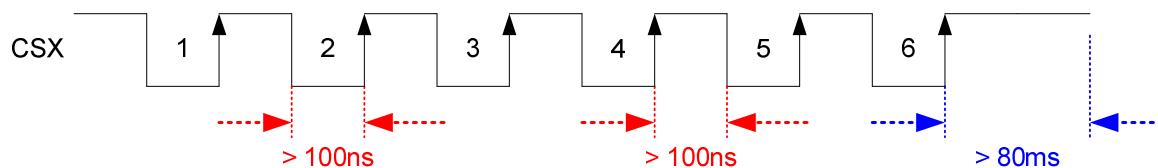
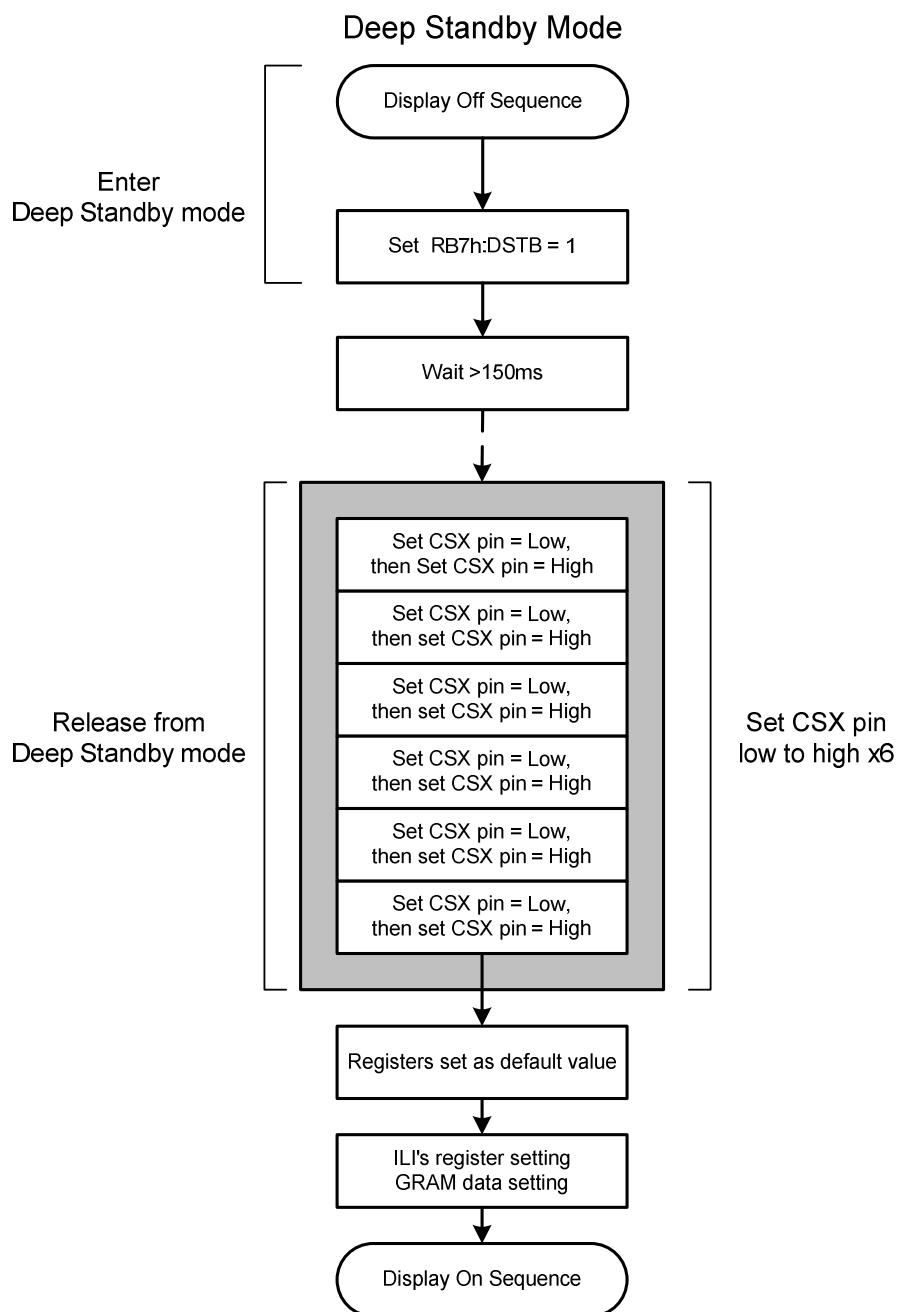


Figure 141: Deep Standby Mode Entry/Exit

17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum ratings are listed in Table 41. When the ILI9488 is used beyond the absolute maximum ratings, it may be permanently damaged. Using the ILI9488 within the following limits of electrical characteristics is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9488 will malfunction and cause poor reliability.

Table 41: Absolute maximum Ratings

| Item | Symbol | Unit | Value |
|------------------------|--------------|------|--------------------|
| Supply voltage(Analog) | VCI ~ DGND | V | -0.3 ~ +3.3 |
| Supply voltage (I/O) | IOVCC ~ DGND | V | -0.3 ~ +3.3 |
| OTP Supply voltage | DDVDH ~ DGND | V | -0.3 ~ +7.0 |
| Supply voltage | DDVDH ~ DGND | V | -0.3 ~ +6.0 |
| Supply voltage | DDVDL ~ DGND | V | 0.3 ~ -6.0 |
| Supply voltage | VGH ~ DGND | V | -0.3 ~ +25 |
| Supply voltage | VGL ~ DGND | V | 0.3 ~ -16 |
| Driver supply voltage | VCI - VCL | V | \leq 6.0V |
| Driver supply voltage | VGH-VGL | V | \leq 32.0V |
| Input voltage | VIN | V | -0.3 ~ IOVCC + 0.3 |
| HS Input voltage | VHSIN | V | -0.3 ~ + 1.65 |
| Operating temperature | Topr | °C | -30 ~ +70 |
| Storage temperature | Tstg | °C | -55 ~ +110 |

Note: Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

17.2. DC Characteristics for Panel Driving

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|--|-------------|--------------------------|-----------|------|--------------|------|-----------|
| Power & Operation Voltage | | | | | | | |
| Analog operating voltage | VCI | - | 2.5 | 2.8 | 3.3 | V | |
| Logic operating voltage | IOVCC | - | 1.65 | 1.8 | 3.3 | V | Note 1, 2 |
| OTP Supply voltage | DDVDH | - | - | 7 | - | V | Note 1 |
| Logic High level input voltage | VIH | - | 0.7*IOVCC | | IOVCC | V | Note 1 |
| Logic Low level input voltage | VIL | - | -0.3 | | 0.3*IOVCC | V | Note 1 |
| Logic High level output voltage TE, SDO (SDA) , CABC_PWM_OUT | VOH | IOH = -1.0mA | 0.8*IOVCC | | IOVCC | V | Note 1 |
| Logic Low level output voltage TE, SDO (SDA) , CABC_PWM_OUT | VOL | IOL = +1.0mA | 0 | | 0.2*IOVCC | V | Note 1 |
| Gate Driver High Voltage | VGH | - | 10.0 | - | 20 | V | |
| Gate Driver Low Voltage | VGL | - | -15.0 | - | -6.0 | V | |
| Driver Supply Voltage | - | VGH-VGL | 16 | - | 32 | V | |
| Input and Output | | | | | | | |
| Logic High Level Input Voltage | VIH | - | 0.7*IOVCC | - | IOVCC | V | |
| Logic Low Level Input Voltage | VIL | - | DGND | - | 0.3*IOVCC | V | |
| VCOM Operation | | | | | | | |
| DC VCOM Amplitude Voltage | VCOM | - | -2.0 | - | -0.06 | V | Note 3 |
| Source Driver | | | | | | | |
| Source Output Range | VSOUT | - | 0.1 | - | VREG1OUT-0.1 | V | Note 4 |
| Positive Gamma Reference Voltage | VREG1OUT | - | 3.625 | - | 5.5 | V | |
| Negative Gamma Reference Voltage | VREG2OUT | - | -5.5 | - | -3.625 | V | |
| Source Output Setting Time | Tr | Below with 99% precision | - | 10 | - | uS | Note 3, 4 |
| Output Deviation Voltage (Source Output channel) | Vdev | Sout>=4.2V Sout<=0.8V | - | - | 20 | mV | Note 3 |
| | | 4.2V>Sout>0.8V | - | - | 15 | mV | - |
| Output Offset Voltage | VOFFSET | - | - | - | 35 | mV | Note 3 |
| Booster Operation | | | | | | | |
| Booster (VClx2) Voltage | DDVDH | - | | | 6 | V | |
| Booster (VClx2) Voltage | DDVDL | - | -6 | | | V | |
| Booster (VClx2 Drop Voltage) | VCl1x2 drop | loading=1mA | - | - | 5 | % | |
| Gate Driver High Voltage | VGH | - | 10.0 | - | 20 | V | |
| Gate Driver Low Voltage | VGL | - | -15.0 | - | -6.0 | V | |
| Standby mode current consumption (Ta = 25 °C, Interface: DBI and DPI) | | | | | | | |
| Sleep in mode | VCI | VCI=2.8V | - | 100 | - | uA | |
| Deep Standby mode | VCI | IOVCC=1.8V | - | 1 | - | uA | |

Notes:

1. Ta = -30 to 70 °C (no damage up to 85°C (at maximum)), IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, DGND=0V.
2. Supply the digital IOVCC voltage equal to or less than the analog VCI voltage.
3. Source channel loading = 10KΩ, 30pF/channel
4. The maximum value is between 10KΩ, 30pF/channel and Gamma setting value.

17.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

| State Code | Line DC Voltage Levels | |
|------------|------------------------|-------------------|
| | CLOCK_P or DATA_N | CLOCK_N or DATA_P |
| HS-0 | Low (HS) | High (HS) |
| HS-1 | High (HS) | Low (HS) |
| LP-00 | Low (LP) | Low (LP) |
| LP-01 | Low (LP) | High (LP) |
| LP-10 | High (LP) | Low (LP) |
| LP-11 | High (LP) | Low (LP) |

Note: Ta = -30°C to 70°C (no damage up to 85°C (at maximum))

17.3.1. DC Characteristics for Power Lines

| Parameter | Symbol | Condition | Specification | | | Unit |
|-----------------------------------|--------------------------|---|---------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Analog power supply voltage | V _{CI} | Operating voltage | 2.5 | 2.8 | 3.3 | V |
| Digital power supply voltage | V _{IOVCC} | I/O supply voltage | 1.65 | 1.8 | 3.3 | V |
| Analog power supply voltage noise | V _{VCI_NOISE} | Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak) | - | - | 100 | mV |
| | | Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%) | - | - | 500 | mV |
| I/O power supply voltage noise | V _{IOVCC_NOISE} | Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak) | - | - | 100 | mV |

Notes:

1. Ta = -30°C to 70°C (no damage up to 85°C (at maximum))
2. These values are not symmetric amplitude, which center points are IOVCC or VCI. See examples, when V_{VCI_NOISE} and V_{IOVCC_NOISE} are maximums, below for reference purpose.

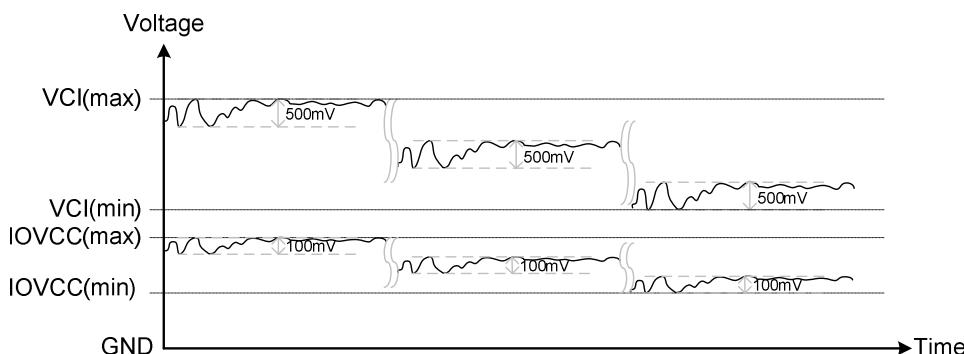


Figure 142: Noise on Power Supply Lines

17.3.2. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10, and LP-11 are defined in the table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD, or LP-TX is mentioned in the condition column. Other logical levels in the table are for the MCU interface.

| Parameter | Symbol | Condition | Specification | | | Unit |
|---------------------------------|-----------------|--|-----------------|---|-----------------|------|
| Logic High level output voltage | V_{OH} | $I_{OUT} = -1mA^{Note\ 2}$ | 0.8 V_{IOVCC} | - | V_{IOVCC} | V |
| Logic Low level output voltage | V_{OL} | $I_{OUT} = -1mA^{Note\ 2}$ | 0.0 | - | 0.2 V_{IOVCC} | V |
| Logic High level input voltage | V_{IHLPCD} | LP-CD ^{Note 3} | 450 | - | 1350 | mV |
| Logic Low level input voltage | V_{ILLPCD} | LP-CD ^{Note 3} | 0.0 | - | 200 | mV |
| Logic High level input voltage | V_{IHLPRX} | LP-RX (CLOCK, DATA) ^{Note 3} | 880 | - | 1350 | mV |
| Logic Low level input voltage | V_{ILLPRX} | LP-RX (CLOCK, DATA) ^{Note 3} | 0.0 | - | 550 | mV |
| Logic Low level input voltage | $V_{ILLPRXULP}$ | LP-RX (CLOCK ULP mode) ^{Note 3} | 0.0 | - | 300 | mV |
| Logic high level output voltage | V_{OHLPTX} | LP-TX (DATA) ^{Note 3} | 1.1 | - | 1.3 | V |
| Logic Low level output voltage | V_{OLLPTX} | LP-TX (DATA) ^{Note 3} | -50 | - | 50 | mV |
| Logic High level input current | I_{IH} | LP-CD, LP-RX ^{Note 3} | - | - | 10 | uA |
| Logic Low level input current | I_{IL} | LP-CD, LP-RX ^{Note 3} | -10 | - | - | uA |

Notes:

1. $T_a = -30^\circ C$ to $70^\circ C$ (no damage up to $85^\circ C$ (at maximum))

2. PWM_OUT, TE signals

3. DSI High Speed mode is Off.

17.3.3. Spike/Glitch Rejection

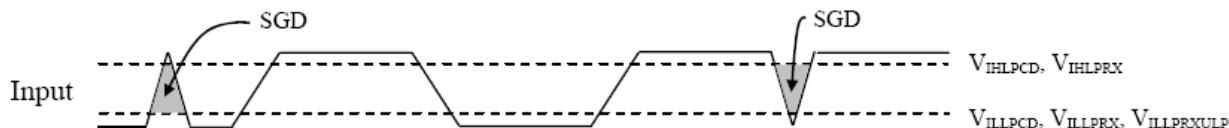


Figure 143: Spike/Glitch Rejection

Note: A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and the Interference Frequency is 450 MHz (at the very least).

Table 42: Spike/Glitch Rejection

| Spike/Glitch Rejection – DSI | | | | | |
|----------------------------------|--------|-------------------------------|-----|-----|------|
| Signal | Symbol | Parameter | Min | Max | Unit |
| MIPI_DATA_P/N, MIPI_CLOCK_P/N | SGD | Input pulse rejection for DSI | - | 300 | Vps |

17.3.4. DC Characteristics for DSI HS Mode

DC levels of the HS-0 and HS-0 are defined in the table below:

Table 43: DC Characteristics for DSI HS Mode

| Parameter | Symbol | Condition | Specification | | | Unit |
|--|-------------------|--|---------------|-----|-----|----------|
| Input Common Mode Voltage for Clock | V_{CMCLK} | MIPI_CLOCK_P/N ^{Note 2,3} | 70 | - | 330 | mV |
| Input Common Mode Voltage for Data | V_{CMDATA} | MIPI_DATA_P/N ^{Note 2,3} | 70 | - | 330 | mV |
| Common Mode Ripple for Clock Equal or Less than 450MHz | $V_{CMRCLKL450}$ | MIPI_CLOCK_P/N ^{Note 4} | -50 | - | 50 | mV |
| Common Mode Ripple for Data Equal or Less than 450MHz | $V_{CMRDATAL450}$ | MIPI_DATA_P/N ^{Note 4} | -50 | - | 50 | mV |
| Common Mode Ripple for Clock More than 450MHz (peak sine wave) | $V_{CMRCLKM450}$ | MIPI_CLOCK_P/N | - | - | 100 | mV |
| Common Mode Ripple for Data More than 450MHz (peak sine wave) | $V_{CMRDATAM450}$ | MIPI_DATA_P/N | - | - | 100 | mV |
| Differential Input Low Level Threshold Voltage for Clock | $V_{THLCLK-}$ | MIPI_CLOCK_P/N | -70 | - | - | mV |
| Differential Input Low Level Threshold Voltage for Data | $V_{THLDATA-}$ | MIPI_DATA_P/N | -70 | - | - | mV |
| Differential Input High Level Threshold Voltage for Clock | $V_{THHCLK+}$ | MIPI_CLOCK_P/N | - | - | 70 | mV |
| Differential Input High Level Threshold Voltage for Data | $V_{THHDATA+}$ | MIPI_DATA_P/N | - | - | 70 | mV |
| Single-ended Input Low Voltage | V_{ILHS} | MIPI_CLOCK_P/N, MIPI_DATA_P/N ^{Note 3} | -40 | - | - | mV |
| Single-ended Input High Voltage | V_{IHHS} | MIPI_CLOCK_P/N, MIPI_DATA_P/N ^{Note 3} | - | - | 460 | mV |
| Differential Termination Resistor | R_{TERM} | MIPI_CLOCK_P/N, MIPI_DATA_P/N | 80 | 100 | 125 | Ω |
| Single-ended Threshold Voltage for Termination Enable | $V_{TERM-EN}$ | MIPI_CLOCK_P/N, MIPI_DATA_P/N | - | - | 450 | mV |
| Termination Capacitor | C_{TERM} | MIPI_CLOCK_P/N, MIPI_DATA_P/N | - | - | 14 | pF |

Notes:

1. $T_a = -30$ to 70 °C (no damage up to 85 °C (at maximum)), $IOVCC = 1.65$ to 3.3 V, $GND = 0$ V
2. Includes 50mV (-50mV to 50mV) ground difference
3. Without VCMRCLKM450/VMRDATAM450
4. Without 50mV (-50mV to 50mV) ground difference

The DSI receiver (HS mode) realizes that there is logical 1 (HS-1) when a differential voltage is more than V_{THH} (CLOCK_P/DATA_P). The DSI receiver (HS mode) realizes that there is logical 0 (HS-0) when a differential voltage is more than V_{THL} (CLOCK_N/DATA_N). There is an undefined state if the differential voltage is less than V_{THH} (CLOCK_P/DATA_P) and less than V_{THL} (CLOCK_N/DATA_N). A reference figure is below.

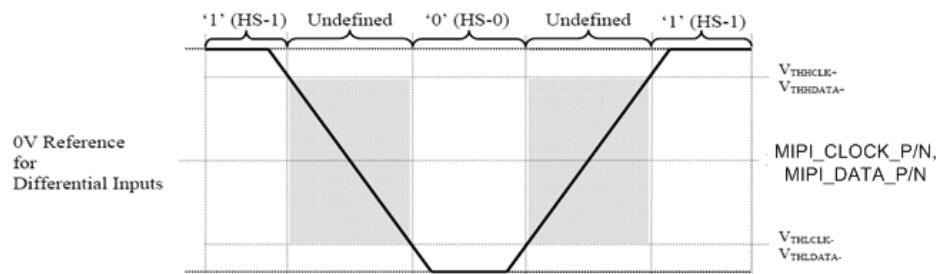


Figure 144: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range

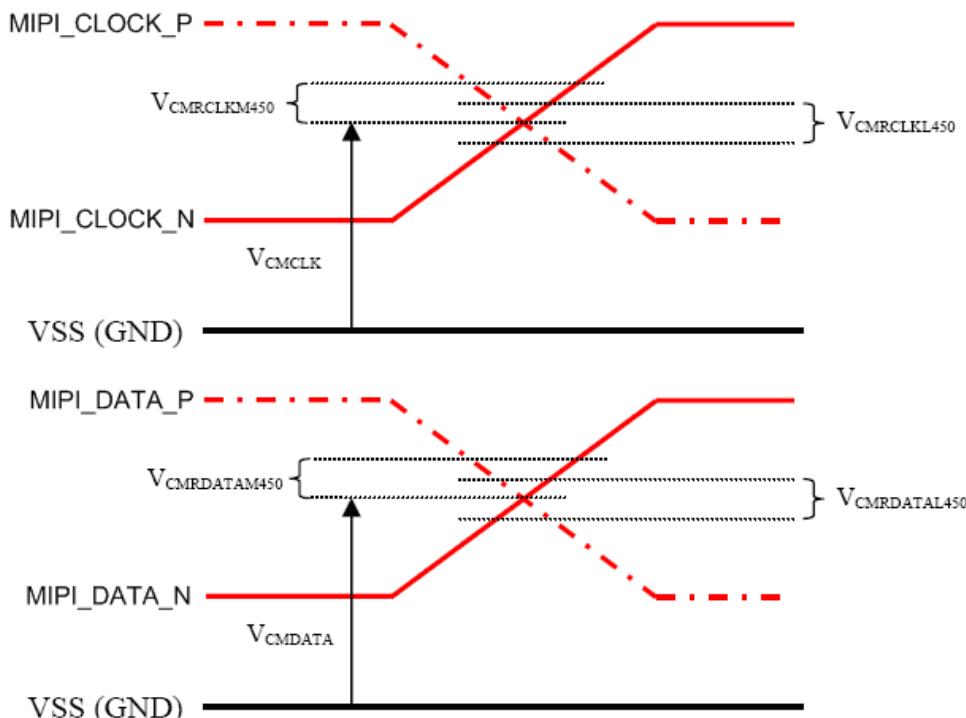


Figure 145: Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (MIPI_CLOCK_P <=> MIPI_CLOCK_N or MIPI_DATA_P <=> MIPI_DATA_N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (MIPI_CLOCK_P <=> MIPI_CLOCK_N or MIPI_DATA_P <=> MIPI_DATA_N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

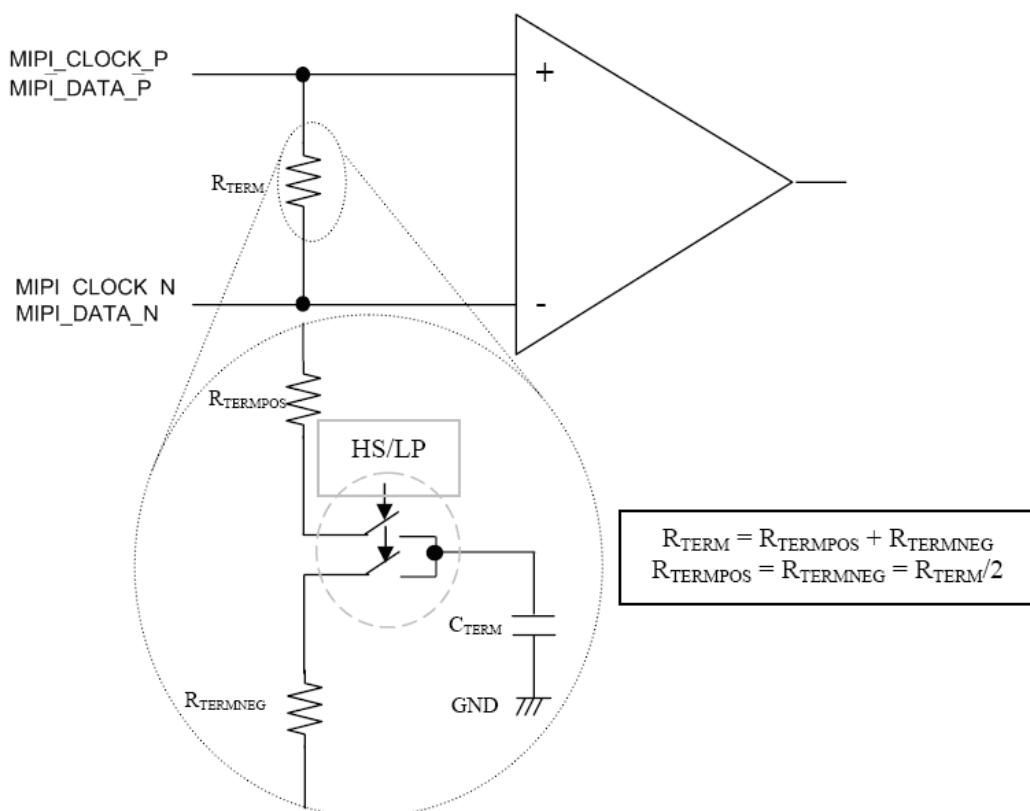
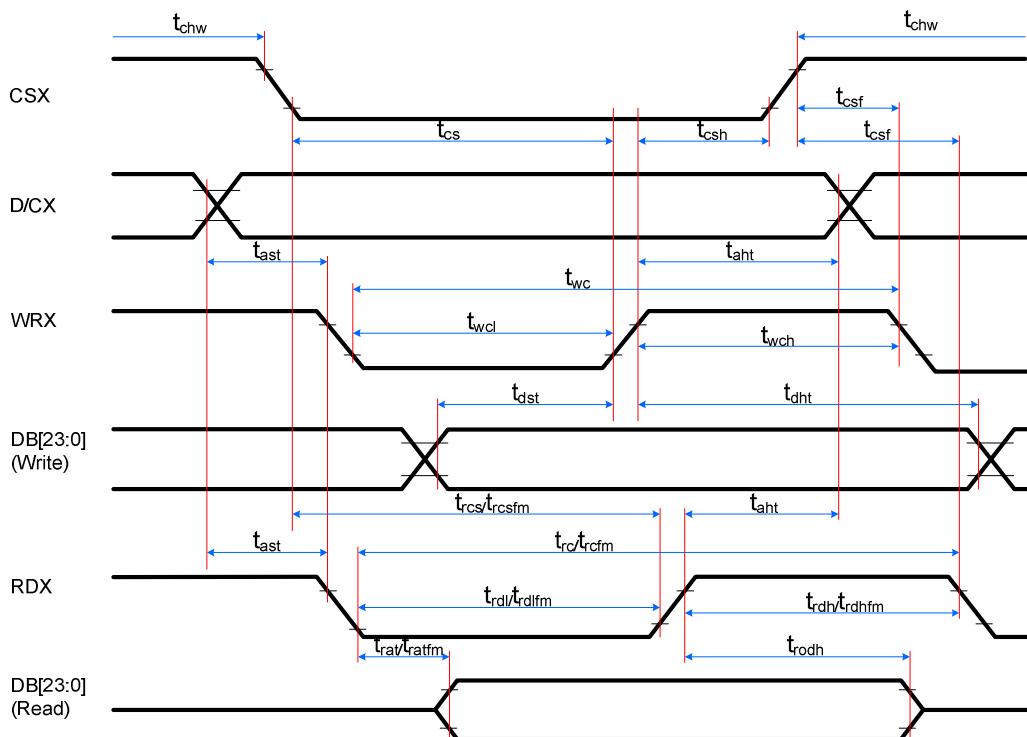


Figure 146: Differential Pair Termination Resister on the Receiver Side

17.4. AC Characteristics

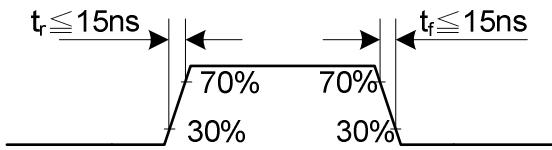
17.4.1. DBI Type B (Display Parallel 8-/9-/16-/18-/24-bit interface) Timing Characteristics



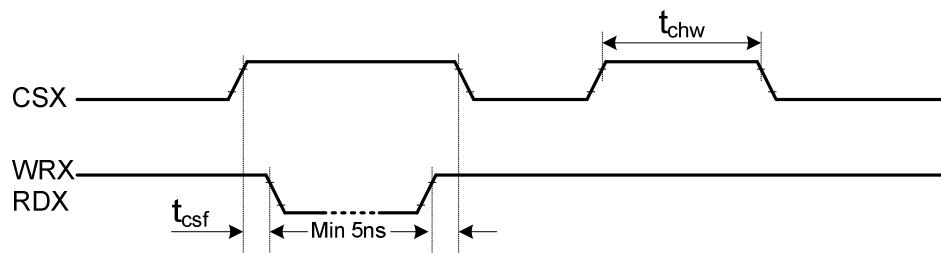
| Signal | Symbol | Parameter | min | max | Unit | Description |
|---|---------------------|------------------------------------|-----|-----|------|---|
| DCX | t _{tast} | Address setup time | 0 | - | ns | - |
| | t _{that} | Address hold time (Write/Read) | 0 | - | ns | - |
| CSX | t _{chw} | CSX "H" pulse width | 0 | - | ns | - |
| | t _{cs} | Chip Select setup time (Write) | 15 | - | ns | - |
| | t _{trcs} | Chip Select setup time (Read ID) | 45 | - | ns | - |
| | t _{trcsfm} | Chip Select setup time (Read FM) | 355 | - | ns | - |
| | t _{csf} | Chip Select Wait time (Write/Read) | 0 | - | ns | - |
| | t _{twc} | Write cycle | 30 | - | ns | - |
| WRX | t _{twrh} | Write Control pulse H duration | 15 | - | ns | - |
| | t _{twrl} | Write Control pulse L duration | 15 | - | ns | - |
| | t _{trcfm} | Read Cycle (FM) | 450 | - | ns | When read from Frame Memory |
| RDX (FM) | t _{trdhfm} | Read Control H duration (FM) | 90 | - | ns | |
| | t _{trdlfm} | Read Control L duration (FM) | 355 | - | ns | |
| | t _{trc} | Read cycle (ID) | 160 | - | ns | When read ID data |
| RDX (ID) | t _{trdh} | Read Control pulse H duration | 90 | - | ns | |
| | t _{trdl} | Read Control pulse L duration | 45 | - | ns | |
| | t _{tdst} | Write data setup time | 10 | - | ns | For maximum, CL=30pF For minimum, CL=8pF |
| DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0] | t _{tdht} | Write data hold time | 10 | - | ns | |
| | t _{trat} | Read access time | - | 40 | ns | |
| | t _{tratfm} | Read access time | - | 340 | ns | |
| | t _{trod} | Read output disable time | 20 | 80 | ns | |

Notes:

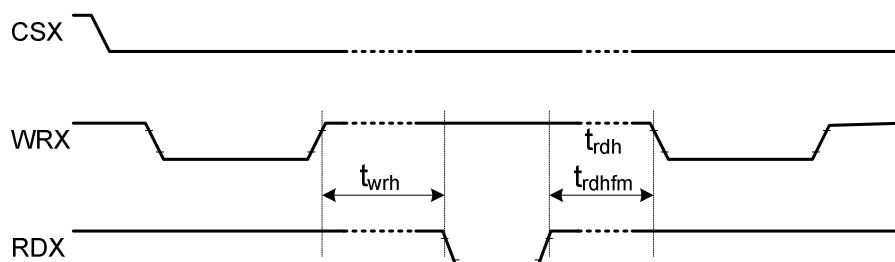
1. $T_a = -30$ to 70 °C, $IOVCC = 1.65V$ to $3.3V$, $VCI = 2.5V$ to $3.3V$, $AGND = DGND = 0V$
2. Logic high and low levels are specified as 30% and 70% of $IOVCC$ for input signals.
3. Input signal rising time and falling time:



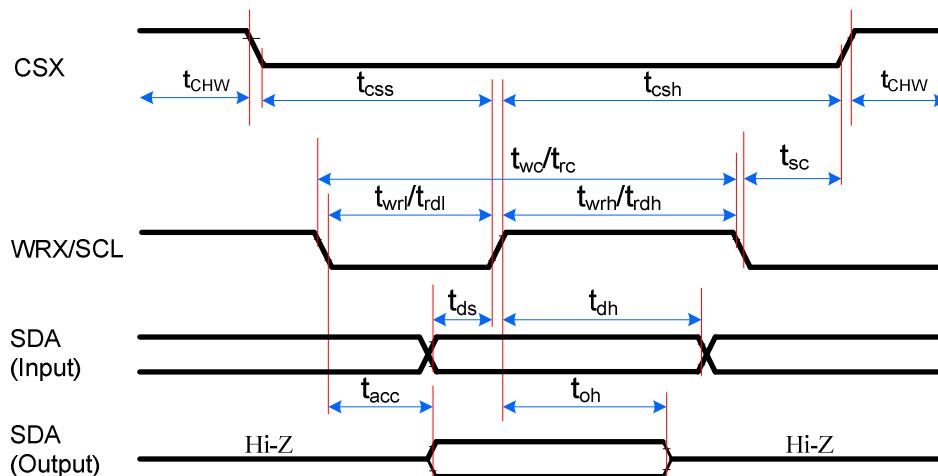
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

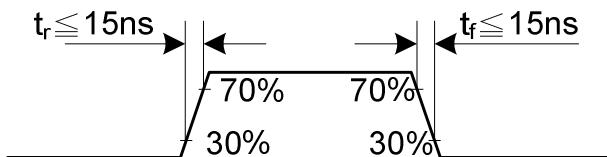


17.4.2. DBI Type C Option 1 (3-Line SPI System) Timing Characteristics

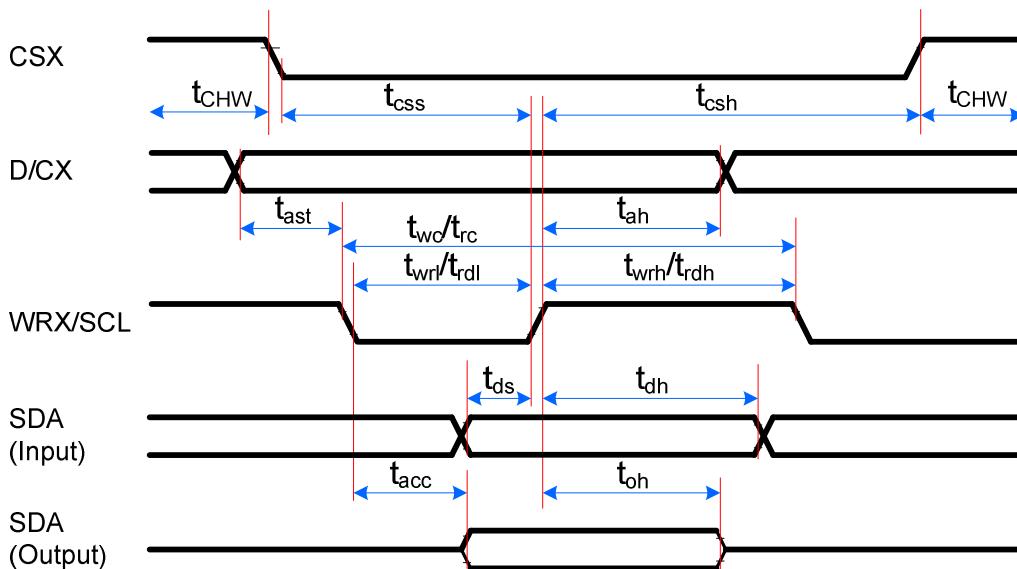


| Signal | Symbol | Parameter | min | max | Unit | Description |
|---------------------|--------|------------------------------|-----|-----|------|---|
| CSX | tsc | SCL-CSX | 15 | - | ns | |
| | tchw | CSX H Pulse Width | 40 | - | ns | |
| | tcss | Chip select time (Write) | 60 | - | ns | |
| | tcsh | Chip select hold time (Read) | 65 | - | ns | |
| SCL | twc | Serial Clock Cycle (Write) | 66 | - | ns | |
| | twrh | SCL H Pulse Width (Write) | 15 | - | ns | |
| | twrl | SCL L Pulse Width (Write) | 15 | - | ns | |
| | trc | Serial Clock Cycle (Read) | 150 | - | ns | |
| | trdh | SCL H Pulse Width (Read) | 60 | - | ns | |
| | trdl | SCL L Pulse Width (Read) | 60 | - | ns | |
| SDA/SDI (Input) | tds | Data setup time (Write) | 10 | - | ns | |
| | tdh | Data hold time (Write) | 10 | - | ns | |
| SDA/DDO (Output) | tacc | Access time (Read) | 10 | 50 | ns | For maximum CL=30pF For minimum CL=8pF |
| | toh | Output disable time (Read) | 15 | 50 | ns | |

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



17.4.3. DBI Type C Option 3 (4-Line SPI System) Timing Characteristics

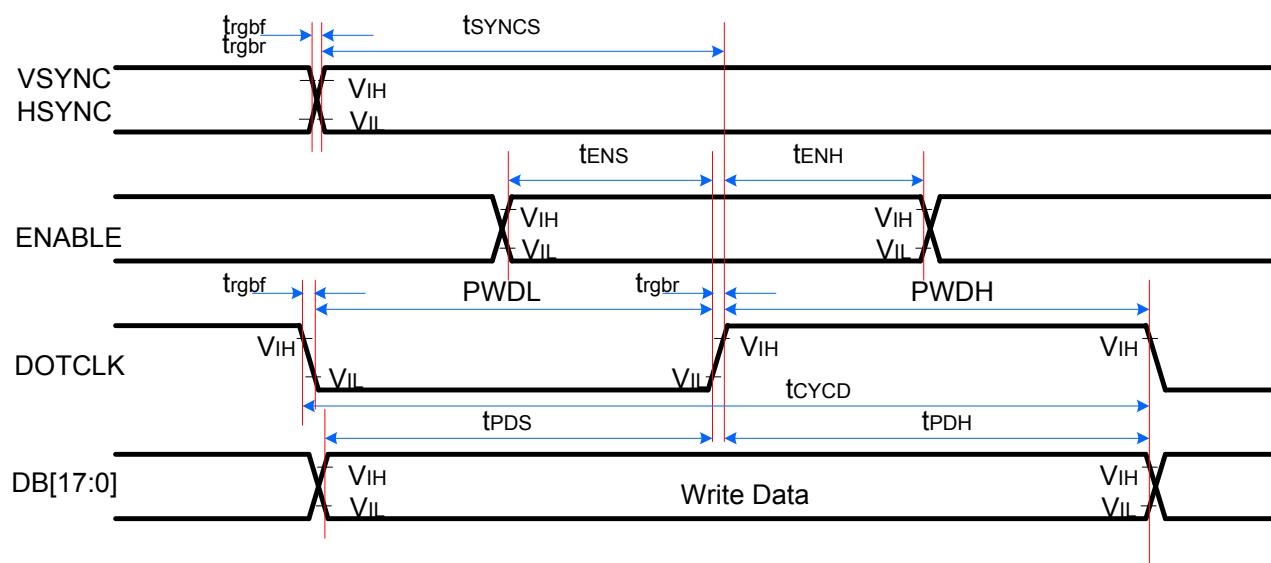


| Signal | Symbol | Parameter | min | max | Unit | Description |
|---------------------|-----------|------------------------------|-----|-----|------|---------------------|
| CSX | t_{css} | Chip select time (Write) | 15 | - | ns | |
| | t_{csh} | Chip select hold time (Read) | 15 | - | ns | |
| | t_{CHW} | CS H pulse width | 40 | - | ns | |
| SCL | t_{wc} | Serial clock cycle (Write) | 50 | - | ns | |
| | t_{wrh} | SCL H pulse width (Write) | 10 | - | ns | |
| | t_{wrh} | SCL L pulse width (Write) | 10 | - | ns | |
| | t_{rc} | Serial clock cycle (Read) | 150 | - | ns | |
| | t_{rdh} | SCL H pulse width (Read) | 60 | - | ns | |
| | t_{rdl} | SCL L pulse width (Read) | 60 | - | ns | |
| D/CX | t_{as} | D/CX setup time | 10 | - | ns | |
| | t_{ah} | D/CX hold time (Write/Read) | 10 | - | ns | |
| SDA/SDI (Input) | t_{ds} | Data setup time (Write) | 10 | - | ns | |
| | t_{dh} | Data hold time (Write) | 10 | - | ns | |
| SDA/SDO (Output) | t_{acc} | Access time (Read) | 10 | 50 | ns | For maximum CL=30pF |
| | t_{od} | Output disable time (Read) | 15 | 50 | ns | For minimum CL=8pF |

Notes:

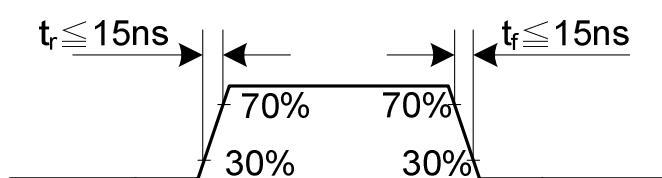
1. $T_a = -30$ to 70 °C, $IOVCC = 1.65V$ to $3.3V$, $VCI = 2.5V$ to $3.3V$, $AGND = DGND = 0V$, $T = 10\pm 0.5ns$.
2. Does not include signal rising and falling times.

17.4.4. DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description |
|-----------------|--------------------|-------------------------------------|-----|-----|------|--|
| VSYNC/ HSYNC | t _{SYNCS} | VSYNC/HSYNC setup time | 15 | - | ns | 16-/18-/24-bit bus RGB interface mode |
| | t _{SYNCH} | VSYNC/HSYNC hold time | 15 | - | ns | |
| ENABLE | t _{ESEN} | ENABLE setup time | 15 | - | ns | 16-/18-/24-bit bus RGB interface mode |
| | t _{ENH} | ENABLE hold time | 15 | - | ns | |
| DB [23:0] | t _{POS} | Data setup time | 15 | - | ns | 16-/18-/24-bit bus RGB interface mode |
| | t _{PDH} | Data hold time | 15 | - | ns | |
| DOTCLK | PWDH | DOTCLK high-level period | 20 | - | ns | 16-/18-/24-bit bus RGB interface mode |
| | PWDL | DOTCLK low-level period | 20 | - | ns | |
| | t _{CYCD} | DOTCLK cycle time | 50 | - | ns | |
| | trgbf, trgbfr | DOTCLK, HSYNC, VSYNC rise/fall time | - | 15 | ns | |

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



17.5. Timing Characteristics of the DSI

17.5.1. High Speed Mode – Clock Channel Timing

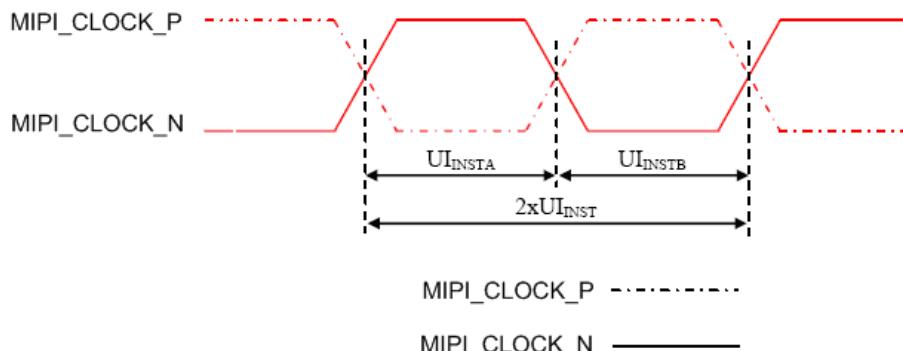


Figure 147: DSI Clock Channel Timing

Table 44: DSI Clock Channel Timing

| Signal | Symbol | Parameter | Min | Max | Unit |
|----------------|--------------------------------------|-------------------------|---------------|------|------|
| MIPI_CLOCK_P/N | $2xUI_{INST}$ | Double UI instantaneous | 4 | 25 | ns |
| MIPI_CLOCK_P/N | UI_{INSTA}, UI_{INSTB} (Note 1) | UI instantaneous Half | 2 (Note 2) | 12.5 | ns |

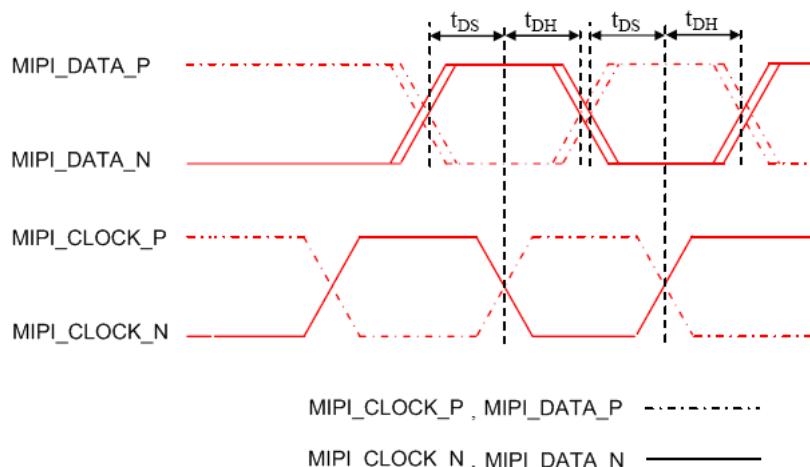
Notes:

1. UI = UIINSTA = UIINSTB
2. See Table 45 for the minimum value of 24 UI per Pixel.

Table 45: Clock Channel Speed Limited

| Data type | One Lanes speed | Unit |
|---|-----------------|------|
| Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel | 500M | bps |
| Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel | 500M | bps |
| Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel | 500M | bps |
| Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel | 500M | bps |

17.5.2. High Speed Mode – Data Clock Channel Timing



| Signal | Symbol | Parameter | Min | Max | Unit |
|---------------|----------|--------------------------|---------|-----|------|
| MIPI_DATA_P/N | t_{DS} | Data to Clock Setup time | 0.15xUI | - | ps |
| MIPI_DATA_P/N | t_{DH} | Clock to Data Hold Time | 0.15xUI | - | ps |

17.5.3. High Speed Mode – Rising and Falling Timings

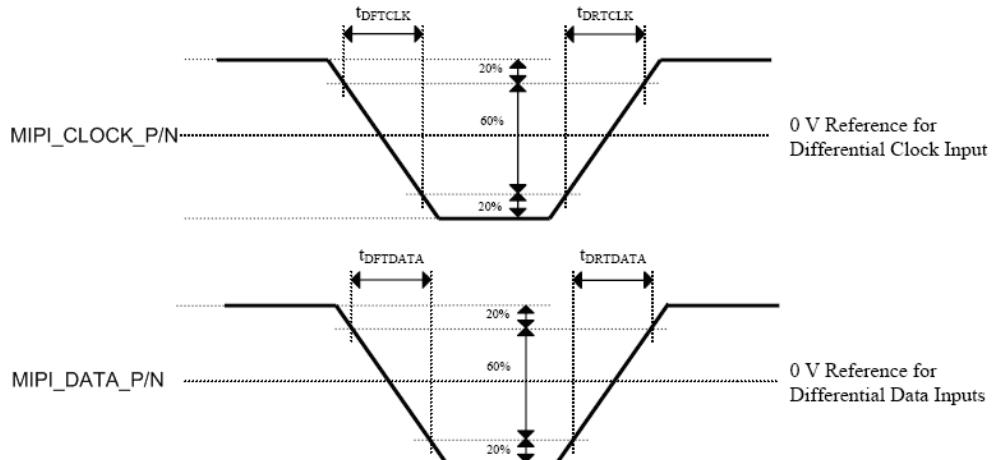


Figure 148: Rising and Falling Timings on Clock and Data Channels

Table 46: Rising and Falling Timings on Clock and Data Channels

| Parameter | Symbol | Condition | Specification | | | |
|----------------------------------|---------------|----------------|---------------|-----|-----|------|
| | | | Min | Typ | Max | Unit |
| Differential Rise Time for Clock | t_{DRTCLK} | MIPI_CLOCK_P/N | - | - | 900 | ps |
| Differential Rise Time for Data | $t_{DRTDATA}$ | MIPI_DATA_P/N | - | - | 900 | ps |
| Differential Fall Time for Clock | t_{DFTCLK} | MIPI_CLOCK_P/N | - | - | 900 | ps |
| Differential Fall Time for Data | $t_{DFTDATA}$ | MIPI_DATA_P/N | - | - | 900 | ps |

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

17.5.4. Low Power Mode – Bus Turnaround

Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the display module (ILI9488) sequence are illustrated below for reference purpose.

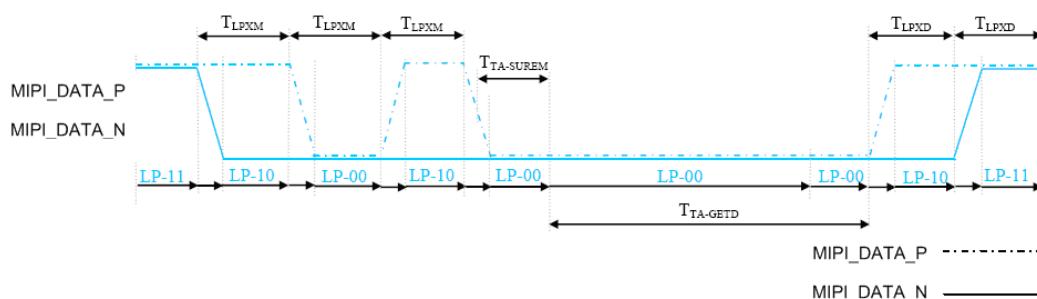


Figure 149: BTA from the MCU to the Display Module

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Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the display module (ILI9488) to the MCU sequence are illustrated below for reference purpose.

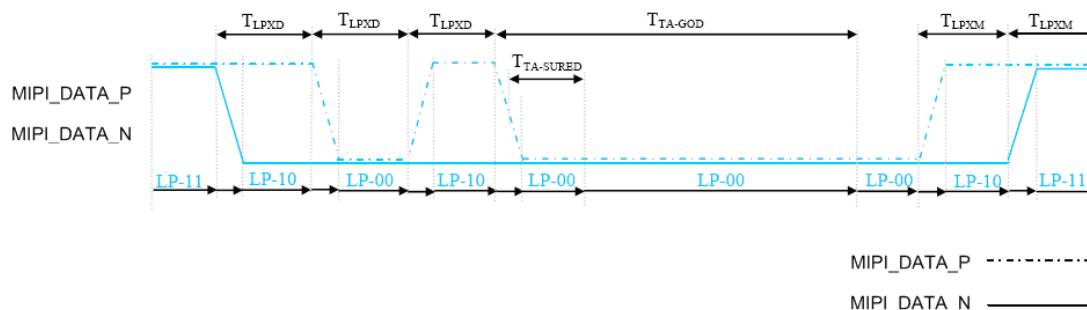


Figure 150: BTA from the Display Module to the MCU

Table 47: Low Power State Period Timings – A

| Signal | Symbol | Description | Min | Max | Unit |
|------------------------|-----------------------|--|-------------------|---------------------|------|
| Input (MIPI_DATA_P/N) | T _{LPXM} | Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9488) | 50 | 75 | ns |
| Output (MIPI_DATA_P/N) | T _{LPXD} | Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9488 → MCU) | 50 | 75 | ns |
| Input (MIPI_DATA_P/N) | T _{TA-SUREM} | Time-out before the ILI9488 starts driving | T _{LPXM} | 2xT _{LPXM} | ns |
| Output (MIPI_DATA_P/N) | T _{TA-SURED} | Time-out before the MCU starts driving | T _{LPXD} | 2xT _{LPXD} | ns |

Table 48: Low Power State Period Timings – B

| Signal | Symbol | Description | Time | Unit |
|------------------------|----------------------|--|---------------------|------|
| Input (MIPI_DATA_P/N) | T _{TA-GETD} | Time to drive LP-00 by the ILI9488 | 5xT _{LPXD} | ns |
| Output (MIPI_DATA_P/N) | T _{TA-GOD} | Time to drive LP-00 after turnaround request – MCU | 4xT _{LPXD} | ns |

17.5.5. Data Lanes from Low Power Mode to High Speed Mode

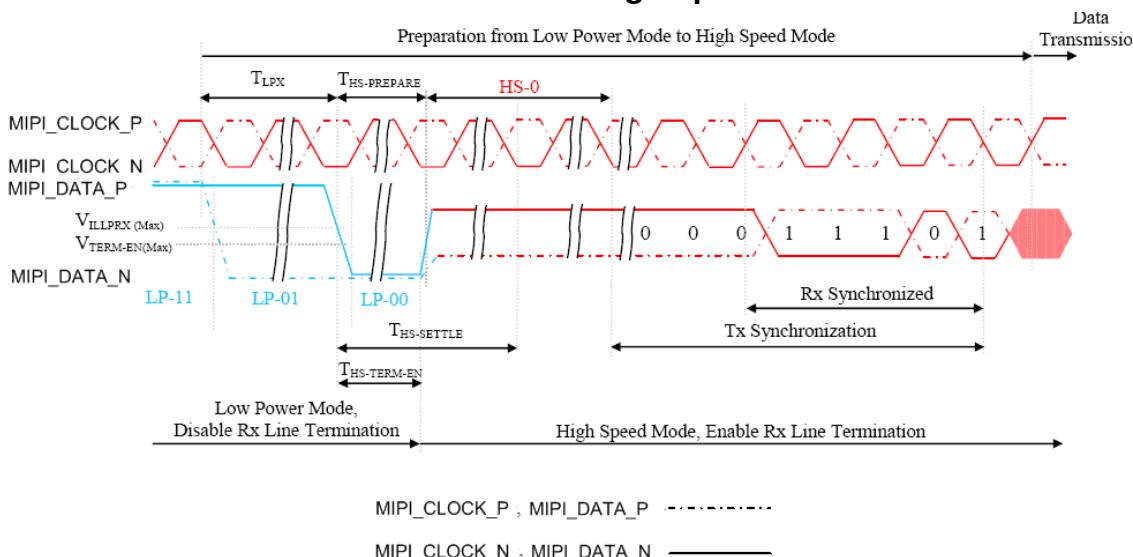


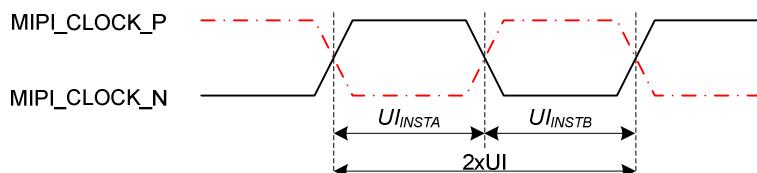
Figure 151: Data Lanes – Low Power Mode to High Speed Mode Timings

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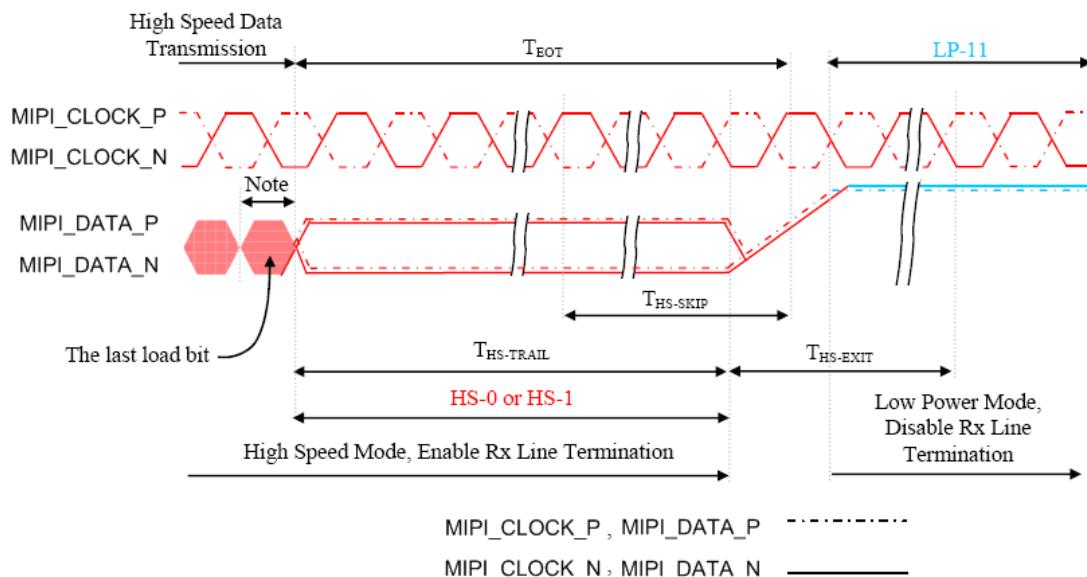
Table 49: Data Lanes – Low Power Mode High Speed Mode Timings

| Signal | Symbol | Description | Min | Max | Unit |
|-----------------------|------------------|---|---------|---------|------|
| Input (MIPI_DATA_P/N) | T_{LPX} | Length of any Low Power State Period | 50 | - | ns |
| Input (MIPI_DATA_P/N) | $T_{HS-PREPARE}$ | Time to Drive LP-00 to prepare for HS Transmission | 40+4xUI | 85+6xUI | ns |
| Input (MIPI_DATA_P/N) | $T_{HS-TERM-EN}$ | Time to enable Data Lane Receiver line termination measured from when D_n crosses V_{ILMAX} | - | 35+4xUI | ns |

Note: UI = $UI_{INSTA} = UI_{INSTB}$



17.5.6. Data Lanes from High Speed Mode to Low Power Mode



Note:

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 152: Data Lanes – High Speed Mode to Low Power Mode Timings
Table 50: Data Lanes – High Speed Mode to Low Power Timings

| Signal | Symbol | Description | Min | Max | Unit |
|-----------------------|---------------|--|-----|---------|------|
| Input (MIPI_DATA_P/N) | $T_{HS-SKIP}$ | Time-out at the ILI9488 to Ignore Transition Period of EoT | 40 | 50+4xUI | ns |
| Input (MIPI_DATA_P/N) | $T_{HS-EXIT}$ | Time to Driver LP-11 after HS burst | 100 | - | ns |

17.5.7. DSI Clock Burst – High Speed Mode to/from Low Power Mode

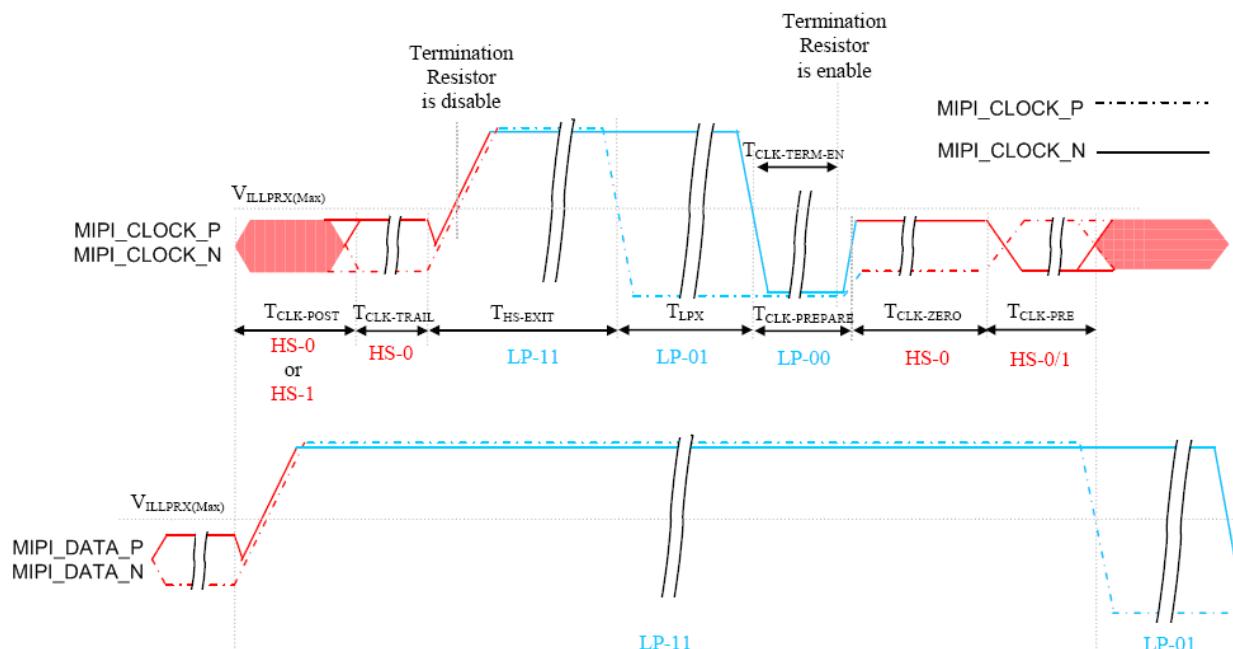
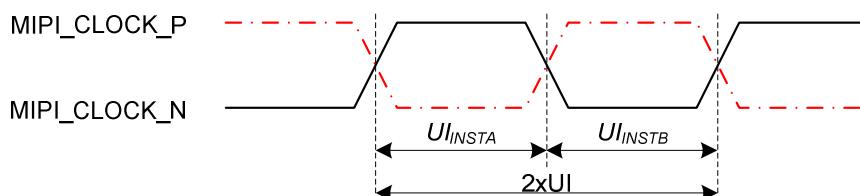


Figure 153: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

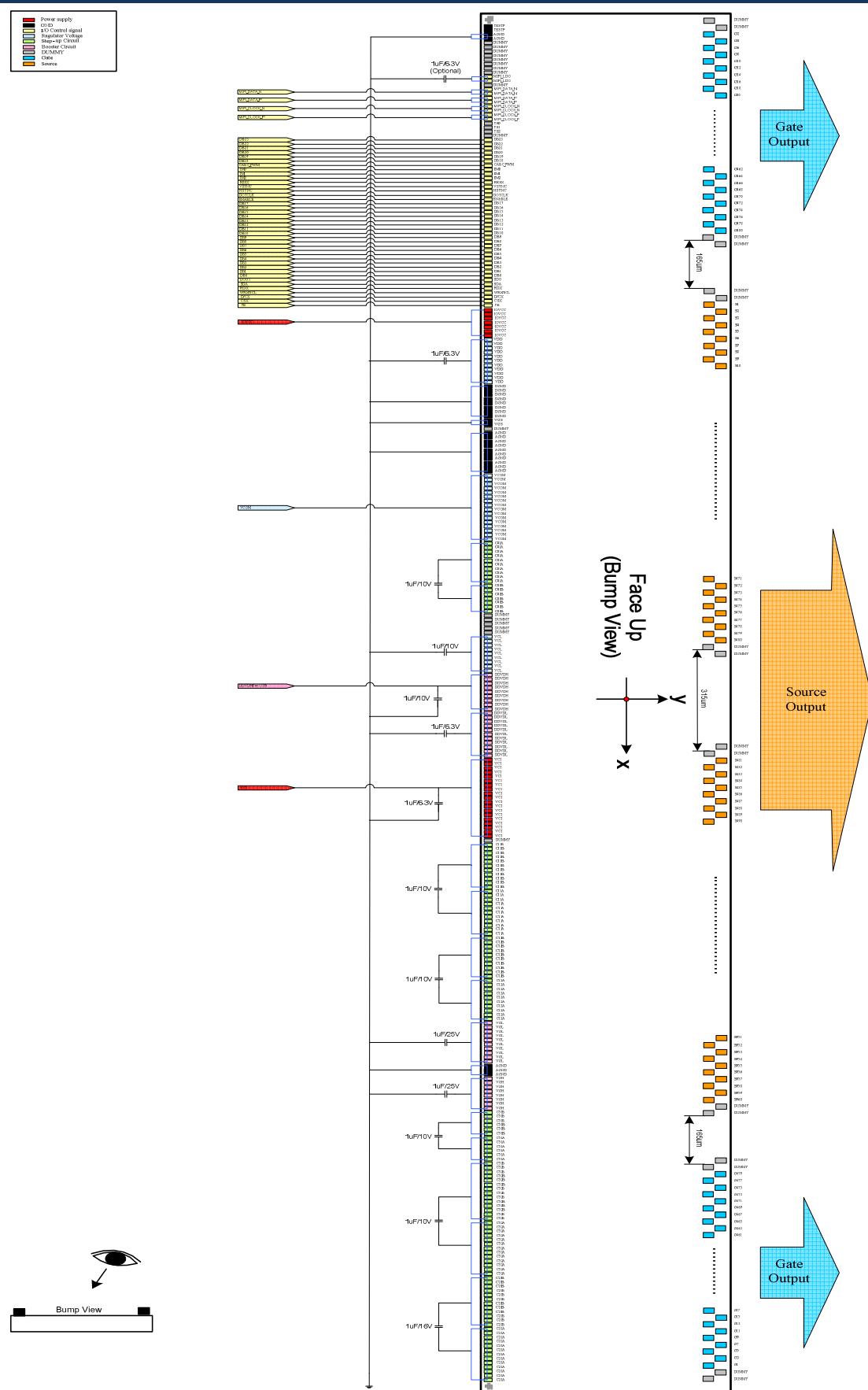
Table 51: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

| Signal | Symbol | Description | Min | Max | Unit |
|------------------------|--------------------------|--|----------|-----|------|
| Input (MIPI_CLOCK_P/N) | T _{CLK-POST} | Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode | 60+52xUI | - | ns |
| Input (MIPI_CLOCK_P/N) | T _{CLK-TRAIL} | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns |
| Input (MIPI_CLOCK_P/N) | T _{HS-EXIT} | Time to drive LP-11 after HS burst | 100 | - | ns |
| Input (MIPI_CLOCK_P/N) | T _{CLK-PREPARE} | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns |
| Input (MIPI_CLOCK_P/N) | T _{CLK-TERM-EN} | Time-out at Clock Lane to enable HS termination | - | 38 | ns |
| Input (MIPI_CLOCK_P/N) | T _{CLK-PREPARE} | Minimum lead HS-0 drive period before starting Clock | 300 | - | ns |
| Input (MIPI_CLOCK_P/N) | T _{CLK-PRE} | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8xUI | - | ns |

Note: UI = UI_{INSTA} = UI_{INSTB}



18. Application Circuit



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18.1. Maximum layout resistance

| Pin Name | Type | Maximum series resistance | Unit |
|------------------|----------------------|---------------------------|------|
| TESTP | DUMMY | 10 | Ω |
| DUMMY | DUMMY | 100 | Ω |
| MIPI_LDO | Power Supply | 10 | Ω |
| MIPI_DATA_N / P | I / O | 10 | Ω |
| MIPI_CLOCK_N / P | Input | 10 | Ω |
| TS0 | DUMMY | 100 | Ω |
| TS1 | DUMMY | 100 | Ω |
| TS2 | DUMMY | 100 | Ω |
| DB[23:0] | I / O | 100 | Ω |
| CABC_PWM | Output | 100 | Ω |
| IM[2:0] | Input | 100 | Ω |
| RESX | Input | 100 | Ω |
| YSYNC | Input | 100 | Ω |
| H SYNC | Input | 100 | Ω |
| DOTCLK | Input | 100 | Ω |
| ENABLE | Input | 100 | Ω |
| SDO | Output | 100 | Ω |
| SDA | I / O | 100 | Ω |
| RDX | Input | 100 | Ω |
| WRX/SCL | Input | 100 | Ω |
| D/CX | Input | 100 | Ω |
| CSX | Input | 100 | Ω |
| TE | Output | 100 | Ω |
| IOVCC | Power Supply | 5 | Ω |
| VDD | Capacitor connection | 5 | Ω |
| DGND | GND | 5 | Ω |
| AGND | GND | 5 | Ω |
| VGS | GND | 10 | Ω |
| C15A/B | Capacitor connection | 5 | Ω |
| DDVDL | Capacitor connection | 5 | Ω |
| DDVDH | Capacitor connection | 5 | Ω |
| VCL | Capacitor connection | 5 | Ω |
| VCI | Power Supply | 5 | Ω |
| C41A/B | Capacitor connection | 5 | Ω |
| VGL | Capacitor connection | 5 | Ω |
| VGH | Capacitor connection | 5 | Ω |
| C11A/B | Capacitor connection | 5 | Ω |
| C12A/B | Capacitor connection | 5 | Ω |
| C51A/B | Capacitor connection | 5 | Ω |
| C52A/B | Capacitor connection | 5 | Ω |
| C21A/B | Capacitor connection | 5 | Ω |
| VCOM | Output | 5 | Ω |

18.2. External Component

The Table 52 shows specifications of external elements connected to the power supply circuit of the ILI9488.

Table 52: External Component Table

| Items | Recommended Specification | Pin connection |
|--------------------|---------------------------|--|
| Capacity 1 μ F | 6.3V | VDD, VCI, MIPI_LDO(optional, for MIPI-DSI only) |
| | 10V | DDVDH, DDVDL, VCL, C41A/B, C11A/B, C15A/B, C51A/C51B, C52A/C52B, C12A/B |
| | 16V | C21A/C21B |
| | 25V | VGH, VGL |

19. Liquid Crystal Power Supply Specifications

Table 53: Liquid Crystal Power Supply Specifications

| Item | Description | |
|-----------------------------------|-----------------------------------|---------------------|
| TFT Source Driver | 960 pins, 320 (RGB) | |
| TFT Gate Driver | 480 pins | |
| TFT Display's Capacitor Structure | Cst structure only (Cs on Common) | |
| Liquid Crystal Drive Output | S1 ~ S960 | V0 ~ V63 grayscales |
| | G1 ~ G480 | VGH – VGL |
| | VCOM | -2.0 ~ 0V |
| Input Voltage | IOVCC | 1.65 ~ 3.30V |
| | VCI | 2.50 ~ 3.30V |
| Liquid Crystal Drive Voltages | DDVDH | 4.5 ~ 6.5V |
| | DDVDL | -6.5 ~ -4.5V |
| | VGH | 10.0V ~ 20.0V |
| | VGL | -15.0V ~ -6.0V |
| | VCL | -3.0V ~ -2.0 V |
| | VGH – VGL | Max. 32.0V |
| Internal Step-up Circuits | VGH | VCI1 x4, x5, x6, |
| | VGL | VCI1 x-3, x-4, x-5 |

20. Revision History

| Version No. | Date | Page | Description |
|-------------|------------|------|-------------|
| V090 | 2012/10/19 | All | New created |
| | | | |
| | | | |