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RESPONSES TO REVIEWERS AND EDITORS

We would like to thank the reviewers and editors for their thoughtful comments and suggestions, which certainly helped us improve the paper. Specific as well as general changes were made based on the reviewers' and editor's comments. Below is a detailed explanation of the changes made to the paper.

CHANGE1

The address of the first author in this paper has been adjusted from "Shaanxi Key Laboratory of Small & Special Electrical Machine and Drive Technology, Northwestern Polytechnical University, Xi'an 710072, China" to "Yangtze River Delta Research Institute of NPU, Taicang; Shaanxi Key Laboratory of Small & Special Electrical Machine and Drive Technology Northwestern Polytechnical University, Xi'an 710072, China;".

CHANGE2

Partially incorrect syntax has been fixed in this paper. For an example, the expression "In[26], a virtual space vector modulation technique is present, which suffers from low voltage utilization." Has been modified as "In[26], a virtual space vector modulation technique is presented, which suffers from low voltage utilization." in the first chapter.

Part of the vocabulary spelling has been unified and revised. For an example, the expression "modulation voltage(s)" has been unified as "modulated voltage(s)" in the second chapter and the sixth chapter.

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Third Harmonic Injection SPWM Method Based on Alternating Carrier Polarity to Suppress the Common Mode Voltage

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ABSTRACT In this paper, a third harmonic injection sinusoidal pulse width modulation (THISPWM) method based on alternating carrier polarity (ACP) is proposed for three-phase PWM inverter. Compared to the space vector pulse width modulation (SVPWM), the THISPWM has the advantage of lower low-frequency common mode voltage (CMV). However, the phase of the third harmonic injected must be strictly synchronous with the phase of the reference voltage. The synchronization will cause the difficulty of the injected third harmonic generation. Firstly, the relationship between the injected third harmonic and the reference voltage of PWM inverter output is analyzed to obtain a real-time conversion method, thereby solving the synchronization problem. Then, a modulation method based on ACP is proposed to eliminate zero switch states of PWM inverter. The middle amplitude modulated voltage is used to select the negative polarity carrier. And the low-frequency and high-frequency CMV, which are separately defined according to the modulated fundamental voltage frequency and the carrier frequency, are taken into account. Therefore, the analysis results manifest that the proposed method could suppress both the low-frequency and high-frequency CMV, and has the same voltage utilization as the SVPWM. Finally, a three-phase PWM inverter circuit based on FPGA was built, and the experimental results verified the proposed method.

INDEX TERMS sinusoidal pulse width modulation; third harmonic injection; common mode voltage; alternating carrier polarity

I.INTRODUCTION

With the development of electrical transportation, the motor number and power will gradually increase, such as electric propeller, electric jet engine and electric actuator [1]-[5]. The motors are driven by pulse width modulation (PWM) inverters, which will generate high frequency and abundant common mode voltage (CMV). When the peak voltage exceeds a certain threshold, the bearings break over and electric discharge machining currents flow, resulting in bearing damage [6]. The CMV can also cause common mode electromagnetic interference. In the strict military standards, the interference frequency has been as low as 30Hz regulated by international conducive electromagnetic compatibility standard CE101 [7], which leads to a demand for low-frequency CMV rejection. At present, the research of CMV suppression mainly includes installing electromagnetic filters, optimizing power topology and PWM modulation strategy.

The types of the filters are passive, active and hybrid [8] [9]. In order to remove both the low-frequency and high-frequency CMV, the electromagnetic filter requires a wide suppression effect, which is difficult to implement in terms of size, weight, and system complexity [10].

The topological methods mainly include the addition of auxiliary power devices, multiphase PWM inverter, open-end winding permanent magnet synchronous motor (PMSM) driver and multilevel converter. In [11] and [12], a balance inverter topology and dual-winding stator configuration are proposed. However, the balance inverter topology adds three additional power devices. In [13], a topology with two addition switches placed in series on the DC lines is presented. The CMV during zero switch states is reduced by floating the inverter from the DC source. In [14], a minimum CMV method is proposed for generalized two-level N-phase voltage-source inverters (VSIs) with odd phase numbers. In [15], a CMV elimination method based on a new modulation scheme is proposed for flying-capacitor modular multilevel converter. Compared with

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conventional three-phase inverters, these methods increase the number of power devices. Meanwhile the power topologies and control methods are complicated.

Except for the filters and topological methods, more optimized PWM modulation strategies have been proposed. The optimized PWM modulation strategies include optimization method based on space vector pulse width modulation (SVPWM), and carrier based PWM. In the SVPWM method, the main research includes optimized injected zero-sequence voltages, predictive current control, the active zero-state PWM (AZSPWM), the near-state PWM (NSPWM), open-end winding motor drives, introducing dwell time and so on [16]-[21]. However, under the SVPWM method, the low-frequency CMV based on the frequency of modulated fundamental voltage contains abundant harmonics [22].

Optimized carrier based PWM includes midpoint-fluctuation carrier (MFC) scheme, interleaving pulse width modulation, peak position modulation and so on. In [23], a MFC scheme is proposed by adding a midpoint-fluctuation signal on the standard symmetrical triangular carrier. Although this method can reduce the low-frequency CMV, it does not consider the suppression of the high-frequency CMV. In [24], the interleaving pulse width modulation method is used. Whereas, when the modulation index is higher than 1/2, the method has limited effect on suppressing the low-frequency CMV. In [25], a carrier peak position modulation, which adjusts the position of the carrier peak and has low voltage utilization, is proposed. In [26], a virtual space vector modulation technique is presented, which suffers from low voltage utilization.

The above methods can effectively reduce the CMV of the PWM inverter. However, these methods either require additional volume and weight [11]-[15], or are not compatible with both the high-frequency and low-frequency CMV suppression [16]-[23], or suffer from low DC-voltage utilization [24]-[26].

This paper proposes a third harmonic injection SPWM (THISPWM) method based on alternating carrier polarity (ACP) for the three-phase PWM inverter. The method not only suppresses both the low-frequency and high-frequency CMV, but also makes the voltage utilization is consistent with SVPWM. The mathematical relationship between the injected third harmonic and the reference voltage of PWM inverter output is analyzed. Meanwhile, the real-time conversion formula is obtained. The problem, that the phase of the third harmonic injected must be strictly synchronous with the phase of the reference voltage [23], can be avoided. The formula shows that when the modulation index is less than one, the low-frequency CMV can theoretically be eliminated. When the modulation index is greater than one, the low-frequency CMV is concentrated only on the third harmonic of the fundamental voltage, and the amplitude is reduced. Then, a modulation method based on alternating carrier polarity (ACP) is proposed. The method can dynamically alternate the polarity of the carrier according to the three-phase modulated voltages to reduce the high-frequency CMV. Both the low-frequency and high-frequency characteristics of the common mode voltage are analyzed, and the simulation curves are obtained. Finally, a FPGA-based test platform is built to verify the proposed method.

II.Theory of THISPWM based on ACP

The algorithm process of THISPWM based on ACP consists of two steps, as shown in Figure 1. The first step is to generate three-phase modulated voltages (TPMV) from the reference voltage. The second step is to generate six PWM signals through ACP method.

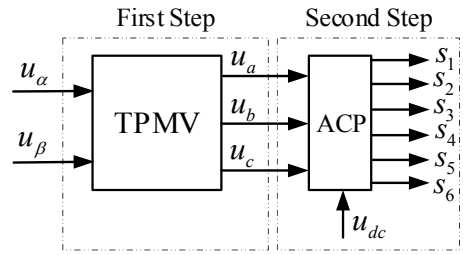

FIGURE 1. The algorithm of THISPWM based on ACP.

In Figure 1, u_α and u_β represent the reference voltages of the PWM inverter output in the stator coordinate system, respectively. u_a, u_b and u_c are the three-phase modulated voltages. u_{dc} is the bus supply voltage. s_{1-6} are the six PWM signals generated by ACP method.

A. The Three-Phase Modulated Voltages Generation

The reference voltage vector $\overrightarrow{U_S}$ of the PWM inverter output can be expressed as:

$$\overrightarrow{U_S} = 3U_m / 2e^{j\varphi} = 3U_m / 2(\cos\varphi + j\sin\varphi) = u_\alpha + ju_\beta \quad (1)$$

where, $3U_m/2$ is the modulus of $\overrightarrow{U_S}$, and φ is its angle.

The three-phase sinusoidal modulated voltages are

$$\begin{cases} u_a = U_1 \sin\theta \\ u_b = U_1 \sin(\theta - 2\pi/3) \\ u_c = U_1 \sin(\theta - 4\pi/3) \end{cases} \quad (2)$$

where, U_1 is the magnitude of u_a, and θ is its angle. u_a, u_b and u_c differ by $2\pi/3$ electrical degrees. $\overrightarrow{U_S}$ can be synthesized by the follows,

$$\overrightarrow{U_S} = u_a + u_b e^{-j2\pi/3} + u_c e^{-j4\pi/3} \quad (3)$$

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Substituting (3) into (1), the voltages of u_α , u_β are obtained,

$$\begin{cases} u_\alpha = 3/2U_1 \sin\theta = 3/2U_m \cos\varphi \\ u_\beta = 3/2U_1 \cos\theta = 3/2U_m \sin\varphi \end{cases} \tag{4}$$

Through (4), the follow equations are got,

$$\begin{cases} U_1 = U_m \\ \varphi + \theta = \pi/2 \end{cases} \tag{5}$$

From (5) and (2), the sinusoidal modulated voltages can be expressed as,

$$\begin{cases} u_a = 2u_\alpha/3 \\ u_b = -u_\alpha/3 + \sqrt{3}u_\beta/3 \\ u_c = -u_\alpha/3 - \sqrt{3}u_\beta/3 \end{cases} \tag{6}$$

When $U_m \le u_{dc}/2$, the modulation index m is less than 1. The sinusoidal modulated voltages in (6) can synthesize the reference voltages.

When $u_{dc}/2 < U_m \le u_{dc}/\sqrt{3}$, a third harmonic is needed to inject the sinusoidal modulated voltages in order to increase the bus voltage utilization. The three-phase modulated voltages are

$$\begin{cases} u_a = U_1 \sin\theta + U_3 \sin\theta_3 \\ u_b = U_1 \sin(\theta - 2\pi/3) + U_3 \sin\theta_3 \\ u_c = U_1 \sin(\theta - 4\pi/3) + U_3 \sin\theta_3 \end{cases} \tag{7}$$

where, U_3 is the amplitude of the third harmonic, and θ_3 is its angle. According to [23], the follows can be obtained,

$$\begin{cases} \theta_3 = 3\theta \\ U_3 = U_1/6 \end{cases} \tag{8}$$

From (4), the relationship among θ , u_α and u_β can be expressed as follow,

$$\frac{\sin 3\theta}{\sin\theta} = -\frac{u_\alpha^2 - 3u_\beta^2}{u_\alpha^2 + u_\beta^2} \tag{9}$$

According to (5), (8) and (9), we have,

$$\begin{aligned} U_3 \sin\theta_3 &= U_1 \sin 3\theta/6 \\ &= u_\alpha \sin 3\theta/\sin\theta/9 \\ &= -u_\alpha \left(u_\alpha^2 - 3u_\beta^2\right)/\left(u_\alpha^2 + u_\beta^2\right)/9 \end{aligned} \tag{10}$$

From (6), (7) and (10) the three-phase modulated voltages is generated, when $1 < m \le 1.154$.

$$\begin{cases} u_a = 2u_\alpha/3 - u_\alpha\left(u_\alpha^2 - 3u_\beta^2\right)/\left(u_\alpha^2 + u_\beta^2\right)/9 \\ u_b = -u_\alpha/3 + \sqrt{3}u_\beta/3 - u_\alpha\left(u_\alpha^2 - 3u_\beta^2\right)/\left(u_\alpha^2 + u_\beta^2\right)/9 \\ u_c = -u_\alpha/3 - \sqrt{3}u_\beta/3 - u_\alpha\left(u_\alpha^2 - 3u_\beta^2\right)/\left(u_\alpha^2 + u_\beta^2\right)/9 \end{cases} \tag{11}$$

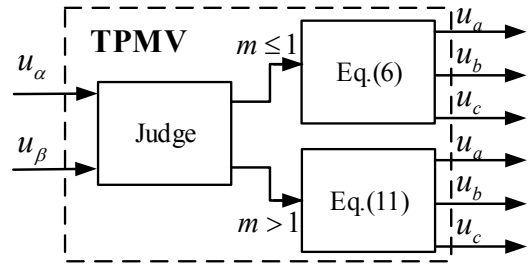

FIGURE 2. **Three-phase modulated voltages generation.**

Three-phase modulated voltages generation is shown in Figure 2. When $m \le 1$, the modulated voltages are three-phase sinusoidal. Since the sum of the three-phase sinusoidal voltages is zero, the low-frequency CMV can theoretically be eliminated. When $1 < m \le 1.154$, the modulated voltages contain the third harmonic in addition to the three-phase sinusoidal voltages. This third harmonic can be dynamically calculated by u_α and u_β according to (10).

B. Theory of Alternating Carrier Polarity

Figure 3 illustrates a three-phase two-level voltage-source inverter (VSI). The CMV is defined as

$$u_{OO'} = \left(u_{aO'} + u_{bO'} + u_{cO'}\right)/3 \tag{12}$$

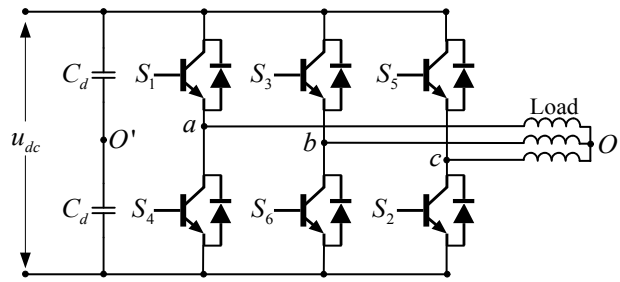

FIGURE 3. **Three-phase two-level voltage-source inverter (VSI).**

The switch state is defined by (13), where $i = a, b, c$.

$$S_i = \begin{cases} 1, & up \text{ is on and } down \text{ is off} \\ 0, & down \text{ is on and } up \text{ is off} \end{cases} \tag{13}$$

There are eight switch states (S_a, S_b, S_c) , as shown in TABLE I.

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TABLE I
RELATIONSHIP BETWEEN SWITCH STATES AND CMV.

Switch state	Phase voltage to terminal O'			CMV
	$u_{aO'}$	$u_{bO'}$	$u_{cO'}$	$u_{OO'}$
000	$-u_{dc}/2$	$-u_{dc}/2$	$-u_{dc}/2$	$-u_{dc}/2$
001	$-u_{dc}/2$	$-u_{dc}/2$	$u_{dc}/2$	$-u_{dc}/6$
011	$-u_{dc}/2$	$u_{dc}/2$	$u_{dc}/2$	$u_{dc}/6$
010	$-u_{dc}/2$	$u_{dc}/2$	$-u_{dc}/2$	$-u_{dc}/6$
110	$u_{dc}/2$	$u_{dc}/2$	$-u_{dc}/2$	$u_{dc}/6$
100	$u_{dc}/2$	$-u_{dc}/2$	$-u_{dc}/2$	$-u_{dc}/6$
101	$u_{dc}/2$	$-u_{dc}/2$	$u_{dc}/2$	$u_{dc}/6$
111	$u_{dc}/2$	$u_{dc}/2$	$u_{dc}/2$	$u_{dc}/2$

(001), (011), (010), (110), (100) and (101) are non-zero switch states, while (000) and (111) are zero switch states. The CMV of non-zero switch states is $\pm u_{dc}/6$. While, it is $\pm u_{dc}/2$ when zero switch state. Therefore, elimination of zero switch states can reduce the CMV.

In this paper, an alternating carrier polarity method shown in Figure 4 is proposed to eliminate the zero switch states. According to the characteristic of the three-phase modulated voltages, it is divided into six regions.

In the region I shown in Figure. 4, the PWM signal PA of modulated voltage A is a gray dotted line when the positive carrier is selected. Zero switch states appear. If modulated voltage A selects a negative carrier, PA is a solid black line. Thus, zero switch states are eliminated as shown in Figure 5.

Similarly, in the region II and III, if modulated voltage C and B select the responding negative carrier respectively, both the PWM signals PC and PB change from the gray dotted line to the black solid line, and zero switch states will be eliminated.

TABLE II
RELATIONSHIP BETWEEN MODULATED VOLTAGES AND CARRIERS.

Region	Middle amplitude modulated waveform	Carrier waveforms
I	u_a	$A-\ B+\ C+$
II	u_c	$A+\ B+\ C-$
III	u_b	$A+\ B-\ C+$
IV	u_a	$A-\ B+\ C+$
V	u_c	$A+\ B+\ C-$
VI	u_b	$A+\ B-\ C+$

It can be seen that when the middle amplitude modulated voltage selects the negative polarity carrier, the zero switch states are eliminated. The relationship between modulated voltages and carriers is shown in TABLE II. $A+$, $B+$ and $C+$ represent the positive carriers for A, B and C modulated voltages respectively. $A-$, $B-$ and $C-$ represent the negative carriers separately. The block diagram of ACP method is shown in Figure 5. Firstly, the middle amplitude modulated voltage is detected from the three modulated voltages. Secondly, three carriers are generated based on TABLE II. Thirdly, the modulated per-unit voltages u_a^*, u_b^* and u_c^* are calculated according to the bus voltage and the three modulated voltages. Finally, a comparison module with a dead zone unit generates six PWM signals.

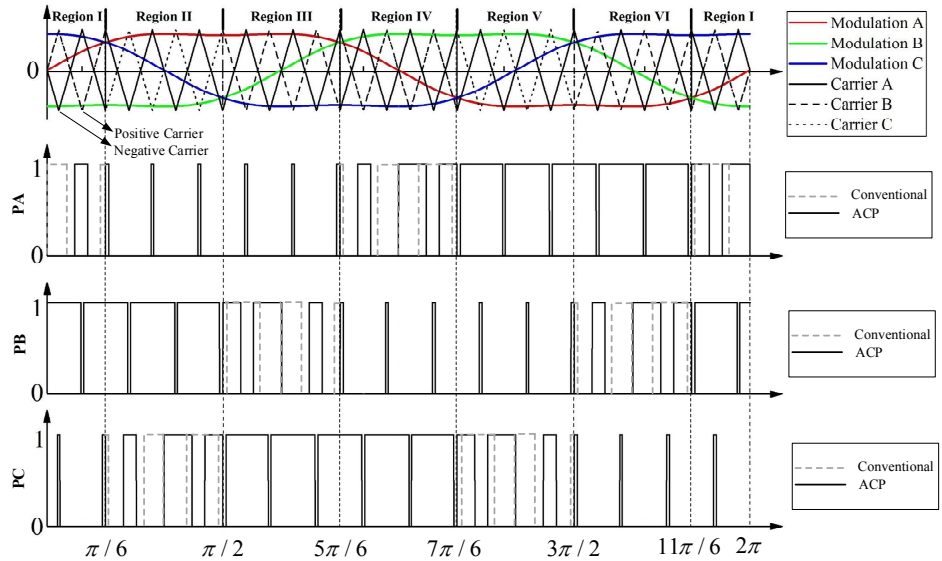

FIGURE 4. ACP method in one modulation period.

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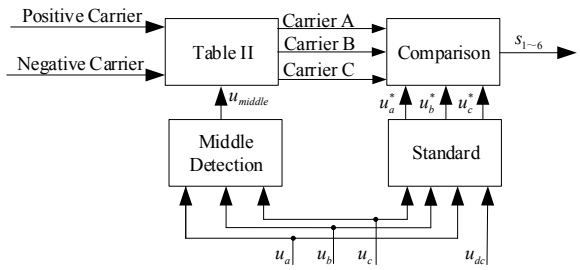

FIGURE 5. The block diagram of ACP method.

Taking PMSM drive as an example, the reference voltage of PWM inverter output is expressed as u_α and u_β. According to Figure 2 and Figure 5, THISPWM based on ACP can generate six PWM signals instead of SVPWM.

III. Common Mode Voltage Generation Based on the Proposed Method

A. Low-frequency CMV Based on Modulated Fundamental Voltage Frequency

The frequency of the modulated fundamental voltage, which is typically lower than that of the carrier, is taken as the fundamental frequency of low-frequency CMV. The modulated per-unit voltages $u_i^*(t)$ ($i=a,b,c$) consist of two parts,

$$u_i^*(t)=U_i^*(t)+e_i^*(t) \tag{14}$$

where $U_i^*(t)$ is the per-unit fundamental voltage and $e_i^*(t)$ is the per-unit injected CMV.

The CMV under SVPWM can be expressed

$$e_{i\_SVPWM}^*(t)=1/2\left(1-u_{\max}^*(t)\right)+1/2\left(-1-u_{\min}^*(t)\right) \tag{15}$$

In the region III, $u_{\max}^*(t)$ and $u_{\min}^*(t)$ is given

$$\begin{cases} u_{\max}^*(t)=U_a^*(t)=m\sin\theta \\ u_{\min}^*(t)=U_a^*(t)=m\sin(\theta-4\pi/3) \end{cases} \tag{16}$$

Substituting (16) into (15), $e_{i\_SVPWM}^*(t)$ is obtain.

$$e_{i\_SVPWM}^*(t)=-\frac{m}{2}\sin(\theta-2\pi/3) \tag{17}$$

In a modulated period, the CMV can be expressed as

$$e_{j\_SVPWM}(t)=\begin{cases} -m/2\sin(\theta-\pi/3) & \theta\in(\pi/6,\ \pi/2]\cup(7\pi/6,\ 3\pi/2] \\ -m/2\sin(\theta-2\pi/3) & \theta\in(\pi/2,\ 5\pi/6]\cup(3\pi/2,\ 11\pi/6] \\ m/2\sin\theta & \theta\in(5\pi/6,\ 7\pi/6]\cup(11\pi/6,\ \pi/6] \end{cases} \tag{18}$$

The Fourier expansion of (18) is

$$e_{j\_SVPWM}(t)=\sum_{n=1}^{\infty}\left(-\frac{\sqrt{3}\left(-\sin\left(\frac{5\pi}{6}n\right)+\sin\left(\frac{\pi}{2}n\right)-\sin\left(\frac{\pi}{6}n\right)\right)\sin(n\theta)}{\pi\left(n^2-1\right)}\right) \tag{19}$$

From (17) and (19), under SVPWM, the amplitude of the CMV consisting of the third harmonic and triple multiple harmonics is $m/4$, and the amplitude of the third harmonic is $m/5$.

In THISPWM based on ACP, when $m\le1$, three-phase modulated voltages are sinusoidal. The CMV is:

$$e_{j\_\mathrm{THSPWMBACP}}(t)=0 \tag{20}$$

When $1<m\le1.154$, the CMV is

$$e_{j\_\mathrm{THSPWMBACP}}(t)=\frac{m}{6}\sin(3\theta) \tag{21}$$

Compared with SVPWM, when $m\le1$, the proposed THISPWM based on ACP method can eliminate the low-frequency CMV. When $1<m\le1.154$, this method reduces the amplitude of the low-frequency CMV from $m/4$ to $m/6$ and eliminates its triple multiple harmonics.

B. High-frequency CMV Based on Carrier Frequency

The carrier frequency is taken as the fundamental frequency of high-frequency CMV.

Under SVPWM, the PWM signal consists of 4 switch states, (000), (100), (110) and (111) in region I. Zero switch states lead to higher amplitude $\pm U_{dc}/2$ of CMV, as is shown in Figure 7.

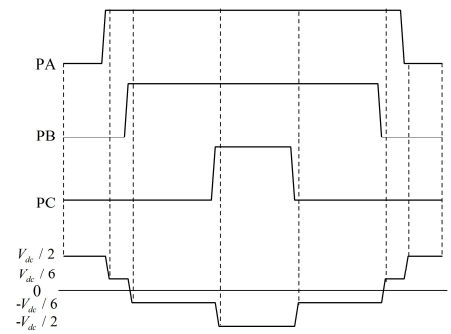

FIGURE 6. Common mode voltage generation of region I in SVPWM.

To avoid zero switch states, NSPWM and AZSPWM were put forward. NSPWM can reduce the amplitude of common mode voltage to $\pm U_{dc}/6$. However, its disadvantage is only working with high modulation index [18]. AZSPWM have more complex algorithm and lower performance in low frequency compared to SPWM method [27] [28].

Phase shift of carrier THISPWM (PSC-THISPWM) method has been brought forward to improve the

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performances of SPWM in the CMV suppression and the bus voltage utilization. When $m < 1/2$, PSC-THISPWM method can eliminate the zero switch states. However, when $m \geq 1/2$, for example, the modulation index is 0.9, the zero state appears as shown in Figure 7.

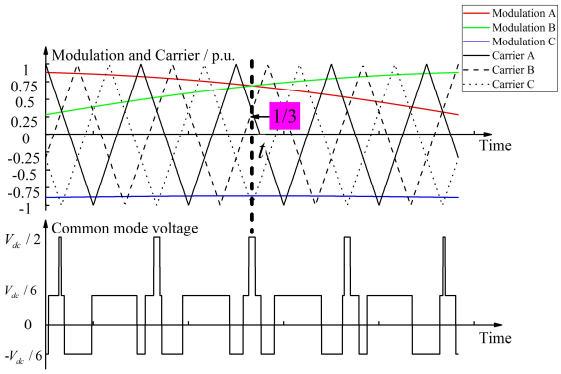


FIGURE 7. The CMV of PSC-THISPWM when $m = 0.9$

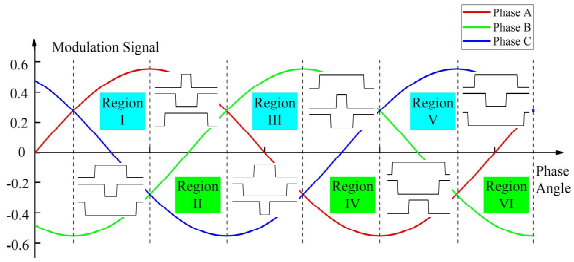


FIGURE 8. Relationship of the modulated voltages and PWM signals under THISPWM based on ACP method when $m \leq 1$.

Under the proposed THISPWM based on ACP method, when $m \leq 1$, the modulated voltages and PWM signals are shown in Figure 8. In region I, the relationship between PWM signals and CMV is shown in Figure 9.

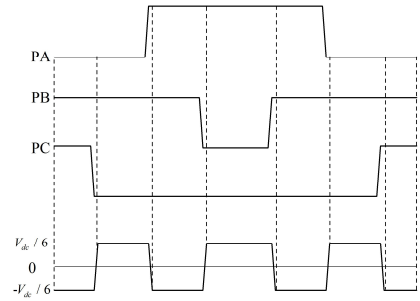


FIGURE 9. The CMV of THISPWM based on ACP in region I.

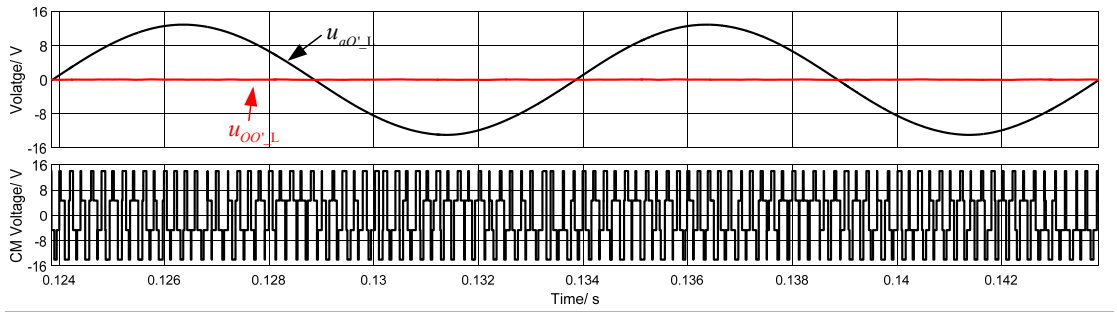
When $m > 1$, THISPWM based on ACP method can also reduce the amplitude of CMV which is the same as Figure 9.

As a result, zero switch states are eliminated in the proposed THISPWM based on ACP. Thus, the high-frequency CMV is reduced.

V. Simulation

The THISPWM, PSC-THISPWM, SVPWM and THISPWM based on ACP models are built in the Matlab/Simulink environment. The modulated fundamental voltage frequency is set to 100 Hz, the carrier frequency is set to 5 kHz, and the supply voltage is 28 V. The phase resistance of the three-phase load is 12 ohms, and the inductance is 1.2 mH.

When $m = 0.90$, the simulation results are shown in Figure 10. $u_{aO'\_L}$ and $u_{OO'\_L}$ are obtained respectively from $u_{aO'}$ and $u_{OO'}$, which are filtered by a filter, and the cut-off frequency of the filter is 3 kHz. The bus voltage utilization of the four methods is the same, for the RMS values of u_{aO} are all 8.9 V. The low-frequency CMV is eliminated in THISPWM, PSC-THISPWM and THISPWM based on ACP. The maximum amplitude of $u_{OO'}$ is 14 V under THISPWM, PSC-THISPWM and SVPWM. While, it is 4.67 V under the proposed THISPWM based on ACP.



(a) THISPWM

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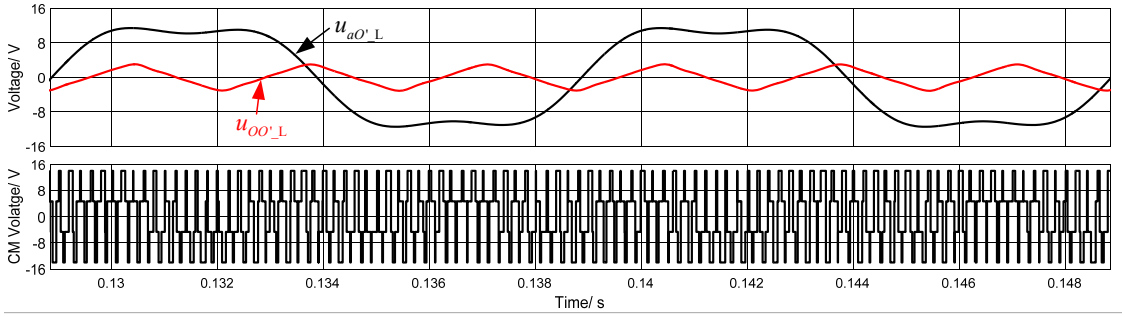
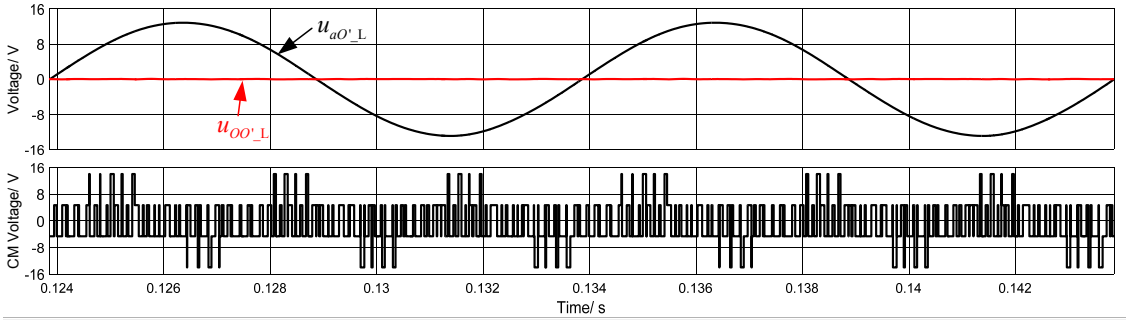
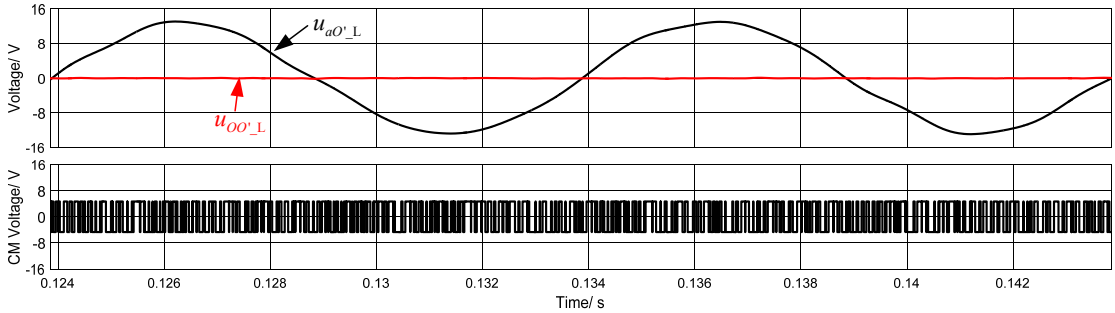


(b) SVPWM

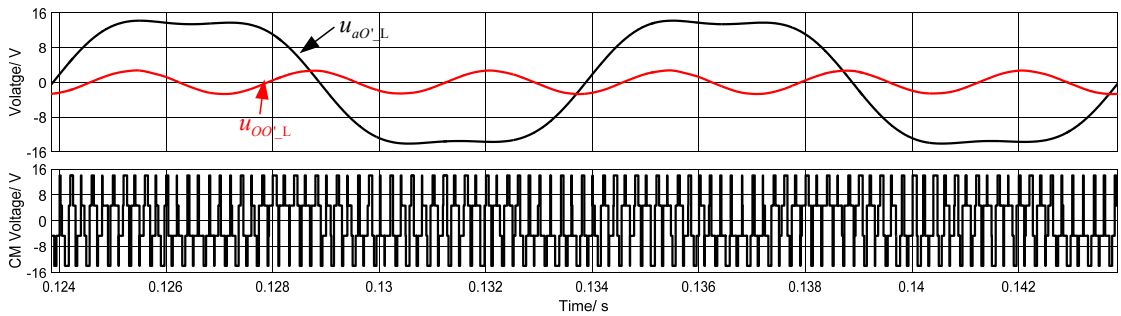


(c) PSC-THISPWM



(d) THISPWM based on ACP

FIGURE 10. The simulation results when $m = 0.90$.



(a) THISPWM

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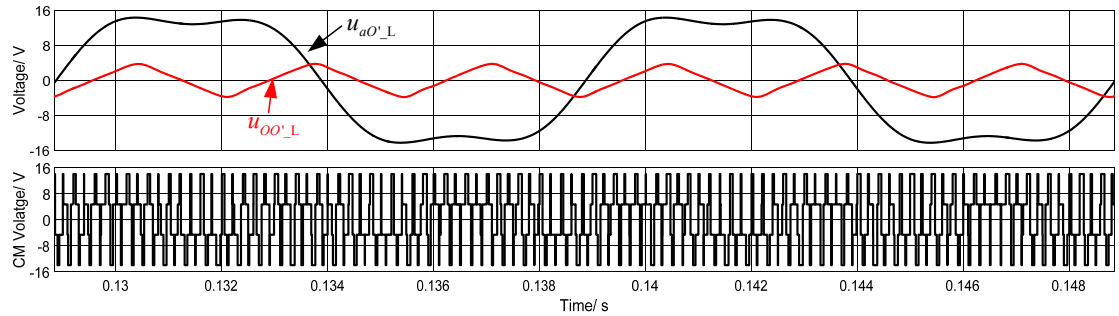
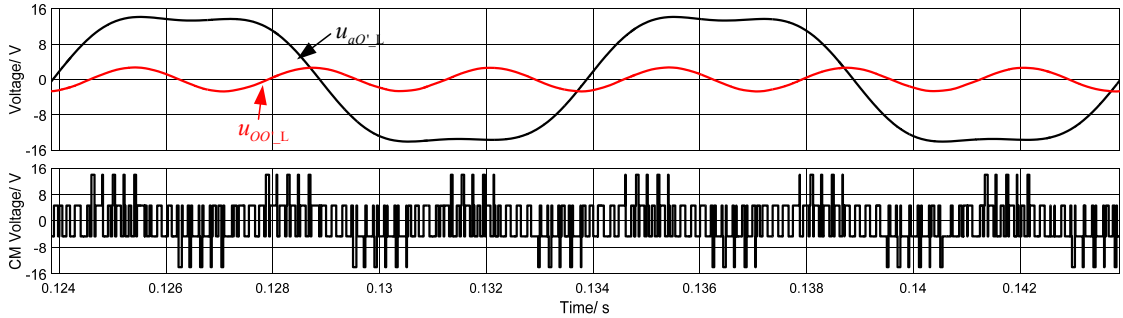
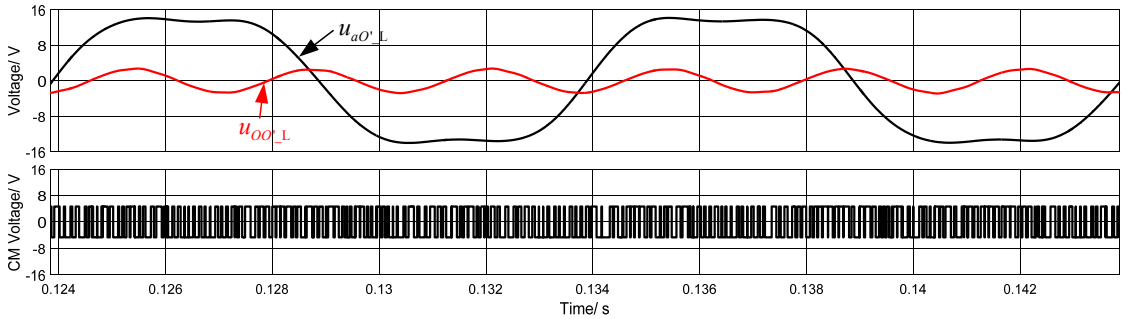


(b) SVPWM



(c) PSC-THISPWM



(d) THISPWM based on ACP

FIGURE 11. The simulation results when $m = 1.10$.

When $m = 1.10$, the simulation results are given in Figure 11. The RMS values of u_{aO} are all 10.9V. Under THISPWM, PSC-THISPWM and THISPWM based on ACP, $u_{OO'\_L}$ is sinusoidal. While, $u_{OO'\_L}$ is approximately triangular and has a higher amplitude in SVPWM.

The simulated results show that the proposed THISPWM based on ACP method has the same bus voltage utilization as SVPWM, and can reduce both the low-frequency and high-frequency CMV.

VI. Experiment

A. Experiment Platform Construction

In order to compare the CMV of THISPWM, PSC-THISPWM, SVPWM and THISPWM based on ACP methods, an experiment platform has been established. The experiment platform mainly consists of controller and load shown in Figure 12. The controller consists of DSP, FPGA and inverter. DSP and FPGA respectively complete step 1 and step 2 of algorithm as shown in Figure 1. Firstly, the DSP produces a rotating voltage vector with frequency of 100 Hz and adjustable modulation. Three-phase modulated voltages u_a^*, u_b^* and u_c^* are generated by SVPWM or (6) and (11). Secondly, FPGA receives the three-phase modulated voltages through the parallel bus, and compares the modulated waveforms with the triangular carriers to generate PWM signals $s_1 - s_6$. For THISPWM and SVPWM methods, triangular carriers are fixed. For PSC-THISPWM, the three-phase carriers differ by 120°. For THISPWM based on ACP, three-phase triangular carriers

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are generated according to Figure 5. Finally, the inverter receives PWM signals and converts 28 VDC voltage into AC output voltage. Star windings of three-phase asynchronous motor with central point is chosen as the load. The resistance and inductance of motor phase is 12 Ω and 1.2 mH separately. The Experiment platform is shown in Figure 13.

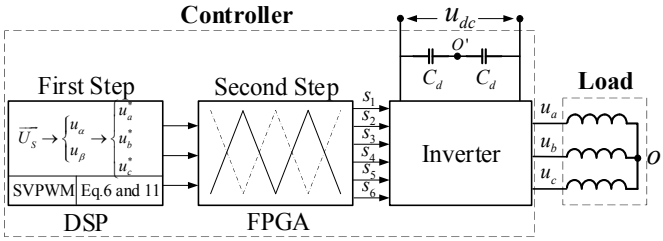


FIGURE 12. **System block diagram.**

Under THISPWM based on ACP method, the drive signals of s_4, s_6 and s_2 are shown in Figure 14. In the red circle, the carrier polarities of the u_a^* and u_b^* changes synchronously, resulting in a synchronous change of S_4 and S_6.

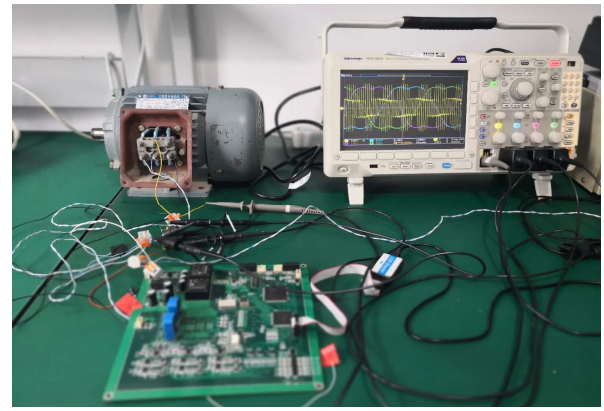


FIGURE 13. **Experiment platform.**

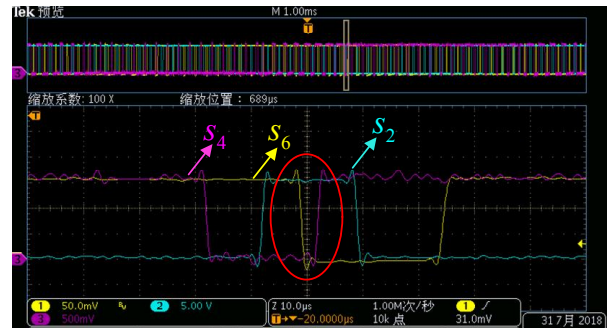
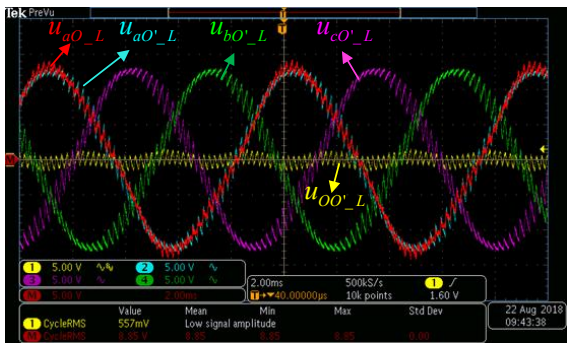
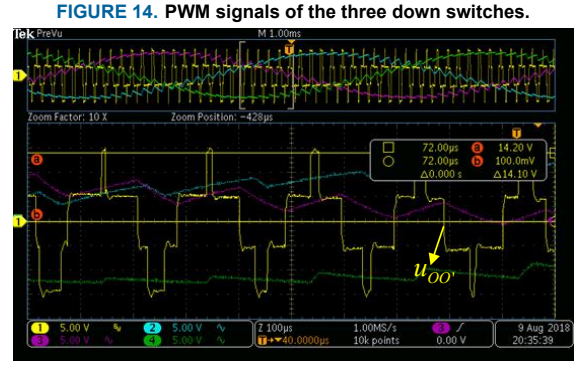
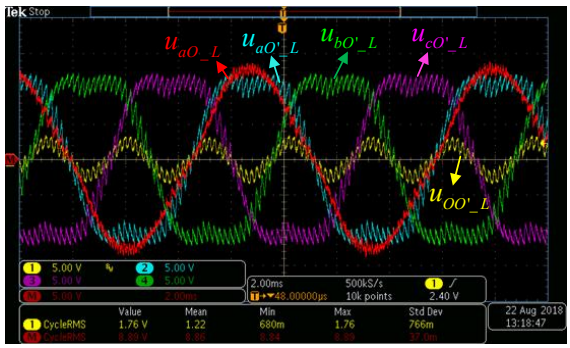


FIGURE 14. **PWM signals of the three down switches.**





(a)THISPWM



(b) SVPWM

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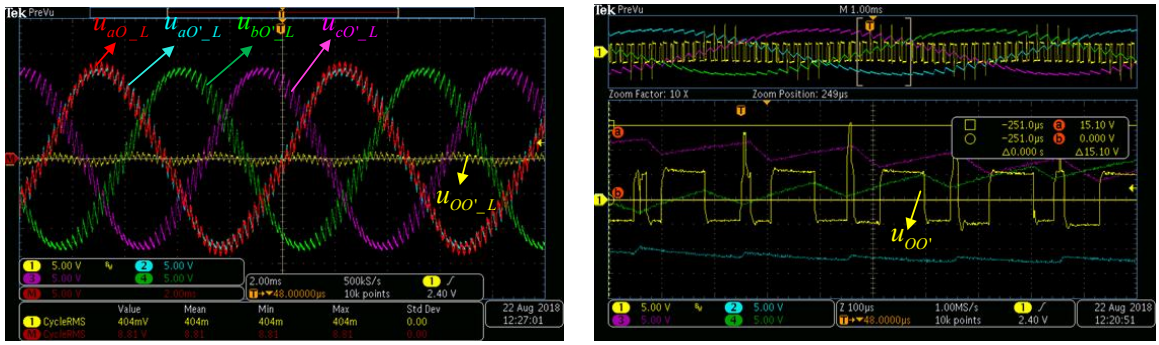
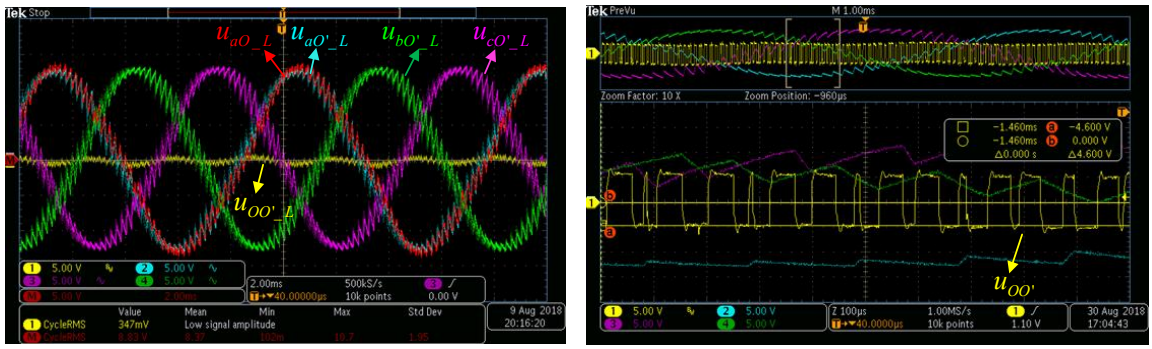
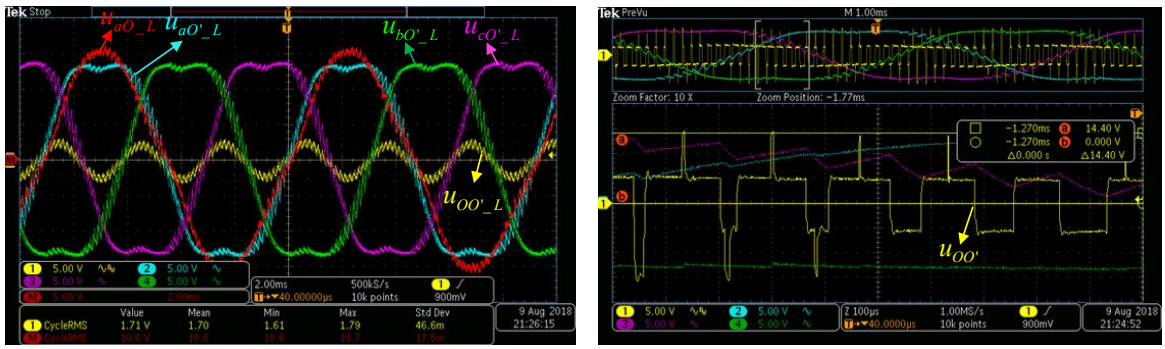


(c) PSC-THISPWM

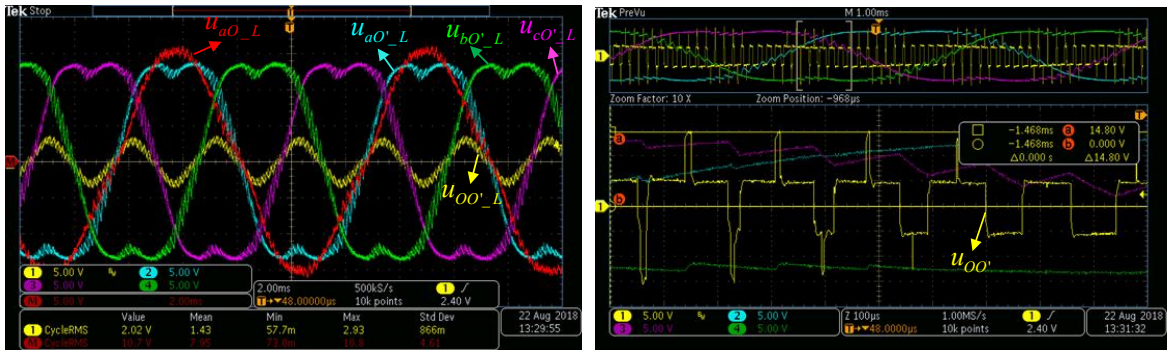


(d) THISPWM based on ACP

FIGURE 15. Experimental results when $m = 0.90$.



(a) THISPWM



(b) SVPWM

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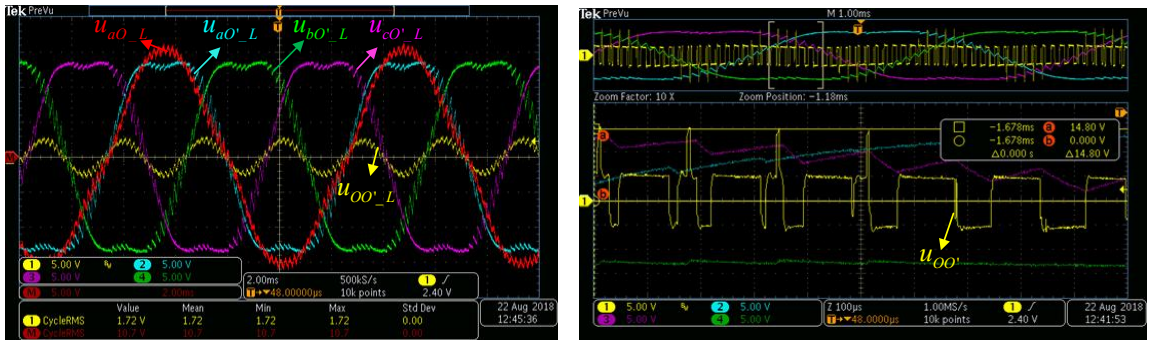
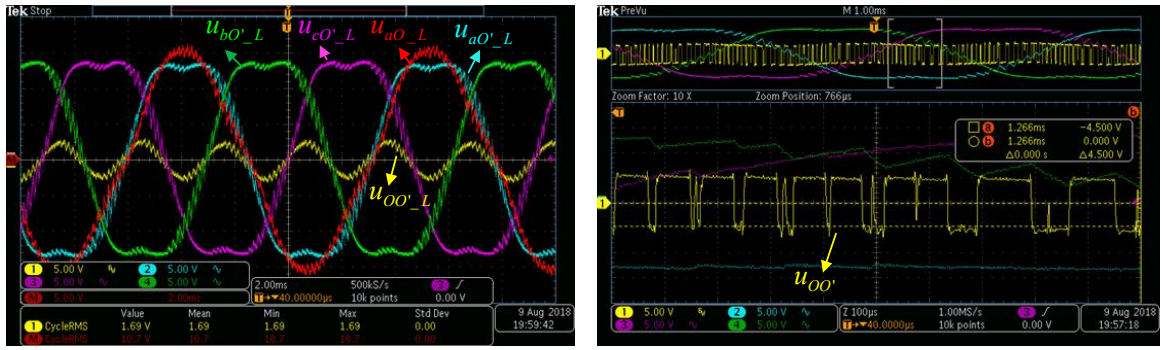


(c) PSC-THISPWM



(d) THISPWM based on ACP

FIGURE 16. Experimental results when $m = 1.10$.

B. Experimental Results

The experimental results are shown in Figure 15 and Figure 16. $u_{aO'\_L}$, $u_{bO'\_L}$ and $u_{cO'\_L}$ are produced by $u_{aO'}$, $u_{bO'}$ and $u_{cO'}$ through a RC low-pass filter, separately. The cut-off frequency of the filter is 454 Hz. The common mode voltage $u_{OO'}$ passing through the RC low-pass filter and the voltage $u_{OO'\_L}$ is generated. u_{aO_L} is produced by subtracting $u_{OO'\_L}$ from $u_{aO'\_L}$. $u_{OO'\_L}$ mainly reflects the third harmonic voltage with frequency of 300 Hz due to the RC filter cut-off frequency of 454 Hz. The following three conclusions can be obtained by the experimental waveforms.

First, when the modulation index is fixed, the amplitudes of u_{aO_L} are the same under the four modulation methods. That is, the voltage utilization of the four modulation methods is the same

Second, the peak values of $u_{OO'}$ under THISPWM based on ACP is 4.5V, while it is 14.8V under the three other methods.

Third, the RMS value of $u_{OO'\_L}$ under THISPWM based on ACP is closed to 0 when $m \le 1$, and is 1/6 times of the u_{aO_L} when $1 < m \le 1.15$. While it is 1/5 times of the u_{aO_L} under SVPWM, on the premise that only the third harmonic voltage is considered.

The comparison of four modulation methods is shown in TABLE III. Both low-frequency and high-frequency CMV are suppressed in the proposed THISPWM based on ACP.

TABLE III.
THE COMPARATION OF COMMON MODE VOLTAGE UNDER THREE MODULATION METHODS.

Modulation method	Modulation index	$U_{OO'\_RMS}$ (V)	U_{aO_RMS} (V)	$U_{OO'\_PK}$ (V)
SVPWM	0.90	1.76	8.89	14.8
	1.10	2.02	10.7	14.8
THISPWM	0.90	0.557	8.85	14.1
	1.10	1.71	10.6	14.4
PSC-THISPWM	0.90	0.404	8.81	15.1
	1.10	1.72	10.7	14.8
THISPWM based on ACP	0.90	0.347	8.83	4.5
	1.10	1.69	10.7	4.5

VII. Conclusion

A third harmonic injection SPWM method based on alternating carrier polarity was proposed in this paper. The proposed THISPWM based on ACP modulation method has the same bus voltage utilization as SVPWM. Comparing with SVPWM, THISPWM based on ACP can maximally reduce the low-frequency CMV by 80.2% when $m < 1$, and 19.5% when $m \ge 1$. Comparing with SVPWM, THISPWM and PSC-THISPWM, THISPWM based on ACP can decrease the peak values of high-frequency CMV

from 14.5 V to 4.5 V. Hence, the proposed method has advantages over SVPWM, THISPWM and PSC-THISPWM in terms of reducing both low-frequency and high-frequency CMV. Moreover, the input voltage u_α and u_β of THISPWM based on ACP are equal to that of SVPWM, such as the drive of three-phase AC motor. Therefore, the proposed method can replace SVPWM more conveniently and has higher practical value.

ACKNOWLEDGMENT

This work was supported in part by Shaanxi Key Research Project (2017GY-048).

REFERENCES

[1] Zhang, Z.; Huang, J.; Jiang, Y.; Geng, W.; Xu, Y. Overview and analysis of PM starter/generator for aircraft electrical power systems. **2017**, *CES Transactions on Electrical Machines and Systems, 1*(2), 117-131. doi:10.23919/TEMS.2017.7961293.

[2] Yin, S.; Tseng, K. J.; Simanjorang, R.; Liu, Y.; Pou, J. A 50-kW High-Frequency and High-Efficiency SiC Voltage Source Inverter for More Electric Aircraft. **2017**, *IEEE Transactions on Industrial Electronics, 64*(11), 9124-9134. doi:10.1109/TIE.2017.2696490.

[3] Sarlioglu, B.; Morris, C. T. More Electric Aircraft: Review, Challenges, and Opportunities for Commercial Transport Aircraft. **2015**, *IEEE Transactions on Transportation Electrification, 1*(1), 54-64. doi:10.1109/TTE.2015.2426499.

[4] Gao, F.; Zheng, X.; Bozhko, S.; Hill, C. I.; Asher, G. Modal Analysis of a PMSG-Based DC Electrical Power System in the More Electric Aircraft Using Eigenvalues Sensitivity. **2015**, *IEEE Transactions on Transportation Electrification, 1*(1), 65-76. doi:10.1109/TTE.2015.2427312.

[5] Ding, X.; Du, M.; Duan, C.; Guo, H.; et al., Analytical and Experimental Evaluation of SiC-Inverter Nonlinearities for Traction Drives Used in Electric Vehicles, *IEEE Transactions on Vehicular Technology*, Jan. **2018**, 67 (1): 146-159.

[6] Tallam, R. M.; Kerkman, R. J.; Leggate D.; Lukaszewski, R. A.; Common-Mode Voltage Reduction PWM Algorithm for AC Drives, *IEEE Transactions on Industry Applications*, Sept.-Oct. **2010**, vol. 46, no. 5, pp. 1959-1969.

[7] Requirements for the Control of Electromagnetic Interference Character-istics of Subsystems and Equipment, MIL-STD-461F C.F.R., **2007**, U.S. Military Standard.

[8] Hedayati, M. H.; Acharya, A. B.; John, V. Common-Mode Filter Design for PWM Rectifier-Based Motor Drives. **2013**, *IEEE Transactions on Power Electronics, 28*(11), 5364-5371. doi:10.1109/TPEL.2013.2238254.

[9] Chen, W.; Yang, X.; Xue, J.; Wang, F. A Novel Filter Topology With Active Motor CM Impedance Regulator in PWM ASD System. **2014**, *IEEE Transactions on Industrial Electronics, 61*(12), 6938-6946. doi:10.1109/TIE.2014.2320222.

[10] Huang, J.; Shi, H. Suppressing low-frequency components of comm on mode voltage through reverse injection in three-phase inverter. **2014**, *IET Power Electronics, 7*(6), 1644-1653. doi:10.1049/iet-pel.2013.0756.

[11] Han, D.; Lee, W.; Li, S.; Sarlioglu, B. New Method for Common Mode Voltage Cancellation in Motor Drives: Concept, Realization, and Asymmetry Influence. **2018**, *IEEE Transactions on Power Electronics, 33*(2), 1188-1201. doi:10.1109/TPEL.2017.2688370.

[12] Han, D.; Morris, C. T.; Sarlioglu, B. Common-Mode Voltage Cancellation in PWM Motor Drives With Balanced Inverter Topology. **2017**, *IEEE Transactions on Industrial Electronics, 64*(4), 2683-2688. doi:10.1109/TIE.2016.2633234.

[13] Morris, C. T.; Han, D.; Sarlioglu, B. Reduction of Common Mode Voltage and Conducted EMI Through Three-Phase Inverter Topology. **2017**, *IEEE Transactions on Power Electronics, 32*(3), 1720-1724. doi:10.1109/TPEL.2016.2608388.

[14] Chen, K.; Hsieh, M. Generalized Minimum Common-Mode Voltage PWM for Two-Level Multiphase VSIs Considering Reference Order. **2017**, *IEEE Transactions on Power Electronics, 32*(8), 6493-6509. doi:10.1109/TPEL.2016.2615111.

[15] Du, S.; Wu, B.; Zargari, N. R. Common-Mode Voltage Elimination for Variable-Speed Motor Drive Based on Flying-Capacitor Modular Multilevel Converter. **2018**, *IEEE Transactions on Power Electronics, 33*(7), 5621-5628. doi:10.1109/TPEL.2017.2740782.

[16] Wu, X.; Tan, G.; Ye, Z.; Liu, Y.; Xu, S. Optimized Common-Mode Voltage Reduction PWM for Three-Phase Voltage-Source Inverters. **2016**, *IEEE Transactions on Power Electronics, 31*(4), 2959-2969. doi:10.1109/TPEL.2015.2451673.

[17] S. K. Hoseini, J. Adabi and A. Sheikholeslami. Predictive modulation schemes to reduce common-mode voltage in three-phase inverters-fed AC drive systems. **2014**, *IET Power Electronics*. 7(4), 840-849. doi: 10.1049/iet-pel.2013.0182.

[18] Un, E. and A. M. Hava. A Near-State PWM Method With Reduced Switching Losses and Reduced Common-Mode Voltage for Three-Phase Voltage Source Inverters. **2009**, *IEEE Transactions on Industry Applications*. 45(2), 782-793. doi: 10.1109/TIA.2009.2013580.

[19] C. Hou, C. Shih, P. Cheng and A. M. Hava. Common-Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters. **2013**, *IEEE Transactions on Power Electronics*. 28(4), 1971-1979. doi: 10.1109/TPEL.2012.2196712.

[20] Baranwal, R.; Basu, K.; Mohan, N. Carrier-Based Implementation of SVPWM for Dual Two-Level VSI and Dual Matrix Converter With Zero Common-Mode Voltage. **2015**, *IEEE Transactions on Power Electronics, 30*(3), 1471-1487. doi:10.1109/TPEL.2014.2316528.

[21] Tallam, R. M.; Leggate, D.; Kirschnik, D. W.; Lukaszewski, R. A. Reducing Common-Mode Current: A Modified Space Vector Pulsewidth Modulation Scheme. **2014**, *IEEE Industry Applications Magazine, 20*(6), 24-32. doi:10.1109/MIAS.2013.2288376.

[22] Hava, A. M.; Çetin, N. O. A Generalized Scalar PWM Approach With Easy Implementation Features for Three-Phase, Three-Wire Voltage-Source Inverters. **2011**, *IEEE Transactions on Power Electronics, 26*(5), 1385-1395. doi:10.1109/TPEL.2010.2081689.

[23] Huang, J.; Liu, Q.; Wang, X.; Li, K. A Carrier-Based Modulation Scheme to Reduce the Third Harmonic Component of Common-Mode Voltage in a Three-Phase Inverter Under High DC Voltage Utilization. **2018**, *IEEE Transactions on Industrial Electronics, 65*(3), 1931-1940. doi:10.1109/TIE.2017.2745439.

[24] J. W. Kimball and M. Zawodniok. Reducing Common-Mode Voltage in Three-Phase Sine-Triangle PWM With Interleaved Carriers. **2011**, IEEE Transactions on Power Electronics. 26(8), 2229-2236. doi: 10.1109/TPEL.2010.2092791.

[25] Huang, J.; Shi, H. Reducing the Common-Mode Voltage through Carrier Peak Position Modulation in an SPWM Three-Phase Inverter. **2014**, *IEEE Transactions on Power Electronics, 29*(9), 4490-4495. doi:10.1109/TPEL.2014.2303897.

[26] Tian, K.; Wang, J.; Wu, B.; Cheng, Z.; Zargari, N. R. A Virtual Space Vector Modulation Technique for the Reduction of Common-Mode Voltages in Both Magnitude and Third-Order Component. **2016**, *IEEE Transactions on Power Electronics, 31*(1), 839-848. doi:10.1109/TPEL.2015.2408812.

[27] Cetin, N. O.; Hava, A. M. Interaction between the filter and PWM units in the sine filter configuration utilizing three-phase AC motor drives employing PWM inverters. Paper presented at the 2010 IEEE Energy Conversion Congress and Exposition, **2010**, 12-16 Sept. 2010.

[28] Hava, A. M.; Cetin, N. O.; Un, E. On the Contribution of PWM Methods to the Common Mode (Leakage) Current in Conventional Three-Phase Two-Level Inverters as Applied to AC Motor Drives. Paper presented at the 2008 IEEE Industry Applications Society Annual Meeting, **2008**, 5-9 Oct. 2008.