An Isolated Full-Bridge DC/DC Converter with Bidirectional Communication Capability

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***Abstract*—This work presents a novel isolated full-bridge DC/DC converter with bidirectional communication capability. The transformer in the proposed converter is utilized as an isolation interface for transferring energy and data. Power delivery and forward data transfer are conducted simultaneously by modifying the full-bridge switching phase. Backward data transfer is realized by manipulating the amplitude of the resonant signal through modulating the impedance of the resonant tank at the secondary side of the transformer. Finally, the operation principle of the proposed converter was verified on a 280mW prototype operating at 400kHz from a 12V DC input.**

***Keywords*—converter circuit, data transmission, industrial communications, resonant converter, switched-mode power supply, transformer.**

I. Introduction

In numerous applications, such as in medical instruments and telecommunications, isolated interfaces are required for safety. In conventional approaches, power conversion and communication function are realized with independent interface circuits. For isolated DC/DC power conversion, a transformer is applied as power transfer interface. For data communication, extra pulse transformers, optical-couplers, or capacitors are applied as data transfer interfaces [1]–[4]. This work presents a novel isolated full-bridge DC/DC converter with bidirectional communication capability. A safe design with reduced cost and device counts is achieved by using a common isolated transformer that facilitates power and data transfer.

Operations of the full-bridge converter in providing bidirectional communication are as follows. (a) Power delivery and forward data transfer can be made simultaneous by altering the full-bridge switching phase. A positive or negative voltage phase across the primary winding of the transformer can deliver a 0 or 1 signal of forward datum, respectively. (b) When in discontinuous conduction mode (DCM) operation, backward data transfer can be achieved through the resonant operation provided by transformer inductance and parasitic capacitors in the bridge stage when the transformer is demagnetized completely. Via the proposed design, no additional supplied power is needed to transfer backward data.

Generally, an L-C resonant tank is employed in the technologies, such as zero-voltage switching converters [5]–[7], series L-L-C resonant converters [8], [9], and parallel resonant converters [10], [11], to achieve zero-voltage soft switching to increase power conversion efficiency. In the proposed design, the resonant technology is utilized for different purpose, data communication. In the proposed design, backward data transfer is attained by manipulating the amplitude of a resonant signal through modulating the impedance of the resonant tank on transformer secondary side. Therefore, backward datum can be retrieved by detecting the amplitude of the resonant signal across the primary winding. Via these two data transfer and retrieve technologies, isolated bidirectional data communication is accomplished.

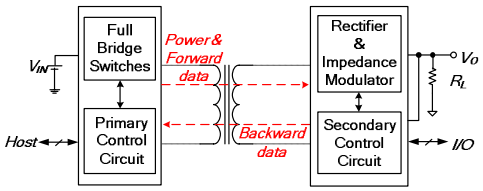

Fig. 1. Block diagram of the proposed power converter

II. Circuit and Operation Principle

Fig. 1 presents the block diagram of the proposed isolated DC/DC converter including the converter and data communication stages. The data communication stage includes a primary control circuit and secondary control circuit to achieve bidirectional communication. The primary control circuit is employed to transfer forward data from the *Host* side to the *I/O* side through the transformer and simultaneously transfer power to the load. The secondary control circuit is utilized to transfer backward data from the *I/O* side to the *Host* side through the transformer. Additionally, the primary and secondary control circuits are also in charge of receiving data transmitted from opposite sides.

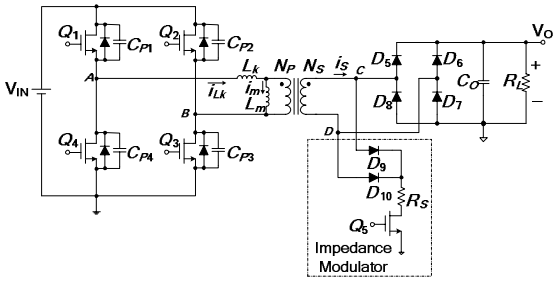

Fig. 2. Proposed DC/DC converter stage including the impedance modulator

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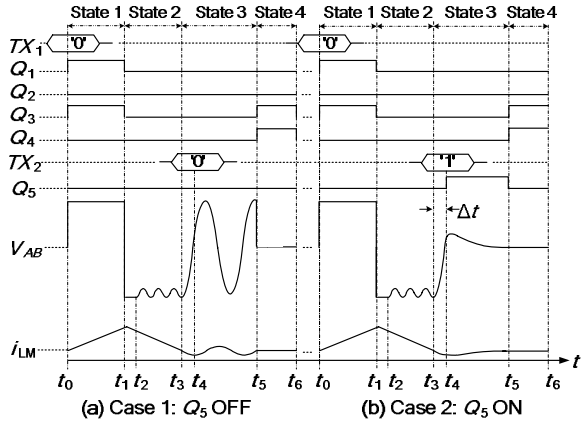

Fig. 3. Key waveforms of the proposed converter

TABLE I.
CONTROL TABLE OF THE ON-TRANSISTORS RELATED TO THE TRANSMITTED DATUM

State / Datum	State 1	State 2	State 3	State 4
$TX_1 = 0$	Q_1, Q_3			Q_3, Q_4
$TX_1 = 1$	Q_2, Q_4			Q_3, Q_4
$TX_2 = 0$				
$TX_2 = 1$			Q_5	

Fig. 2 presents the converter stage of the proposed power converter with the following 4 primary circuit blocks: (1) an isolated transformer that transfers power and data; (2) a full-bridge switching stage, including transistors Q_1, Q_2, Q_3, and Q_4, with body diodes and parasitic capacitors that generates a switching signal according to the forward datum TX_1 sent from the *Host* side; (3) a voltage rectifier, including diodes D_5, D_6, D_7, and D_8, and a output capacitor C_O that provides rectified supply voltage to the load and associated secondary control circuit; and, (4) an impedance modulator, including diodes D_9 and D_{10}, and transistor Q_5, that manipulates the impedance of the transformer according to the backward datum TX_2 given by the *I/O* side.

There are four operational states in a switching cycle for the proposed converter during bidirectional communication (Fig. 3). We assume that all transistors have zero on-resistances, and load current is constant. Table 1 shows the control table of the on-transistors related to the transmitted data, TX_1 and TX_2, in each operation state. The duty ratios of the four operational state are denoted by $D_{1,\,2,\,3,\,\text{or}\,4}$.

1) State 1 [$t_0 - t_1$]: *Duration of power and forward data transfer*

In this state, power is transferred from the input DC bus (V_{IN}) to the load through the full-bridge converter. According to the transistor switching control rules as shown in Table 1, voltage polarity of the full-bridge converter output V_{AB}, is manipulated by the logic state of forward datum TX_1. Under the voltage polarity arrangement, power and forward datum TX_1 can be transferred simultaneously to the secondary side through the isolated transformer. After rectifying the coupled voltage V_{CD} across the transformer secondary winding, a DC output voltage (V_O) is acquired that provides power for the circuits on the transformer secondary side. Meanwhile, the transferred forward datum is retrieved simply by a level-detect circuit on transformer secondary side.

When transmitted forward datum TX_1 is 0, transistors Q_1 and Q_3 are turned on, resulting in $V_{AB} = V_{IN}$; otherwise, $V_{AB} = -V_{IN}$ for the case of $TX_1 = 1$. When $V_{AB} = V_{IN}$, diodes D_5 and D_7 are turned on, and the increasing rate of the magnetizing inductance current of the transformer is given by

$$\frac{i_m(t)}{dt} = \frac{n(V_O + 2V_D)}{L_m} \tag{1}$$

where V_O is average output voltage, and V_D is the forward conduction voltage of each rectifier diode.

Since voltage across leakage inductance of the transformer is very small, such that $V_{Lk} << V_{Lm}$, the voltage on the magnetizing inductance is approximate to input voltage; *i.e.*, $V_{IN} \approx n\,(V_O + 2V_D)$, where n is the turns ratio of the primary winding N_P to the secondary winding N_S. Moreover, leakage inductance can be utilized to limit the maximum current increasing rate of switching components. Once the current slop limit, $(di_{Lk}/dt)_{\max}$, is given, minimum leakage inductance can be determined from the following equation:

$$\frac{di_{Lk}}{dt}\Big|_{\max} = \frac{V_{in} - n\left[(V_O - \Delta V_O/2) + 2V_D\right]}{L_k} \approx \frac{n\Delta V_O}{2L_k} \tag{2}$$

where ΔV_O is output voltage ripple.

2) State 2 [$t_1 - t_3$]: *Duration of transformer demagnetization*

The case of $TX_1 = 0$ is assumed for illustrating the circuit operation. When $t = t_1$, all of the full-bridge transistors are turned off, the leakage inductance of the transformer is demagnetized through the body diodes of transistor Q_2 and Q_4. Thus, the voltage V_{AB} is equal to $-V_{IN}$ and results in $V_{Lk} \approx -2V_{IN}$. This high V_{Lk} causes i_{Lk} reducing fast. After i_{Lk} is less than i_{Lm}, L_m starts to demagnetize through secondary winding of the transformer and shortly i_{Lk} reduces to zero. Thus the rectifier diodes at secondary side, D_6 and D_8 are turned on and result in the voltage V_{Lm} being $-n(V_O + 2V_D)$. In contrast, V_{Lm} will be $n\,(V_O + 2V_D)$ if $TX_1 = 1$.

We assume all parasitic capacitors of the bridge stage have the same value C_P ($C_P = C_{P1} = C_{P2} = C_{P3} = C_{P4}$). At $t = t_2$, leakage inductance L_k has demagnetized completely and turns to resonate with the equivalent parasitic capacitor C_P across terminals A and B. Since voltage $V_{AB} = -V_{IN}$ at $t = t_2$, and $V_{Lm} = -n(V_O + 2V_D) \approx -V_{IN}$, oscillation amplitude of V_{AB} is extremely small.

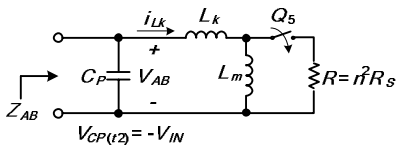

Fig. 4. Equivalent circuit of the proposed converter in State 3

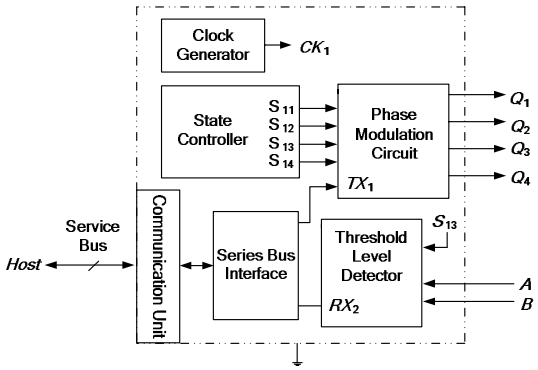

Fig. 5. Primary control circuit

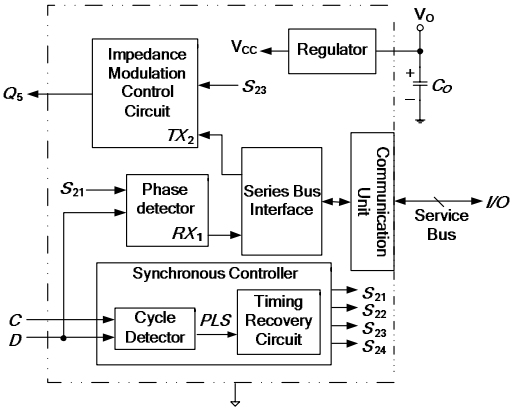

Fig. 6. Secondary control circuit

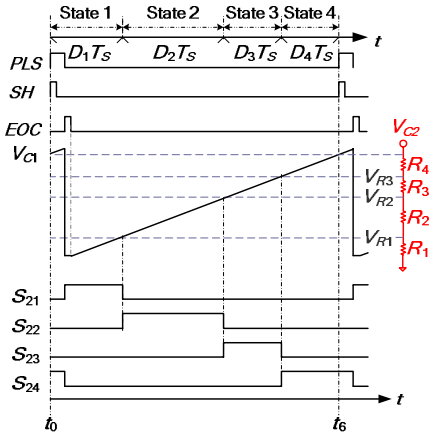

Fig. 7. Associated waveforms of the synchronous controller

3) State 3 [$t_3 - t_5$]: *Duration of L-L-C resonance and backward data transfer*

Fig. 4 shows the equivalent circuit of the proposed converter in State 3. In this state, the resonant quality factor (Q factor) is determined by the conduction state of transistor Q_5.

At $t = t_3$, L_m demagnetizes completely and starts resonating with L_k and C_P. Thus L_k, L_m and C_P form an L-L-C resonant tank with resonant frequency of

$$\omega_{r1} = \frac{1}{\sqrt{C_p(L_m + L_k)}}. \quad (3)$$

Since i_{Lk} and i_{Lm} are 0 at t_3 and transistor Q_5 is off, the amplitude of the resonant signal V_{AB} will be equal to $V_{AB}(t_2)$.

At $t = t_4 = t_3 + \Delta t$, transistor Q_5 turns on according to the logic state of transmitted backward datum TX_2, where Δt is a short delay caused by the synchronization between primary and secondary control circuits. When $TX_2 = 1$, transistor Q_5 is turned on and resistor R_S is connected to terminals C and D. This connection changes the equivalent impedance across terminals A and B, and results in a low quality factor and high oscillation damping (Fig. 3). Conversely, when $TX_2 = 0$, transistor Q_5 is turned off at t_4; thus, infinite Q factor will be obtained and V_{AB} will have a large oscillation amplitude that is approximate to V_{IN}. By detecting the oscillation amplitude of V_{AB}, backward datum can be retrieved. Moreover, no supplied power is required to transfer backward data.

Based on the operation theories described in States 1 and 2, it can be concluded that the times required for magnetizing and demagnetizing L_m are approximately equal. In order to reset the transformer completely, duty ratios must satisfy criterion $D_2 \geq D_1$.

4) State 4 [$t_5 - t_6$]: *Duration of control circuit synchronization*

In this state, Q_3 and Q_4 are both on, and voltages across the primary and secondary windings of the transformer will remain 0 until time t_6. Thus, V_{AB} will have an abrupt edge at the end of this state and the operation will return to State 1. This abrupt edge can be used as a synchronization signal on the transformer secondary side.

Fig. 5 presents a feasible primary control circuit of the proposed power converter. The primary control circuit comprises the following 5 primary circuit blocks: (1) a clock generator that provides a constant clock signal CK_1 for the primary control circuit; (2) a communication unit and a series bus interface for receiving/transferring data from/to the *Host* side; (3) a state controller that generates signals $S_{11,12,13, \text{ and } 14}$ to control operation timing of the proposed converter; (4) a phase-modulation circuit that controls the full-bridge switching phase and transmits the forward datum TX_1; and, (5) a threshold-level detector that retrieves the backward datum into RX_2 by detecting the voltage level of the primary winding voltage $|V_{AB}|$ measured in State 3.

Fig. 6 presents a feasible secondary control circuit for the proposed power converter. The secondary control circuit comprises the following 5 primary circuit blocks: (1) a communication unit and series bus interface that receives/transfers data from/to the *I/O* side; (2) a regulator that supplies power to the circuit on the transformer secondary side; (3) a synchronous controller that generates synchronous state signals $S_{21,22,23, \text{ and } 24}$ to synchronize the operation timing between the primary and secondary control circuits; (4) an impedance modulator that transfers the backward datum TX_2; and, (5) a phase detector that retrieves the forward datum into RX_1 by detecting the voltage of terminal D on the

transformer secondary winding in State 1. When V_D exceeds the reference voltage V_{REF2}, then RX_1 is set to 1; otherwise, RX_1 is set to 0.

Synchronized timing control is important to successfully retrieving forward data sent from the primary control circuit. Fig. 7 shows waveforms produced by the synchronous controller of the secondary control circuit. When a new switching cycle starts and causes an edge-change to V_{CD}, a synchronization pulse signal (PLS) is generated. By sensing the positive and negative edges of the PLS, a sample-and-hold (SH) signal and an end-of-cycle (EOC) signal are generated. The SH signal is used for storing the sampled voltage of V_{C1} at time t_0. The EOC signal discharges capacitance C_1 and initiates the charging cycle of C_1. By using a constant charging current, V_{C1} will be linearly charged up. The duty ratios of the four operational states $D_{1,2,3,\text{ and }4}$ are designed as constants. Duty ratios regeneration is based on the relationship of $R_1 : R_2 : R_3 : R_4 = D_1 : D_2 : D_3 : D_4$. Therefore, synchronous operational timing control signals $S_{21,\ 22,23,\text{ and }24}$ of the secondary control circuit can be generated easily.

III. Design Considerations

Component parameters L_k, L_m, C_P and R must be selected carefully to maximize the performance and reliability of backward data transfer. Once the equivalent parasitic capacitor C_P and leakage inductance of transformer L_k have been measured, magnetizing inductance L_m and resistance of the impedance modulator R_S can be derived. All components are assumed to have zero parasitic resistances.

The two cases of the proposed converter operated in State 3 (Fig. 4), according to the logic state of transmitted backward datum TX_2, are discussed as follows.

1) *Case 1* (Q_5 *OFF*)

The Q factor of a resonant circuit is defined as the ratio of maximum stored energy to energy loss per cycle, and is further equivalent to

$$Q = \omega_r \left(\frac{\text{maximum energy stored}}{\text{average power dissipated}} \right). \tag{4}$$

In Case 1, C_P, L_k, and L_m form the resonant tank with resonant frequency ω_{r1}. As no resistive element exists in the resonant circuit, the Q factor in Case 1 will be approximately infinite. Restated, amplitude of resonant signal V_{AB} will not decay over time. To ensure that backward data can be correctly retrieved by the threshold-level detector of the primary control circuit, at least 1/2 resonant cycle should exist in the duration of State 3. Accordingly, minimum magnetizing inductance L_m can be obtained from

$$\sqrt{C_p(L_m + L_k)} < \frac{D_3 T_S}{\pi}. \tag{5}$$

2) *Case 2* (Q_5 *ON*)

When transistor Q_5 turns on, a resistance R is parallel to magnetizing inductance L_m, where R is equivalent to n^2R_S. Thus, the resonant frequency and the Q factor of the resonant circuit changes. Since the imaginary part of resonant circuit impedance, Im(Z_{AB}), is zero at resonance,

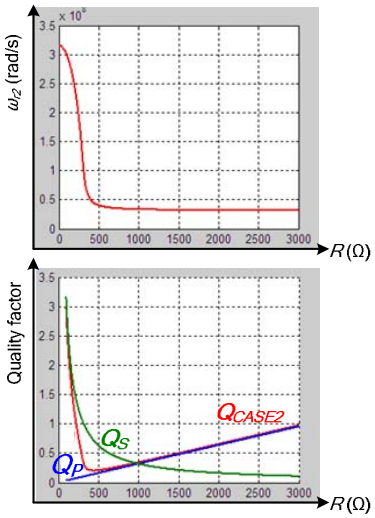

Fig. 8 (a) ω_{r2} vs. R. (b) Q factor vs. R.

resonant frequency in Case 2 can be obtained by

$$\omega_{r2} = \sqrt{\frac{-m + \sqrt{m^2 - 4n}}{2}} \tag{6}$$

where

$$m = \frac{C_p R^2 (L_m + L_k)^2 - L_m^2 L_k}{C_p L_m^2 L_k^2}, \quad n = -\frac{R^2 (L_m + L_k)}{C_p L_m^2 L_k^2}.$$

Thus, the quality factor of the resonant circuit of Case 2, Q_{CASE2}, can be obtained from the Q factor definition and (6), given as

$$Q_{CASE2} = \omega_{r2} C_p \operatorname{Re}(Z_{AB}) = \frac{\omega_{r2}^3 L_m^2 R C_p}{\left[\omega_{r2}^2 C_p R (L_m + L_k) - R\right]^2 + \omega_{r2}^2 L_m^2 \left(\omega_{r2}^2 C_p L_k - 1\right)^2}. \tag{7}$$

As seen in (7), Q_{CASE2} will be infinite when resistance R is infinite. This mathematical result is the same as that in Case 1 since the resonant circuit is the same. Moreover, when setting R as 0, the resonant tank contains only C_P and L_k, and Q_{CASE2} will be infinite too. Thus, Q_{CASE2} has a valley point (Fig. 8). Therefore, choosing an appropriate resistance R is extremely important to achieving a reliable backward data transfer process.

To determine the appropriate resistance R, the following two approximation methods can be employed: (1) when R is a small value satisfying $X_{Lm} >> R$, then L_m can be neglected and the resonant circuit in Case 2 can be approximated to a second-order series R-L_k-C_P resonant circuit with quality factor $Q_S = (\sqrt{}(L_k / C_P))/R$; and, (2) when R is a large value satisfying $X_{Lk} << |R // \mathrm{j} X_{Lm}|$, then L_k can be neglected and the resonant circuit in Case 2 can be approximated to a second-order parallel R-L_m-C_P resonant circuit with quality factor $Q_P = (\sqrt{}(C_P/L_m))*R$.

The resonant signal of a second-order resonant circuit has a decay function $e^{-\alpha t}$, where $\alpha = \omega_r/(2Q)$. When the second-order resonant circuit is operated at a critical damped condition such that $Q = 0.5$, then $e^{-\alpha t}$ will be as small as 0.04 at time $t = \pi/\omega_r$. Therefore, the design satisfying $Q < 0.5$, the overdamped condition, ensures

that backward data can be retrieved by the threshold level detector of the primary control circuit correctly. Similarly, one can also prove that $Q < 0.5$ generates a great data retrieval capability in Case 2.

An example is given below to illustrate the steps to obtain an optimum R value. We assume $C_P = 10$pF, $L_k =$ 1uH, and $L_m = 100$uH. The relation curves of $\omega_{r2}(R)$ and $Q(R)$ with respect to resistance R can then be obtained from (6) and (7) (Fig. 8). For design optimization, a minimal Q value is the best. By finding the minimum value of Q_{CASE2}, $R = R_{min} = 440\Omega$ can be obtained. Furthermore, the Q_{CASE2} curve closely matches the Q_P curve of the parallel R-L_m-C_P resonant tank when R is grater than 500Ω (Fig. 8). Therefore, finding the maximum resistance R_{max} that satisfies $Q_{CASE2} < 0.5$ can be replaced by finding the maximum resistance that satisfies $Q_P < 0.5$. This fact provides a convenient design consideration for finding an appropriate R value through neglecting the leakage inductance L_k. A computation that yields the maximum resistance such that $R_{max} = 1582\Omega$ satisfies the condition of $Q_P = 0.5$. Finally, an appropriate range of R is acquired that provides a reliable backward data retrieval process.

IV. Experimanetal Resulats

An experimental prototype has been built to verify the operation principles of proposed design. The specifications of the prototype are as follows:

V_{in} : 12V

I_O : 0 ~ 70mA

V_O : 4 ~ 12V

f_S : 400kHz

$D_1 : D_2 : D_3 : D_4 = 4 : 5 : 4 : 3$

The converter stage shown in Fig. 2 consists of the following components:

Q_1, Q_2, Q_3, Q_4, Q_5 : FQU2N60C N-channel MOSFETs

D_5, D_6, D_7, D_8, D_9, D_{10} : SB160 diodes

$C_O = 10\mu$F

Transformer : ferrite ring core TN9.6/6.3-3F3,
$N_P : N_S = 2:1$, $L_m = 98.7\mu$H,
and $L_k = 0.97\mu$H

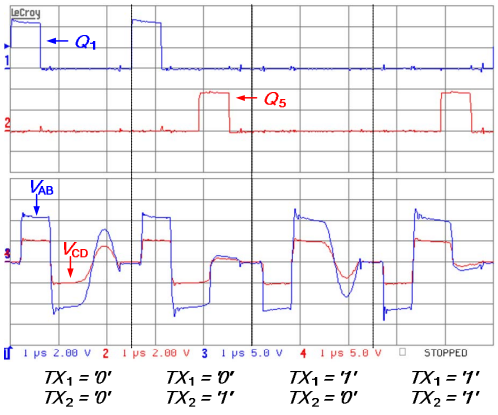

Fig. 9. Experimental waveforms for the proposed design

At first, L_m = 98.7uH was chosen. The measurement result shows that the resonant period of V_{AB} is 1us in State 3 at the condition f_S = 100kHz. Therefore, the equivalent parasitic capacitor of the switches across the terminals A and B of the full-bridge stage should be C_P = 254pF, and the resonant frequency satisfies the requirement given by (5). Finally, The resistance of impedance modulator $Rs = R/n^2 = 22\Omega$ was chosen according to (6) and (7) to achieve a reliable backward data transfer.

Since the transformer operates at DCM, magnetic saturation problem can be solved. Average output voltage V_O is 4.3V when load-current is 70mA, and maximum output voltage is 12V at zero-load condition.

Fig. 9 presents the experimental results of the proposed converter in four possible data-transmission cases. In Fig. 9, probe 1 shows the turned-on signal of Q_1; probe 2 shows the turned-on signal of Q_5; probe 3 shows the voltage across the transformer primary winding (V_{AB}); and, probe 4 shows the voltage across the transformer secondary winding (V_{CD}). For forward data transmission, the voltage phase of V_{AB} has already been successfully presented according to logic states of the forward datum TX_1 transmitted in State 1. For backward data transmission, the amplitudes of oscillation signals as mentioned in State 3 have also been successfully modulated by the transmitted backward datum TX_2 and can be clearly identified by a threshold level as expected. Finally, all the waveforms have well matched the theoretical ones.

V. Conclusion

The isolated full-bridge DC/DC converter with bi-directional communication capability has been presented with illustrations of its operations and analyses. A novel backward data transfer circuit which is achieved by manipulating the amplitude of the resonant signal is presented. An efficient approach for finding an appropriate range of modulation resistance to achieve reliable backward data communication is also presented. Experimental results have demonstrated that the proposed converter provide isolated power conversion and bi-directional communication via the same switching cycle. In conclusion, the proposed power converter provides high isolation capability by using an isolated transformer and has a small device footprint.

Acknowledgment

The authors would like to thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under Contract No. NSC 96-2221-E-009-239-MY3.

References

[1] Jeffrey D. Wilkinson, "Input isolation circuit for computer-controlled medical device," *US Patent*, no.5267150, Nov. 30, 1993.

[2] Chengwu Chen and Michael A. Gley, "Scheme for isolating a computer system from a data transmission network," *US Patent*, no.5473552, Dec. 5, 1995.

[3] Michael J. Gambuzza, "Data access arrangement for a digital subscriber line," *US Patent*, no.6226331, May 1, 2001.

[4] Raphael Rahamim and Grey Beutler, "Modem a digital high voltage isolation barrier," *US Patent*, no.6351530, Feb. 26, 2002.

[5] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters", *IEEE Trans. Industrial Electronics*, vol. 42, pp. 595–603, 1995.

[6] Quan Li and P. Wolfs, "A leakage-inductance-based ZVS two-inductor boost converter with integrated magnetics," *IEEE Power Electronics Letters*, vol. 3, pp. 67–71, 2005.

[7] Tiecheng Sun, Xueqin Zhu, Hongpeng Liu, Lian Liang, and Peng Gao, "A Novel ZVS PWM FB DC/DC Converter Using Auxiliary Resonant Net," in *Proc. 12th International Power Electronics and Motion Control Conference*, pp. 728–732, 2006.

[8] K. Siri and C. Q. Lee, "Constant switching frequency LLC-type series resonant converter," in *Proc. 32nd Midwest Symposium on Circuits and Systems*, vol. 1, pp. 513–516, 1989.

[9] Yilei Gu, Zhengyu Lu and Zhaoming Qian, "A Novel LLC Resonant Converter Topology**:** Voltage Stresses of All Components in Secondary Side Being Half of Output Voltage," in *Proc. of CES/IEEE 5th International Power Electronics and Motion Control Conference*, vol. 1, pp. 1–5, 2006.

[10] C.Q. Lee, R. Liu, and I. Batarseh, "Parallel resonant converter with LLC-type commutation," *IEEE Trans. Aerospace and Electronic Systems*, vol. 25, pp. 844–847, 1989.

[11] A. Bucher, T. Durbaum, D. Kubrich, and A. Stadler, "Comparison of Different Design Methods for the Parallel Resonant Converter," in *Proc. 12th International Power Electronics and Motion Control Conference* , pp. 810–815, 2006.