GYAN PRATIPAT

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Education

Master of Science in Computer Engineering (Computer Systems) 08/2024 - 05/2026
Arizona State University, USA GPA: 3.7/4
- *Coursework:* VLSI Design Automation, Comp. Arch. II, Mobile Computing, Algorithms, Prob. & Random Processes

Bachelor of Technology in Electronics & Communication Engineering 08/2017 – 07/2021
National Institute of Technology Srinagar, India CGPA: 7.8/10
- *Coursework:* Analog Electronics, Digital Electronics, Microcontrollers, VLSI Design, Compilers, Computer Architecture

Skills

Programming: C, C++, Python, Embedded C, Shell Scripting (Bash), CUDA, OpenMP, MySQL
Development Tools: Git, Docker, Visual Studio, Jupyter, Linux (Ubuntu, Debian), CI/CD Pipelines
Scientific Computing: Google Cloud Platform, MATLAB, Simulink, JAX, OriginLab, NumPy, SciPy
Simulation Tools: Gem5, Vivado, Cadence Virtuoso, COMSOL Multiphysics, ModelSim, Ansys HFSS
Frameworks & Libraries: ROS (Robot Operating System), OpenCV, TensorFlow, NumPy, SciPy, PyTorch
Hardware Integration: Microcontroller Programming, Sensor Interfaces (I2C, SPI, UART), Real-time Systems

Experience

Volunteer Researcher 08/2024 – 01/2025
Make Programming Simple Lab @ ASU Tempe, Arizona
- Achieved 90% accuracy in **AI** model training, and gathered 500+ data points to improve **Quantum Machine Learning embeddings**
- Investigated Autodifferentiation in 'Catalyst' Library by Pennylane for Hardware Agnostic Quantum Computation

Scientist B 03/2022 – 08/2024
Centre for Development of Advanced Computing (C-DAC), Govt. Of India Patna, India
- Accelerated a Qiskit-independent, 20 Qubit State-Vector Quantum Simulator using High Level Programming languages
- Prototyped **FPGA** implementation of 1-qubit Quantum gates for quantum circuit simulation for **Machine Learning**
- Trained 100+ Senior Secondary Government teachers in **Python**, positively impacting education of 30,000+ students
- Supervised 10-member team for **Linux**-based server management for recruitment the Indian Coast Guard, contributing to 15% revenue generation

Engineer 08/2021 – 03/2022
Coherent Corp. (Former II-VI Inc.) Hyderabad, India
- Conducted debugging & **signal integrity validation** for optical transceiver DUT, ensuring 40% reduction in bugs
- Migrated 100+ Test Classes from vb.net to **C#** & Managed version control via **Perforce & Git**
- Containerized practical software solutions using **Docker** to enable consistent testing across multiple devices-under-test

Research Intern 09/2019 – 11/2019
Indian Institute of Science Bangalore, India
- Achieved 80% accuracy in outdoor path prediction using **Neural Network** approach for 3D depth estimation technique on monocular images
- Modelled an outdoor setting and Simulated outdoor path prediction model for UAV on **ROS**
- Coded **ESP8266+AtMega** & **RPi** to achieve 3x better real-time wireless control on teleoperated UAV landing vehicle

Project Intern 06/2019 – 08/2019
Defence Research & Development Organisation New Delhi, India
- Tested & debugged **embedded C** code to automate Ammonia detection with Carbon Nanotube sensors
- Achieved 95% accuracy in automated Ammonia sensing by controlling purging frecuency of the sensor through **Arduino**

Projects

Static Timing Analysis Tool for VLSI Circuits | *Python, Data Structures* 01/2025 – 02/2025
- Implemented a netlist parser, liberty file interpreter & topological traversal algorithm for 100,000+ gates in **Python**
- Engineered circuit analysis features like 2D delay interpolation with look-up tables without relying on built-in libraries

GPU-Accelerated Quantum Circuit Simulator | *C++, OpenMP, CUDA, Python, Linux* 02/2023 – 08/2024
- Developed a 20-qubit state vector quantum simulator with parallel execution capabilities on NVIDIA GPUs
- Optimized memory access patterns in **Linux** & computational kernels for **GPU** , achieving 5x speedup over Xeon 6326
- Executed GHZ state preparation, QFT, & HHL algorithms under 60 seconds with performance benchmarking

FPGA-Based Accelerator for Matrix Multiplication | *Verilog, Vivado, ModelSim* 06/2022 – 12/2022
- Prepared **synthesizable RTL using Verilog**, ensuring a 20% reduction in latency
- Optimized multiplication using pipelined MAC units, achieving 2x speedup over sequential software execution
- Implemented fixed-point arithmetic optimizations to reduce FPGA resource utilization

Real-time Vehicle Number Plate Recognition System | *Python, OpenCV, Tesseract* 09/2020 – 05/2021
- Developed a **3-stage image processing pipeline** for number plate extraction & linked it to a **MySQL** database
- Utilized **computer vision** algorithms for feature extraction & pattern recognition on 3000+ car images
- Containerized the application using **Docker** for consistent deployment across testing environments

Achievements

- Received a merit-based **Engineering Graduate Fellowship** for 2024-2025 through the Fulton Schools of Engineering
- Achieved 94.32 percentile in Graduate Aptitude Test in Engineering (GATE) - 2021 in ECE
- Earned a badge for completing IBM Quantum Challenge: Spring 2023