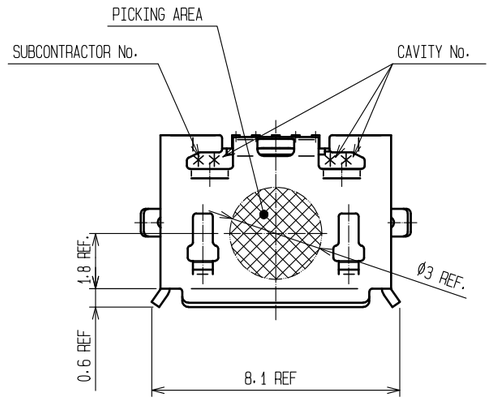
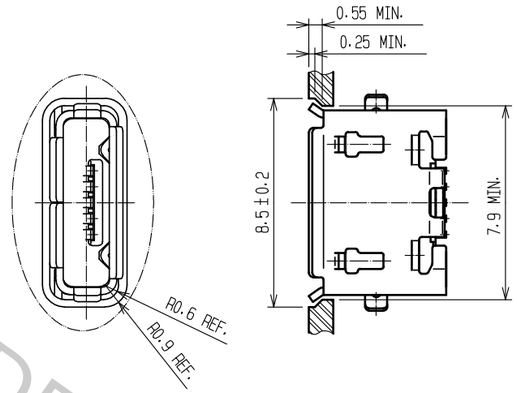
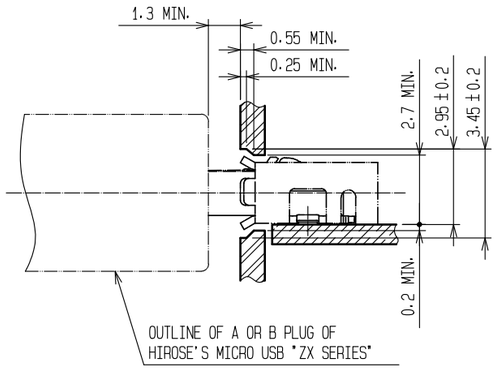
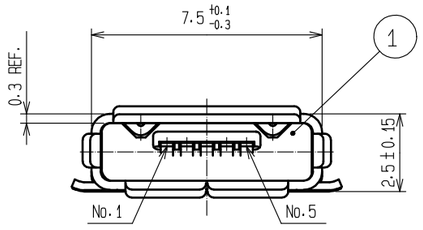


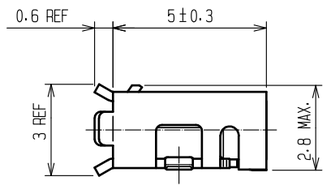
RECOMMENDED PANEL CUTOUT (4:1)

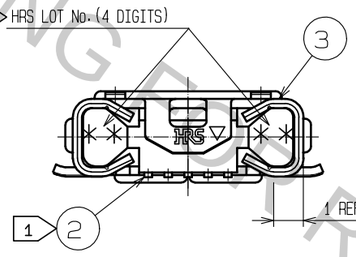


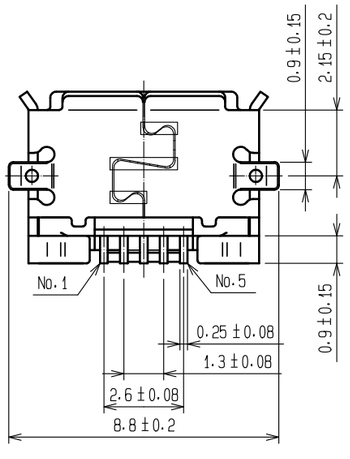
MATED WITH CORRESPONDING PLUG (4:1)











NOTES 1 CO-PLANARITY IS WITHIN 0.08 mm.

2 PLATING
CONTACT AREA : GOLD 0.75μm min.
LEAD AREA : GOLD 0.05μm min.
UNDER PLATING: NICKEL 2μm min.

3 PER REEL : 3500 pcs.

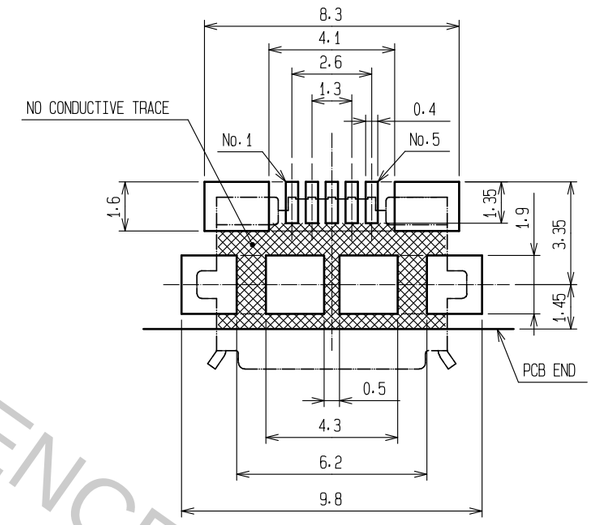
4. INTERFACE DIMENSIONS CONFORM TO USB2.0 SPECIFICATION.

5. AS FOR PART No.3, THE PERFORMANCE REMAINS GOOD EVEN IF THERE ARE RUBBING WOUNDS BY THE ASSEMBLY PROCESS. AND, THE PERFORMANCE REMAINS GOOD THOUGH THERE MIGHT BE A DIFFERENCE IN THE PLATING LUSTER BETWEEN EACH PLATING SUBCONTRACT COMPANIES.

6. AS FOR PART No.1 A PART OF SHAPE MAY BECOME DIFFERENT DEPENDING ON THE PRODUCTION METHOD.

7 CODE CONFIGURATION IS SHOWN IN FIG.1.

PCB LAYOUT



GENERAL TOLERANCE IS ±0.05 mm.

NO.	MATERIAL	FINISH , REMARKS
5	PE	
4	PS	
3	STAINLESS STEEL	OVER PLATING:TIN 1μm min. LUBRICANT
2	COPPER ALLLOY	2
1	LCP	GRAY. UL94V-0

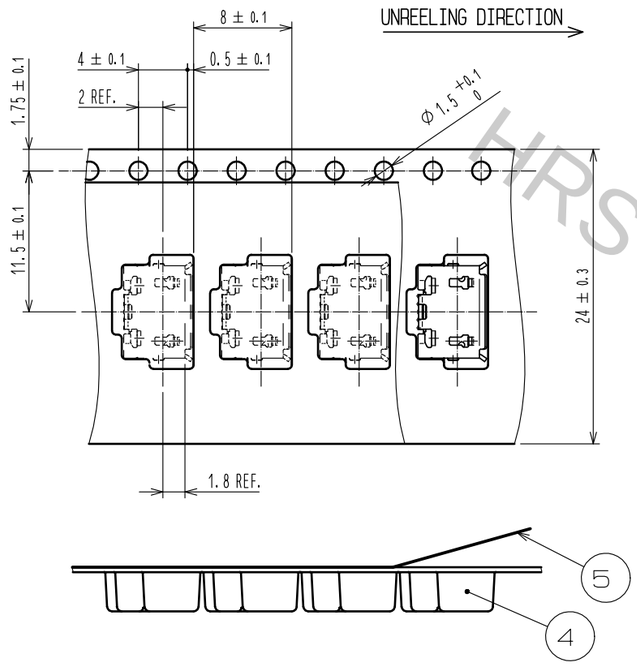
UNITS	SCALE		COUNT	DESCRIPTION OF REVISIONS	DESIGNED	CHECKED	DATE
mm	5 : 1	△0					

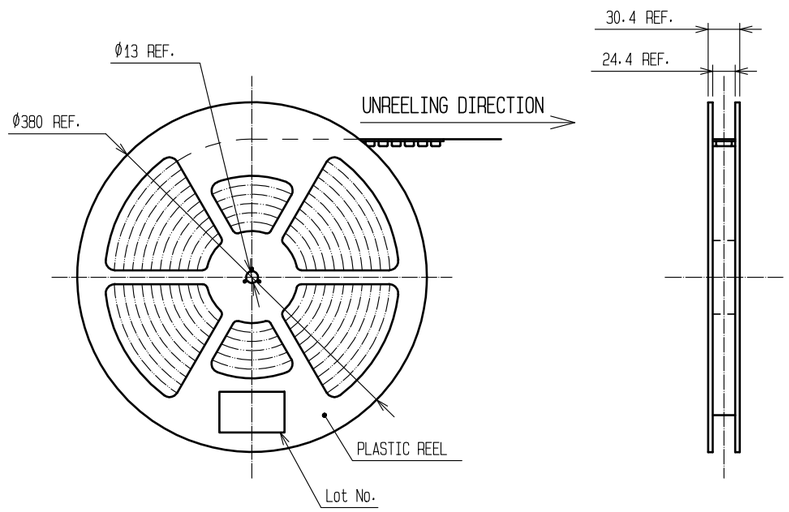
HIROSE ELECTRIC CO., LTD.

APPROVED	NM. NISHIMATSU	15. 10. 27
CHECKED	KN. ICHIKAWA	15. 10. 27
DESIGNED	TS. ITO	15. 10. 27
DRAWN	AK. AKIYAMA	15. 10. 27

DRAWING NO.	EDC-126557-31-00
PART NO.	ZX62-AB-5PA(31)
CODE NO.	CL242-0045-7-31 △0 1/2

3 DRAWING FOR PACKING (FREE)





7 FIG-1 LOT CODE CONFIGRATIONS FOR 4 DIGITS

YEAR		MONTH		DAY						LINE No.	
YEAR	CODE	MONTH	CODE	DAY	CODE	DAY	CODE	DAY	CODE	LINE No.	CODE
2007	7	Jan.	A	1	1	11	B	21	M	1	A
2008	8	Feb.	B	2	2	12	C	22	N	2	B
2009	9	Mar.	C	3	3	13	D	23	P	3	C
2010	0	Apr.	D	4	4	14	E	24	Q	4	D
2011	1	May.	E	5	5	15	F	25	R	5	E
		Jun.	F	6	6	16	G	26	S	6	F
		Jul.	G	7	7	17	H	27	T	7	G
		Aug.	H	8	8	18	J	28	U	8	H
		Sep.	I	9	9	19	K	29	V	9	I
		Oct.	J	10	A	20	L	30	W	10	J
		Nov.	K					31	X	11	K
		Dec.	L								

HRS	DRAWING NO.	EDC-126557-31-00
	PART NO.	ZX62-AB-5PA(31)
	CODE NO.	CL242-0045-7-31

△0 2/2