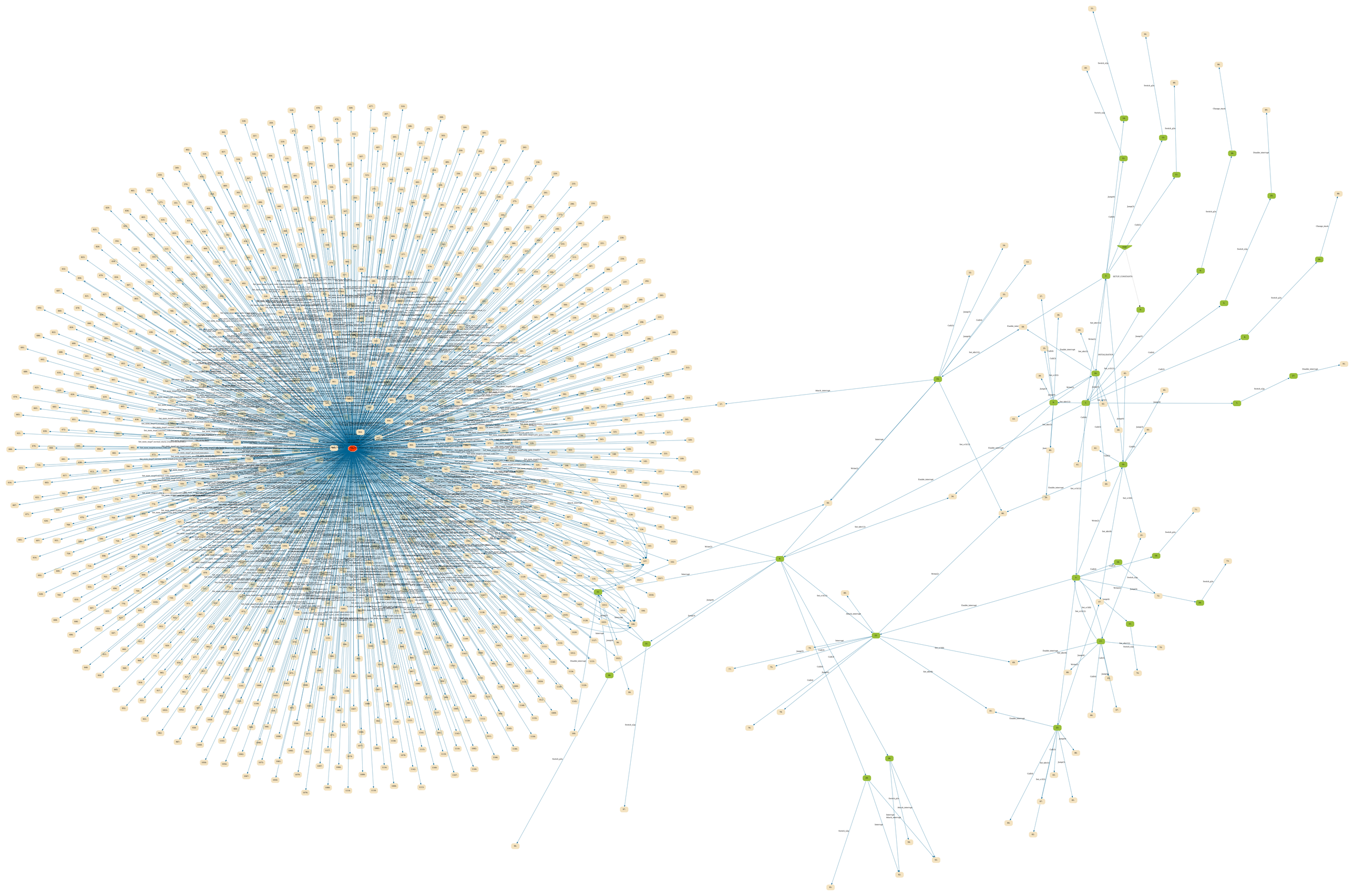
Attack_interrupt
Interrupt
Switch_a2p
Switch_p2a
Change_stack
Disable_interrupt
Enable_interrupt
Set_ebr(12)
Set_ebr(0)
Set_ssp(12)
Set_ssp(0)
Set_cr3(12)
Set_cr3(0)
Set_cr4(12)
Set_cr4(0)
Set_cr0(12)
Set_cr0(0)
Set_cr2(12)
Set_cr2(0)
Set_cr8(12)
Set_cr8(0)
Set_msr(12)
Set_msr(0)
Set_gdtr(12)
Set_gdtr(0)
Set_idtr(12)
Set_idtr(0)
Set_ldtr(12)
Set_ldtr(0)
Set_tr(12)
Set_tr(0)
Set_fpu(12)
Set_fpu(0)
Set_sse(12)
Set_sse(0)
Set_avx(12)
Set_avx(0)
Set_pkru(12)
Set_pkru(0)
Set_xcr0(12)
Set_xcr0(0)
Set_pat(12)
Set_pat(0)
Set_efer(12)
Set_efer(0)
Set_debugctl(12)
Set_debugctl(0)
Set_smbase(12)
Set_smbase(0)
Set_rflags(12)
Set_rflags(0)
Set_rip(12)
Set_rip(0)
Set_dr7(12)
Set_dr7(0)
Set_rsp(12)
Set_rsp(0)
Set_cs(12)
Set_cs(0)
Set_ds(12)
Set_ds(0)
Set_es(12)
Set_es(0)
Set_fs(12)
Set_fs(0)
Set_gs(12)
Set_gs(0)
Set_ss(12)
Set_ss(0)
Set_tsc(12)
Set_tsc(0)
Set_dr0(12)
Set_dr0(0)
Set_dr1(12)
Set_dr1(0)
Set_dr2(12)
Set_dr2(0)
Set_dr3(12)
Set_dr3(0)
Set_dr6(12)
Set_dr6(0)
Set_r8(12)
Set_r8(0)
Set_r9(12)
Set_r9(0)
Set_r10(12)
Set_r10(0)
Set_r11(12)
Set_r11(0)
Set_r12(12)
Set_r12(0)
Set_r13(12)
Set_r13(0)
Set_r14(12)
Set_r14(0)
Set_r15(12)
Set_r15(0)
Set_rax(12)
Set_rax(0)
Set_rbx(12)
Set_rbx(0)
Set_rcx(12)
Set_rcx(0)
Set_rdx(12)
Set_rdx(0)
Set_rsi(12)
Set_rsi(0)
Set_rdi(12)
Set_rdi(0)
Set_rbp(12)
Set_rbp(0)
Jump(12)
Jump(0)
Call(12)
Call(0)
Write(12)
Write(0)
Enable_interrupt
Disable_interrupt
Switch_a2p
Switch_p2a
Change_stack
Attack_interrupt
Interrupt
Jump(12)
Jump(0)
Call(12)
Call(0)
Write(12)
Write(0)
Enable_interrupt
Disable_interrupt
Switch_a2p
Switch_p2a
Change_stack
Attack_interrupt
Interrupt