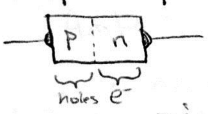
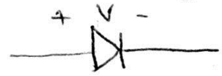
Group IV w/5 → type n-semiconductor
Group IV w/3 → type p-semiconductor



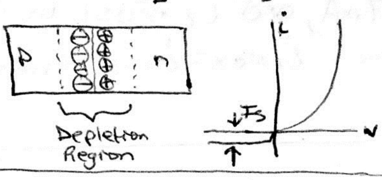
→ i_D - diffusion current
← i_S - Drift current



$i_D = I_S(e^{V_D/nV_T} - 1) = PWL$

$V_T = \frac{KT}{q} = 25mV$ @ room temp.

Reverse Bias: $i_D \ll I_S$
Forward Bias: $i_D \gg I_S$



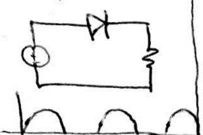
Piecewise Linear Diode Models (PWL)

$i_D = I_S(e^{V_D/nV_T} - 1)$: Normal Diodes

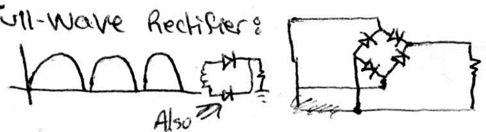
V_D/V_F are the turn on voltages.
$r_d = nV_T / I_D$

Rectifier Circuits

Half-Wave Rectifier:



Full-Wave Rectifier:



DC voltage = V_{pk} + $\frac{1}{2}V_{ripple}$
$V_D | V_F \approx 0.7$ volts (Depending)

half wave rectifier:

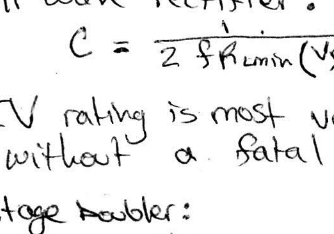
$$C = \frac{1}{f R_{Lmin}(V_r/V_p)} = \frac{i_{Lmax}}{f V_r}$$

Full wave rectifier:

$$C = \frac{1}{2 f R_{Lmin}(V_r/V_p)} = \frac{i_{Lmax}}{2 f V_r}$$

PIV rating is most voltage withstand without a fatal Breakdown.

Voltage doubler:



$V_L = 2V_{sec}$

Peak Diode current

$i_{Dmax} = I_L(1 + 2\pi\sqrt{2V_p/V_r})$ half wave rect.

$i_{Dmax} = I_L(1 + 2\pi\sqrt{V_p/2V_r})$ fullwave rect.

LAB Things

% ripple = 100 $\frac{V_{ripple}}{V_{DC\,avg.}}$

$$\frac{V_{ripple}}{V_{peak}} = \frac{T}{2R_LC}$$

$i_S = \frac{V_C - V_Z}{R_S}$ finding R_S (Zener rect.)

$V_C = V_{sec} - 2V_F$

$i_S = i_{Zmin} + i_{Lmax}$ (R max value)

$R_S = \frac{V_{sec} - 2V_F - V_Z}{i_{Zmin} + i_{Lmax}}$

$P_{Zmax} = V_Z i_S$

$C_{min} = \frac{i_S}{2f(V_C - V_Z)}$

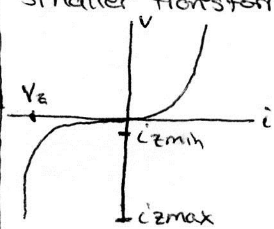
Caps SC for AC voltage
Caps OC for DC voltage

X_C = reactance = $-\frac{1}{2\pi f C}$

Capacitor Reactance for an attenuator

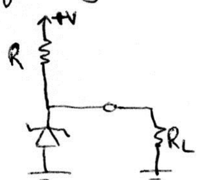
Zener Diodes

- Clamp the voltage at or below a certain level.
- Convert to higher freq, then smaller transformer.



i_{Zmax} determined by max power Dissipation rating.
if too big then reverse breakdown

voltage regulator:



R_{max}
i_Z min
i_L max

$i_{Lmax} < 0.5 P_{Zmax}/V_Z$

2x safe for Zener power

R_{min}
i_Z max (all current)

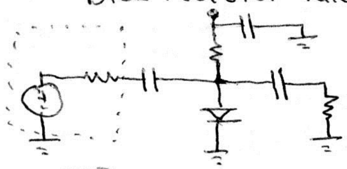
Rule of Thumbs

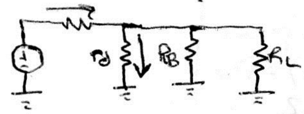
V_{sec} is 30-50% higher V_L
i_{Zmin} is 1/20 i_{Zmax}
Cap used is 5 x C_{min}
Make power diss. 1/2 P_{max}

Seperate AC/DC analysis: Superposition
Caps SC for AC
Caps OC for DC

DC v & i is much higher than AC

Design path → r_d values → I_D values, Bias resistor values.





AC analysis, current all through r_D, solve for r_d.

After find r_D, use $r_d = \frac{nV_T}{I_D}$ to find I_D.
Use these I_D values to find R_B using DC.

inductors Block AC, Pass DC
Capacitors Block DC, Pass AC

Varacter & Schottkey Diodes

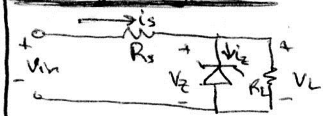
Varacter diode:
Voltage Variable Capacitor (VVC)
std. Pn-junction under reverse bias
$C = \epsilon A / d$ (dielectric con)(Area)/sep. dist.

Schottkey Diode:
Low forward voltage
Voltage clamping.
Fast switching time

PWL Model of a Diode

If forward bias: $V_D = V_{D0} + i_D r_d$

Voltage regulator



$i_{Lmax} = \frac{V_Z}{R_{Lmin}}$

i_{Lmax} is relatively stable

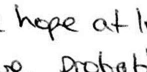
$R_{max} = \frac{V_{inmin} - V_Z}{i_{Smin}} = \frac{V_{inmin} - V_Z}{i_{Zmin} + i_{Lmax}}$

$R_{min} = \frac{V_{inmax} - V_Z}{i_{Zmax}}$

$R_{min} < R < R_{max}$ (we hope at least)
If this isn't true, probably too small of a Zener diode for the size of the load

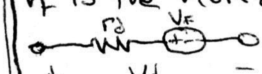
PWL iv characteristics

$r_d = \frac{1}{\text{slope of line}}$

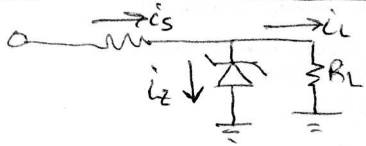


$= \frac{\Delta V}{\Delta i}$

V_F is the horizontal intercept (x-int)

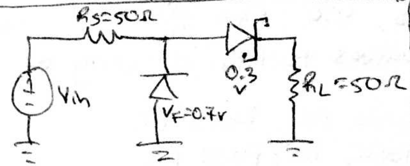


Give reason's not to use large Caps to make very small ripple voltages:
1) relatively expensive as size increases
2.) Take up a lot of space and are heavy

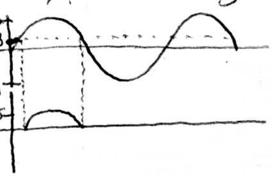


For Full-wave rect (only 2 diodes) if are installed backwards then no current gets to the load, $V_o = 0$

The max i_L value must also be able to go through the zener. The zener power should be $V_z(i_{zmax}) = P_{wz}$ with safety factor x2

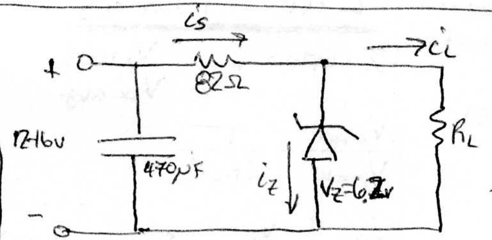


When $V_{in} > 0.3v$ for shottkey, the voltage in excess over 0.3v is divided up over both resistors as a percent. In this case, evenly. Thus, the following occurs:



goes to 0.35 cause max diff is 0.7v. It's divided up evenly across Rs.

Zener works like normal diode in Fwd bias



$i_{zmin} = 4mA$
How large i_L until zener fails.

If $V_L = 6.2v$,

$$i_{s\,min} = \frac{V_{e\,min} - V_L}{82\Omega} = \frac{12-6.2}{82} = 70.7mA$$

$$i_{s\,max} = \frac{V_{e\,max} - V_L}{82\Omega} = \frac{16-6.2}{82} = 119.5mA$$

$i_s = i_z + i_L$

i_s can be as low as 70.7mA, and i_z must be ≥4mA, so i_L can be no larger than: $i_{L\,max} = i_{s\,min} - i_{z\,min}$
$= 70.7 - 4 = \boxed{66.7mA}$

Negligible ripple means diode on. ripple significant means the diode is off and cap. is discharging.