

CSE 321

Real -Time and Embedded Operating Systems

 University at Buffalo
Department of Computer Science
and Engineering
School of Engineering and Applied Sciences

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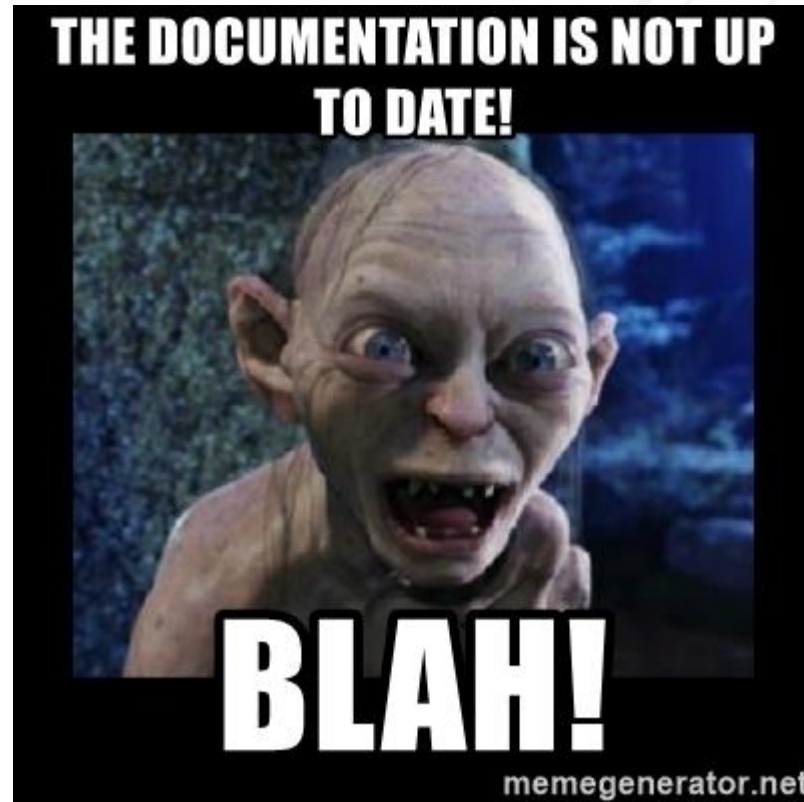


Documentation

- In general, documentation is critical
- Allows for proper design
- Allows for efficient maintenance

This is a critical idea all around and it comes in many forms

- Some cases will need all the types of documentation, some will not



Why do we care about this now?

- *Why not care?*
- Reality is collaborative...you are one step closer to those projects and jobs if you aren't there already
 - Others will read, maintain, debug, and modify your code
- Academic Integrity

What things can go in documentation?

- Specifications
- Features
- Applications
- Revision History
- Quick Start
- Conventions
- Block Diagrams
- Logic Description
- Schematics
- Timing Diagrams
- Circuit Description
- Behavior Table
- Test Plan
- Active Levels
- Name Explanations
- Reference Designations
 - Pin configurations and functions
- Operating Properties
- Glossary
- Bill of Materials
- ASM (Algorithm State Machine)
- FSM (Finite State Machine)
- Flow Chart

How do you know what to include?

- It will be in the assignment instructions for each project
 - A template **Table of Contents** will be provided to guide you in building the content for your documentation



Some Key Documentation Elements



Specification

- Often referred to as *spec*
- Describes what the system should do
 - Inputs
 - Outputs
 - Functions
- The *what* not the *how* in this part (you can have some with how in it)

Applications

- The where and when for using this design



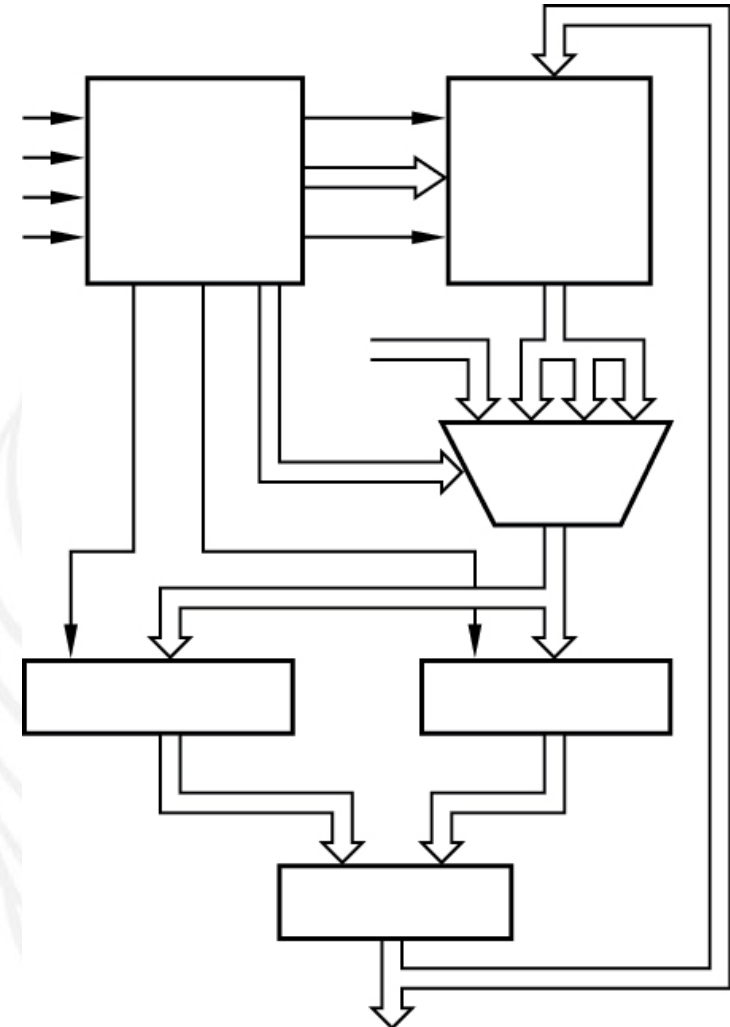
Revisions

- Frequently things are “snowballed” ... they are built on top of legacy materials
 - Not from scratch

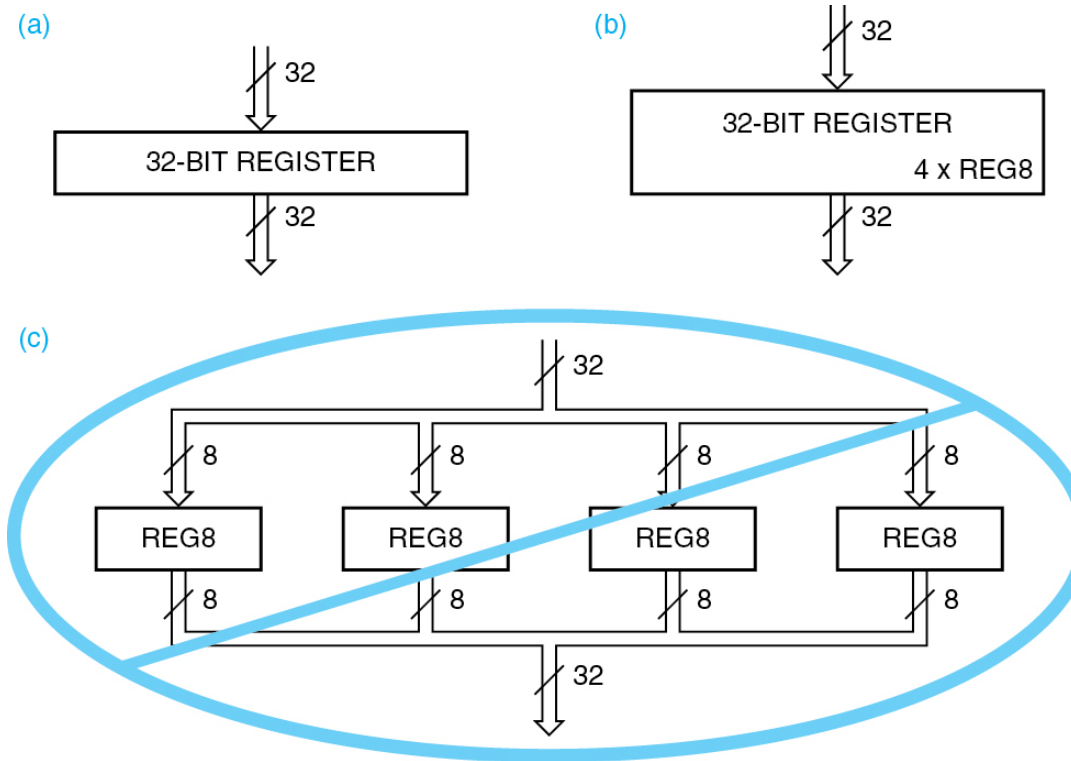


Block diagram

- A high level graphical overview
 - Function modules
 - Basic interconnects



How much detail?



Logic-device description

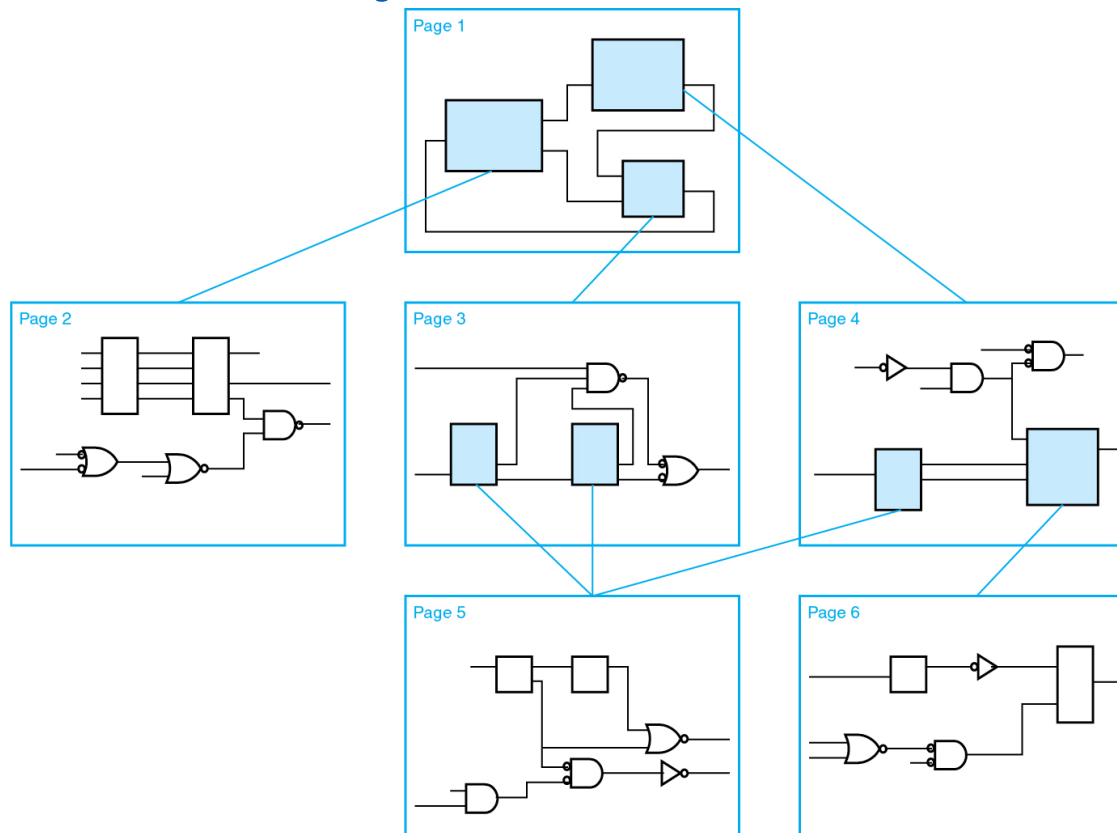
- Functions that are custom
 - You see this with ASIC, FPGA, PLD, and CPLD type devices
 - ASIC- application specific integrated circuits
 - FPGA-field programmable gate array
 - PLD- programmable logic device
 - CPLD- complex programmable logic device
- Mostly in English - but internal specifications need another approach to describe the behavior
 - Diagrams, equations and tables
 - HDL- Hardware descriptive language
 - Conventional languages (like C)

Logic Diagram vs Logic Schematic

Diagram: Basic

Schematic: More detailed, contains all the necessary stuff to actually build it, including electrical properties

Not all schematics have the electrical detail, sometimes it is just more detail

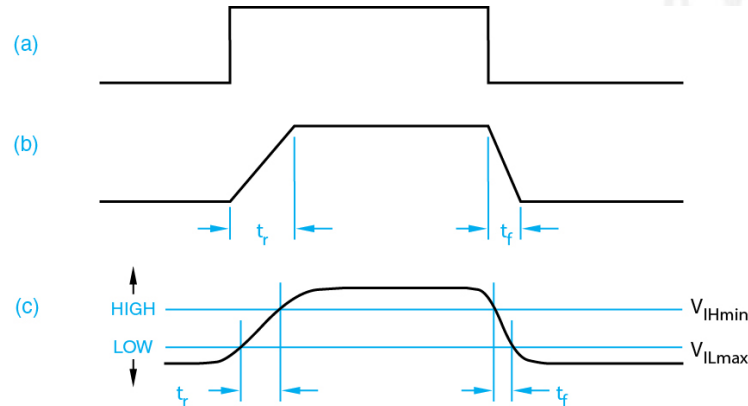


BOM - Bill of materials

- You saw this on UB Learns
 - It typically won't have links or as many options
- It is the list of the components that are needed for implementation

Timing Diagram

- Time is real
- Nothing is ideal
- Nothing happens instantly
- There are delays that can happen from the changes
- This means everything is actually a signal

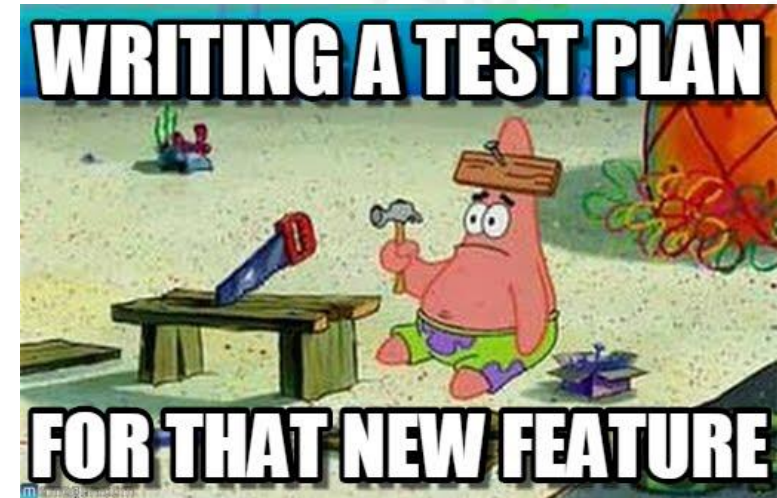


Circuit Description

- This gives more details to how the circuit works internally
- There are a lot of operational considerations

Test Plan

- Plans are good and important
- What do good plans include?
 - Methods and resources to verify/test proper operation
 - This is for before, during, and after construction



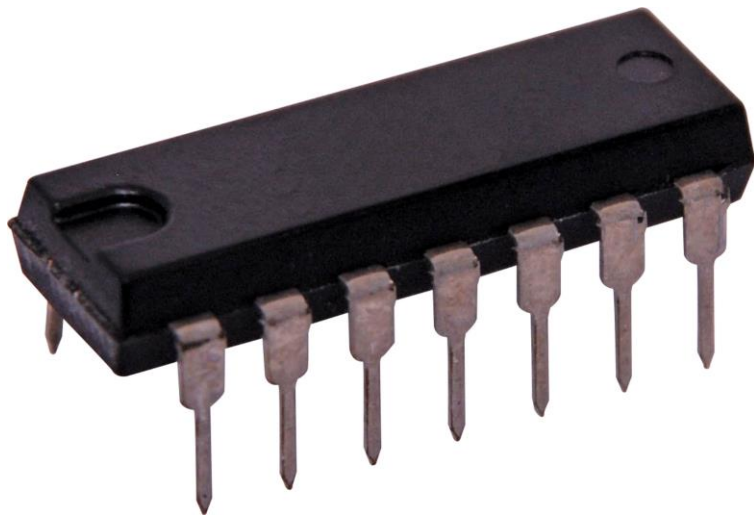
Names

- Arbitrary, but good skills are important
- What does a good name tell you?
 - What the purpose is for that signal or input
 - Active high or active low functionality
 - Be safe and define it still

<i>Active Low</i>	<i>Active High</i>
READY-	READY+
ERROR.L	ERROR.H
ADDR15(L)	ADDR15(H)
RESET*	RESET
ENABLE-	ENABLE
-GO	GO
/RECEIVE	RECEIVE
TRANSMIT_L	TRANSMIT

Reference Designation

- Consider the notch or dot on your ICs from lab
- Tells you orientation info



Pin Functions

NAME	PIN				I/O	DESCRIPTION
	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	6	6	6	I	Gate 2 input
2B	5	7	7	8	I	Gate 2 input
2Y	6	5	5	9	O	Gate 2 output
3A	10	—	9	13	I	Gate 3 input
3B	9	—	10	14	I	Gate 3 input

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Product Folder Links: [SN5400](#) [SN54LS00](#) [SN54S00](#) [SN7400](#) [SN74LS00](#) [SN74S00](#)

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00

SDLS025D – DECEMBER 1983 – REVISED MAY 2017

TEXAS
INSTRUMENTS

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Pin Functions (continued)

NAME	PIN				I/O	DESCRIPTION
	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V _{CC}	14	8	4	20	—	Power supply

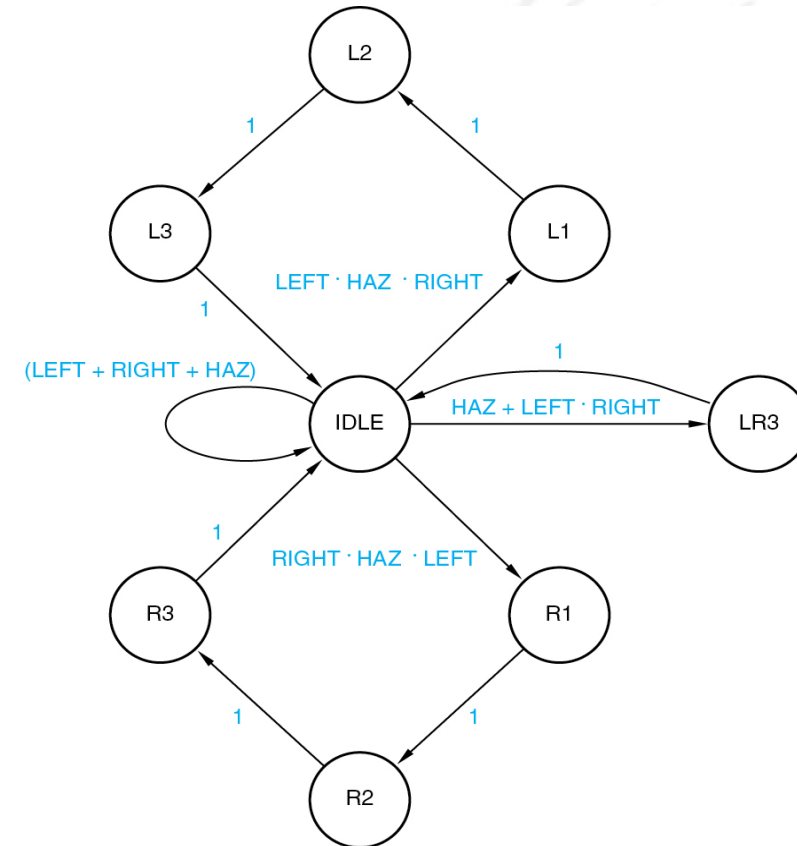
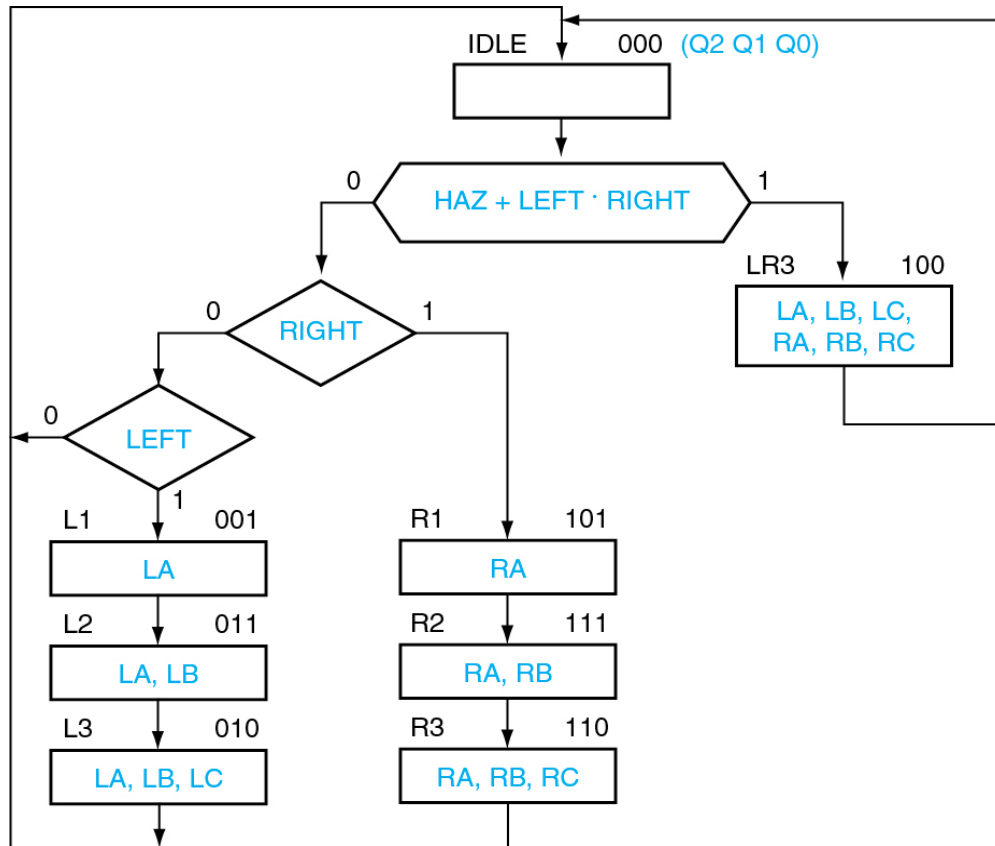
Time Properties

6.9 Switching Characteristics: SNx4LS00

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

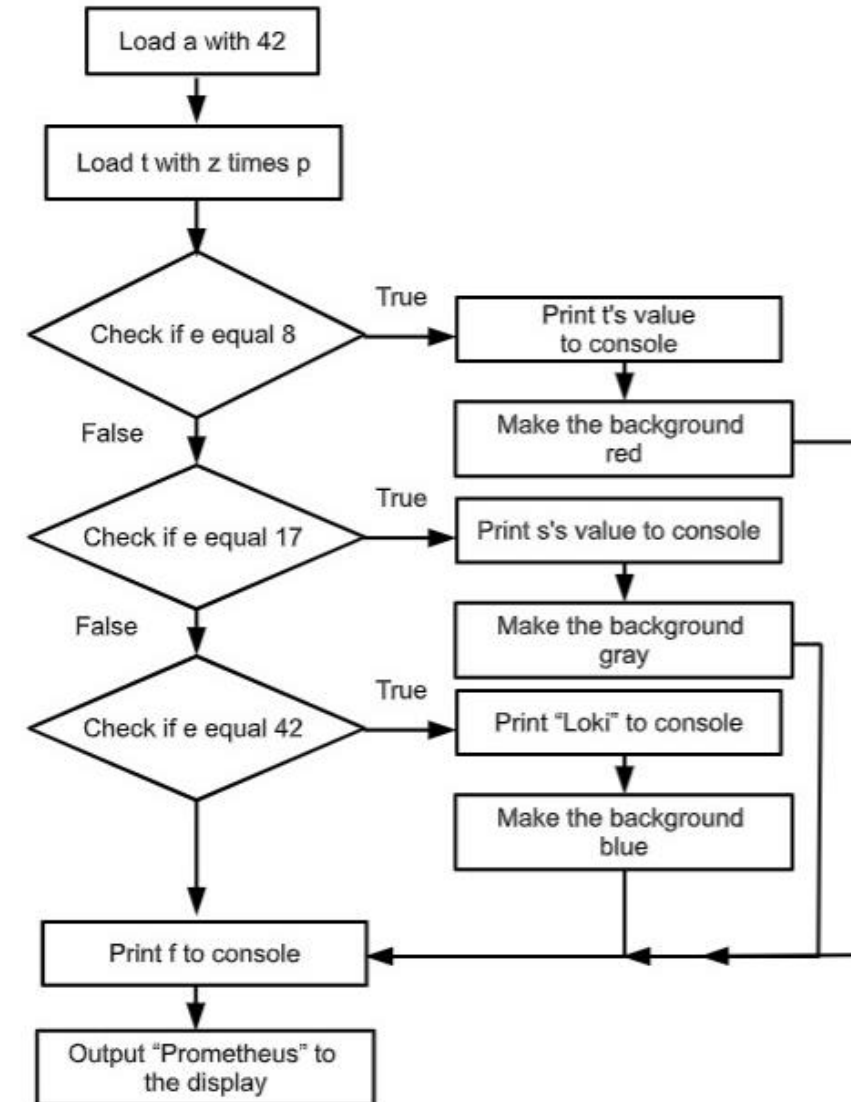
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2\text{ k}\Omega$ and $C_L = 15\text{ pF}$		9	15	ns
t_{PHL}					10	15	

ASM vs FSM



Flow Chart

- Very Very similar to an ASM...
but flow charts don't have timing considered



Language

- Complete sentences outside of lists
- Captions on all figures
- No pronouns
- Descriptive
- Concise
- Tends to be passive tone
 - That dry “it shall be known...” type

Need help with grammar/spelling...try my friend [grammarly.com](https://www.grammarly.com) (the free version is really helpful)

- You can use the UB Writing center on your work: <http://www.buffalo.edu/writing.html>
- Other references: [Purdue OWL](#), [Excelsior OWL](#), [IEEE Citation Guide](#)
- Talk with a TA/Instructor

References

- “Digital Design: Principles and Practice” 5th Edition, by John F. Wakerly. Pearson, 2017. ISBN-13: 978-0134460093, ISBN-10: 013446009X
- “Digital Design With An Introduction to the Verilog HDL, VHDL, and SystemVerilog” 6th Edition, by M.Morris Mano and Michael D. Ciletti
- “Fundamentals of Digital Logic with Verilog Design”, 1st Edition, by Stephen Brown and Zvonko Vranesic

Plus more in the notes on many pages



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