LCM Modeling for SONOS 3D NAND

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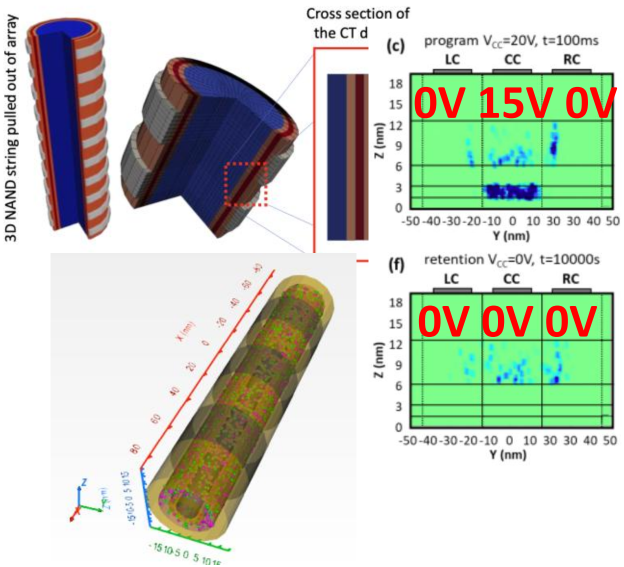
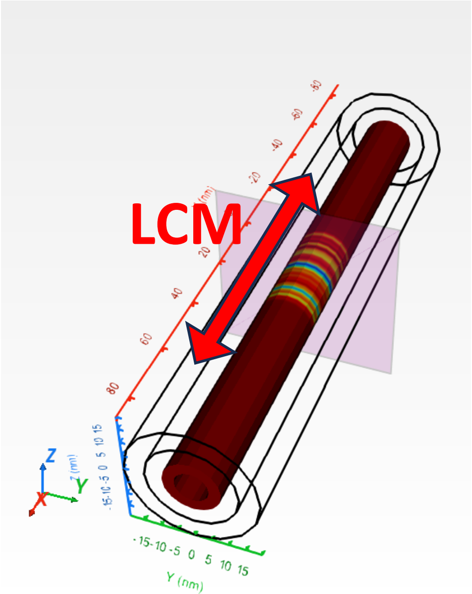
LCM Modeling

- **3D NAND model built on AMAT Ginestra (template from Prasanna*)** pravindran6@gatech.edu
  - Base Device: Cylindrical SONOS 3D CT-NAND
  - Added: LCM model (PGM 1e-2s → Retention 1e4s)



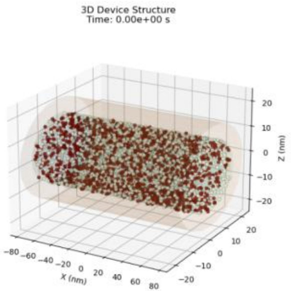


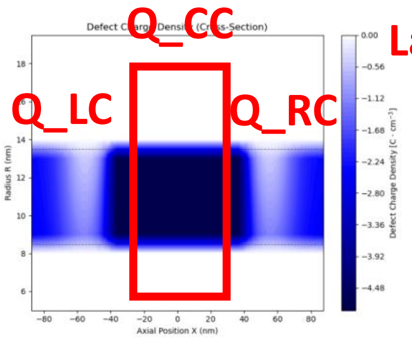
* Work based on IRPS 2019 (A. Padovani et al.) Understanding and Variability of Lateral Charge Migration in 3D CT-NAND Flash

LCM Modeling

$$Q = \int \rho_{def}(r,t)dr$$

- **Retention loss** is defined as **defect charge density**
  - Direct Retention prediction available using the defect charge density ratio
  - Will be defined as:
    - **Q_VCM = |Q_total(0) - Q_total(t_ret)|**
    - **Q_LCM = |Q_LC(t_ret)+Q_RC(t_ret)| - |Q_LC(0)+Q_RC(0)|**
  - **→ Minimize Q_Loss = α ∗|dQcc(t_ret)|+ β ∗ Q_LCM**

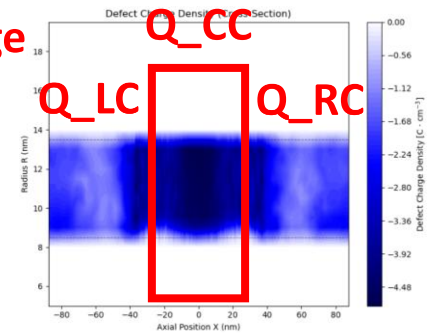




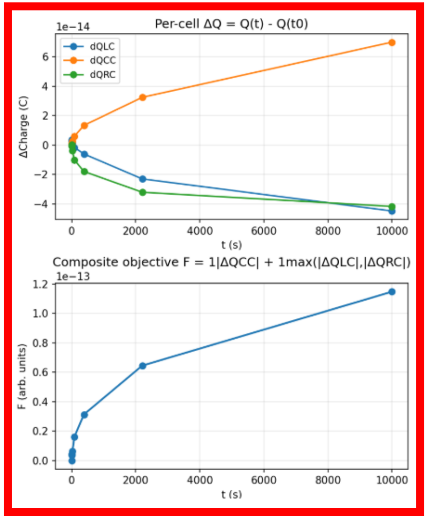
t=0

Lateral Change = LCM loss

Net Change = VCM loss



t=1e4s (=t_ret)



LCM Modeling

- **Data Synthesis Plan (5*3*3=45 sweeps, ~1.5hrs per each node)**
  - **Variables (according to IRPS 2019):**
    - **1. Tunnel layer Thickness**
      - t_TL = 2, 2.5, 3, 3.5, 4nm to → **Thick t_TL: LCM ratio (dQlcl/dQcc) increases**
    - **2. PGM voltage**
      - V_PGM = 10, 15, 20V → **High PGM: LCM dominant**
    - **3. Cell Spacing**
      - L_sp = 20, 25, 30nm → **Observe change in neighboring cells**
  - **→ Accelerated Design Space Exploration & Retention Loss Optimization**

Loss = $\alpha * |dQcc(t\_ret)| + \beta * Q\_LCM$
w.r.t. t_TL, V_pgm L_sp ?

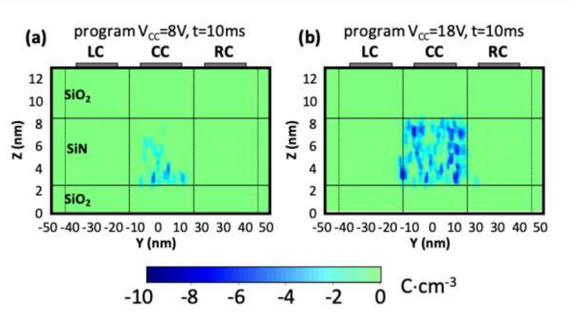


Fig. 8. Trapped charge distributions obtained from the simulation of a device with nominal stack after (a) 8V and (b) 18V program operation.

Thick t_TL suppresses VCM → LCM dominant