Application on the Semiconductor Devices and Deposition Method of ZrO_2

Semiconductor Processing Midterm Report

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1. Application of the ZrO_2 in the Semiconductor Device

1.1. High-K Dielectric

ZrO_2 is mostly used as the high-K dielectric in the semiconductor device as the gate oxide and the capacitor. We will first discuss the basics of high-K dielectrics to understand why we use the ZrO_2 as a high-K dielectric.

Modern CMOS performance improvement was mainly developed through physical scaling. As the size of the device was reduced as Moore's Law, which shows the development of semiconductor process technology, the scaling problem of dielectric material between the gate and the channel began to arise. As the size of the device decreased, the thickness of the dielectric decreased, and various corresponding side effects occurred. Engineers began to find ways to solve this problem.

The biggest problem during the gate oxide thickness scaling is the gate leakage current by gate tunneling. Before we scope on the dielectric material, let us discuss the equivalent oxide thickness (EOT), which is an indicator of the effective thickness of the oxide. Namely, it indicates the effective SiO_2 thickness required to produce the same effect when an oxide material is a High-K material.

$$EOT = t_{high-K}\frac{\varepsilon_{SiO2}}{\varepsilon_{high-K}}$$

For instance, to obtain the same effect of the 1nm of SiO_2 ($\varepsilon_{SiO2} = 3.9$), the ZrO_2, which is the most favorable high-k material ($\varepsilon_{ZrO2} = 22$), can have 5.6nm thickness. In that case, we can have the same capacitance with a thicker dielectric, hence reduce the leakage current.

Device scaling using SiO_2 is done by increasing gate capacitance by reducing the oxide thickness. However, the gate leakage problem emerged as the oxide thickness approaches to atomic-wise dimension. As a result, the thickness of the gate oxide needs to be increased again. However, if the thickness of SiO_2 is not reduced, the capacitance of the MOS-cap is reduced, thus the drain current is insufficient. Due to this trade-off, engineers investigated to maintain capacitance while reducing the thickness of the dielectric. In other words, they find a way to maintain EOT. As a result, instead of increasing the thickness by using other oxide materials, gate leakage can be reduced through a high-K material, hence the scaling can be done without performance degradation while maintaining the gate capacitance.

However, not all high-K materials are available for silicon-based semiconductor. For instance, Ta_2O_5(~22) and TiO_2(~100) react with the substrate, thus forms SiO_2 during annealing. Therefore, the barrier material should be inserted in the middle, i.e., cannot scale the EOT effectively. Also, the excessive-high-k dielectrics form interference on the channel region by the strong electric field, which induces the short channel effect. In contrast, Al_2O_3, HfO_2, ZrO_2 do not react with the substrate after annealing.

Material	Bandgap [eV]	Relative-K
SiO_2	9	3.9
Al_2O_3	8.8	9.5~12
ZrO_2	5.7	~25
HfO_2	5.6	~25
$ZrSiO_4$ (Zr-Silicate)	~6	10~22
$HfSiO_4$ (Hf-Silicate)	~6	~10

Table 1. List of the High-K material compared to SiO_2 [1]

As shown in Table 1, ZrO_2 and HfO_2 shows higher dielectric constant compared to Al_2O_3. ZrO_2 and HfO_2 show relatively high bandgap(~5.7eV), moderately high dielectric constant(k~25), and high thermo-dynamical stability. According to these properties, ZrO_2 and HfO_2 are both commonly used in the sub-70nm semiconductor process as the gate dielectric and the capacitor material.

Now, let us discuss the advantage of ZrO_2 compared to HfO_2. According to Kim [2], Those two materials show almost identical C-V characteristics, leakage, and other characteristics. The only and huge difference between the two materials is that the as-grown microstructures by the ALD process: polycrystalline and amorphous phases, respectively. The dielectric constants of the dielectrics depended significantly on the nature of phases; the dielectric constant of ZrO_2 was ~30, and that of HfO_2 was ~20, thus ZrO_2 shows a more superb dielectric constant. Fig. 1. shows the comparison of the characteristics between the ZrO_2 and HfO_2. However, these high-k films are not the predominant factor controlling the majority of important electrical properties, hence both are them are widely used in the semiconductor process.

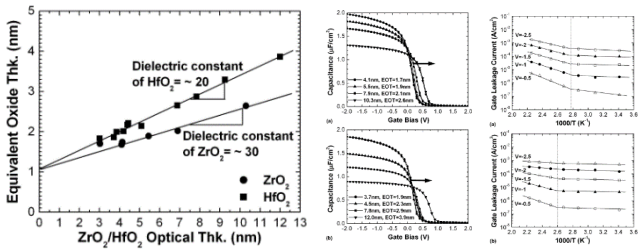


Figure 1. Characteristics comparison of ZrO_2 and HfO_2

1.2. Application on Memory Devices

High-K dielectric application is not the only application of ZrO_2. According to Panda [3], ZrO_2 is widely used in memory applications: volatile DRAM, nonvolatile flash memory, resistive switching memory (resistive-RAM, RRAM), and so on.

For instance, ZrO_2 dielectric material is used as a charge trapping layer due to the high permittivity in flash memory devices. As shown in Fig.2., A lower charge loss rate was observed for ZrO_2-based devices compared to SiO_2-based memory devices. For simplicity, the memory windows can be regarded as the trapping capability of material, i.e., data capability of the memory devices (y-axis), and Ge-NCs are the layer that contains ZrO_2 as a trapping layer [4].

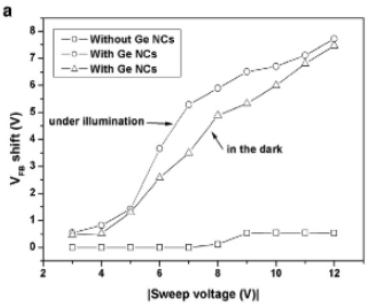


Figure 2. Memory windows obtained from MOS cap with and without Ge NCs

2. Deposition Method of ZrO_2

2.1. Basics of Deposition

Before we go through the deposition method, let us briefly explore the basics of deposition. So far, we have learned diffusion, ion implantation- doping the dopant to wafer and oxidation to form oxide in the lecture. However, with these methods, we cannot make gate dielectrics, barrier materials, and atomic-sized sophisticated oxides. In practice, many films, made of various materials are deposited during a standard CMOS process.

There are several requirements for deposition: desired composition, low contaminants, good electrical properties, uniform thickness across the wafer, and good step coverage. Each deposition method has its own advantages and shortages on these requirements.

Two main types of deposition methods have been developed and are used in CMOS technology: Chemical vapor deposition (CVD) and Physical vapor deposition (PVD)- thus ZrO_2 is also deposited by these methods. In recent days, atomic layer deposition (ALD) is used since the method offers novel thickness control, step coverage, and wafer uniformity. Recently, ALD processes are primarily used for ZrO_2 deposition. However, we will first scope on the CVD process since the process shows the basics of deposition.

2.2. CVD Process

Let us discuss the basic mechanism of the CVD process to understand the ZrO2 deposition. Several steps must occur in every CVD reaction cycle as shown in Fig. 3.

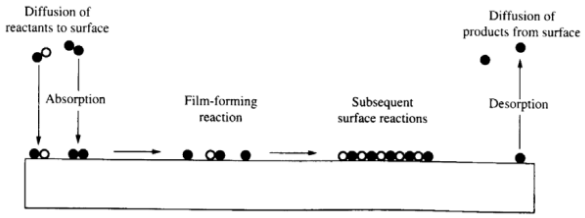


Figure 3. Steps of CVD process

In practical CVD, the chemical reactions leading to the formation of a solid material may take place not only on the wafer surface- heterogeneous reaction- but also in the gas phase- homogeneous reaction. Heterogeneous reactions are more desirable because the reactions occur selectively only on the heated surfaces and can produce the film with superb quality.

CVD can be classified by the condition of process type, such as pressure or the existence of plasma. For the ZrO_2 CVD, PECVD (Plasma enhanced CVD), LPCVD (Low-Pressure CVD) and RTCVD (Rapid thermal chemical CVD) are used. CVD process shows good interface quality and high throughput compared to another deposition method since the mass production is available. [5] However, we will not go into detail in the CVD process since the ALD process is more widely used in the state-of-the-art semiconductor process.

2.3. ALD Process

ALD process can be regarded as a special modification of CVD. Unlike CVD, the ALD process does not inject precursor and reactant gas at the same time. Ideal film uniformity is obtained by eliminating homogeneous reaction.

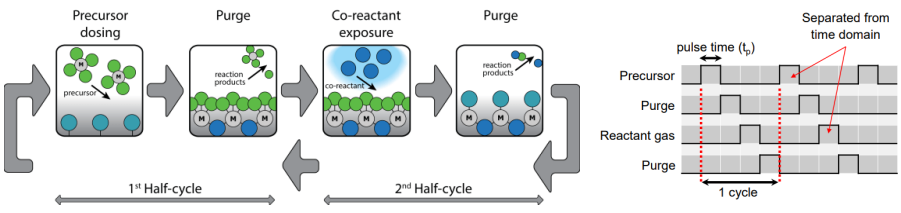
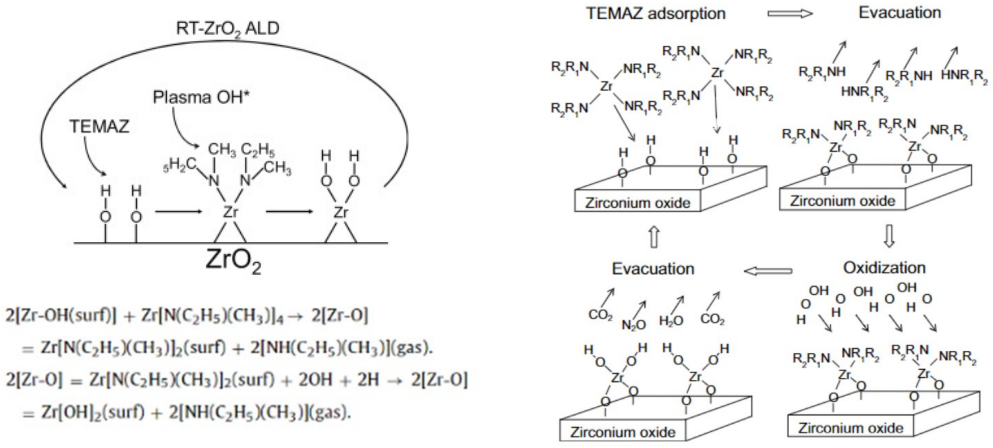


Figure 4. Steps and timing diagram of ALD process

As shown in Fig. 4., the typical ALD reaction sequence consists of four steps: Exposure of the precursor, unreacted precursor purge, i.e., evacuation of the reactor, exposure of the reactant gas, and then purge the residual gas, i.e., by-product purge. The bottom line of the process is that the precursor and the reactant material cannot react with each other since the reaction is fundamentally separated by time.

Now, let us substitute the ZrO_2 for the general case. The widely-used precursor in ZrO_2 ALD is the so-called TEMAZ (Tetrakis ethyl-methyl-amino Zirconium), which contains the ZrO_2 which would be deposited on the surface. The general reactant in ZrO_2 ALD is plasma hydrogen and hydroxide, which are produced from plasma-excited humidified atoms. [6]



$$2[Zr\text{-}OH(surf)] + Zr[N(C_2H_5)(CH_3)]_4 \rightarrow 2[Zr\text{-}O] = Zr[N(C_2H_5)(CH_3)]_2(surf) + 2[NH(C_2H_5)(CH_3)](gas).$$

$$2[Zr\text{-}O] = Zr[N(C_2H_5)(CH_3)]_2(surf) + 2OH + 2H \rightarrow 2[Zr\text{-}O] = Zr[OH]_2(surf) + 2[NH(C_2H_5)(CH_3)](gas).$$

Figure 5. ZrO_2 ALD reaction model and the chemical reaction formula

As shown in Fig.5., the TEMAZ precursors are injected first. Second, TEMAZ reacts with substrate reactive sites- -OH radicals. Third, excess TEMAZ and by-products are purged. Then, reactants are injected into TEMAZ covered surface. After that, TEMAZ and reactant gas react and form the by-products. Finally, the ZrO_2 atomic layer is deposited by the ALD process. With the repetitive process of the cycle, ZrO_2 film deposition can be done.

As we discussed before, ZrO_2 is usually utilized to form the high-K dielectric for the metal gate and capacitor oxide. As shown in Fig. 6., ALD offers excellent step coverage, wafer uniformity, and sophisticated thickness control. ALD is the sole process to ensure the perfect step coverage, which is necessary for modern semiconductor processing such as FinFET or nanowire.

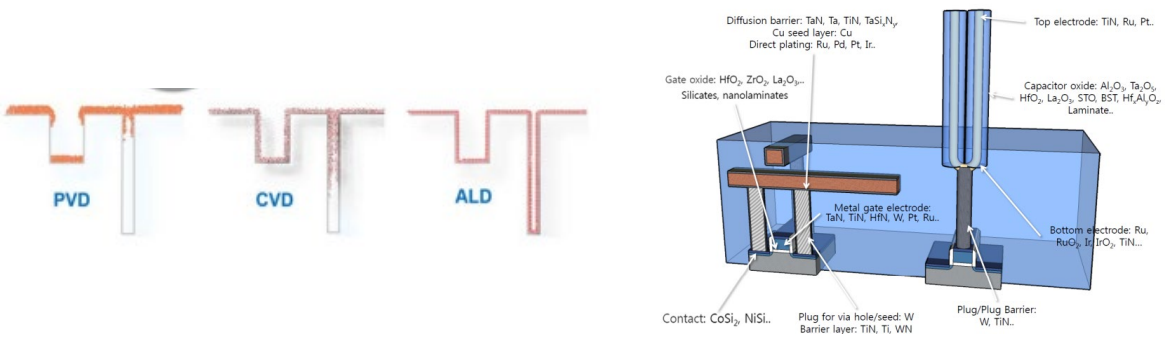


Figure 6. Step coverage and the application of ALD

2.4. PVD Process

The basic principle of PVD is that the physical vapors generated by various methods are deposited on the substrate. There are two types of PVD: Evaporation and sputtering. Since the sputtering process is widely used for the ZrO_2 PVD [7], we will go into detail in sputter deposition. The principle of sputter deposition is that the transfer of momentum from an incident projectile to a target resulting in the ejection of surface molecules. Sputtering is achieved by bombarding a target with energetic ions- Ar+ in general. Sputtering of ZrO_2 or ZrO_xN_y, i.e., dielectrics, requires RF power to supply energy to the bombarding atoms [8]. Due to the mobility difference between ion and electron, the plasma biased positively with respect to both electrodes, thus ensures sputtering.

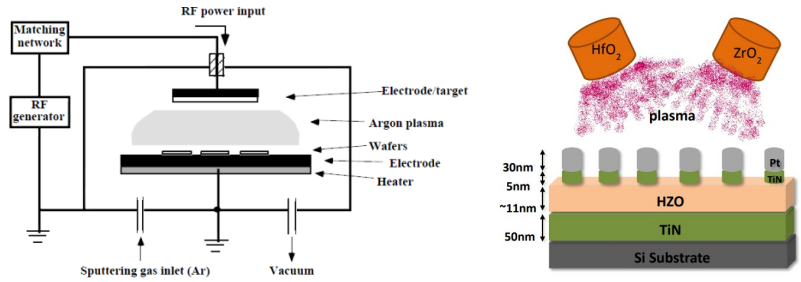


Figure 7. Schematics for the RF Sputtering of the ZrO_2

Now, we will discuss the advantage of the PVD process. The wafer electrode can be separately biased (RF), which allows cleaning or controlled sputtering of the wafer with Ar+ ions. This can allow more conformal deposition because the ions are highly directional and sputter selectively, i.e., a high aspect ratio could be achieved. The sputtering deposition also has an advantage on the low impurities and fast growth rate compared to the ALD process. Also, PVD is generally processed at room temperature, hence no restraint on the temperature, which has an advantage compared to the CVD process [8].

The deposition method is determined by the purpose of the deposition. For instance, if we want to deposit very accurately, we utilize the ALD process, and if we want to deposit in the room temperature due to the thermal limit such as the presence of the passivation materials, we utilize the PVD process.

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