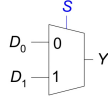


1 Multiplexers (Mux)

- 여러 개의 입력, 한 개의 출력
- select signal이 존재함
- 하나의 input을 골라 output에 연결



S	D ₁	D ₀	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

S	Y
0	D ₀
1	D ₁

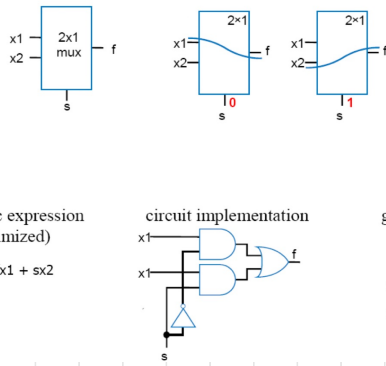
입력이 바뀌면 출력도 바뀜

전형적인 combinational logic

MUX	S	총 input 개수	⇒ 2 ⁿ + 1
2 : 1	1	2	
4 : 1	2	6	⇒ 2 ² : 1
8 : 1	3	11	

⇒ S도 input임을 기억하자!

definition example



s	x1	x2	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

logic expression (optimized)

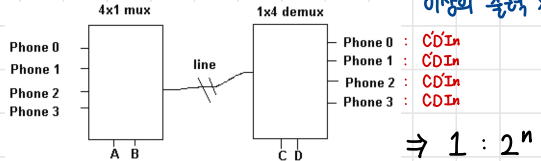
$$f = s'x1 + sx2$$

circuit implementation

graphical symbol

+ 2 DeMultiplexer (Demux)

- 한 개의 입력, 여러 개의 출력 → 동시에 그해 이상의 출력 x

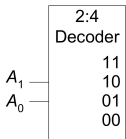


$$\Rightarrow 1 : 2^n$$

2. Decoders

- N개의 입력, 2^N개의 출력
- ↳ binary encoding이 되었음 → binary decoding
- ⇒ N : 2^N
- input output

- One-hot output의 형태



A ₁	A ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

+ 2 Encoders

- 2^N개의 입력, N개의 출력 ⇒ 2^N : N
- One-hot input의 형태

I0	I1	I2	I3	I4	I5	I6	I7	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

+ 2 Demux vs. Decoder

	Demultiplexer	Decoder
Definition	1 data input 2 ⁿ outputs	It has n inputs 2 ⁿ outputs It has n control inputs
Characteristic	Connects the data input to the data output	Selects one of the 2 ⁿ outputs by decoding the binary value on the basis of n inputs
Reverse of	Multiplexer	Encoder

1:2 Decoder:

$$\text{Out0} = S'$$

$$\text{Out1} = S$$

2:4 Decoder:

$$\text{Out0} = S1' \cdot S0'$$

$$\text{Out1} = S1' \cdot S0$$

$$\text{Out2} = S1 \cdot S0'$$

$$\text{Out3} = S1 \cdot S0$$

3:8 Decoder:

$$\text{Out0} = S2' \cdot S1' \cdot S0'$$

$$\text{Out1} = S2' \cdot S1' \cdot S0$$

$$\text{Out2} = S2' \cdot S1 \cdot S0'$$

$$\text{Out3} = S2' \cdot S1 \cdot S0$$

$$\text{Out4} = S2 \cdot S1' \cdot S0'$$

$$\text{Out5} = S2 \cdot S1' \cdot S0$$

$$\text{Out6} = S2 \cdot S1 \cdot S0'$$

$$\text{Out7} = S2 \cdot S1 \cdot S0$$