ASICS ws

Multi Protocol Audio Controller (MPAC) User Manual

Ver. 0.3

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Draft – Subject to change without notice !

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Change Log

Revision	Modifications
0.1 March 5, 2018	- Initial Draft
0.3 Marcg 17, 2018	- Updated doc

License

1. Introduction

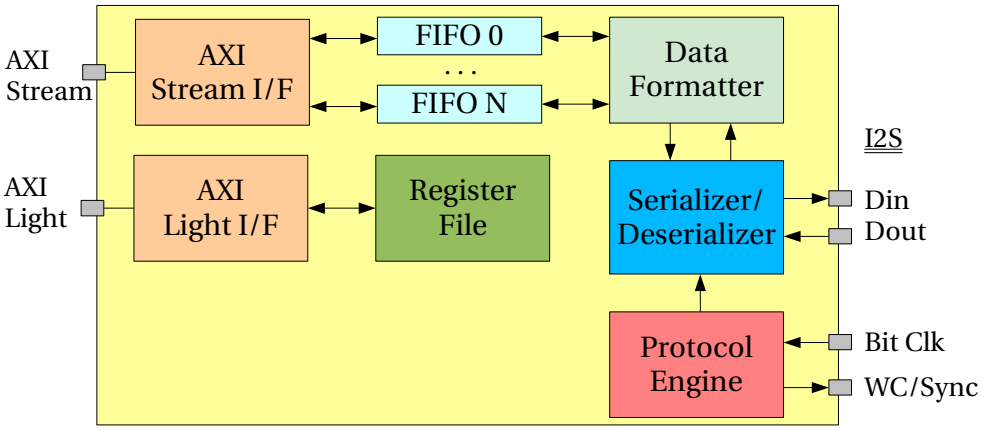
This IP Core provide a standard interface to external codecs and other audio devices.

It allows a internal controller to stream one or multiple audio channel from or to the controller with minimal CPU intervention.

Some of the main features are:

1. Multiple protocol support: I2S, TDM, AC97
2. 16, 18, 20, 24 and 32 bit Sample Size Support
3. up to 8 Output Channels
4. up to 8 input Channels
5. Configurable Internal buffers
6. External DMA Engine Support
7. AXI Light interface for registers
8. AXI Streaming interface for data

2. Architecture

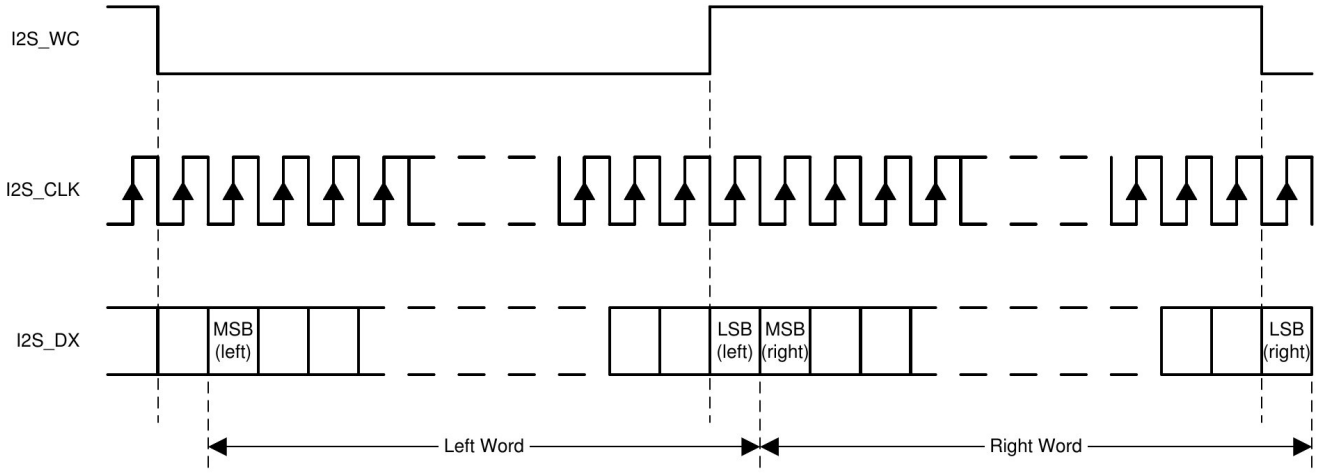


3. Protocols

The Audio Master Controller supports 3 main protocols: I2S, TDM and AC97.

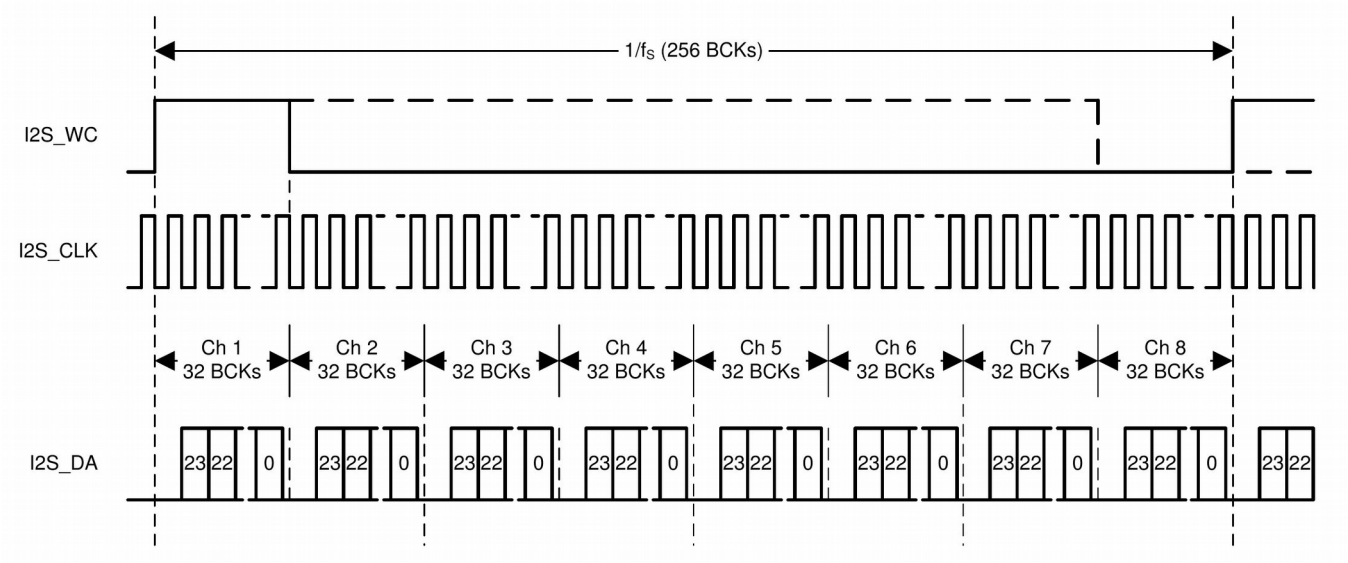
3.1. I2S protocol

The I2S mode is equivalent the TDM mode, except only two channels are used.. Typically the channels are Right & Left. I2S support a variety of sample sizes: 16, 18, 20, 24 and 32 bit.



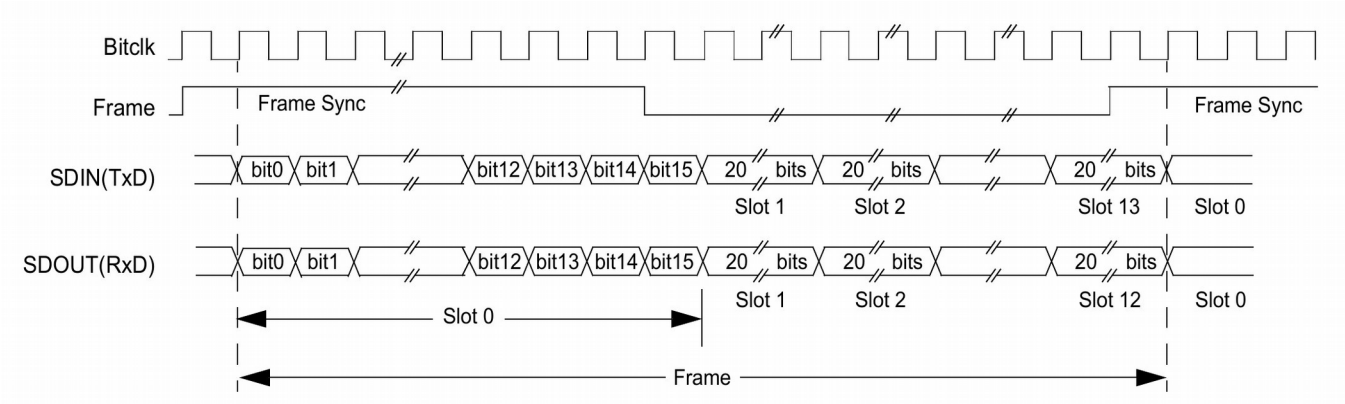
3.2. TDM Protocol

In the Time Division Mode (TDM), up to 16 input and output channels can be configured.



3.3. AC97 Protocol

In the AC97 mode, the standard AC97 channel layout and communication are supported.



4. Data Alignment and Packing

4.1. Data Alignment

All internal data of the MPAC is right (lsb) aligned. If the system however uses left (msb) aligned data, the ALIGN bit can be sat to change the alignment of the streams between the MPAC and the system.

4.1.1. Right Justified samples in a 32 bit frame (CFG.ALIGN = 0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
UNUSED (all zeros)																16 bit sample															
UNUSED (all zeros)																		18 bit sample													
UNUSED (all zeros)																				20 bit sample											
UNUSED (all zeros)																24 bit sample															
32 bit sample																															

4.1.2. Left Justified samples in a 32 bit frame (CFG.ALIGN = 1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16 bit sample																UNUSED (all zeros)															
18 bit sample																		UNUSED (all zeros)													
20 bit sample																				UNUSED (all zeros)											
24 bit sample																								UNUSED (all zeros)							
32 bit sample																															

4.2. Data Packing

The data stream between the MPAC and SoC is 32 bits wide. It can however hold sample in different packed modes.

4.2.1. Example 16 bit sample packing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Sample 1																Sample 0															
Sample 3																Sample 2															
Sample 5																Sample 4															

4.2.2. Example 18 bit sample packing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S1 [13:0]														S0																	
S3 [9:0]										S2																		S1 [17:14]			
S5 [5:0]								S4												S3 [17:10]											
S7 [1:0]	S6																			S5 [17:6]											
S8 [15:0]																S7 [17:2]															
S10 [11:0]												S9																	S8 [17:16]		
S12 [7:0]								S11														S10 [17:12]									
S14 [3:0]	S13																			S12 [17:8]											
S15																S14 [17:4]															

4.2.3. Example 20 bit sample packing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S1 [11:0]												S0																			
S3 [3:0]				S2																S1 [19:12]											
S4 [15:0]																S3 [19:4]															
S6 [7:0]								S5																				S4 [19:16]			
S7																				S6 [19:8]											

4.2.4. Example 24 bit sample packing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S1 [7:0]								S0																							
S2 [15:0]																S1 [23:8]															
S3																				S2 [23:16]											

5. Operation

5.1. Introduction

6. Core Registers

6.1. Register Address Map

All RESERVED and unspecified/missing bits should always be written with zero. Reading RESERVED and unspecified/missing bits will return undefined values. Software should follow this model to be compatible to future releases of this core.

Address Offset	Register Name	Description
0x00	CSR	Control and status register
0x04	VER	Version register
0x08	MUTE	Mute register
0x0C	MVAL	Mute Value
0x10	CFG	Configuration Register
0x14		RESERVED
0x18	IB_STAT	In buffer status
0x1c	OB_STAT	Out buffer status
0x20	BF_OVUN	Buffer overflow/underflow
0x24	BO_INT_EN	Buffer overflow/underflow interrupt enable
0x28	INT_MASK	Interrupt mask register
0x2c	INT_SRC	Interrupt source register
0x30		RESERVED
0x34	TIMER	Timer register
0x38		

6.2. Control and status register (CSR)

This register provides basic configuration and control.

Field	Bit(s)	Access	Description
SRST	31	WO	Soft Reset Writing a '1' to this bits resets the IP Core
RESERVED	30:16	RO	RESERVED
OCH_CNT	15:12	RW	Number of output channels to use (less one)
ICH_CNT	11:8	RW	Number of input channels to use (less one)
RESERVED	7:1	RO	RESERVED
ENABLE	0	RW	Enable IP Core

6.3. Version Register (VER)

This register holds the hardware revision number as well as various hardware configuration options.

Field	Bit(s)	Access	Description
RESERVED	31:25	RO	RESERVED
HAVE_TIMER	24	RO	Indicated whether the timer module is present or not
HW_OCH	23:20	RO	Number of max output channels supported by hardware, less one
HW_ICH	19:16	RO	Number of max input channels supported by hardware, less one
HW_FD	15:12	RO	Buffer FIFOs depth (for each channel)
VER	11:0	RO	Hardware revision MAJ[11:8].MIN[7:0]

6.4. Mute Register (MUTE)

This register the muting of channels.

Field	Bit(s)	Access	Description
RESERVED	31:24	RO	RESERVED
IMUTE	31:16	RW	Mute bits for input channels 15-0 A '1' will force the Mute Value to be written to the corresponding input channel
OMUTE	15:0	RW	Mute bits for output channels 15-0 A '1' will force the Mute Value to be written to the corresponding output channel

6.5. Mute Value Register (MVAL)

This register the muting of channels.

Field	Bit(s)	Access	Description
MAVL	31:0	RW	Mute Value

6.6. Configuration Register (CFG)

This register configures various internal parameters.

Field	Bit(s)	Access	Description
RESERVED	31:27	RO	RESERVED
PROT_SEL	26:24	RW	Protocol Select 0 – I2S/TDM 1 – AC97 2-7 – Reserved
RESERVED	31:24	RO	RESERVED

Field	Bit(s)	Access	Description
SYS_SS	20:18	RW	System Sample size 0 – 16 bit 1 – 18 bit 2 – 20 bit 3 – 24 bit 4 – 32 bit 5-7 – Reserved
ALIGN	17	RW	Sample alignment 0 – Left (LSB) 1 – Right (MSB)
PACKED	16	RW	Samples are packed 0 – One Sample per DW 1 – Samples are packed
RESERVED	15:11	RO	RESERVED
SL_WI	10:8	RW	Output slot width 0 – 16 bit 1 – 18 bit 2 – 20 bit 3 – 24 bit 4 – 32 bit 5-7 – Reserved
RESERVED	7:5	RO	RESERVED
SYNC_STAR	4:3	RW	Sync start 0 – Aligned with first data bit 1 – One cycle before first data bit
SYNC_WIDTH	2:1	RW	Sync duration 0 – Active one cycle at the beginning 1 – 50% duty cycle 2 – One cycle in-active at the end 3 - Reserved
SYNC_INV	0	RW	Invert Sync 0 – Not inverted (high-low) 1 – Inverted (low-high)

6.7. In buffer status (IB_STAT)

This register provide the fill status of the input buffers. Unused/not implemented buffers should be ignored.

The status encoding is:

Value	Description
0	0-25% empty
1	25-50% empty
2	50-75% empty
3	75-100% empty

Field	Bit(s)	Access	Description
ICH15_STAT	31:30	RO	In channel 15 status
ICH14_STAT	29:28	RO	In channel 14 status
ICH13_STAT	27:26	RO	In channel 13 status
ICH12_STAT	25:24	RO	In channel 12 status
ICH11_STAT	23:22	RO	In channel 11 status
ICH10_STAT	21:20	RO	In channel 10 status
ICH9_STAT	19:18	RO	In channel 9 status
ICH8_STAT	17:16	RO	In channel 8 status
ICH7_STAT	15:14	RO	In channel 7 status
ICH6_STAT	13:12	RO	In channel 6 status
ICH5_STAT	11:10	RO	In channel 5 status
ICH4_STAT	9:8	RO	In channel 4 status
ICH3_STAT	7:6	RO	In channel 3 status
ICH2_STAT	5:4	RO	In channel 2 status
ICH1_STAT	3:2	RO	In channel 1 status
ICH0_STAT	1:0	RO	In channel 0 status

6.8. Out buffer status (OB_STAT)

This register provide the fill status of the output buffers. Unused/not implemented buffers should be ignored.

The status encoding is:

Value	Description
0	0-25% full
1	25-50% full
2	50-75% full
3	75-100% full

Field	Bit(s)	Access	Description
OCH15_STAT	31:30	RO	Out channel 15 status
OCH14_STAT	29:28	RO	Out channel 14 status
OCH13_STAT	27:26	RO	Out channel 13 status
OCH12_STAT	25:24	RO	Out channel 12 status
OCH11_STAT	23:22	RO	Out channel 11 status
OCH10_STAT	21:20	RO	Out channel 10 status
OCH9_STAT	19:18	RO	Out channel 9 status
OCH8_STAT	17:16	RO	Out channel 8 status
OCH7_STAT	15:14	RO	Out channel 7 status
OCH6_STAT	13:12	RO	Out channel 6 status
OCH5_STAT	11:10	RO	Out channel 5 status
OCH4_STAT	9:8	RO	Out channel 4 status
OCH3_STAT	7:6	RO	Out channel 3 status
OCH2_STAT	5:4	RO	Out channel 2 status
OCH1_STAT	3:2	RO	Out channel 1 status
OCH0_STAT	1:0	RO	Out channel 0 status

6.9. Buffer overflow/underflow (BF_OVUN)

This register contains buffer overflow/underflow conditions.

Field	Bit(s)	Access	Description
IN_OVFL	31:16	RW	Indicates a overflow condition on the in channels. This occurs when the FIFOs are full while we try to latch a new sample from the I2S bus. Write a '1' to clear this condition.
OUT_UNFL	15:0	RW	Indicates a underflow condition on the in channels. This occurs when the FIFOs are empty while we try to latch a new sample to the I2S bus serializer. Write a '1' to clear this condition.

6.10. Buffer overflow/underflow Interrupt Enable (BO_INT_EN)

This register contains buffer overflow/underflow interrupt enables.

Field	Bit(s)	Access	Description
IN_OVFL_IE	31:16	RW	Interrupt Enable for input channel overflow conditions. Each bit corresponds to a channel.
OUT_UNFL_IE	15:0	RW	Interrupt Enable for output channel underflow conditions. Each bit corresponds to a channel.

6.11. Interrupt mask (INT_MASK)

This register contains buffer overflow/underflow conditions.

Field	Bit(s)	Access	Description
RESERVED	31:10	RO	RESERVED
IN_OFL_INT	9	RO	In buffer overflow interrupt enable
OUT_UFL_INT	8	RO	Out buffer underflow interrupt enable
RESERVED	7:1	RO	RESERVED
TIMER_INT	0	RW	Timer Interrupt enable

6.12. Interrupt source (INT_SRC)

This register contains buffer overflow/underflow conditions.

Field	Bit(s)	Access	Description
RESERVED	31:10	RO	RESERVED
IN_OFL_INT	9	RO	In buffer overflow interrupt occurred
OUT_UFL_INT	8	RO	Out buffer underflow interrupt occurred
RESERVED	7:1	RO	RESERVED
TIMER_INT	0	RW	Timer Interrupt occurred

6.13. Timer Register (TIMER)

The Timer register provides a basic timer implementation. It allows for generation of .

Bit #	Access	Description
31:0	R	Current Timer Value
31	W	Enable Interrupt
29:28	W	Pre-scalar 00 – Timer runs of System Clock (divided by 1) 01 – Timer runs of System Clock divided by 2 10 – Timer runs of System Clock divided by 4 11 – Timer runs of System Clock divided by 8
27:0	W	Timer Interrupt Value

7. Core Parameters

When instantiating this IP Core, it is important to set the configuration parameters to appropriate values.

7.1. NO_IN_CH

This parameter specifies the maximum number of input channels the hardware can support. Actual number that is used is set in the configuration register. Valid values are 1-16.

7.2. NO_IN_CH

This parameter specifies the maximum number of output channels the hardware can support. Actual number that is used is set in the configuration register. Valid values are 1-16.

7.3. MAX_FIFO_DEPTH

This parameter specifies the maximum FIFO buffer depth (for each channel) as log2. The size specifies the number of DW entries in the buffer. Afor example, a value of 6, sets the FIFO depth to 64 (2^6) DW, or 256 bytes, There is no hardware limitation to the FIFO buffer size.

The FIFO buffer size should be chosen carefully, considering the highest audio sample rate and the frequency of interrupt to re-fill the buffers.

8. Core IOs

This IP Core offers the choice of native WISHBONE or native AXI Light SoC interfaces. The PHY and GPIO interfaces remain unchanged regardless of the SoC interface.

All signals are active high unless noted otherwise. The 'Dir' column illustrates the direction of the signals. 'I' indicates an input to the IP Core, 'O' indicates an output from the IP Core.

8.1. General System Inputs

Name	Width	Dir.	Description
clock_i	1	I	main core clock
reset_i	1	I	system reset

8.2. AXI Interconnect Signals

The AXI interface is compliant to the AXI Lite 4.0 Interface Specification. All AXI Interfaces run at the SoC clock (clock_i) and use SoC reset (reset_i).

8.2.1. AXI Lite Register File Interface

This interface is used to access the register file.

Name	Width	Dir.	Description
AXI Light Write Channel			
axl_awaddr_i	32	I	Master Write address (byte address)
axl_awprot_i	3	I	Master Protection type
axl_awvalid_i	1	I	Master Write address valid
axl_awready_o	1	O	Slave Write address ready
axl_wdata_i	32	I	Master Write data
axl_wstrb_i	4	I	Master Write strobes
axl_wvalid_i	1	I	Master Write valid

Name	Width	Dir.	Description
axl_wready_o	1	O	Slave Write ready
axl_bresp_o	2	O	Slave Write response
axl_bvalid_o	1	O	Slave Write response valid
axl_bready_i	1	I	Master Response ready
AXI Light Read Channel			
axl_araddr_i	32	I	Master Read address (byte address)
axl_arprot_i	3	I	Master Protection type
axl_arvalid_i	1	I	Master Read address valid
axl_arready_o	1	O	Slave Read address ready
axl_rdata_o	32	O	Slave Read data
axl_rresp_o	2	O	Slave Read response
axl_rvalid_o	1	O	Slave Read valid
axl_rready_i	1	I	Master Read ready

8.2.2. AXI Light Streaming Interface

This Interface is used for high speed data transfer, from and to the internal data FIFOs.

Name	Width	Dir.	Description
AXI Stream Transmit Data Channel			
axs_tx_tid_i	4	I	Transmit data channel ID
axs_tx_tvalid_o	1	O	Transmit data channel valid
axs_tx_tready_i	1	I	Transmit data channel ready
axs_tx_tlast_o	1	O	Transmit data channel last word
axs_tx_tdata_o	32	O	Transmit data channel data
AXI Stream Receive Data Channel			
axs_rx_tid_i	4	I	Receive data channel ID
axs_rx_tvalid_i	1	I	Receive data channel valid
axs_rx_tready_o	1	O	Receive data channel ready
axs_rx_tlast_i	1	I	Receive data channel last word
axs_rx_tdata_i	32	I	Receive data channel data

8.3. I2S Interface

This Interface is used for connection to an external Codec.

Name	Width	Dir.	Description
i2s_clk	1	I/O TBD	Bit Clock
i2s_wc	1	O	Word/Frame/LR/Sync Clock
i2s_di	1	I	Serial Data Input
i2s_do	1	O	Serial Data Output

Appendix A: Sample Rates

This table illustrates some of the possible sampling rates and associated timings.

Sample Rate (kHz)	Sample Size (bits)	Channels	I2S Clock (MHz)	Bandwidth MB/s	Bandwidth Packed
32	16	2	1.024	0.128	0.064
44.1	16	2	1.4112	0.176	0.088
48	16	2	1.536	0.192	0.096
96	16	2	3.072	0.384	0.192
192	16	2	6.144	0.768	0.384
32	18	2	1.152	0.144	0.081
44.1	18	2	1.5876	0.198	0.112
48	18	2	1.728	0.216	0.122
96	18	2	3.456	0.432	0.243
192	18	2	6.912	0.864	0.486
32	20	2	1.28	0.160	0.100
44.1	20	2	1.764	0.221	0.138
48	20	2	1.92	0.240	0.150
96	20	2	3.84	0.480	0.300
192	20	2	7.68	0.960	0.600
32	24	2	1.536	0.192	0.144
44.1	24	2	2.1168	0.265	0.198
48	24	2	2.304	0.288	0.216
96	24	2	4.608	0.576	0.432
192	24	2	9.216	1.152	0.864
32	32	2	2.048	0.256	0.256
44.1	32	2	2.8224	0.353	0.353
48	32	2	3.072	0.384	0.384
96	32	2	6.144	0.768	0.768
192	32	2	12.288	1.536	1.536
32	16	4	2.048	0.256	0.128
44.1	16	4	2.8224	0.353	0.176
48	16	4	3.072	0.384	0.192
96	16	4	6.144	0.768	0.384
192	16	4	12.288	1.536	0.768
32	18	4	2.304	0.288	0.162
44.1	18	4	3.1752	0.397	0.223
48	18	4	3.456	0.432	0.243
96	18	4	6.912	0.864	0.486
192	18	4	13.824	1.728	0.972

Sample Rate (kHz)	Sample Size (bits)	Channels	I2S Clock (MHz)	Bandwidth MB/s	Bandwidth Packed
32	20	4	2.56	0.320	0.200
44.1	20	4	3.528	0.441	0.276
48	20	4	3.84	0.480	0.300
96	20	4	7.68	0.960	0.600
192	20	4	15.36	1.920	1.200
32	24	4	3.072	0.384	0.288
44.1	24	4	4.2336	0.529	0.397
48	24	4	4.608	0.576	0.432
96	24	4	9.216	1.152	0.864
192	24	4	18.432	2.304	1.728
32	32	4	4.096	0.512	0.512
44.1	32	4	5.6448	0.706	0.706
48	32	4	6.144	0.768	0.768
96	32	4	12.288	1.536	1.536
192	32	4	24.576	3.072	3.072
32	16	8	4.096	0.512	0.256
44.1	16	8	5.6448	0.706	0.353
48	16	8	6.144	0.768	0.384
96	16	8	12.288	1.536	0.768
192	16	8	24.576	3.072	1.536
32	18	8	4.608	0.576	0.324
44.1	18	8	6.3504	0.794	0.447
48	18	8	6.912	0.864	0.486
96	18	8	13.824	1.728	0.972
192	18	8	27.648	3.456	1.944
32	20	8	5.12	0.640	0.400
44.1	20	8	7.056	0.882	0.551
48	20	8	7.68	0.960	0.600
96	20	8	15.36	1.920	1.200
192	20	8	30.72	3.840	2.400
32	24	8	6.144	0.768	0.576
44.1	24	8	8.4672	1.058	0.794
48	24	8	9.216	1.152	0.864
96	24	8	18.432	2.304	1.728
192	24	8	36.864	4.608	3.456

Sample Rate (kHz)	Sample Size (bits)	Channels	I2S Clock (MHz)	Bandwidth MB/s	Bandwidth Packed
32	32	8	8.192	1.024	1.024
44.1	32	8	11.2896	1.411	1.411
48	32	8	12.288	1.536	1.536
96	32	8	24.576	3.072	3.072
192	32	8	49.152	6.144	6.144