1. Description

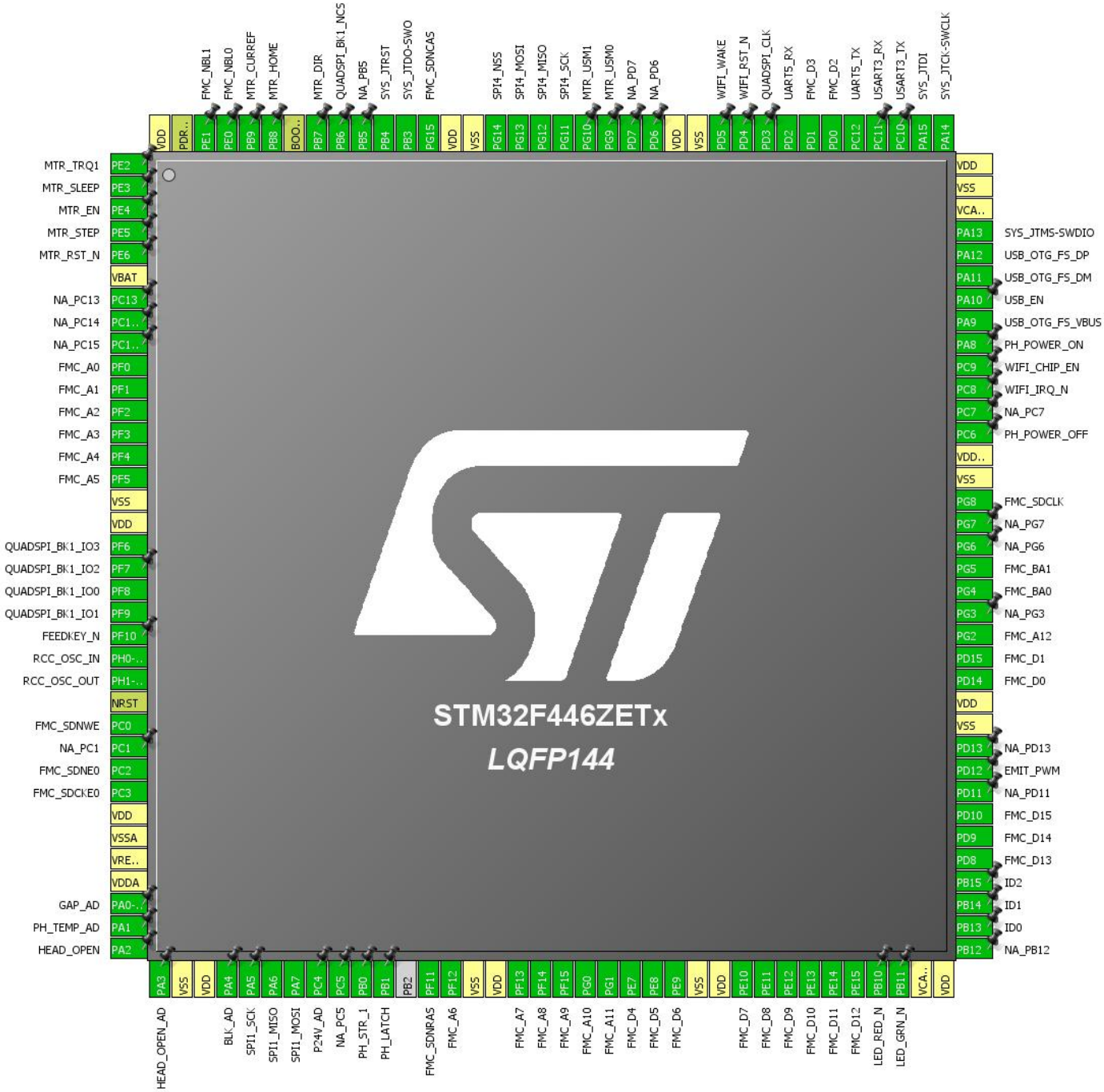
1.1. Project

Project Name	PRE_ALPHA_EVT
Board Name	PRE_ALPHA_EVT
Generated with:	STM32CubeMX 4.23.0
Date	10/27/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	MTR_TRQ1
2	PE3 *	I/O	GPIO_Output	MTR_SLEEP
3	PE4 *	I/O	GPIO_Output	MTR_EN
4	PE5 *	I/O	GPIO_Output	MTR_STEP
5	PE6 *	I/O	GPIO_Output	MTR_RST_N
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	NA_PC13
8	PC14-OSC32_IN *	I/O	GPIO_Input	NA_PC14
9	PC15-OSC32_OUT *	I/O	GPIO_Input	NA_PC15
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
19	PF7	I/O	QUADSPI_BK1_IO2	
20	PF8	I/O	QUADSPI_BK1_IO0	
21	PF9	I/O	QUADSPI_BK1_IO1	
22	PF10 *	I/O	GPIO_Input	FEEDKEY_N
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1 *	I/O	GPIO_Input	NA_PC1
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	ADC1_IN0	GAP_AD
35	PA1	I/O	ADC1_IN1	PH_TEMP_AD
36	PA2 *	I/O	GPIO_Input	HEAD_OPEN

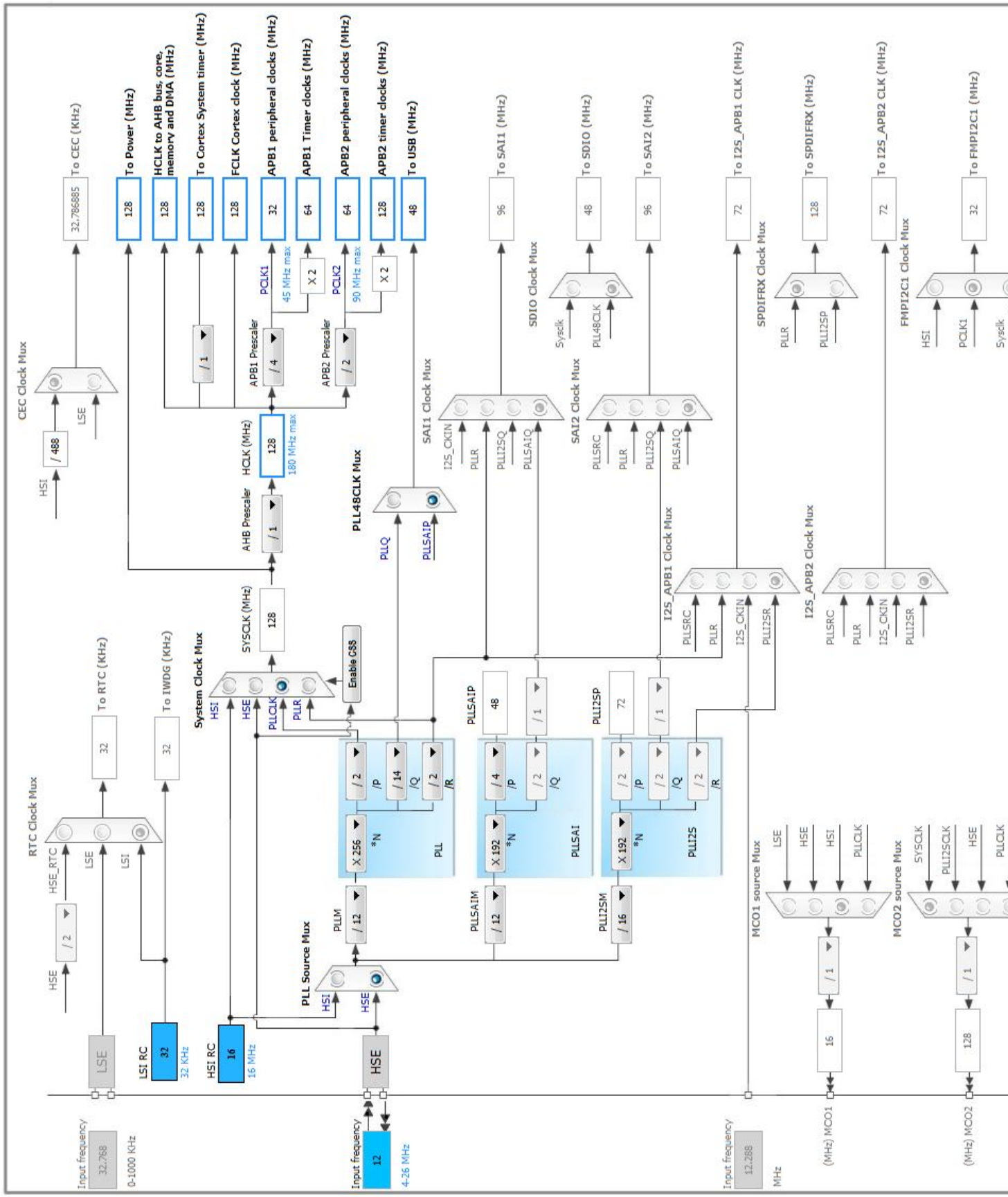
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PA3	I/O	ADC1_IN3	HEAD_OPEN_AD
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN4	BLK_AD
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
44	PC4	I/O	ADC1_IN14	P24V_AD
45	PC5 *	I/O	GPIO_Input	NA_PC5
46	PB0 *	I/O	GPIO_Output	PH_STR_1
47	PB1 *	I/O	GPIO_Output	PH_LATCH
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10 *	I/O	GPIO_Output	LED_RED_N
70	PB11 *	I/O	GPIO_Output	LED_GRN_N
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Input	NA_PB12
74	PB13 *	I/O	GPIO_Input	ID0
75	PB14 *	I/O	GPIO_Input	ID1
76	PB15 *	I/O	GPIO_Input	ID2

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11 *	I/O	GPIO_Input	NA_PD11
81	PD12	I/O	TIM4_CH1	EMIT_PWM
82	PD13 *	I/O	GPIO_Input	NA_PD13
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
88	PG3 *	I/O	GPIO_Input	NA_PG3
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6 *	I/O	GPIO_Input	NA_PG6
92	PG7 *	I/O	GPIO_Input	NA_PG7
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6 *	I/O	GPIO_Output	PH_POWER_OFF
97	PC7 *	I/O	GPIO_Input	NA_PC7
98	PC8	I/O	GPIO_EXTI8	WIFI_IRQ_N
99	PC9 *	I/O	GPIO_Output	WIFI_CHIP_EN
100	PA8 *	I/O	GPIO_Output	PH_POWER_ON
101	PA9	I/O	USB_OTG_FS_VBUS	
102	PA10 *	I/O	GPIO_Output	USB_EN
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15	I/O	SYS_JTDI	
111	PC10	I/O	USART3_TX	
112	PC11	I/O	USART3_RX	
113	PC12	I/O	UART5_TX	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
116	PD2	I/O	UART5_RX	
117	PD3	I/O	QUADSPI_CLK	
118	PD4 *	I/O	GPIO_Output	WIFI_RST_N
119	PD5 *	I/O	GPIO_Output	WIFI_WAKE
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Input	NA_PD6
123	PD7 *	I/O	GPIO_Input	NA_PD7
124	PG9 *	I/O	GPIO_Output	MTR_USM0
125	PG10 *	I/O	GPIO_Output	MTR_USM1
126	PG11	I/O	SPI4_SCK	
127	PG12	I/O	SPI4_MISO	
128	PG13	I/O	SPI4_MOSI	
129	PG14	I/O	SPI4_NSS	
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
133	PB3	I/O	SYS_JTDO-SWO	
134	PB4	I/O	SYS_JTRST	
135	PB5 *	I/O	GPIO_Input	NA_PB5
136	PB6	I/O	QUADSPI_BK1_NCS	
137	PB7 *	I/O	GPIO_Output	MTR_DIR
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	MTR_HOME
140	PB9	I/O	TIM4_CH4	MTR_CURREF
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

mode: IN3

mode: IN4

mode: IN14

mode: Temperature Sensor Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	PCLK2 divided by 2
Resolution	**10 bits (13 ADC Clock cycles) ***
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***
ADC_Regular_ConversionMode:	
Number Of Conversion	**6 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**144 Cycles ***
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**144 Cycles ***
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**144 Cycles ***

Rank	**4 ***
Channel	**Channel 14 ***
Sampling Time	**144 Cycles ***
Rank	**5 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**480 Cycles ***
Rank	**6 ***
Channel	**Channel 4 ***
Sampling Time	**144 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. CRC

mode: Activated

5.3. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0
Internal bank number: 4 banks
Address: 13 bits
Data: 16 bits
Byte enable: set

5.3.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	13 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**5 ***
Self-refresh time	**3 ***
SDRAM common row cycle delay	**4 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**1 ***
Row to column delay	**1 ***

5.4. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

5.4.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 2
Power Over Drive	Disabled

5.6. SPI1

Mode: Full-Duplex Master

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.7. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.8. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

5.9. TIM2

Clock Source : Internal Clock

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**32 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.10. TIM3

Clock Source : Internal Clock

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**32 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**2000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.11. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel4: PWM Generation CH4

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**200 ***
Internal Clock Division (CKD)	**Division by 4 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.12. TIM5

mode: Clock Source

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**32 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**200 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. UART5

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.14. USART3

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.15. USB_OTG_FS

Mode: Device_Only

mode: Activate_VBUS

5.15.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

5.16. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.16.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	**256 ***
USB CDC Tx Buffer Size	**256 ***

5.16.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	GAP_AD
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	PH_TEMP_AD
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	HEAD_OPEN_AD
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	BLK_AD
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	P24V_AD
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
QUADSPI	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PD3	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
SPI4	PG11	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PG12	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PG13	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG14	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4	SYS_JTRST	n/a	n/a	n/a	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	**Pull-up ***	Low	EMIT_PWM
	PB9	TIM4_CH4	Alternate Function Push Pull	**Pull-up ***	Low	MTR_CURREF
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PC10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PC11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_TRQ1
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_SLEEP
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_EN
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_STEP
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_RST_N
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC13
	PC14-OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC14
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC15
	PF10	GPIO_Input	Input mode	**Pull-up ***	n/a	FEEDKEY_N
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC1
	PA2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HEAD_OPEN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC5
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PH_STR_1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PH_LATCH
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED_N
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GRN_N
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PB12
	PB13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID0
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID1
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID2
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PD11
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PD13
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PG3
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PG6
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PG7
	PC6	GPIO_Output	Output Push Pull	**Pull-up ***	Low	PH_POWER_OFF
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PC7
	PC8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	WIFI_IRQ_N
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_CHIP_EN
	PA8	GPIO_Output	Output Push Pull	**Pull-up ***	Low	PH_POWER_ON
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_EN
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_RST_N
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_WAKE
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PD6
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PD7
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_USM0
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_USM1
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NA_PB5
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_DIR
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MTR_HOME

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA2_Stream3	Memory To Peripheral	**High ***
ADC1	DMA2_Stream4	Peripheral To Memory	**Very High ***
MEMTOMEM	DMA2_Stream2	Memory To Memory	**Medium ***
SPI4_TX	DMA2_Stream1	Memory To Peripheral	Low
SPI4_RX	DMA2_Stream0	Peripheral To Memory	Low

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

MEMTOMEM: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	**Word ***
Dst Memormy Data Width:	**Word ***
Src Memory Burst Size:	Single

Dst Memormy Burst Size:	Single

SPI4_TX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	1	0
ADC1, ADC2 and ADC3 interrupts	true	2	0
TIM2 global interrupt	true	4	0
TIM3 global interrupt	true	4	0
DMA2 stream0 global interrupt	true	4	0
DMA2 stream1 global interrupt	true	4	0
DMA2 stream3 global interrupt	true	4	0
DMA2 stream4 global interrupt	true	4	0
USB On The Go FS global interrupt	true	3	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
FMC global interrupt	unused		
TIM5 global interrupt	unused		
UART5 global interrupt	unused		
DMA2 stream2 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
QUADSPI global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446ZETx
Datasheet	027107_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	PRE_ALPHA_EVT
Project Folder	C:\temp\STM32F446ZE\FORD_PROTO_B\PRE_ALPHA_EVT
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.17.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No