Report from Lab 5

Data path unit

I declare that this piece of work, which is the basis for recognition of achieving learning outcomes in the Digital Circuits course, was completed on my own.

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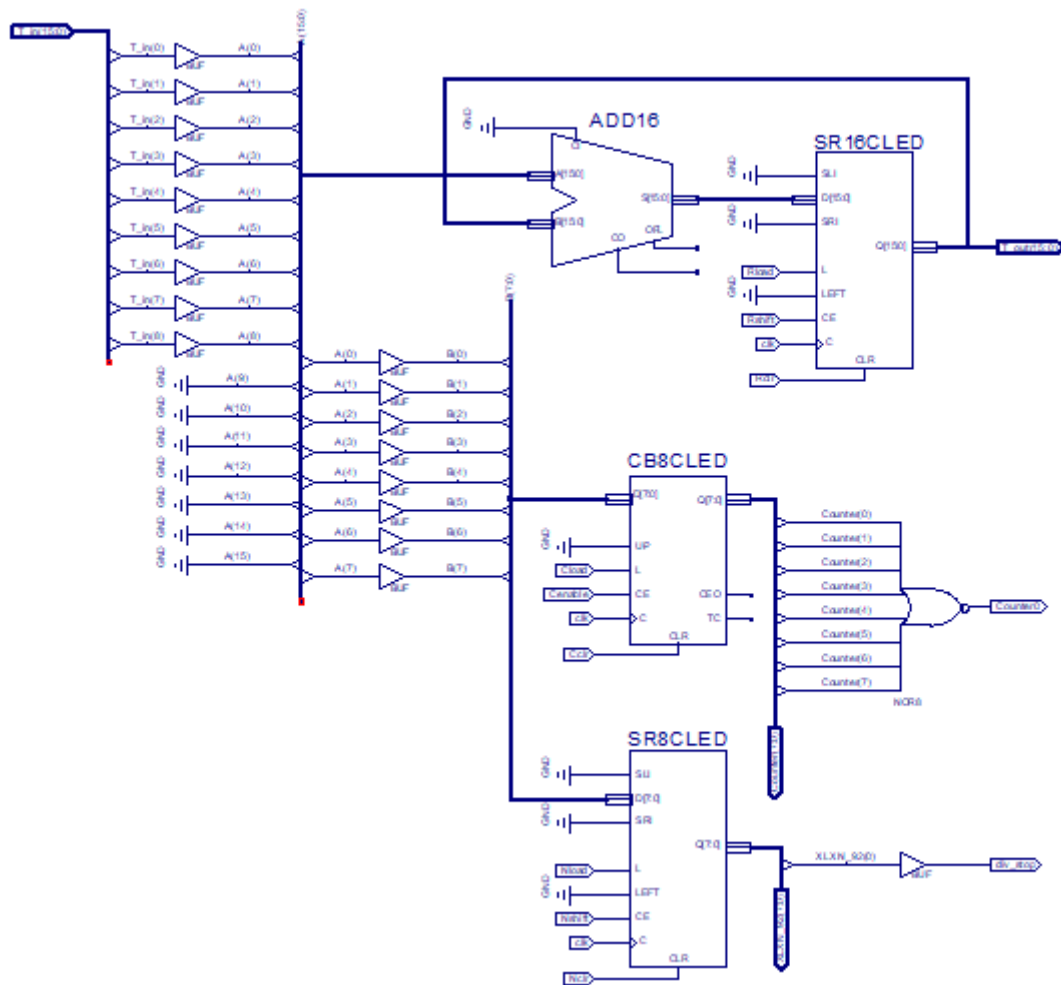Date: 21.05.2021

Theoretical design

Our task was to create schematic for data path unit that calculates the average number:

$$Y = Int\left[\sum_{i=1}^{n} x_i / n\right]$$

There isn't much in terms of theoretical design so I just went to creating a schematic in Xilinix.

Xilinix schematics and test results

Schematic can be seen on the next page:

From T_in(15:0) we take first 9 bits as k assigned to my group was 9. From those 9 bits, I have transferred 8 to the counter and bottom register for the first clock cycle, because during that cycle through input comes n. After that, we no longer load counter and bottom register and start loading adder and, in result, top register. They are loaded with 9 lowest bits from input and rest is filled with 0. Addition takes place until counter reaches 0. Then bottom register starts shifting together with the top register until lowest bit of the bottom register is equal to 1. After that, we have our result ready.

Simulation is on the next page, split into two parts so that binary numbers are visible:
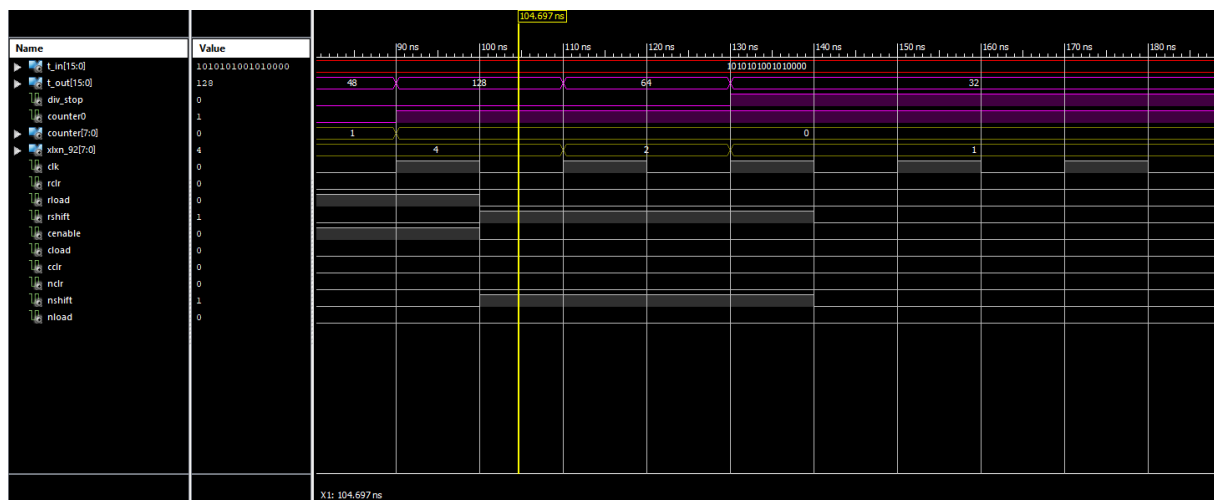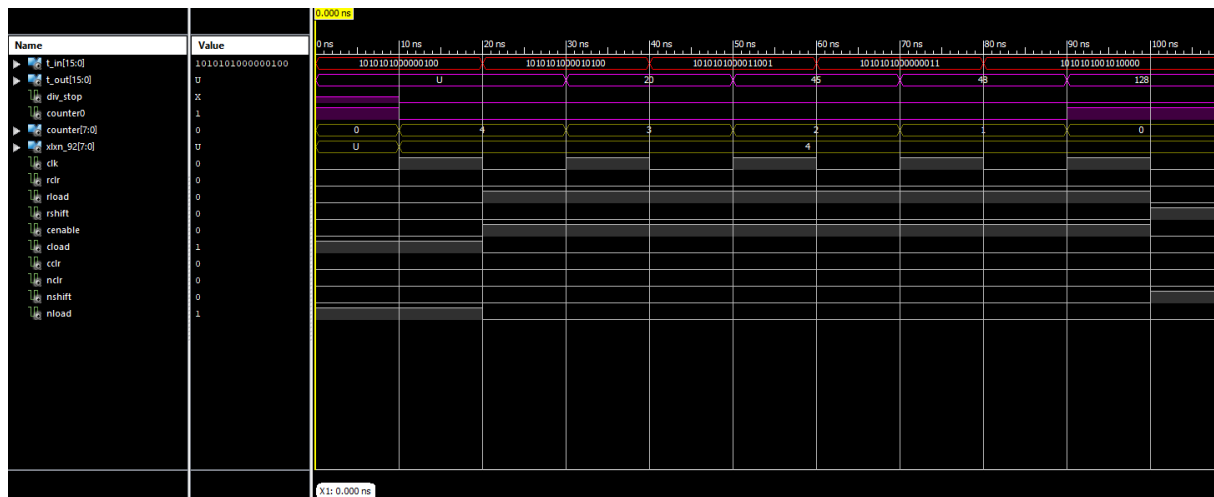
Numbers in the input, if we take into consideration only the first 9 bits are in order:
20, 25, 3, 80

Troubleshooting

I had an issue with div_stop not showing correct result so I have added a new output XLXN_92 that shows the number on the bottom register to find the mistake and I have managed to do so, the problem came out to be insignificant and I no longer remember what was wrong.

Conclusions

Overall, the experiment succeeded. I have managed to finish the task rather quickly and without major issues.