CMOS 300 MSPS正交

完整DDS

**AD9854**

**特征**

300 MHz内部时钟速率

FSK、BPSK、PSK、chirp、AM操作

双集成12位数模转换器，超高速比较器，3 ps均方根抖动

优良的动态性能

80 dB SFDR，100 MHz(±1 MHz）AOUT

4？至20？可编程基准时钟乘法器，双48位可编程频率寄存器，双14位可编程相位偏移寄存器，12位可编程幅度调制和

开/关输出形状键控功能，单脚FSK和BPSK数据接口，PSK能力通过输入/输出接口

具有单引脚频率保持功能的线性或非线性调频啁啾函数

频移FSK

时钟发生器模式下总抖动<25 ps rms

自动双向扫频Sin(x)/x校正

简化控制界面

10 MHz串行2线或3线SPI兼容100 MHz并行8位编程

3.3V单电源

多种掉电功能

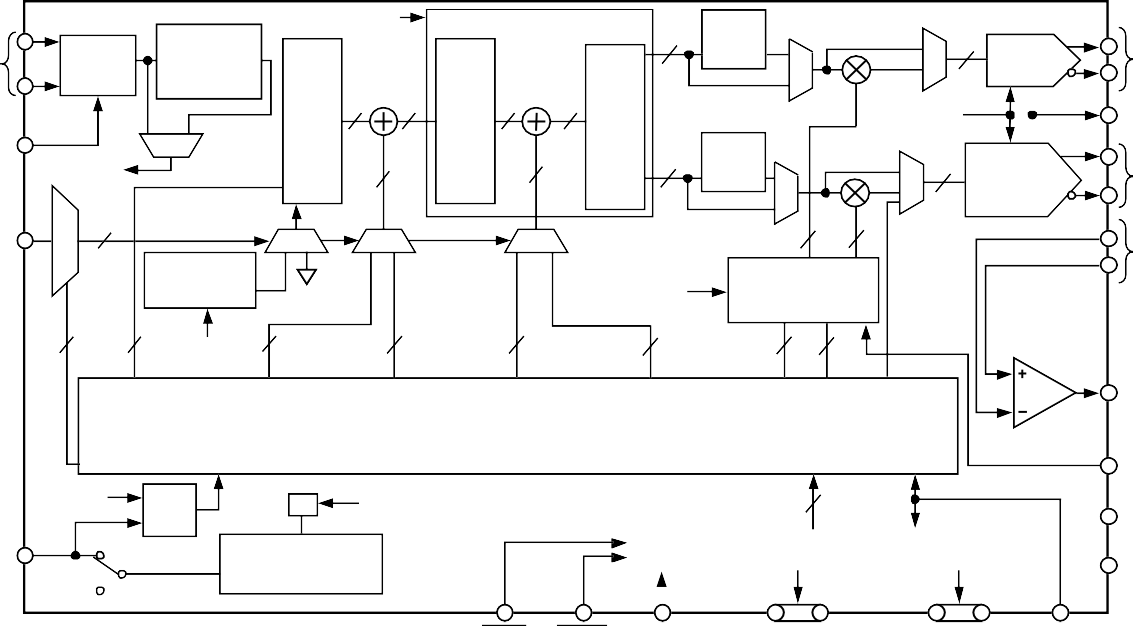
单端或差分输入基准时钟小，80引脚LQFP或TQFP，焊盘裸露

**应用程序**

敏捷的正交LO频率合成可编程时钟发生器

雷达和扫描系统测试和测量设备用调频啁啾源

商用和业余射频激励器

**功能框图**

**三角洲 频率 字词**

**频率 调谐 字词 1**

**频率 第一个14位 第二14位 I和Q 12位 12位 DC 调谐 相位/偏移 相位/偏移 我 调制 控制**

**字词 2**

**字词**

**字词**

**模式 选择**

**程序设计 寄存器**

参考时钟输入

参考CLK缓冲器

4×至20×REF CLK乘法器

系统时钟

DDS内核

**相位 累加器 行政协调会 2**

**INV**

12sinc

IFilter

**数字乘法器**

12

**频率 累加器 行政协调会 1**

**多路复用**

**多路复用**

12位I

**DAC**

模拟输出

**差异/单**

**选择**

**系统**

**多路复用**

4848

1717

INV

**相到- 振幅 变换器**

12sinc

系统时钟

12

**多路复用**

**多路复用**

**12位**

DAC R

**设置**

**FSK/BPSK/保持**

中的数据

钟表

3

**解复用**

**多路复用**

4814

MUXMUX

过滤器

**Q**

**12**

**12**

Q DAC或控制DAC

**ANALOG OUT**

**ANALOG**

**DELTA FREQUENCY RATE TIMER**

**SYSTEM CLOCK**

**IN**

**PROGRAMMABLE AMPLITUDE AND RATE CONTROL**

**COMPARATOR**

**2 48**

**SYSTEM CLOCK**

**48 48 14 14**

**12 12**

**CLOCK OUT**

**BIDIRECTIONAL**

**SYSTEM**

**CLOCK CK Q**

**D**

**INT**

**÷2**

**INTERNAL**

**SYSTEM CLOCK**

**AD9854**

**BUS**

**I/O PORT BUFFERS**

**OSK**

**GND**

**INTERNAL/EXTERNAL I/O UPDATE CLOCK**

**EXT**

**PROGRAMMABLE UPDATE CLOCK**

**+VS**

**READ WRITE SERIAL/**

**PARALLEL SELECT**

*Figure 1.*

**6-BIT ADDRESS OR SERIAL PROGRAMMING LINES**

**8-BIT PARALLEL LOAD**

**MASTER RESET**

00636-001

**Rev. E**

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**REVISION HISTORY**

**7/07—Rev. D to Rev. E**

Changed AD9854ASQ to AD9854ASVZ Universal

Changed AD9854AST to AD9854ASTZ. Universal

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**11/06—Rev. C to Rev. D**

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**9/04—Rev. B to Rev. C**

Updated Format Universal

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**3/02—Rev. A to Rev. B**

Updated Format Universal

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**GENERAL DESCRIPTION**

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high speed, high performance quadrature DACs to form a digitally programmable I and Q synthesizer function. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase, amplitude-programmable sine and cosine outputs that can be used as an agile LO in communications, radar, and many other applications. The innovative high speed DDS core of the AD9854 provides 48-bit frequency resolution (1 μHz tuning resolution with 300 MHz SYSCLK). Maintaining 17 bits ensures excellent SFDR.

The circuit architecture of the AD9854 allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to

100 million new frequencies per second. The sine wave output (externally filtered) can be converted to a square wave by the internal comparator for agile clock generator applications.

The device provides two 14-bit phase registers and a single pin for BPSK operation.

For higher-order PSK operation, the I/O interface can be used for phase changes. The 12-bit I and Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrow-band output SFDR. The Q DAC can also be configured

as a user-programmable control DAC if the quadrature function is not desired. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in high speed clock generator applications.

Two 12-bit digital multipliers permit programmable amplitude modulation, on/off output shaped keying, and precise amplitude control of the quadrature output. Chirp functionality is also included to facilitate wide bandwidth frequency sweeping applications. The programmable 4× to 20× REFCLK multiplier circuit of the AD9854 internally generates the 300 MHz system clock from an external lower frequency reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source.

Direct 300 MHz clocking is also accommodated with either single- ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of ramped FSK are supported. The AD9854 uses advanced 0.35 μm CMOS technology to provide a high level of functionality on a single 3.3 V supply.

The AD9854 is pin-for-pin compatible with the AD9852 single- tone synthesizer. It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

**SPECIFICATIONS**

VS = 3.3 V ± 5%, RSET = 3.9 kΩ, external reference clock frequency = 30 MHz with REFCLK multiplier enabled at 10× for AD9854ASVZ, external reference clock frequency = 20 MHz with REFCLK multiplier enabled at 10× for AD9854ASTZ, unless otherwise noted.

**Table 1.**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Temp** | **Test Level** | **AD9854ASVZ**  **Min Typ Max** | **AD9854ASTZ**  **Min Typ Max** | **Unit** |
| REFERENCE CLOCK INPUT CHARACTERISTICS1  Internal System Clock Frequency Range REFCLK Multiplier Enabled  REFCLK Multiplier Disabled  External Reference Clock Frequency Range REFCLK Multiplier Enabled  REFCLK Multiplier Disabled Duty Cycle  Input Capacitance Input Impedance  Differential Mode Common-Mode Voltage Range Minimum Signal Amplitude2  Common-Mode Range  VIH (Single-Ended Mode) VIL (Single-Ended Mode) | Full | VI | 20 300 | 20 200 | MHz |
| Full | VI | DC 300 | DC 200 | MHz |
| Full | VI | 5 75 | 5 50 | MHz |
| Full | VI | DC 300 | DC 200 | MHz |
| 25°C | IV | 45 50 55 | 45 50 55 | % |
| 25°C | IV | 3 | 3 | pF |
| 25°C | IV | 100 | 100 | kΩ |
| 25°C | IV | 400 | 400 | mV p-p |
| 25°C | IV | 1.6 1.75 1.9 | 1.6 1.75 1.9 | V |
| 25°C | IV | 2.3 | 2.3 | V |
| 25°C | IV | 1 | 1 | V |
| DAC STATIC OUTPUT CHARACTERISTICS |  |  |  |  |  |
| Output Update Speed | Full | I | 300 | 200 | MSPS |
| Resolution | 25°C | IV | 12 | 12 | Bits |
| I and Q Full-Scale Output Current | 25°C | IV | 5 10 20 | 5 10 20 | mA |
| I and Q DAC DC Gain Imbalance3 | 25°C | I | −0.5 +0.15 +0.5 | −0.5 +0.15 +0.5 | dB |
| Gain Error | 25°C | I | −6 +2.25 | −6 +2.25 | % FS |
| Output Offset | 25°C | I | 2 | 2 | μA |
| Differential Nonlinearity | 25°C | I | 0.3 1.25 | 0.3 1.25 | LSB |
| Integral Nonlinearity | 25°C | I | 0.6 1.66 | 0.6 1.66 | LSB |
| Output Impedance | 25°C | IV | 100 | 100 | kΩ |
| Voltage Compliance Range | 25°C | I | −0.5 +1.0 | −0.5 +1.0 | V |
| DAC DYNAMIC OUTPUT CHARACTERISTICS |  |  |  |  |  |
| I and Q DAC Quadrature Phase Error | 25°C | IV | 0.2 1 | 0.2 1 | Degrees |
| DAC Wideband SFDR |  |  |  |  |  |
| 1 MHz to 20 MHz AOUT | 25°C | V | 58 | 58 | dBc |
| 20 MHz to 40 MHz AOUT | 25°C | V | 56 | 56 | dBc |
| 40 MHz to 60 MHz AOUT | 25°C | V | 52 | 52 | dBc |
| 60 MHz to 80 MHz AOUT | 25°C | V | 48 | 48 | dBc |
| 80 MHz to 100 MHz AOUT | 25°C | V | 48 | 48 | dBc |
| 100 MHz to 120 MHz AOUT | 25°C | V | 48 | 48 | dBc |
| DAC Narrow-Band SFDR |  |  |  |  |  |
| 10 MHz AOUT (±1 MHz) | 25°C | V | 83 | 83 | dBc |
| 10 MHz AOUT (±250 kHz) | 25°C | V | 83 | 83 | dBc |
| 10 MHz AOUT (±50 kHz) | 25°C | V | 91 | 91 | dBc |
| 41 MHz AOUT (±1 MHz) | 25°C | V | 82 | 82 | dBc |
| 41 MHz AOUT (±250 kHz) | 25°C | V | 84 | 84 | dBc |
| 41 MHz AOUT (±50 kHz) | 25°C | V | 89 | 89 | dBc |
| 119 MHz AOUT (±1 MHz) | 25°C | V | 71 | 71 | dBc |
| 119 MHz AOUT (±250 kHz) | 25°C | V | 77 | 77 | dBc |
| 119 MHz AOUT (±50 kHz) | 25°C | V | 83 | 83 | dBc |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Temp** | **Test Level** | **Min** | **AD9854ASVZ**  **Typ Max** | | **Min** | **AD9854ASTZ**  **Typ Max** | | **Unit** |
| Residual Phase Noise  (AOUT = 5 MHz, External Clock = 30 MHz REFCLK Multiplier Engaged at 10×)  1 kHz Offset  10 kHz Offset  100 kHz Offset  (AOUT = 5 MHz, External Clock = 300 MHz, REFCLK Multiplier Bypassed)  1 kHz Offset  10 kHz Offset  100 kHz Offset | 25°C | V | 140 | | | 140 | | | dBc/Hz |
| 25°C | V | 138 | | | 138 | | | dBc/Hz |
| 25°C | V | 142 | | | 142 | | | dBc/Hz |
| 25°C | V | 142 | | | 142 | | | dBc/Hz |
| 25°C | V | 148 | | | 148 | | | dBc/Hz |
| 25°C | V | 152 | | | 152 | | | dBc/Hz |
| PIPELINE DELAYS4 , 5 , 6  DDS Core (Phase Accumulator and Phase-to-Amp Converter)  Frequency Accumulator Inverse Sinc Filter Digital Multiplier  DAC  I/O Update Clock (Internal Mode) I/O Update Clock (External Mode) | 25°C | IV | 33 | | | 33 | | | SYSCLK cycles |
| 25°C | IV | 26 | | | 26 | | | SYSCLK cycles |
| 25°C | IV | 16 | | | 16 | | | SYSCLK cycles |
| 25°C | IV | 9 | | | 9 | | | SYSCLK cycles |
| 25°C | IV | 1 | | | 1 | | | SYSCLK cycles |
| 25°C | IV | 2 | | | 2 | | | SYSCLK cycles |
| 25°C | IV | 3 | | | 3 | | | SYSCLK cycles |
| MASTER RESET DURATION | 25°C | IV | 10 | | | 10 | | | SYSCLK cycles |
| COMPARATOR INPUT CHARACTERISTICS |  |  |  |  |  |  |  |  |  |
| Input Capacitance | 25°C | V |  | 3 |  |  | 3 |  | pF |
| Input Resistance | 25°C | IV |  | 500 |  |  | 500 |  | kΩ |
| Input Current | 25°C | I |  | ±1 | ±5 |  | ±1 | ±5 | μA |
| Hysteresis | 25°C | IV |  | 10 | 20 |  | 10 | 20 | mV p-p |
| COMPARATOR OUTPUT CHARACTERISTICS |  |  |  |  |  |  |  |  |  |
| Logic 1 Voltage, High-Z Load | Full | VI | 3.1 |  |  | 3.1 |  |  | V |
| Logic 0 Voltage, High-Z Load | Full | VI |  |  | 0.16 |  |  | 0.16 | V |
| Output Power, 50 Ω Load, 120 MHz Toggle Rate | 25°C | I | 9 | 11 |  | 9 | 11 |  | dBm |
| Propagation Delay | 25°C | IV |  | 3 |  |  | 3 |  | ns |
| Output Duty Cycle Error7 | 25°C | I | −10 | ±1 | +10 | −10 | ±1 | +10 | % |
| Rise/Fall Times, 5 pF Load | 25°C | V |  | 2 |  |  | 2 |  | ns |
| Toggle Rate, High-Z Load | 25°C | IV | 300 | 350 |  | 300 | 350 |  | MHz |
| Toggle Rate, 50 Ω Load | 25°C | IV | 375 | 400 |  | 375 | 400 |  | MHz |
| Output Cycle-to-Cycle Jitter8 |  | IV |  |  | 4.0 |  |  | 4.0 | ps rms |
| COMPARATOR NARROW-BAND SFDR9 |  |  |  | | |  | | |  |
| 10 MHz (±1 MHz) | 25°C | V | 84 | | | 84 | | | dBc |
| 10 MHz (±250 MHz) | 25°C | V | 84 | | | 84 | | | dBc |
| 10 MHz (±50 MHz) | 25°C | V | 92 | | | 92 | | | dBc |
| 41 MHz (±1 MHz) | 25°C | V | 76 | | | 76 | | | dBc |
| 41 MHz (±250 MHz) | 25°C | V | 82 | | | 82 | | | dBc |
| 41 MHz (±50 MHz) | 25°C | V | 89 | | | 89 | | | dBc |
| 119 MHz (±1 MHz) | 25°C | V | 73 | | |  | | | dBc |
| 119 MHz (±250 MHz) | 25°C | V | 73 | | |  | | | dBc |
| 119 MHz (±50 MHz) | 25°C | V | 83 | | |  | | | dBc |
| CLOCK GENERATOR OUTPUT JITTER9 |  |  |  | | |  | | |  |
| 5 MHz AOUT | 25°C | V | 23 | | | 23 | | | ps rms |
| 40 MHz AOUT | 25°C | V | 12 | | | 12 | | | ps rms |
| 100 MHz AOUT | 25°C | V | 7 | | | 7 | | | ps rms |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Temp** | **Test Level** | **AD9854ASVZ**  **Min Typ Max** | | | **Min** | **AD9854ASTZ**  **Typ Max** | | **Unit** |
| PARALLEL I/O TIMING CHARACTERISTICS |  |  |  |  |  |  |  |  |  |
| tASU (Address Setup Time to WR Signal Active) | Full | IV | 8.0 | 7.5 |  | 8.0 | 7.5 |  | ns |
| tADHW (Address Hold Time to WR Signal Inactive) | Full | IV | 0 |  |  | 0 |  |  | ns |
| tDSU (Data Setup Time to WR Signal Inactive) | Full | IV | 3.0 | 1.6 |  | 3.0 | 1.6 |  | ns |
| tDHD (Data Hold Time to WR Signal Inactive) | Full | IV |  | 0 |  | 0 |  |  | ns |
| tWRLOW (WR Signal Minimum Low Time) | Full | IV | 2.5 | 1.8 |  | 2.5 | 1.8 |  | ns |
| tWRHIGH (WR Signal Minimum High Time) | Full | IV | 7 |  |  | 7 |  |  | ns |
| tWR (Minimum WR Time) | Full | IV | 10.5 |  |  | 10.5 |  |  | ns |
| tADV (Address to Data Valid Time) | Full | V | 15 |  | 15 | 15 |  | 15 | ns |
| tADHR (Address Hold Time to RD Signal Inactive) | Full | IV | 5 |  |  | 5 |  |  | ns |
| tRDLOV (RD Low to Output Valid) | Full | IV |  |  | 15 |  |  | 15 | ns |
| tRDHOZ (RD High to Data Three-State) | Full | IV |  |  | 10 |  |  | 10 | ns |
| SERIAL I/O TIMING CHARACTERISTICS |  |  |  |  |  |  |  |  |  |
| tPRE (CS Setup Time) | Full | IV | 30 |  |  | 30 |  |  | ns |
| tSCLK (Period of Serial Data Clock) | Full | IV | 100 |  |  | 100 |  |  | ns |
| tDSU (Serial Data Setup Time) | Full | IV | 30 |  |  | 30 |  |  | ns |
| tSCLKPWH (Serial Data Clock Pulse Width High) | Full | IV | 40 |  |  | 40 |  |  | ns |
| tSCLKPWL (Serial Data Clock Pulse Width Low) | Full | IV | 40 |  |  | 40 |  |  | ns |
| tDHLD (Serial Data Hold Time) | Full | IV | 0 |  |  | 0 |  |  | ns |
| tDV (Data Valid Time) | Full | V |  | 30 |  |  | 30 |  | ns |
| CMOS LOGIC INPUTS10 |  |  |  |  |  |  |  |  |  |
| Logic 1 Voltage | 25°C | I | 2.2 |  |  | 2.2 |  |  | V |
| Logic 0 Voltage | 25°C | I |  |  | 0.8 |  |  | 0.8 | V |
| Logic 1 Current | 25°C | IV |  |  | ±5 |  |  | ±12 | μA |
| Logic 0 Current | 25°C | IV |  |  | ±5 |  |  | ±12 | μA |
| Input Capacitance | 25°C | V |  | 3 |  |  | 3 |  | pF |
| POWER SUPPLY11 , 15 |  |  |  |  |  |  |  |  |  |
| VS Current11, 12 , 15 | 25°C | I |  | 1050 | 1210 |  | 755 | 865 | mA |
| VS Current11, 13 , 15 | 25°C | I |  | 710 | 816 |  | 515 | 585 | mA |
| VS Current14 | 25°C | I |  | 600 | 685 |  | 435 | 495 | mA |
| PDISS  11, 12, 15 | 25°C | I |  | 3.475 | 4.190 |  | 2.490 | 3.000 | W |
| PDISS  11, 13, 15 | 25°C | I |  | 2.345 | 2.825 |  | 1.700 | 2.025 | W |
| PDISS14 | 25°C | I |  | 1.975 | 2.375 |  | 1.435 | 1.715 | W |
| PDISS Power-Down Mode | 25°C | I |  | 1 | 50 |  | 1 | 50 | mW |

1 The reference clock inputs are configured to accept a 1 V p-p (typical) dc offset square or sine wave centered at one-half the applied VDD or a 3 V TTL-level pulse input.

2 An internal 400 mV p-p differential voltage swing equates to 200 mV p-p applied to both REFCLK input pins.

3 The I and Q gain imbalance is digitally adjustable to less than 0.01 dB.

4 Pipeline delays of each individual block are fixed; however, if the first eight MSBs of a tuning word are 0s, the delay appears longer. This is due to insufficient phase accumulation per system clock period to produce enough LSB amplitude to the DAC.

5 If a feature such as the inverse sinc, which has 16 pipeline delays, can be bypassed, the total delay is reduced by that amount.

6 The I/O UD CLK transfers data from the I/O port buffers to the programming registers. This transfer is measured in system clocks.

7 Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.

8 Represents the comparator’s inherent cycle-to-cycle jitter contribution. The input signal is a 1 V, 40 MHz square wave, and the measurement device is a Wavecrest DTS-2075. 9 Comparator input originates from the analog output section via the external 7-pole elliptic low-pass filter. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.

10 Avoid overdriving digital inputs. (Refer to the equivalent circuits in Figure 3.)

11 If all device functions are enabled, it is not recommended to simultaneously operate the device at the maximum ambient temperature of 85°C and at the maximum internal clock frequency. This configuration may result in violating the maximum die junction temperature of 150°C. Refer to the Power Dissipation and Thermal Considerations section for derating and thermal management information.

12 All functions engaged.

13 All functions except inverse sinc engaged.

14 All functions except inverse sinc and digital multipliers engaged.

15 In most cases, disabling the inverse sinc filter reduces power consumption by approximately 30%.

**ABSOLUTE MAXIMUM RATINGS**

**Table 2.**

|  |  |
| --- | --- |
| **Parameter** | **Rating** |
| Maximum Junction Temperature | 150°C |
| VS | 4 V |
| Digital Inputs | −0.7 V to +VS |
| Digital Output Current | 5 mA |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Maximum Clock Frequency (ASVZ) | 300 MHz |
| Maximum Clock Frequency (ASTZ) | 200 MHz |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**THERMAL RESISTANCE**

The heat sink of the AD9854ASVZ 80-lead TQFP package must be soldered to the PCB.

**Table 3.**

|  |  |  |
| --- | --- | --- |
| **Thermal Characteristic** | **TQFP** | **LQFP** |
| θJA (0 m/sec airflow)[1, 2, 3](#_bookmark6) | 16.2°C/W | 38°C/W |
| θJMA (1.0 m/sec airflow)[2, 3, 4, 5](#_bookmark7) | 13.7°C/W |  |
| θJMA (2.5 m/sec airflow)[2, 3, 4, 5](#_bookmark7) | 12.8°C/W |  |
| ΨJT[1, 2](#_bookmark7) | 0.3°C/W |  |
| θJC  [6, 7](#_bookmark7) | 2.0°C/W |  |

1 Per JEDEC JESD51-2 (heat sink soldered to PCB).

2 2S2P JEDEC test board.

3 Values of θJA are provided for package comparison and PCB design considerations.

4 Per JEDEC JESD51-6 (heat sink soldered to PCB).

5 Airflow increases heat dissipation, effectively reducing θJA. Furthermore, the more metal that is directly in contact with the package leads from metal traces through holes, ground, and power planes, the more θJA is reduced.

6 Per MIL-Std 883, Method 1012.1.

7 Values of θJC are provided for package comparison and PCB design considerations when an external heat sink is required.

To determine the junction temperature on the application PCB use the following equation:

*TJ* = *Tcase* + (*ΨJT* × *PD*)

where:

*TJ* is the junction temperature expressed in degrees Celsius. *Tcase* is the case temperature expressed in degrees Celsius, as measured by the user at the top center of the package.

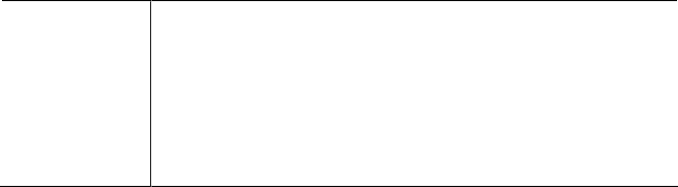
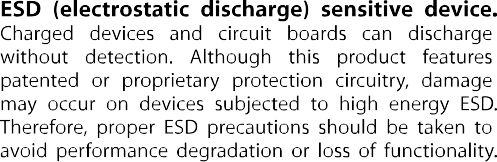
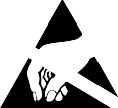
*ΨJT* = 0.3°C/W.

*PD* is the power dissipation (PD); see the [Power Dissipation and](#_bookmark55) [Thermal Considerations](#_bookmark55) section for the method to calculate PD.

**EXPLANATION OF TEST LEVELS**

**Table 3.**

|  |  |
| --- | --- |
| **Test Level** | **Description** |
| I | 100% production tested. |
| III | Sample tested only. |
| IV | Parameter is guaranteed by design and characterization testing. |
| V | Parameter is a typical value only. |
| VI | Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range. |

**ESD CAUTION**

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**

**DVDD DVDD DGND DGND DGND DGND DVDD DVDD DGND**

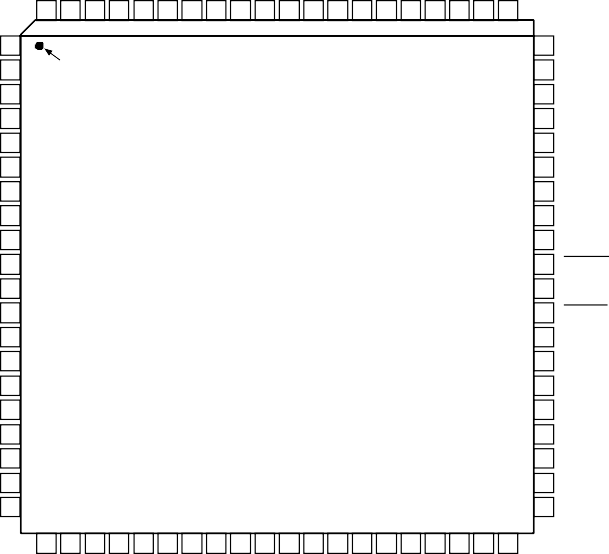
**MASTER RESET S/P SELECT REFCLK REFCLK**

**AGND AGND AVDD**

**DIFF CLK ENABLE NC**

**AGND**

**PLL FILTER**

**DV DV DG DG**

**80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61**

**D5 3**

**D4 4**

**D3 5**

**D2 6**

**D1 7**

**D0 8**

**DD 9**

**DD 10**

**ND 11**

**ND 12**

**NC 13**

**A5 14**

**A4 15**

**A3 16**

**ET 17**

**DO 18**

**IO 19**

**LK 20**

**AD9854**

**TOP VIEW**

**(Not to Scale)**

**58 NC**

**57 NC**

**56 DAC RSET**

**55 DACBP**

**54 AVDD**

**53 AGND**

**52 IOUT2**

**51 IOUT2**

**50 AVDD**

**49 IOUT1**

**48 IOUT1**

**47 AGND**

**46 AGND**

**45 AGND**

**44 AVDD**

**43 VINN**

**42 VINP**

**41 AGND**

**21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40**

**A2/IO RES**

**A1/S A0/SD**

**I/O UD C**



**NC = NO CONNECT**

**WR/SCLK RD/CS DVDD DVDD DVDD DGND DGND DGND**

**FSK/BPSK/HOLD**

**OSK AVDD AVDD AGND AGND NC VOUT AVDD AVDD AGND AGND**

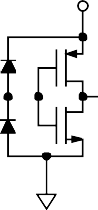
*Figure 2. Pin Configuration*

00636-002

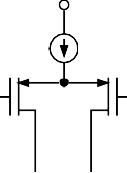
**Table 4. Pin Function Descriptions**

|  |  |  |
| --- | --- | --- |
| **Pin No.** | **Mnemonic** | **Description** |
| 1 to 8 | D7 to D0 | 8-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode. |
| 9, 10, 23, 24, 25, | DVDD | Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND |
| 73, 74, 79, 80 |  | and DGND. |
| 11, 12, 26, 27, 28, | DGND | Connections for the Digital Circuitry Ground Return. Same potential as AGND. |
| 72, 75 to 78 |  |  |
| 13, 35, 57, 58, 63 | NC | No Internal Connection. |
| 14 to 16 | A5 to A3 | Parallel Address Inputs for Program Registers (Part of 6-Bit Parallel Address Inputs for Program |
|  |  | Register, A5:A0). Used only in parallel programming mode. |
| 17 | A2/IO RESET | Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program |
|  |  | Register, A5:A0)/IO Reset. A2 is used only in parallel programming mode. IO RESET is used when |
|  |  | the serial programming mode is selected, allowing an IO RESET of the serial communication bus |
|  |  | that is unresponsive due to improper programming protocol. Resetting the serial bus in this |
|  |  | manner does not affect previous programming, nor does it invoke the default programming |
|  |  | values listed in [Table 8](#_bookmark43). Active high. |
| 18 | A1/SDO | Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program |
|  |  | Register, A5:A0)/Unidirectional Serial Data Output. A1 is used only in parallel programming |
|  |  | mode. SDO is used in 3-wire serial communication mode when the serial programming mode is |
|  |  | selected. |
| 19 | A0/SDIO | Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program |
|  |  | Register, A5:A0)/Bidirectional Serial Data I/O. A0 is used only in parallel programming mode. SDIO |
|  |  | is used in 2-wire serial communication mode. |

|  |  |  |
| --- | --- | --- |
| **Pin No.** | **Mnemonic** | **Description** |
| 20 | I/O UD CLK | Bidirectional I/O Update Clock. Direction is selected in control register. If this pin is selected as an |
|  |  | input, a rising edge transfers the contents of the I/O port buffers to the programming registers. If I/O |
|  |  | UD CLK is selected as an output (default), an output pulse (low to high) with a duration of eight |
|  |  | system clock cycles indicates that an internal frequency update has occurred. |
| 21 | WR/SCLK | Write Parallel Data to I/O Port Buffers. Shared function with SCLK. Serial clock signal associated |
|  |  | with the serial programming bus. Data is registered on the rising edge. This pin is shared with WR |
|  |  | when the parallel mode is selected. The mode is dependent on Pin 70 (S/P SELECT). |
| 22 | RD/CS | Read Parallel Data from Programming Registers. Shared function with CS. Chip-select signal |
|  |  | associated with the serial programming bus. Active low. This pin is shared with RD when the |
|  |  | parallel mode is selected. |
| 29 | FSK/BPSK/HOLD | Multifunction pin according to the mode of operation selected in the programming control |
|  |  | register. In FSK mode, logic low selects F1 and logic high selects F2. In BPSK mode, logic low |
|  |  | selects Phase 1 and logic high selects Phase 2. In chirp mode, logic high engages the hold |
|  |  | function, causing the frequency accumulator to halt at its current location. To resume or |
|  |  | commence chirp mode, logic low is asserted. |
| 30 | OSK | Output Shaped Keying. Must first be selected in the programming control register to function. A |
|  |  | logic high causes the I and Q DAC outputs to ramp up from zero-scale to full-scale amplitude at a |
|  |  | preprogrammed rate. Logic low causes the full-scale output to ramp down to zero scale at the |
|  |  | preprogrammed rate. |
| 31, 32, 37, 38, 44, | AVDD | Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND |
| 50, 54, 60, 65 |  | and DGND. |
| 33, 34, 39, 40, 41, | AGND | Connections for Analog Circuitry Ground Return. Same potential as DGND. |
| 45, 46, 47, 53, 59, |  |  |
| 62, 66, 67 |  |  |
| 36 | VOUT | Noninverted Output of the Internal High Speed Comparator. Designed to drive 10 dBm to 50 Ω |
|  |  | load as well as standard CMOS logic levels. |
| 42 | VINP | Voltage Input Positive. The noninverting input of the internal high speed comparator. |
| 43 | VINN | Voltage Input Negative. The inverting input of the internal high speed comparator. |
| 48 | IOUT1 | Unipolar Current Output of I, or the Cosine DAC. (Refer to [Figure 3](#_bookmark9).) |
| 49 | IOUT1 | Complementary Unipolar Current Output of I, or the Cosine DAC. |
| 51 | IOUT2 | Complementary Unipolar Current Output of Q, or the Sine DAC. |
| 52 | IOUT2 | Unipolar Current Output of Q, or the Sine DAC. This DAC can be programmed to accept external |
|  |  | 12-bit data in lieu of internal sine data, allowing the AD9854 to emulate the AD9852 control DAC |
|  |  | function. |
| 55 | DACBP | Common Bypass Capacitor Connection for Both I and Q DACs. A 0.01 μF chip capacitor from this |
|  |  | pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible, but |
|  |  | results in a slight degradation in SFDR. |
| 56 | DAC RSET | Common Connection for Both I and Q DACs. Used to set the full-scale output current. RSET = 39.9/IOUT. |
|  |  | Normal RSET range is from 8 kΩ (5 mA) to 2 kΩ (20 mA). |
| 61 | PLL FILTER | Connection for the External Zero-Compensation Network of the REFCLK Multiplier’s PLL Loop |
|  |  | Filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 μF |
|  |  | capacitor. The other side of the network should be connected to AVDD as close as possible to |
|  |  | Pin 60. For optimum phase noise performance, the REFCLK multiplier can be bypassed by setting |
|  |  | the bypass PLL bit in Control Register 1E hex. |
| 64 | DIFF CLK ENABLE | Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK |
|  |  | and REFCLK (Pin 69 and Pin 68, respectively). |
| 68 | REFCLK | Complementary (180° Out of Phase) Differential Clock Signal. User should tie this pin high or low  when single-ended clock mode is selected. Same signal levels as REFCLK. |
| 69 | REFCLK | Single-Ended Reference Clock Input (CMOS Logic Levels Required) or One of Two Differential |
|  |  | Clock Signals. In differential reference clock mode, both inputs can be CMOS logic levels or have |
|  |  | greater than 400 mV p-p square or sine waves centered about 1.6 V dc. |
| 70 | S/P SELECT | Selects serial programming mode (logic low) or parallel programming mode (logic high). |
| 71 | MASTER RESET | Initializes the serial/parallel programming bus to prepare for user programming; sets |
|  |  | programming registers to a do-nothing state defined by the default values listed in [Table 8](#_bookmark43). |
|  |  | Active on logic high. Asserting this pin is essential for proper operation upon power-up. |

**DVDD**

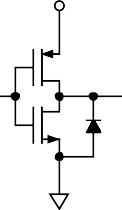
**AVDD**

**IOUT IOUTB**

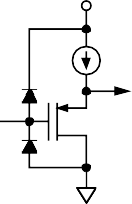
**MUST TERMINATE OUTPUTS FOR CURRENT FLOW. DO NOT EXCEED THE OUTPUT**

**VOLTAGE COMPLIANCE RATING.**

**AVDD**

**COMPARATOR OUT**

**VINP/ VINN**

**AVDD**

**DIGITAL IN**

**AVOID OVERDRIVING DIGITAL INPUTS. FORWARD BIASING ESD DIODES MAY COUPLE DIGITAL NOISE ONTO POWER PINS.**

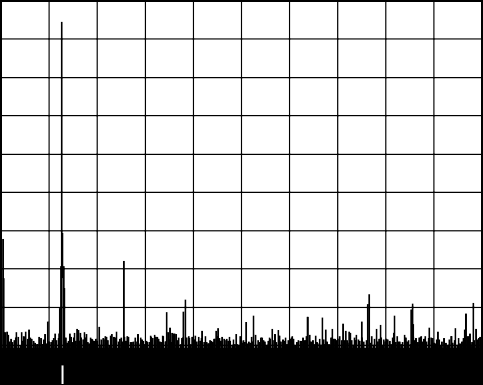
00636-003

**A. DAC OUTPUTS B. COMPARATOR OUTPUT C. COMPARATOR INPUT D. DIGITAL INPUTS**

*Figure 3. Equivalent Input and Output Circuits*

**TYPICAL PERFORMANCE CHARACTERISTICS**

[Figure 4](#_bookmark11) to [Figure 9](#_bookmark12) indicate the wideband harmonic distortion performance of the AD9854 from 19.1 MHz to 119.1 MHz fundamental output, reference clock = 30 MHz, REFCLK multiplier = 10×. Each graph is plotted from 0 MHz to 150 MHz (Nyquist).

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

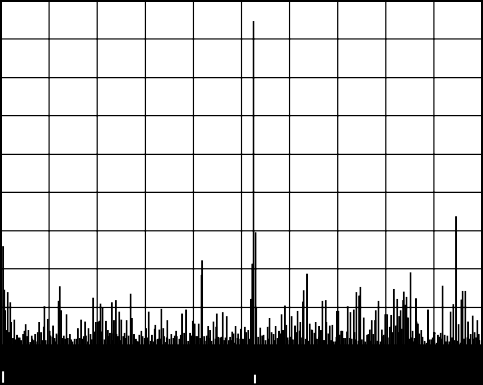
**–70**

**–80**

**–90**

00636-004

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**START 0Hz**

**15MHz/ STOP 150MHz**

**–100**

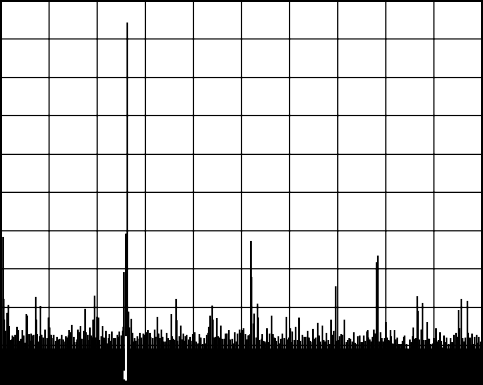
**START 0Hz**

**15MHz/**

**STOP 150MHz**

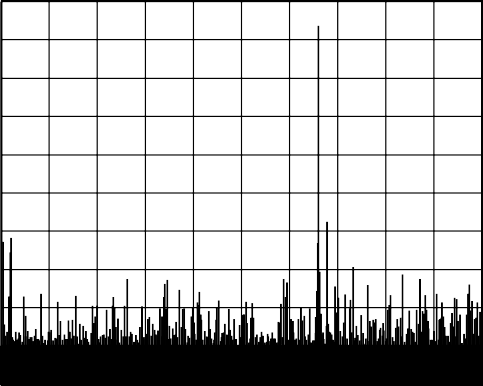
00636-007

*Figure 4. Wideband SFDR, 19.1 MHz Figure 7. Wideband SFDR, 79.1 MHz*

**0**

**–10**

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**START 0Hz**

**15MHz/**

**STOP 150MHz**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**START 0Hz**

**15MHz/**

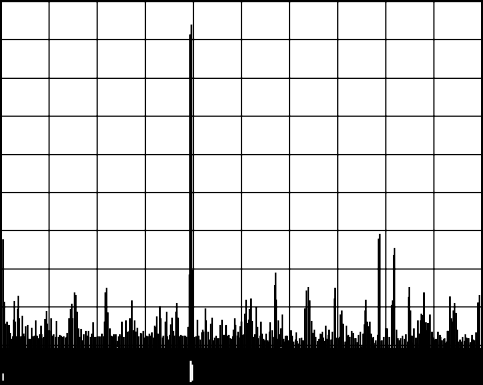
**STOP 150MHz**

00636-008

*Figure 5. Wideband SFDR, 39.1 MHz*

00636-005

*Figure 8. Wideband SFDR, 99.1 MHz*

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

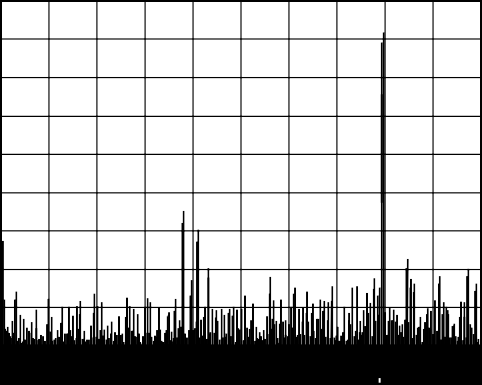
**–100**

**START 0Hz**

**15MHz/**

**STOP 150MHz**

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**START 0Hz**

**15MHz/ STOP 150MHz**

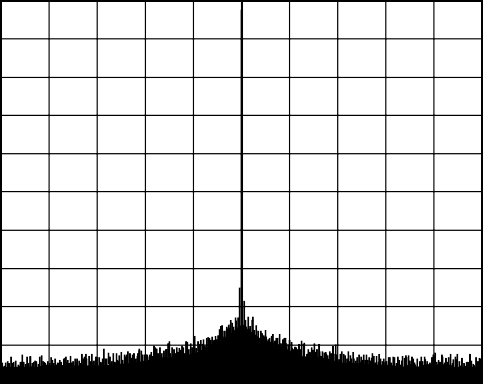
*Figure 6. Wideband SFDR, 59.1 MHz*

00636-006

*Figure 9. Wideband SFDR, 119.1 MHz*

00636-009

[Figure 10](#_bookmark13) to [Figure 15](#_bookmark15) show the trade-off in elevated noise floor, increased phase noise (PN), and discrete spurious energy when the internal REFCLK multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown. Compare the noise floor of [Figure 11](#_bookmark14) and [Figure 12](#_bookmark16) with that of [Figure 14](#_bookmark14) and [Figure 15](#_bookmark15). The improvement seen in [Figure 11](#_bookmark14) and [Figure 12](#_bookmark16) is a direct result of sampling the fundamental at a higher rate. Sampling at a higher rate spreads the quantization noise of the DAC over a wider bandwidth, which effectively lowers the noise floor.

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

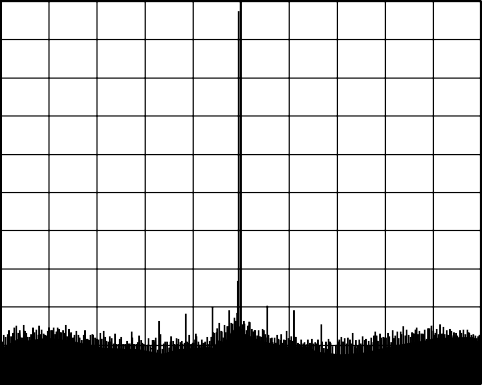
**–70**

**–80**

**–90**

00636-010

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

**100kHz/ SPAN 1MHz**

**–100**

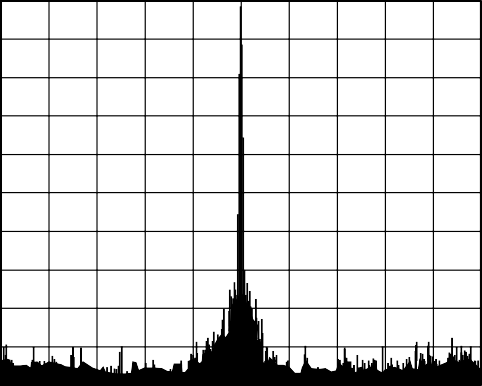
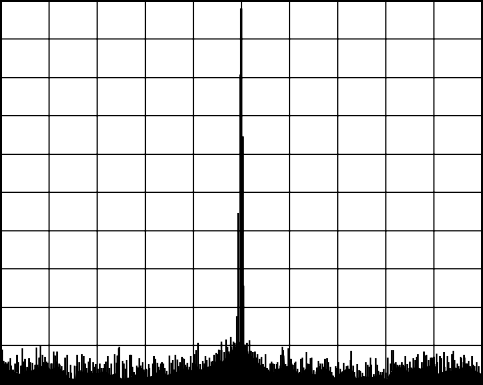
**CENTER 39.1MHz**

**100kHz/ SPAN 1MHz**

00636-012

*Figure 10. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed*

*Figure 13. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×*

**0 0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

**5kHz/**

**SPAN 50kHz**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

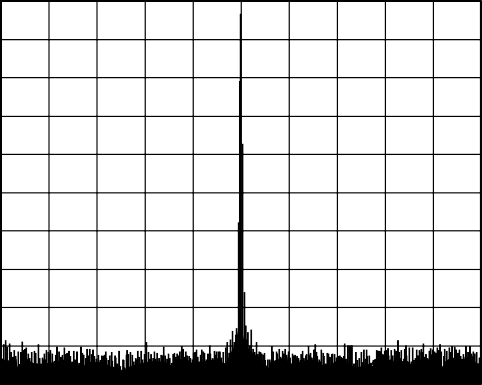
**5kHz/ SPAN 50kHz**

00636-013

*Figure 11. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed*

00636-011

*Figure 14. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×*

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

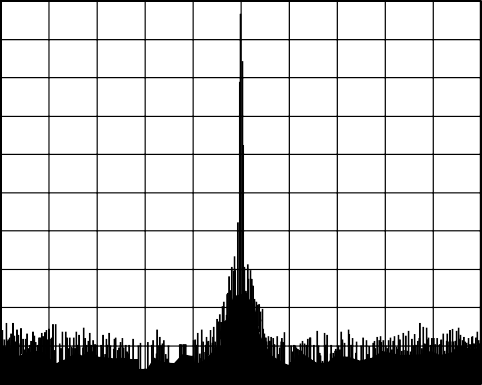
**–70**

**–80**

**–90**

00636-014

**0**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

**5kHz/**

**SPAN 50kHz**

**–100**

**CENTER 39.1MHz**

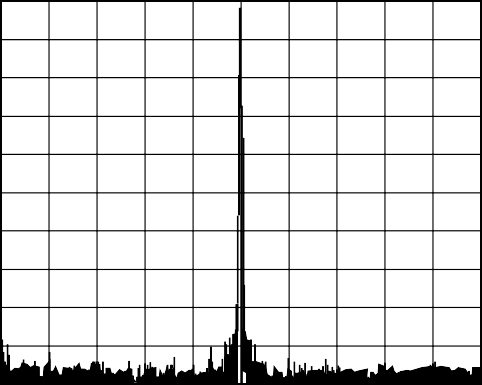
**5kHz/ SPAN 50kHz**

00636-015

*Figure 12. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 100 MHz REFCLK with REFCLK Multiplier Bypassed*

*Figure 15. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 10 MHz REFCLK with REFCLK Multiplier = 10×*

[Figure 16](#_bookmark17) and [Figure 17](#_bookmark18) show the narrow-band performance of the AD9854 when operating with a 200 MHz reference clock with the REFCLK multiplier bypassed vs. a 20 MHz reference clock and the REFCLK multiplier enabled at 10×.

**0**

**–10**

**–20**

**–30**

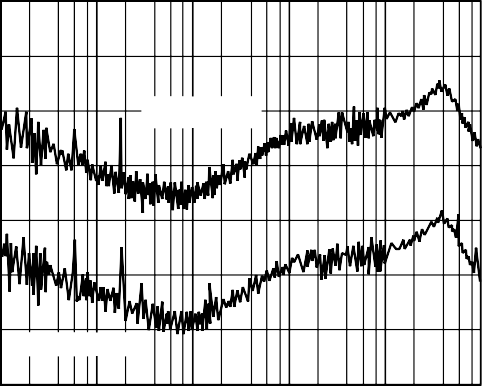
**–40**

**–50**

**–60**

**–70**

**–90**

**–100**

**AOUT = 80MHz**

**AOUT = 5MHz**

**–110**

**PHASE NOISE (dBc/Hz)**

**–120**

**–130**

**–140**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

**5kHz/**

**SPAN 50kHz**

**–150**

**–160**

**10**

**100**

**1k 10k**

**100k 1M**

00636-019

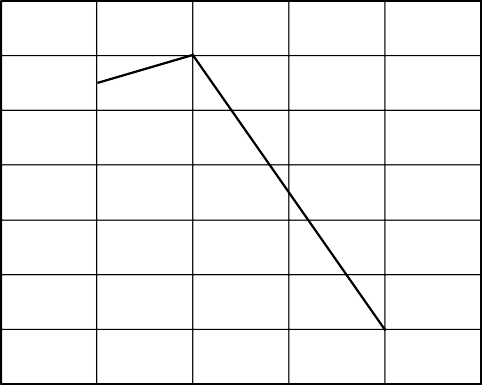
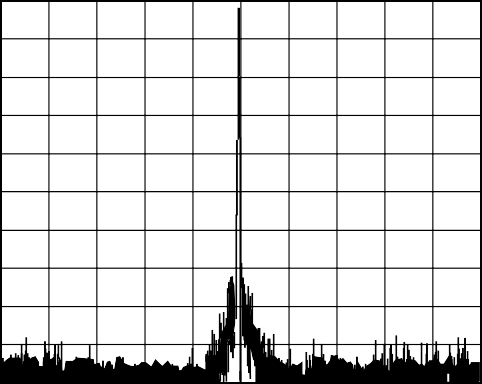
*Figure 16. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 200 MHz REFCLK with REFCLK Multiplier Bypassed*

**FREQUENCY (Hz)**

*Figure 19. Residual Phase Noise,*

00636-016

*30 MHz REFCLK with REFCLK Multiplier = 10×*

**0 55**

**–10**

**–20**

**–30**

**–40**

**–50**

**–60**

**–70**

**–80**

**–90**

**–100**

**CENTER 39.1MHz**

**5kHz/**

**SPAN 50kHz**

**54**

**53**

**52**

**SFDR (dBc)**

**51**

**50**

**49**

**48**

00636-020

**0 5 10 15 20 25**

**DAC CURRENT (mA)**

*Figure 17. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 20 MHz REFCLK with REFCLK Multiplier = 10×*

00636-017

*Figure 20. SFDR vs. DAC Current, 59.1 AOUT, 300 MHz REFCLK with REFCLK Multiplier Bypassed*

**–100**

**–110**

**–120**

**PHASE NOISE (dBc/Hz)**

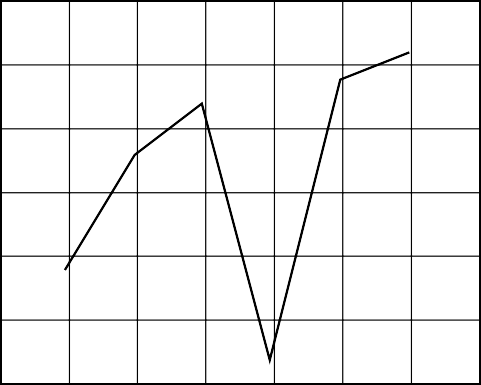
**–130**

**–140**

**–150**

00636-018

**620**

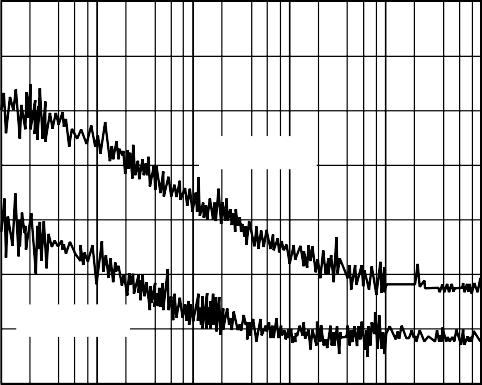
**615**

**610**

**SUPPLY CURRENT (mA)**

**605**

**600**

**–160**

**AOUT = 80MHz**

**AOUT = 5MHz**

**–170**

**10**

**100**

**1k 10k**

**100k 1M**

**595**

**590 0**

**20 40 60 80 100 120 140**

00636-021

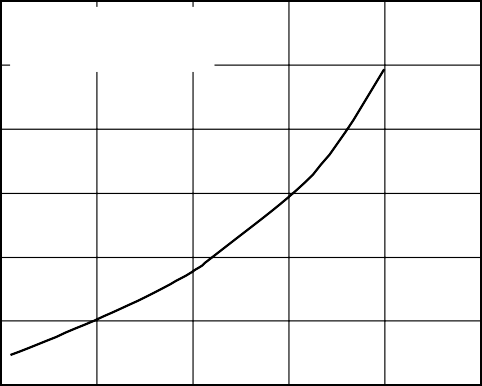
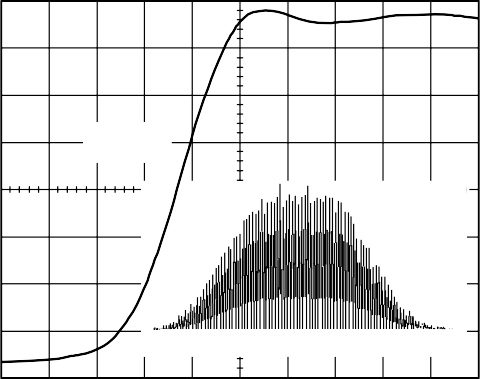
**FREQUENCY (Hz)**

*Figure 18. Residual Phase Noise,*

*300 MHz REFCLK with REFCLK Multiplier Bypassed*

**FREQUENCY (MHz)**

*Figure 21. Supply Current vs. Output Frequency (Variation Is Minimal, Expressed as a Percentage, and Heavily Dependent on Tuning Word)*

**1200**

**RISE TIME**

**1.04ns**

**JITTER [10.6ps RMS]**

**–33ps**

**0ps**

**+33ps**

**MINIMUM COMPARATOR INPUT DRIVE**

**VCM = 0.5V**

**1000**

**800**

**AMPLITUDE (mV p-p)**

**600**

**400**

**200**

**500ps/DIV 232mV/DIV 50Ω INPUT**

00636-022

*Figure 22. Typical Comparator Output Jitter, 40 MHz AOUT, 300 MHz RFCLK with REFCLK Multiplier Bypassed*

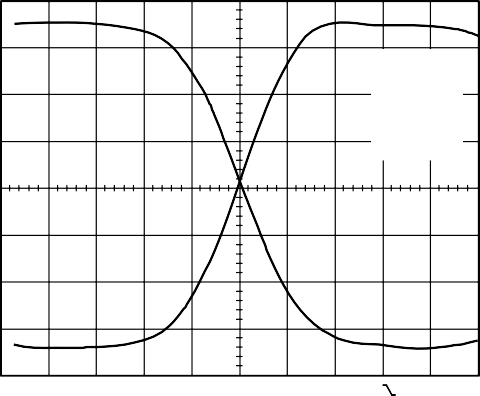
**0**

**0 100 200 300 400 500**

00636-024

**FREQUENCY (MHz)**

*Figure 24. Comparator Toggle Voltage Requirement*

*Figure 23. Comparator Rise/Fall Times*

**REF1 RISE 1.174ns**

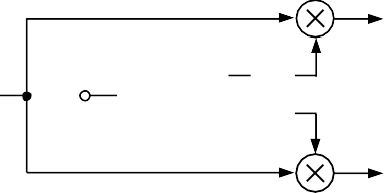
**C1 FALL 1.286ns**

**CH1 500mVΩ**

**M 500ps CH1**

**980mV**

00636-023

**TYPICAL APPLICATIONS**

**COS**

**REFCLK**

**SIN**

**LPF**

**LPF**

**AD9854**

**RF/IF INPUT**

**CHANNEL SELECT FILTERS**

*Figure 25. Quadrature Downconversion*

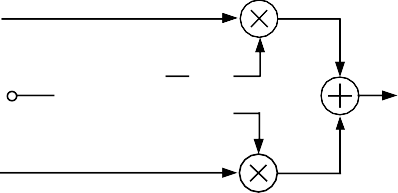
**I BASEBAND**

**Q BASEBAND**

**LPF**

**LPF**

00636-025

**I BASEBA**

**ND**

**COS**

**REFCLK**

**SIN**

**ND**

**LPF**

**LPF**

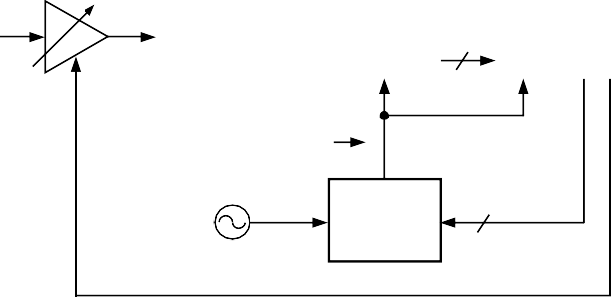
**AD9854**

**RF OUTPUT**

**Q BASEBA**

*Figure 26. Direct Conversion Quadrature Upconverter*

00636-026

**Rx RF IN**

**8**

**8**

**VCA**

**ADC CLOCK FREQUENCY**

**LOCKED TO Tx CHIP/ ADC ENCODE SYMBOL/PN RATE**

**AD9854 48**

**CLOCK GENERATOR**

**REFERENCE CLOCK**

**CHIP/SYMBOL/PN RATE DATA**

**DUAL 8-/10-BIT**

**ADC**

**AGC**

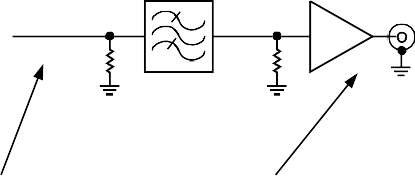
**DIGITAL DEMODULATOR**

|  |  |
| --- | --- |
| **I/Q MIXER** | **I** |
|  |
| **AND** |  |
| **LOW-PASS FILTER** | **Q** |
|  |

**Rx BASEBAND DIGITAL DATA OUT**

*Figure 27. Chip Rate Generator in Spread Spectrum Application*

00636-027

**BAND-PASS FILTER**

**IOUT**

**50Ω**

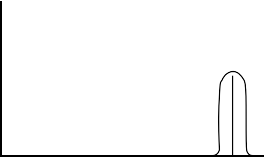
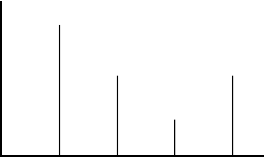
**50Ω**

**AD9854**

**AMPLIFIER**

**AD9854 SPECTRUM**

**FINAL OUTPUT SPECTRUM**

**FC + FO IMAGE**

**FUNDAMENTAL**

**FC – FO IMAGE**

**FC + FO IMAGE**

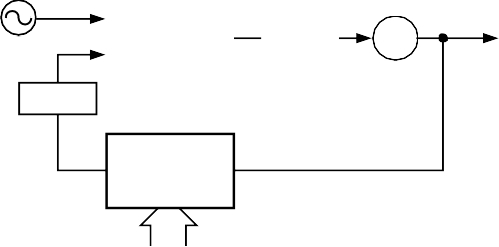
**FCLK**

**BAND-PASS FILTER**

00636-028

*Figure 28. Using an Aliased Image to Generate a High Frequency*

**REFERENCE CLOCK**

**RF FREQUENCY OUT**

**LOOP FILTER**

**PHASE COMPARATOR**

**VCO**

**FILTER**

**DAC OUT**

**TUNING WORD**

**REF CLK IN**

**PROGRAMMABLE DIVIDE-BY-N FUNCTION**

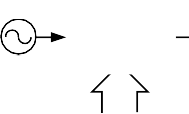
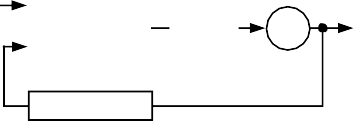
**DDS**

**AD9854**

**(WHERE N = 248/TUNING WORD)**

00636-029

*Figure 29. Programmable Fractional Divide-by-N Synthesizer*

**RF FREQUENCY**

**OUT**

**VCO**

**DIVIDE-BY-N**

**LOOP FILTER**

**PHASE COMPARATOR**

**REF CLOCK**

**FILTER**

**AD9854**

**DDS**

**TUNING WORD**

*Figure 30. Agile High Frequency Synthesizer*

00636-030

**36dB TYPICAL**

**SSB**

**AD8346 QUADRATURE MODULATOR**

**COSINE (DC TO 70MHz)**

**REJECTION**

**50Ω VOUT**

**Σ**

**LO**

**90**

**AD9854 QUADRATURE DDS**

**PHASE SPLITTER**

**0.8 TO 2.5GHz**

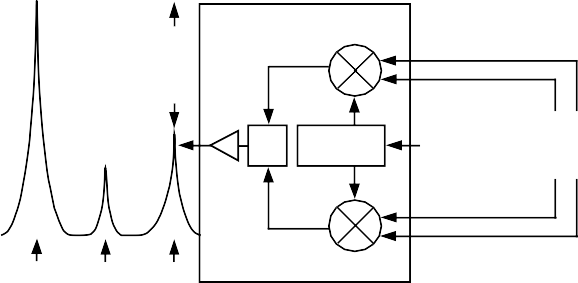
**0**

**LO**

**SINE (DC TO 70MHz)**

**DDS – LO LO DDS**

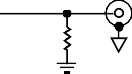
**+ LO**

**NOTES**

1. **FLIP DDS QUADRATURE SIGNALS TO SELECT ALTERNATE SIDEBAND. ADJUST DDS SINE OR COSINE SIGNAL AMPLITUDE FOR GREATEST SIDEBAND SUPPRESSION. DDS DAC OUTPUTS MUST BE LOW-PASS FILTERED PRIOR TO USE WITH THE AD8346.**

00636-031

*Figure 31. Single Sideband Upconversion*

**DIFFERENTIAL TRANSFORMER-COUPLED**

**50Ω**

**FILTER**

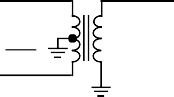
**REFERENCE CLOCK**

**DDS**

**AD9854**

**IOUT**

**OUTPUT**

**50Ω**

**IOUT**

00636-032

**1:1 TRANSFORMER**

**(Mini-Circuits® T1-1T)**

*Figure 32. Differential Output Connection for Reduction of Common-Mode Signals*

**REFERENCE CLOCK**

**AOUT = 100MHz**

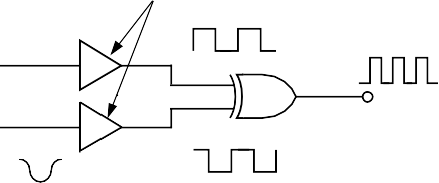
**AD9854**



**COMPARATORS**





*Figure 33. Clock Frequency Doubler*

**SIN**

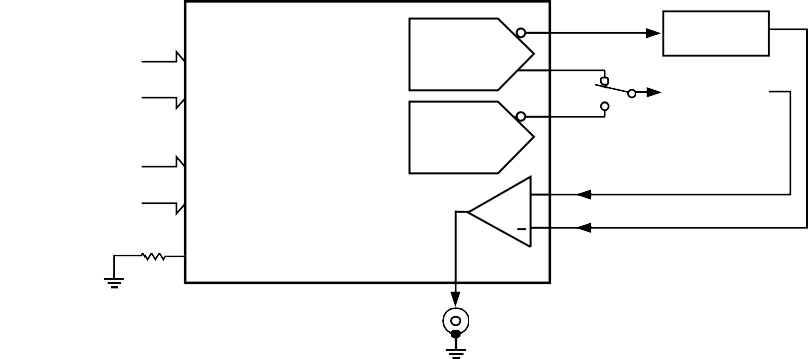
**CLOCK OUT = 200MHz**

**COS**

**LPF**

**LPF**

00636-033

**NOTES**

**AD9854**

**8-BIT PARALLEL OR SERIAL PROGRAMMING DATA AND CONTROL SIGNALS**

**I DAC**

**LOW-PASS FILTER**

**1**

**Q DAC OR CONTROL DAC**

**2**

**300MHz MAX DIRECT MODE OR 15MHz TO 75MHz MAX IN THE 4× TO 20× CLOCK**

**MULTIPLIER MODE**

**2kΩ**

**RSET**

**CMOS LOGIC CLOCK OUT**

**LOW-PASS FILTER**

**REFERENCE CLOCK**

**µPROCESSOR/ CONTROLLER FPGA, ETC.**

* 1. **IOUT**

**= APPROX 20mA MAX WHEN R**

**SET**

**= 2kΩ.**

* 1. **SWITCH POSITION 1 PROVIDES COMPLEMENTARY SINUSOIDAL SIGNALS TO THE COMPARATOR**

**TO PRODUCE A FIXED 50% DUTY CYCLE FROM THE COMPARATOR.**

* 1. **SWITCH POSITION 2 PROVIDES THE SAME DUTY CYCLE USING QUADRATURE SINUSOIDAL SIGNALS TO THE COMPARATOR OR A DC THRESHOLD VOLTAGE TO ALLOW SETTING OF THE COMPARATOR DUTY CYCLE (DEPENDS ON THE CONFIGURATION OF THE Q DAC).**

*Figure 34. Frequency Agile Clock Generator Applications for the AD9854*

00636-034

**THEORY OF OPERATION**

The AD9854 quadrature output digital synthesizer is a highly flexible device that addresses a wide range of applications. The device consists of an NCO with a 48-bit phase accumulator, a programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, a high speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, an agile clock generator, or an FSK/BPSK modulator.

Analog Devices, Inc., provides a technical tutorial about the operational theory of the functional blocks of the device. The tutorial includes a technical description of the signal flow through a DDS device and provides basic applications information for a variety of digital synthesis implementations. The document, *A Technical Tutorial on Digital Signal Synthesis,* is available from the DDS Technical Library, on the Analog Devices DDS website at [www.analog.com/dds](http://www.analog.com/dds).

**MODES OF OPERATION**

The AD9854 has five programmable operational modes. To select a mode, three bits in the control register (parallel Address 1F hex) must be programmed, as described in [Table 5](#_bookmark21).

**Table 5. Mode Selection Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mode 2** | **Mode 1** | **Mode 0** | **Result** |
| 0 | 0 | 0 | Single tone |
| 0 | 0 | 1 | FSK |
| 0 | 1 | 0 | Ramped FSK |
| 0 | 1 | 1 | Chirp |
| 1 | 0 | 0 | BPSK |

**Table 6. Functions Available for Modes**

In each mode, some functions may be prohibited. [Table 6](#_bookmark22) lists the functions and their availability for each mode.

***Single Tone (Mode 000)***

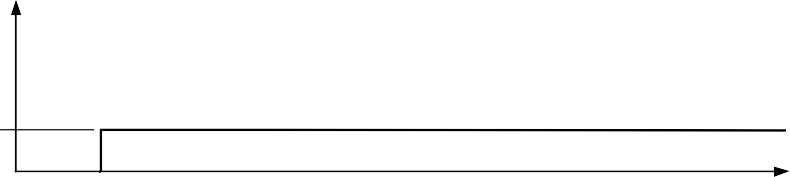
This is the default mode when the MASTER RESET pin is asserted. It can also be accessed if the user programs this mode into the control register. The phase accumulator, responsible for generating an output frequency, is presented with a 48-bit value from the Frequency Tuning Word 1 registers that have default values of 0. Default values from the remaining applicable registers further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hz and zero phase. At power-up and reset, the output from the I and Q DACs is a dc value equal to

the midscale output current. This is the default mode amplitude setting of 0. See the [On/Off Output Shaped Keying (OSK)](#_bookmark38) section for more details about the output amplitude control. All or some of the 28 program registers must be programmed to produce a user-defined output signal.

[Figure 35](#_bookmark23) shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Function** | **Mode** | | | | |
| **Single Tone** | **FSK** | **Ramped FSK** | **Chirp** | **BPSK** |
| Phase Adjust 1  Phase Adjust 2  Single-Pin FSK/BPSK or HOLD Single-Pin Shaped Keying Phase Offset or Modulation  Amplitude Control or Modulation Inverse Sinc Filter  Frequency Tuning Word 1  Frequency Tuning Word 2 Automatic Frequency Sweep | ●  ●  ●  ●  ●  ● | ●  ●  ●  ●  ●  ●  ●  ● | ●  ●  ●  ●  ●  ●  ●  ●  ● | ●  ●  ●  ●  ●  ●  ●  ● | ●  ●  ●  ●  ●  ●  ● |

**F1 0**

**FREQUENCY**

**MODE**

**000 (DEFAULT)**

**000 (SINGLE TONE)**

**MASTER RESET**

**I/O UD CLK**

**TW1**





*Figure 35. Default State to User-Defined Output Transition*

**0**

**F1**

00636-035

As with all Analog Devices DDS devices, the value of the frequency tuning word is determined by

*FTW* = (*Desired Output Frequency* × 2*N*)/*SYSCLK*

where:

*N* is the phase accumulator resolution (48 bits in this instance).

*Desired Output Frequency* is expressed in hertz.

*FTW* (frequency tuning word) is a decimal number.

After a decimal number has been calculated, it must be rounded to an integer and then converted to binary format, that is, a series of 48 binary-weighted 1s and 0s. The fundamental sine wave DAC output frequency range is from dc to one-half SYSCLK.

Changes in frequency are phase continuous, meaning that the first sampled phase value of the new frequency is referenced from the time of the last sampled phase value of the previous frequency.

The I and Q DACs of the AD9854 are always 90° out of phase. The 14-bit phase registers do not independently adjust the phase of each DAC output. Instead, both DACs are affected equally by a change in phase offset.

The single-tone mode allows the user to control the following signal qualities:

* Output frequency to 48-bit accuracy
* Output amplitude to 12-bit accuracy
  + Fixed, user-defined amplitude control
  + Variable, programmable amplitude control
  + Automatic, programmable, single-pin-controlled on/off output shaped keying
* Output phase to 14-bit accuracy

These qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel byte rate or at

a 10 MHz serial rate. Incorporating this attribute permits FM, AM, PM, FSK, PSK, and ASK operation in single-tone mode.

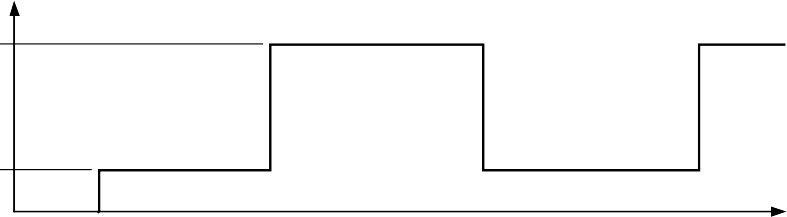
***Unramped FSK (Mode 001)***

When the unramped FSK mode is selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word Register 1 and Frequency Tuning Word Register 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (Frequency Tuning Word 1, Parallel Address 4 hex to Parallel Address 9 hex), and a logic high chooses F2 (Frequency Tuning Word 2, Parallel Register Address A hex to Parallel Register Address F hex). Changes in frequency are phase continuous and are internally coincident with the FSK data pin (Pin 29); however, there is deterministic pipeline delay between the FSK data signal and the DAC output. (Refer to the pipeline delays in [Table 1](#_bookmark4).)

The unramped FSK mode, shown in [Figure 36](#_bookmark24), represents traditional FSK, radio teletype (RTTY), or teletype (TTY) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF spectrum. Ramped FSK, shown in [Figure 37](#_bookmark25), is a method of conserving bandwidth.

***Ramped FSK (Mode 010)***

This mode is a method of FSK whereby changes from F1 to F2 are not instantaneous, but are accomplished in a frequency sweep or ramped fashion (the ramped notation implies that the sweep is linear). Although linear sweeping, or frequency ramping, is easily and automatically accomplished, it is only one of many schemes. Other frequency transition schemes can be implemented by changing the ramp rate and ramp step size on the fly in a piecewise fashion.

**F2**

**FREQUENCY**

**F1 0**

**MODE**

**000 (DEFAULT)**

**001 (FSK NO RAMP)**

**TW1 TW2**

**0**

**F1**

**0**

**F2**

**I/O UD CLK**

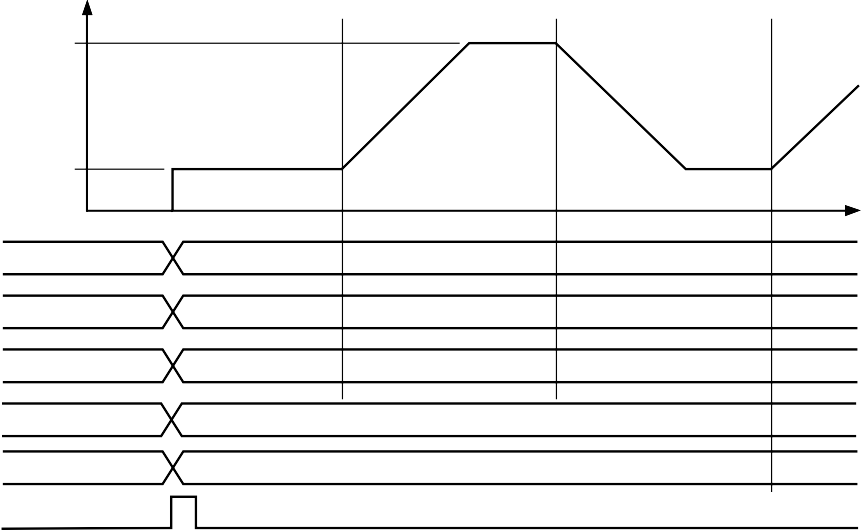
00636-036

**FSK DATA (PIN 29)**



*Figure 36. Unramped (Traditional) FSK Mode*

**FREQUENCY**

**MODE TW1 TW2**

**F2**

**F1 0**

**000 (DEFAULT)**

**010 (RAMPED FSK)**

**0**

**F1**

**0**

**F2**

**REQUIRES A POSITIVE TWOS COMPLEMENT VALUE**

**RAMP RATE**

**DFW**

**I/O UD CLK**

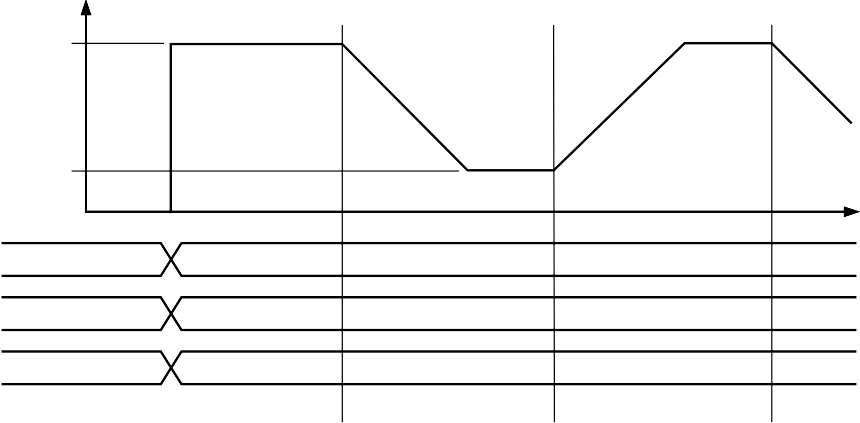
00636-037

**FSK DATA (PIN 29)**



*Figure 37. Ramped FSK Mode (Start at F1)*

**FREQUENCY**

**MODE TW1 TW2**

**F2**

**F1 0**

**000 (DEFAULT)**

**010 (RAMPED FSK)**

**0**

**F1**

**0**

**F2**

**I/O UD CLK**

00636-038

**FSK DATA**



*Figure 38. Ramped FSK Mode (Start at F2)*

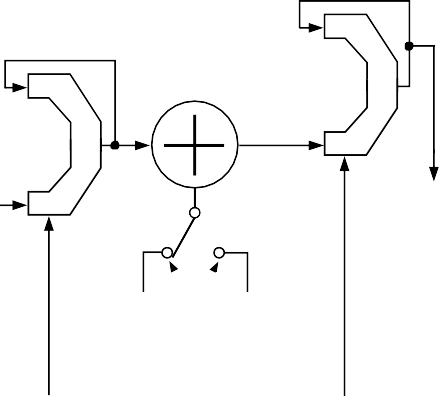
Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 are output in addition to the primary F1 and F2 frequencies.

[Figure 37](#_bookmark25) and [Figure 38](#_bookmark26) depict the frequency vs. time characteristics of a linear ramped FSK signal.

Note that in ramped FSK mode, the delta frequency word (DFW) is required to be programmed as a positive twos complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

The purpose of ramped FSK is to provide better bandwidth

The allowable range of N is from 1 to (220 − 1). The output of this counter clocks the 48-bit frequency accumulator shown in [Figure 39](#_bookmark27). The ramp rate clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The dwell time spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

**PHASE**

containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of inter- mediate frequencies, and the time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency to be loaded into F2 registers.

**20-BIT RAMP RATE CLOCK**

Several registers must be programmed to instruct the DDS on the resolution of intermediate frequency steps (48 bits) and the

**FREQUENCY ACCUMULATOR**

**48-BIT DELTA FREQUENCY WORD (TWOS COMPLEMENT)**

**ADDER ACCUMULATOR**

**FSK (PIN 29)**

**FREQUENCY TUNING WORD 1**

**FREQUENCY TUNING WORD 2**



**INSTANTANEOUS PHASE OUT**

time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to ensure that the frequency accumulator is starting from an all 0s output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in progress to affect the desired response.

Parallel Register Address 1A hex to Parallel Register Address 1C hex comprise the 20-bit ramp rate clock registers. This is a countdown counter that outputs a single pulse whenever the count reaches

1. The counter is activated when a logic level change occurs on the FSK input, Pin 29. This counter is run at the system clock rate, 300 MHz maximum. The time period between each output pulse is given as

(*N* + 1) × *System Clock Period*

where *N* is the 20-bit ramp rate clock value programmed by the user.

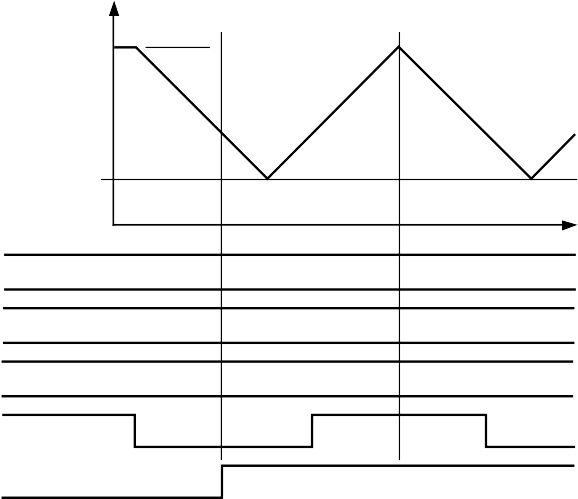
*Figure 39. Block Diagram of Ramped FSK Function*

Parallel Register Address 10 hex to Parallel Register Address 15 hex comprise the 48-bit, twos complement, delta frequency word registers. This 48-bit word is accumulated (added to the accumulator’s output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is added to or subtracted from the F1 or F2 frequency word, which is then fed into the input of the 48-bit phase accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency according to the logic state of Pin 29. This ramping rate is a function of the 20-bit ramp rate clock. When the destination frequency is achieved, the ramp rate clock is stopped, halting the frequency accumulation process.

**SYSTEM CLOCK**

00636-039

Generally speaking, the delta frequency word is a much smaller value compared with the value of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the delta frequency word might be only 25 Hz.

**MODE TW1 TW2**

**F2**

**F1**

**0**

**F2**

**F1**

**010 (RAMPED FSK)**

**FREQUENCY**

**FSK DATA**

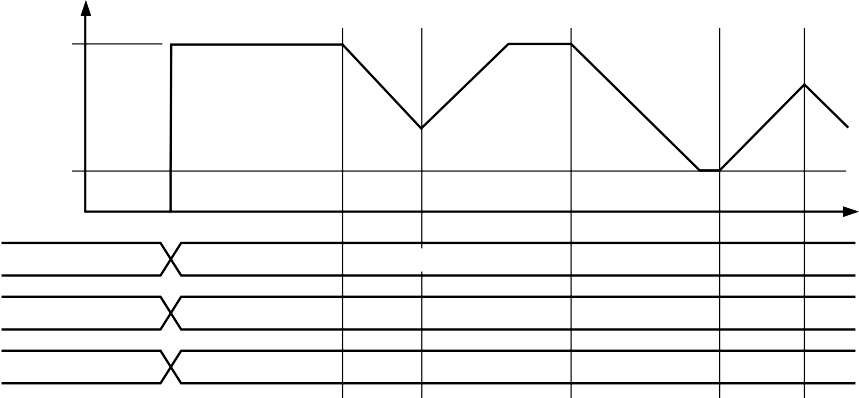
**TRIANGLE**

**BIT**

00636-040

**I/O UD CLK**

*Figure 40. Effect of Triangle Bit in Ramped FSK Mode*

**MODE TW1 TW2**

**F2**

**F1 0**

**000 (DEFAULT)**

**010 (RAMPED FSK)**

**0**

**F1**

**0**

**F2**

**FREQUENCY**

**I/O UD CLK**

00636-041

**FSK DATA**



*Figure 41. Effect of Premature Ramped FSK Data*

[Figure 41](#_bookmark29) shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution until the original frequency is reached.

The control register contains a triangle bit at Parallel Register Address 1F hex. Setting this bit high in Mode 010 causes an automatic ramp-up and ramp-down between F1 and F2 to occur without toggling Pin 29, as shown in [Figure 40](#_bookmark28). The logic state of Pin 29 has no effect once the triangle bit is set high. This function uses the ramp rate clock time period and the step size of the delta frequency word to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Use this function to automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode with the triangle bit set high, an automatic frequency sweep begins at either F1 or F2, according

to the logic level on Pin 29 (FSK input pin) when the triangle bit’s rising edge occurs ([Figure 42](#_bookmark30)). If the FSK data bit is high instead of low, F2, rather than F1, is chosen as the start frequency.

Additional flexibility in the ramped FSK mode is provided by the AD9854’s ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp rate counter at any time during the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps with different slopes in a piecewise fashion. This is done by programming and executing a linear ramp at a rate or slope and then altering the slope (by changing the ramp rate clock or delta frequency word, or both). Changes in slope can be made as often as needed before the destination frequency has been reached to form the desired nonlinear frequency sweep response. These piecewise changes can be precisely timed using

the 32-bit internal update clock (see the [Internal and External](#_bookmark38) [Update Clock](#_bookmark38) section).

Nonlinear ramped FSK has the appearance of the chirp function shown in [Figure 43](#_bookmark31). The difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2, whereas chirp operation has no F2 limit frequency.

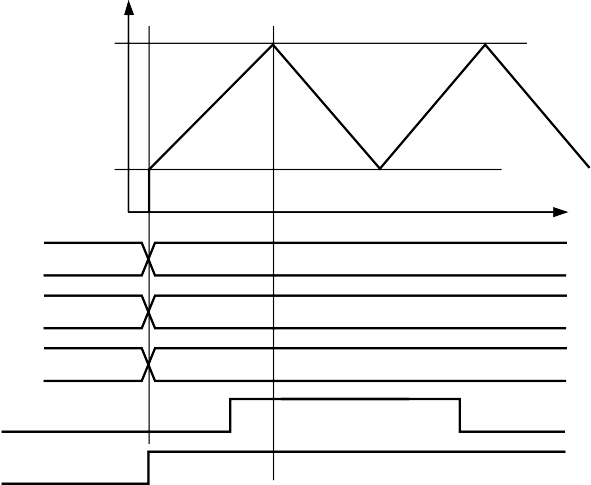
Two additional control bits (CLR ACC1 and CLR ACC2) are available in the ramped FSK mode that allow more options. If CLR ACC1 (Register Address 1F hex) is set high, it clears the 48-bit frequency accumulator (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1

bit is left high, a one-shot pulse is delivered on the rising edge of every update clock. The effect is to interrupt the current ramp, reset the frequency to the start point (F1 or F2), and then continue to ramp up (or down) at the previous rate. This occurs even when a static F1 or F2 destination frequency has been achieved.

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

***Chirp (Mode 011)***

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern, but the AD9854 can also support nonlinear patterns. In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the result that a single-frequency radar system would produce. [Figure 43](#_bookmark31) shows a very low resolution nonlinear chirp, demonstrating the different slopes that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

**F2**

**FREQUENCY**

**F1 0**

**MODE 000 (DEFAULT) 010 (RAMPED FSK)**

**TW1 0 F1**

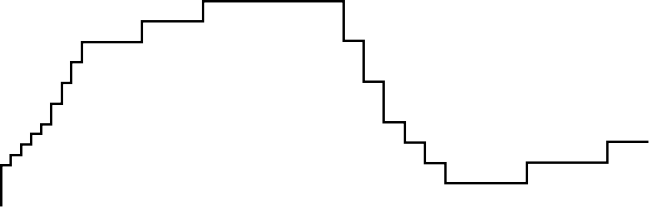
**TW2 0 F2**

**FSK DATA**

**TRIANGLE BIT**

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*Figure 42. Automatic Linear Ramping Using the Triangle Bit*

**MODE TW1 DFW**

**F1 0**

**000 (DEFAULT)**

**010 (RAMPED FSK)**

**0**

**F1**

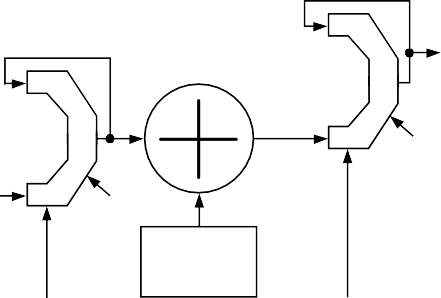
**FREQUENCY**

**RAMP RATE**

**I/O UD CLK**

00636-043

*Figure 43. Example of a Nonlinear Chirp*

The AD9854 permits precise, internally generated linear, or externally programmed nonlinear, pulsed or continuous FM over the complete frequency range, duration, frequency resolution, and sweep direction(s). All of these are user programmable. [Figure 44](#_bookmark32) shows a block diagram of the FM chirp components.

**OUT**

**ADDER PHASE ACCUMULATOR**

**FREQUENCY**

**ACCUMULATOR CLR ACC2**

**48-BIT DELTA FREQUENCY WORD (TWOS COMPLEMENT)**

**CLR ACC1**

Two control bits (CLR ACC1 and CLR ACC2) are available in the FM chirp mode that allow the return to the beginning frequency, FTW1, or to 0 Hz. When the CLR ACC1 bit (Register Address 1F hex) is set high, the 48-bit frequency accumulator (ACC1) output is cleared with a retriggerable one-shot pulse of one system clock duration. The 48-bit delta frequency word input to the accumulator is unaffected by the CLR ACC1 bit. If the CLR ACC1 bit is held high, a one-shot

pulse is delivered to the frequency accumulator (ACC1) on every rising edge of the I/O update clock. The effect is to interrupt the current chirp, reset the frequency to that programmed into FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the output of the frequency accumulator in the chirp mode is illustrated in [Figure 45](#_bookmark33). Shown in the diagram

**HOLD**

**FREQUENCY TUNING WORD 1**

**SYSTEM CLOCK**

*Figure 44. FM Chirp Components*

**20-BIT RAMP RATE CLOCK**

is the I/O update clock, which is either user supplied or internally generated.

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high,

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**Basic FM Chirp Programming Steps**

1. Program a start frequency into Frequency Tuning Word 1 (FTW1) at Parallel Register Address 4 hex to Parallel Register Address 9 hex.
2. Program the frequency step resolution into the 48-bit, twos complement delta frequency word (Parallel Register Address 10 hex to Parallel Register Address 15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit ramp rate clock (Parallel Register Address 1A hex to Parallel Register Address 1C hex).

When programming is complete, an I/O update pulse at Pin 20 engages the program commands.

The necessity for a twos complement delta frequency word is to define the direction in which the FM chirp moves. If the 48-bit delta frequency word is negative (MSB is high), the incremental frequency changes are in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), the incremental frequency changes are in a positive direction from FTW1.

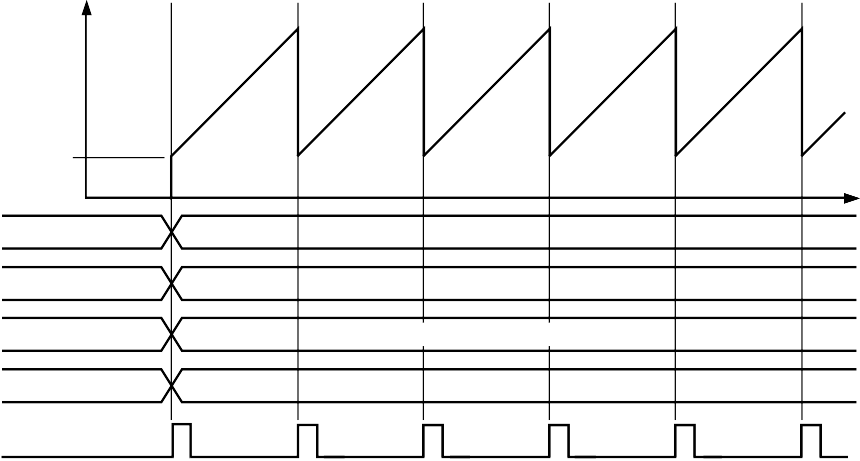
It is important to note that FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp begins, it is free to move (under program control) within the Nyquist bandwidth (dc to one-half the system clock). However, instant return to FTW1 can be easily achieved.

the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to the previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

[Figure 46](#_bookmark34) illustrates the effect of the CLR ACC2 bit on the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function that is available only in chirp mode is the HOLD pin (Pin 29). This function stops the clock signal to the ramp rate counter, halting any further clocking pulses to

the frequency accumulator, ACC1. The effect is to halt the chirp at the frequency existing just before the HOLD pin is pulled high. When Pin 29 is returned low, the clock and chirp resumes. During a hold condition, the user can change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of 0 is obtained before a new ramp rate count can be loaded. [Figure 47](#_bookmark35) shows the effect of the hold function on the DDS output frequency.

**MODE FTW1 DFW**

**F1 0**

**000 (DEFAULT)**

**011 (CHIRP)**

**0**

**F1**

**DELTA FREQUENCY WORD**

**RAMP RATE**

**FREQUENCY**

**RAMP RATE**

**I/O UD CLK**

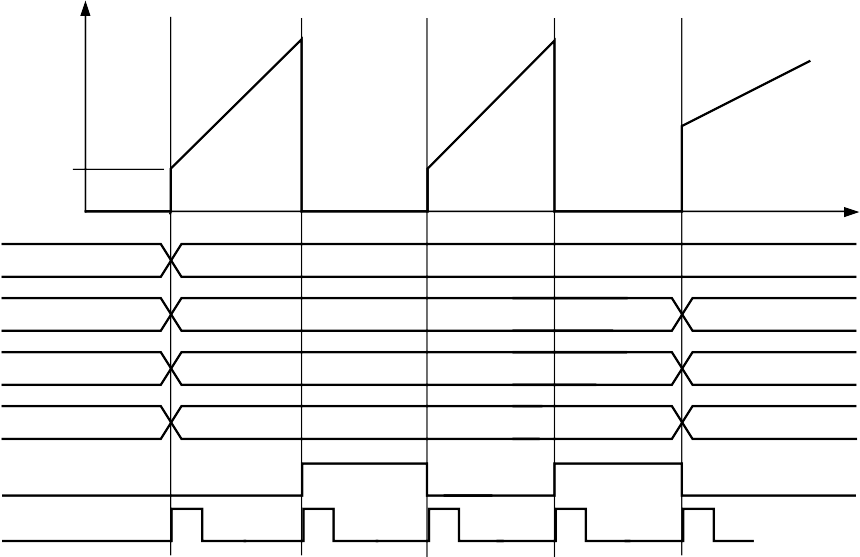
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**CLR ACC1**



*Figure 45. Effect of CLR ACC1 in FM Chirp Mode*

**FREQUENCY**

**MODE TW1 DPW**

**F1 0**

**000 (DEFAULT)**

**0**

**011 (CHIRP)**

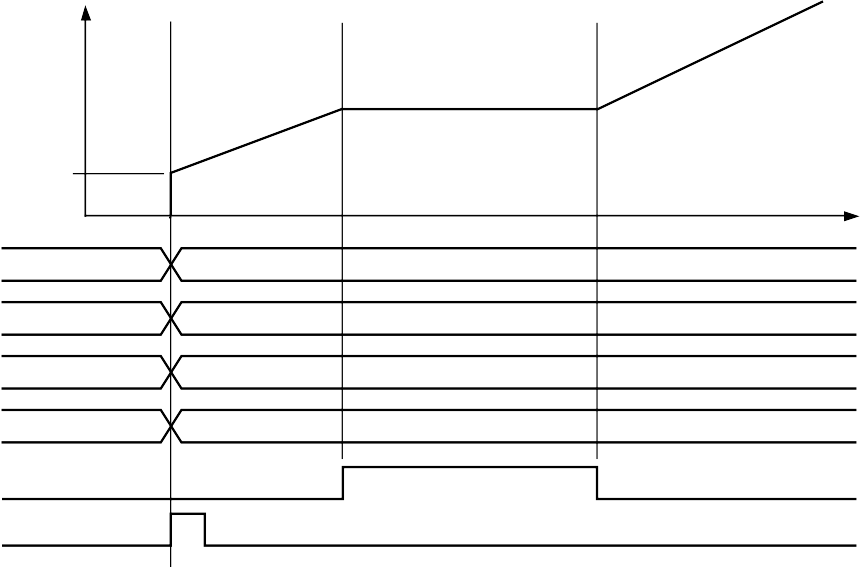
**RAMP RATE**

**CLR ACC2**

**I/O UD CLK**

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*Figure 46. Effect of CLR ACC2 in Chirp Mode*

**F1 0**

**FREQUENCY**

**MODE TW1 DFW**

**RAMP RATE**

**000 (DEFAULT)**

**0**

**011 (CHIRP) F1**

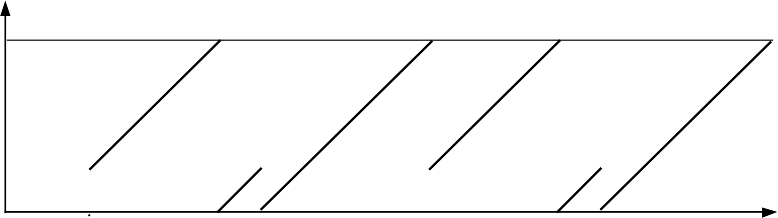
**DELTA FREQUENCY WORD**

**RAMP RATE**

**HOLD**

**I/O UD CLK**

00636-047

*Figure 47. Example of Hold Function*

**360**

**PHASE**

**0**

**MODE FTW1**

**000 (DEFAULT)**

**100 (BPSK)**

**0**

**F1**

**270°**

**PHASE ADJUST 1**

**PHASE ADJUST 2**

**90°**

**BPSK DATA**

00636-048

**I/O UD CLK**



*Figure 48. BPSK Mode*

The 32-bit automatic I/O update counter can be used to construct complex chirp or ramped FSK sequences. Because this internal counter is synchronized with the AD9854 system clock, precisely timed program changes are possible. For such changes, the user need only reprogram the desired registers before the automatic I/O update clock is generated.

In chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS automatically confines itself to the frequency range between dc and Nyquist. Unless terminated by the user, the chirp continues until power is removed.

When the chirp destination frequency is reached, the user can choose any of the following actions:

* Stop at the destination frequency by using the HOLD pin or by loading all 0s into the delta frequency word registers of the frequency accumulator (ACC1).
* Use the HOLD pin function to stop the chirp, and then ramp down the output amplitude by using the digital multiplier stages and the output shaped keying pin (Pin 30), or by using the program register control (Address 21 to Address 24 hex).
* Abruptly end the transmission with the CLR ACC2 bit.
* Continue chirp by reversing direction and returning to

the previous or another destination frequency in a linear or user-directed manner. If this involves reducing the frequency, a negative 48-bit delta frequency word (the MSB is set to 1) must be loaded into Register 10 hex to Register 15 hex. Any decreasing frequency step of the delta frequency word requires the MSB to be set to logic high.

* Continue chirp by immediately returning to the beginning frequency (F1) in a sawtooth fashion, and then repeating the previous chirp process using the CLR ACC1 control bit. An automatic, repeating chirp can be set up by using the 32-bit update clock to issue the CLR ACC1 command at precise time intervals. Adjusting the timing intervals or changing the delta frequency word changes the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

***BPSK (Mode 100)***

Binary, biphase, or bipolar phase shift keying is a means to rapidly select between two preprogrammed 14-bit output phase offsets that equally affect both the I and Q outputs of the AD9854. The logic state of Pin 29, the BPSK pin, controls the

selection of Phase Adjust Register 1 or Phase Adjust Register 2. When low, Pin 29 selects Phase Adjust Register 1; when high, it selects Phase Adjust Register 2. [Figure 48](#_bookmark36) illustrates phase changes made to four cycles of an output carrier.

***Basic BPSK Programming Steps***

1. Program a carrier frequency into Frequency Tuning Word 1.
2. Program the appropriate 14-bit phase words into Phase Adjust Register 1 and Phase Adjust Register 2.
3. Attach the BPSK data source to Pin 29.
4. Activate the I/O update clock when ready.

Note that for higher-order PSK modulation, the user can select the single-tone mode and program Phase Adjust Register 1 using the serial or high speed parallel programming bus.

**USING THE AD9854**

**INTERNAL AND EXTERNAL UPDATE CLOCK**

This update clock function is comprised of a bidirectional

I/O pin (Pin 20) and a programmable 32-bit down-counter. To program changes that are to be transferred from the I/O buffer registers to the active core of the DDS, a clock signal (low-to- high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit update clock.

When the user provides an external update clock, it is internally synchronized with the system clock to prevent a partial transfer of program register information due to a violation of data setup or hold time. This mode allows the user to completely control when updated program information becomes effective. The default mode for the update clock is internal (the internal update clock control register bit is logic high). To switch to external update clock mode, the internal update clock control register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses at intervals set by the user.

An internally generated update clock can be established by programming the 32-bit update clock registers (Address 16 hex to Address 19 hex) and setting the internal update clock control register bit (Address 1F hex) to logic high. The update clock down-counter function operates at half the rate of the system

**ON/OFF OUTPUT SHAPED KEYING (OSK)**

The on/off OSK feature allows the user to control the amplitude vs. time slope of the I and Q DAC output signals. This function is used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the OSK EN bit (Control Register Address 20 hex) to logic high in the control register.

Otherwise, if the OSK EN bit is set low, the digital multipliers responsible for amplitude control are bypassed and the I and Q DAC outputs are set to full-scale amplitude.

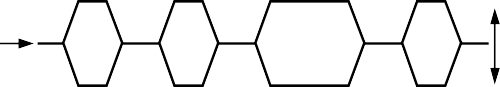
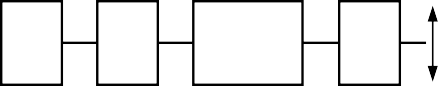
In addition to setting the OSK EN bit, a second control bit, OSK INT (also at Address 20 hex), must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp- down function. A logic low in the OSK INT bit switches control of the digital multipliers to user-programmable 12-bit registers, allowing users to dynamically shape the amplitude transition in practically any fashion. These 12-bit registers, labeled Output Shape Key I and Output Shape Key Q, are located at Address 21 hex through Address 24 hex, as listed in [Table 8](#_bookmark43). The maximum output amplitude is a function of the RSET resistor and is not programmable when OSK INT is enabled.

**ABRUPT ON/OFF KEYING**

clock (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O update of the DDS output or functions is generated. The update clock is internally and externally routed to Pin 20 to allow users to synchronize the programming of update information with the update clock rate.

The time between update pulses is given as (*N* + 1)(*System Clock Period* × 2)

**ZERO SCALE**

**ZERO SCALE**

**SHAPED ON/OFF KEYING**

*Figure 49. On/Off Output Shaped Keying*

**FULL SCALE**

**FULL SCALE**

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where *N* is the 32-bit value programmed by the user, and the allowable range of N is from 1 to (232 − 1).

The internally generated update pulse that is output from Pin 20 has a fixed high time of eight system clock cycles.

Programming the update clock register to a value less than five causes the I/O UD CLK pin to remain high. Although the update clock can function in this state, it cannot be used to indicate when data is transferring. This is an effect of the minimum high pulse time when I/O UD CLK functions as an output.

The transition time from zero scale to full scale must also be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the program- mable 8-bit ramp rate counter. This is a down-counter that is clocked at the system clock rate (300 MHz maximum) and that generates one pulse whenever the counter reaches 0. This pulse is routed to a 12-bit counter that increments with each pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all 0s at its inputs, the input signal is multiplied by 0, producing zero scale. When the multiplier has a value of all 1s, the input signal is multiplied by a value of 4095 or 4096, producing nearly full scale. There are 4094 remaining fractional multiplier values that produce output amplitudes scaled according to their binary values.

**DDS DIGITAL**

**OUTPUT**

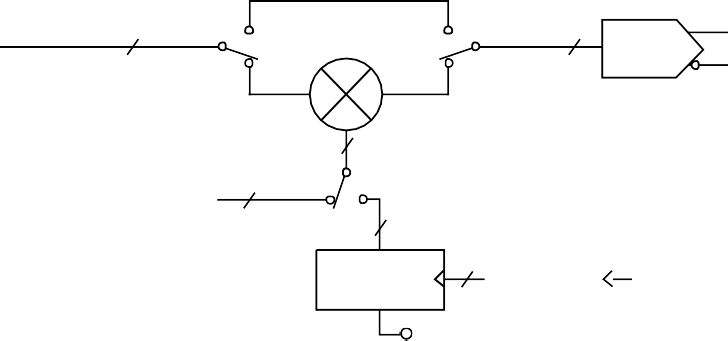
**DIGITAL SIGNAL IN**

**OSK EN = 0**

**12**

**OSK EN = 1**

**(BYPASS MULTIPLIER) 12-BIT DIGITAL**

**MULTIPLIER**

**OSK EN = 0**

**12**

**OSK EN = 1**

**SINE DAC**

**12**

**USER-PROGRAMMABLE 12-BIT Q CHANNEL MULTIPLIER**

**OUTPUT SHAPED KEYING Q MULTIPLIER REGISTER**

**12**

**OSK INT = 0**

**OSK INT = 0 12**

**12-BIT 1**

**SYSTEM CLOCK**

**8-BIT RAMP RATE COUNTER**

**UP/DOWN COUNTER**

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**ON/OFF OUTPUT SHAPED KEYING PIN**

*Figure 50. Block Diagram of Q DAC Pathway of the Digital Multiplier Section Responsible for the Output Shaped Keying Function*

The two fixed elements of the transition time are the period of the system clock (which drives the ramp rate counter) and the number of amplitude steps (4096). For example, if the system clock of the AD9854 is 100 MHz (10 ns period) and the ramp rate counter is programmed for a minimum count of 3, the transition takes two system clock periods (one rising edge loads the countdown value, and the next edge decrements the counter from 3 to 2). If the countdown value is less than 3, the ramp rate counter stalls and therefore produces a constant scaling value to the digital multipliers. This stall condition may have an application for the user.

The relationship of the 8-bit countdown value to the time between output pulses is given as

(*N* + 1) × *System Clock Period*

where *N* is the 8-bit countdown value.

It takes 4096 of these pulses to advance the 12-bit up-counter from zero scale to full scale. Therefore, the minimum output shaped keying ramp time for a 100 MHz system clock is

4096 × 4 × 10 ns ≈ 164 μs

The maximum ramp time is

4096 × 256 × 10 ns ≈ 10.5 ms

Finally, changing the logic state of Pin 30, output shaped keying automatically performs the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp up to full-scale amplitude and to hold until the logic level is changed to low, causing the outputs to ramp down to zero scale.

**I AND Q DACS**

The sine and cosine outputs of the DDS drive the Q and I DACs, respectively (300 MSPS maximum). The maximum amplitudes of these output are set by the DAC RSET resistor at Pin 56. These are current-output DACs with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides the best spurious-free dynamic range (SFDR) performance. The value

of RSET is 39.93/IOUT, where IOUT is expressed in amps. DAC output compliance specifications limit the maximum voltage developed at the outputs to −0.5 V to +1 V. Voltages developed beyond this limitation cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to the compliance limits. Both DAC outputs should be terminated equally for best SFDR, especially at higher output frequencies, where harmonic distortion errors are more prominent.

Both DACs are preceded by inverse sin(x)/x filters (also called inverse sinc filters) that precompensate for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. Both DACs can be powered down when not needed by setting the DAC PD bit high (Address 1D hex of the control register). I DAC outputs are designated as IOUT1 and IOUT1, Pin 48 and Pin 49, respectively. Q DAC outputs are designated as IOUT2 and IOUT2, Pin 52 and Pin 51, respectively.

**CONTROL DAC**

The 12-bit Q DAC can be reconfigured to perform as a control or auxiliary DAC. The control DAC output can provide dc control levels to external circuitry, generate ac signals, or enable duty cycle control of the on-board comparator. When the SRC Q DAC bit in the control register (Parallel Address 1F hex) is set high, the Q DAC inputs are switched from internal 12-bit

Q data source (default setting) to external 12-bit, twos complement data supplied by the user. Data is channeled through the serial or parallel interface to the 12-bit Q DAC register (Address 26 hex and Address 27 hex) at a maximum data rate of 100 MHz. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the I DAC. The single RSET resistor on the AD9854 sets the full-scale output current for both DACs. When not needed, the control DAC can be separately powered down to conserve power by setting the Q DAC power-down bit high (Address 1D hex).

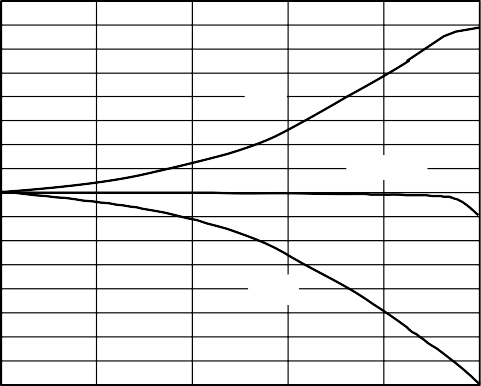
Control DAC outputs are designated as IOUT2 and IOUT2, Pin 52 and Pin 51, respectively.

**INVERSE SINC FUNCTION**

The inverse sinc function precompensates input data to both DACs for the sin(x)/x roll-off characteristic inherent in the DAC’s output spectrum. This allows wide bandwidth signals (such as QPSK) to be output from the DACs without appreciable amplitude variations as a function of frequency. The inverse sinc function can be bypassed to reduce power consumption significantly, especially at higher clock speeds.

When the Q DAC is configured as a control DAC, the inverse sinc function does not apply to the Q path.

Inverse sinc is engaged by default and is bypassed by bringing the bypass inverse sinc bit high in Control Register 20 hex, as noted in [Table 8](#_bookmark43).

**4.0**

**ISF**

**SYSTEM**

**SINC**

**3.5**

**3.0**

**2.5**

**2.0**

**1.5**

**MAGNITUDE (dB)**

**1.0**

**0.5**

**0**

**–0.5**

**–1.0**

**–1.5**

**–2.0**

**–2.5**

**–3.0**

**–3.5**

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should be set to Logic 0. The PLL range bit adjusts the PLL loop parameters for best phase noise performance within each range.

***PLL Filter***

The PLL FILTER pin (Pin 61) provides the connection for the external zero-compensation network of the PLL loop filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 μF capacitor. The other side of the network should be connected as close as possible to Pin 60, AVDD. For optimum phase noise performance, the clock multiplier can be bypassed by setting the bypass PLL bit in Control Register Address 1E hex.

***Differential REFCLK Enable***

A high level on the DIFF CLK ENABLE pin enables the differ- ential clock inputs, REFCLK and REFCLK (Pin 69 and Pin 68, respectively). The minimum differential signal amplitude required is 400 mV p-p at the REFCLK input pins. The center point or common-mode range of the differential signal can range from

1.6 V to 1.9 V.

When Pin 64 (DIFF CLK ENABLE) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as single-ended mode. In this mode, Pin 68 (REFCLK) should be tied low or high.

**High Speed Comparator**

**–4.0**

**0 0.1**

**0.2 0.3 0.4 0.5**

The comparator is optimized for high speed and has a toggle rate

**FREQUENCY NORMALIZED TO SAMPLE RATE**

*Figure 51. Inverse Sinc Filter Response*

**REFCLK MULTIPLIER**

The REFCLK multiplier is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20×. With this function, users can input as little as 15 MHz at the REFCLK input to produce a 300 MHz internal system clock. Five bits in Control Register 1E hex set the multiplier value, as detailed in [Table 7](#_bookmark42).

The REFCLK multiplier function can be bypassed to allow direct clocking of the AD9854 from an external clock source. The system clock for the AD9854 is either the output of the REFCLK multiplier (if it is engaged) or the REFCLK inputs. REFCLK can be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE, low or high, respectively.

***PLL Range Bit***

The PLL range bit selects the frequency range of the REFCLK multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate), the PLL range bit should be set to Logic 1. For operation below 200 MHz, the PLL range bit

greater than 300 MHz, low jitter, sensitive input, and built-in hysteresis. It also has an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be powered down separately to conserve power. This com- parator is used in clock-generator applications to square up the filtered sine wave generated by the DDS.

**Power-Down**

The programming registers allow several individual stages to be powered down to reduce power consumption while maintaining the functionality of the desired stages. These stages are identified in [Table 8](#_bookmark43), Address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, the inverse sinc filters and the digital multiplier stages can be bypassed to achieve significant power reduction by programming the control registers in Address 20 hex. Again, logic high causes the stage to be bypassed. Of particular importance is the inverse sinc filter; this stage consumes a significant amount of power.

A full power-down occurs when all four PD bits in Control Register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

**PROGRAMMING THE AD9854**

The AD9854 register layout table ([Table 8](#_bookmark43)) contains information for programming the chip for the desired functionality. Although many applications require very little programming to configure the AD9854, some use all 12 accessible register banks. The AD9854 supports an 8-bit parallel I/O operation or an SPI®- compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

S/P SELECT (Pin 70) is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to VDD. Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of the mode, the I/O port data is written to a buffer memory and only affects operation of the part after the contents of the buffer memory are transferred to the register banks. This transfer of information occurs synchronously to the system clock in one of two ways:

* Internally, at a rate programmable by the user.
* Externally, by the user. I/O operations can occur in the absence of REFCLK, but the data cannot be moved from the buffer memory to the register bank without REFCLK. (See the [Internal and External Update Clock](#_bookmark38) section for more details.)

**MASTER RESET**

The MASTER RESET pin must be held at logic high active for a minimum of 10 system clock cycles. This initializes the communications bus and loads the default values listed in the [Table 8](#_bookmark43) section.

**Table 7. REFCLK Multiplier Control Register Values**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Multiplier Value** | **Reference Multiplier** | | | | |
| **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 |

**Table 8. Register Layout1**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parallel Address (Hex)** | **Serial Address (Hex)** | **AD9854 Register Layout** | | | | | | | | **Default Value (Hex)** |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| 00  01 | 0 | Phase Adjust Register 1 <13:8> (Bits 15, 14, don’t care)  Phase Adjust Register 1 <7:0> | | | | | Phase 1 |  |  | 00  00 |
| 02  03 | 1 | Phase Adjust Register 2 <13:8> (Bits 15, 14, don’t care)  Phase Adjust Register 2 <7:0> | | | | | Phase 2 |  |  | 00  00 |
| 04 | 2 | Frequency Tuning Word 1 <47:40> | | | | | Freq 1 |  |  | 00 |
| 05 |  | Frequency Tuning Word 1 <39:32> | | | | |  | 00 |
| 06 |  | Frequency Tuning Word 1 <31:24> | | | | |  | 00 |
| 07 |  | Frequency Tuning Word 1 <23:16> | | | | |  | 00 |
| 08 |  | Frequency Tuning Word 1 <15:8> | | | | |  | 00 |
| 09 |  | Frequency Tuning Word 1 <7:0> | | | | |  | 00 |
| 0A | 3 | Frequency Tuning Word 2 <47:40> | | | | |  |  |  |  |
| 0B |  | Frequency Tuning Word 2 <39:32> | | | | | 00 |
| 0C |  | Frequency Tuning Word 2 <31:24> | | | | | 00 |
| 0D |  | Frequency Tuning Word 2 <23:16> | | | | | 00 |
| 0E |  | Frequency Tuning Word 2 <15:8> | | | | | 00 |
| 0F |  | Frequency Tuning Word 2 <7:0> | | | | | 00 |
| 10 | 4 | Delta frequency word <47:40> | | | | |  |  |  | 00 |
| 11 |  | Delta frequency word <39:32> | | | | | 00 |
| 12 |  | Delta frequency word <31:24> | | | | | 00 |
| 13 |  | Delta frequency word <23:16> | | | | | 00 |
| 14 |  | Delta frequency word <15:8> | | | | | 00 |
| 15 |  | Delta frequency word <7:0> | | | | | 00 |
| 16 | 5 | Update clock <31:24> | | | | |  |  |  | 00 |
| 17 |  | Update clock <23:16> | | | | | 00 |
| 18 |  | Update clock <15:8> | | | | | 00 |
| 19 |  | Update clock <7:0> | | | | | 40 |
| 1A | 6 | Ramp rate clock <19:16> (Bits 23, 22, 21, 20, don’t care) | | | | |  |  |  | 00 |
| 1B |  | Ramp rate clock <15:8> | | | | | 00 |
| 1C |  | Ramp rate clock <7:0> | | | | | 00 |
| 1D | 7 | Don’t | Don’t | Don’t | Comp | Reserved, | QDAC PD | DAC PD | DIG PD | 10 |
|  |  | care | care | care | PD | always low |  |  |  |  |
|  |  | CR [31] |  |  |  |  |  |  |  |  |
| 1E |  | Don’t | PLL | Bypass | Ref | Ref Mult 3 | Ref Mult 2 | Ref | Ref Mult 0 | 64 |
|  |  | care | range | PLL | Mult 4 |  |  | Mult 1 |  |  |
| 1F |  | CLR | CLR | Triangle | SRC | Mode 2 | Mode 1 | Mode 0 | Internal/external | 01 |
|  |  | ACC 1 | ACC 2 |  | QDAC |  |  |  | update clock |  |
| 20 |  | Don’t | Bypass | OSK EN | OSK | Don’t care | Don’t care | LSB first | SDO active CR [0] | 20 |
|  |  | care | inv sinc |  | INT |  |  |  |  |  |
| 21 | 8 | Output shaped keying I multiplier <11:8> (Bits 15, 14, 13, 12 don’t care) | | | | | | | | 00 |
| 22 |  | Output shaped keying I multiplier <7:0> | | | | | | | | 00 |
| 23 | 9 | Output shaped keying Q multiplier <11:8> (Bits 15, 14, 13, 12 don’t care) | | | | | | | | 00 |
| 24 |  | Output shaped keying Q multiplier <7:0> | | | | | | | | 00 |
| 25 | A | Output shaped keying ramp rate <7:0> | | | | | | | | 80 |
| 26 | B | QDAC <11:8> (Bits 15, 14, 13, 12 don’t care) | | | | | | | | 00 |
| 27 |  | QDAC <7:0> (data is required to be in twos complement format) | | | | | | | |  |

1 The shaded sections comprise the control register.

**PARALLEL I/O OPERATION**

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry-standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits, and separate write/read control inputs comprise the I/O port pins.

Parallel I/O operation allows write access to each byte of any register in a single I/O operation of up to one per 10.5 ns.

Readback capability for each register is included to ease designing with the AD9854. (Reads are not guaranteed at 100 MHz because they are intended for software debugging only.)

Parallel I/O operation timing diagrams are shown in [Figure 52](#_bookmark46) and [Figure 53](#_bookmark47).

**SERIAL PORT I/O OPERATION**

With the S/P SELECT pin tied low, the serial I/O mode is active. The serial port is a flexible, synchronous, serial communication port, allowing easy interface to many industry-standard micro- controllers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and Intel® 8051 SSR protocols. The

**Table 9. Serial I/O Pin Requirements**

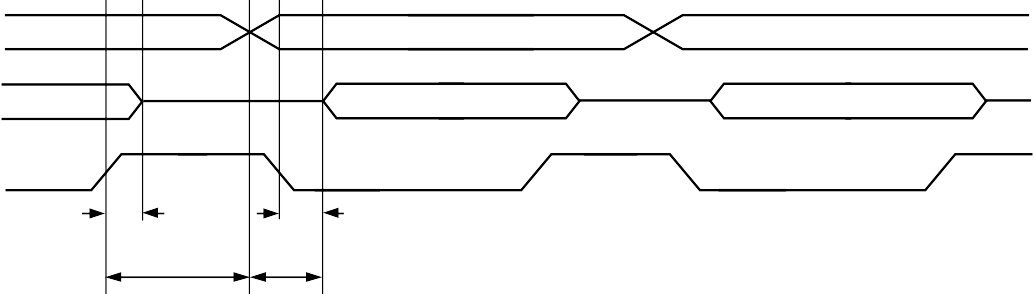
interface allows read/write access to all 12 registers that configure the AD9854 and can be configured as a single-pin I/O (SDIO) or two unidirectional pins for input and output (SDIO/SDO). Data transfers are supported in MSB-or the LSB-first format for up to 10 MHz.

When configured for serial I/O operation, most AD9854 parallel port pins are inactive; only some pins are used for the serial I/O operation. [Table 9](#_bookmark45) describes pin requirements for serial I/O operation.

Note that when operating the device in serial I/O mode, it is best to use the external I/O update clock mode to avoid an

update occurring during a serial communication cycle. Such an occurrence may cause incorrect programming due to a partial data transfer. To exit the default internal update mode, program the device for external update operation at power-up before starting the REFCLK signal but after a master reset. Starting the REFCLK causes this information to transfer to the register bank, forcing the device to switch to external update mode.

|  |  |  |
| --- | --- | --- |
| **Pin Number** | **Mnemonic** | **Serial I/O Description** |
| 1 to 8 | D [7:0] | The parallel data pins are not active; tie to VDD or GND. |
| 14 to 16 | A [5:3] | The A5, A4, and A3 parallel address pins are not active; tie these pins to VDD or GND. |
| 17 | A2/IO RESET | IO RESET. |
| 18 | A1/SDO | SDO. |
| 19 | A0/SDIO | SDIO. |
| 20 | I/O UD CLK | Update Clock. Same functionality for serial mode as parallel mode. |
| 21 | WR/SCLK | SCLK. |
| 22 | RD/CS | CS—Chip Select. |

**A<5:0>**

**A1**

**A2**

**A3**

**D1**

**D2**

**D3**

**tRDHOZ**

**tRDLOV**

**tAHD**

**tADV**

**D<7:0>**



**RD**

**SPECIFICATION VALUE DESCRIPTION**

**tADV tAHD tRDLOV tRDHOZ**

**15ns 5ns 15ns 10ns**

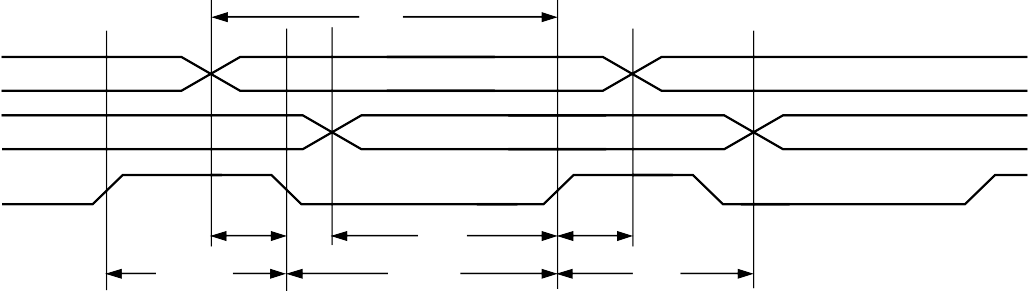
**ADDRESS TO DATA VALID TIME (MAXIMUM)**

**ADDRESS HOLD TIME TO RD SIGNAL INACTIVE (MINIMUM) RD LOW TO OUTPUT VALID (MAXIMUM)**

00636-052

**RD HIGH TO DATA THREE-STATE (MAXIMUM)**

*Figure 52. Parallel Port Read Timing Diagram*

**A<5:0>**

**tWR**

**A1**

**A2**

**A3**

**D1**

**D2**

**D3**

**tASU**

**tAHD**

**tWRHIGH**

**tDSU**

**tWRLOW**

**tDHD**

**D<7:0>**



**WR**

**SPECIFICATION VALUE DESCRIPTION**

**tASU tDSU tADH tDHD**

**8.0ns 3.0ns 0ns 0ns**



**ADDRESS SETUP TIME TO WR SIGNAL ACTIVE DATA SETUP TIME TO WR SIGNAL ACTIVE ADDRESS HOLD TIME TO WR SIGNAL INACTIVE DATA HOLD TIME TO WR SIGNAL INACTIVE**

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**tWRLOW**

**2.5ns WR SIGNAL MINIMUM LOW TIME**

**tWRHIGH**

**tWR**

**7ns 10.5ns**



**WR SIGNAL MINIMUM HIGH TIME MINIMUM WRITE TIME**

*Figure 53. Parallel Port Write Timing Diagram*

**GENERAL OPERATION OF THE SERIAL INTERFACE**

There are two phases of a serial communication cycle with the AD9854. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9854 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9854 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write and the register address to be acted upon.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9854. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9854 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. ([Table 10](#_bookmark49) describes how many bytes must be

**Table 10. Register Address vs. Data Bytes Transferred**

transferred.) The AD9854 internal serial I/O controller expects every byte of the register being accessed to be transferred.

Therefore, the user should write between I/O update clocks.

At the completion of a communication cycle, the AD9854 serial port controller expects the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IO RESET pin immediately terminates the current communication cycle. After IO RESET returns low, the AD9854 serial port controller requires the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9854 is registered on the rising edge of SCLK, and all data is driven out of the AD9854 on the falling edge of SCLK.

[Figure 54](#_bookmark50) and [Figure 55](#_bookmark51) show the general operation of the AD9854 serial port.

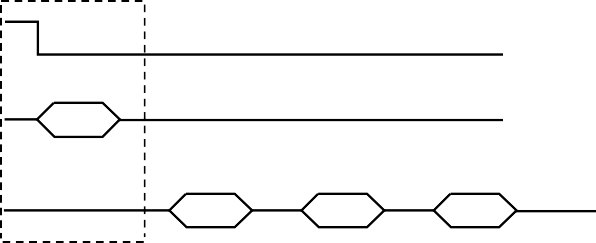
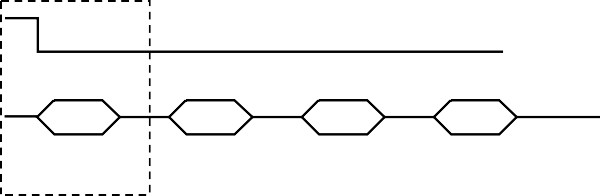
|  |  |  |
| --- | --- | --- |
| **Serial Register Address** | **Register Name** | **Number of Bytes Transferred** |
| 0 | Phase Offset Tuning Word Register 1 | 2 |
| 1 | Phase Offset Tuning Word Register 2 | 2 |
| 2 | Frequency Tuning Word 1 | 6 |
| 3 | Frequency Tuning Word 2 | 6 |
| 4 | Delta frequency register | 6 |
| 5 | Update clock rate register | 4 |
| 6 | Ramp rate clock register | 3 |
| 7 | Control register | 4 |
| 8 | I path digital multiplier register | 2 |
| 9 | Q path digital multiplier register | 2 |
| A | Shaped on/off keying ramp rate register | 1 |
| B | Q DAC register | 2 |



**CS**

**SDIO**

00636-054

*Figure 54. Using SDIO as a Read/Write Transfer*

**INSTRUCTION**

**BYTE DATA BYTE 1 DATA BYTE 2 DATA BYTE 3**

**INSTRUCTION CYCLE**

**DATA TRANSFER**

**INSTRUCTION BYTE**

**INSTRUCTION DATA TRANSFER**

**CYCLE DATA BYTE 1 DATA BYTE 2 DATA BYTE 3**



**CS**

**SDIO**

**SDO**

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**DATA TRANSFER**

*Figure 55. Using SDIO as an Input and SDO as an Output*

**INSTRUCTION BYTE**

The instruction byte contains the following information:

**MSB LSB**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| R/W | X | X | X | A3 | A2 | A1 | A0 |



R/W—Bit 7 determines whether a read or write data transfer occurs following the instruction byte. Logic high indicates read operation. Logic 0 indicates a write operation.

Bit 6, Bit 5, and Bit 4 are dummy bits (don’t care).

A3, A2, A1, A0—Bit 3, Bit 2, Bit 1, and Bit 0 determine which register is accessed during the data transfer portion of the communication cycle (see [Table 8](#_bookmark43) for register address details).

**SERIAL INTERFACE PORT PIN DESCRIPTIONS**

***SCLK***

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9854 and to run the internal state machines. The SCLK maximum frequency is 10 MHz.



***CS***

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communication line. The SDO and SDIO pins go to a high impedance state when this input is high. If this pin is driven high during a communication cycle, the cycle is suspended until CS is reactivated low. The chip select pin can be tied low in systems that maintain control of SCLK.

***SDIO***

Serial Data I/O (Pin 19). Data is always written to the AD9854 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of Register Address 20 hex. The default is Logic 0, which configures the SDIO pin as bidirectional.

***SDO***

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9854 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

***IO RESET***

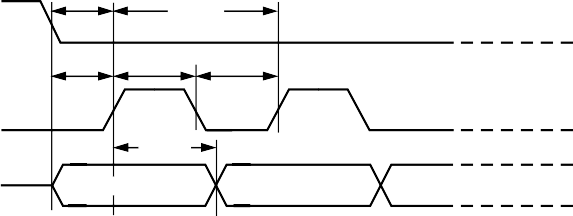
Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the contents of the addressable registers. An active high input on the IO RESET pin causes the current communication cycle to terminate. After the IO RESET pin returns low (Logic 0), another communication cycle can begin, starting with the instruction byte.

**NOTES ON SERIAL PORT OPERATION**

The AD9854 serial port configuration bits reside in Bit 1 and Bit 0 of Register Address 20 hex. It is important to note that the configuration changes immediately upon a valid I/O update.

For multibyte transfers, writing to this register can occur during the middle of a communication cycle. The user must compensate for this new configuration for the remainder of the current com- munication cycle.

The system must maintain synchronization with the AD9854; otherwise, the internal control logic is not able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register and then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle properly write the first two data bytes into the AD9854, but the subsequent eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9854, the IO RESET pin provides a means to re- establish synchronization without reinitializing the entire chip. Asserting the IO RESET pin (active high) resets the AD9854 serial port state machine, terminating the current I/O operation and forcing the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The IO RESET pin must be deasserted (low) before the next instruction byte write can begin. Any information written to the AD9854 registers during a valid communication cycle prior to loss of synchroni- zation remains intact.

**tPRE**

**tSCLK**

**tDSU tSCLKPWH tSCLKPWL**

**tDHLD**

**FIRST BIT**

**SECOND BIT**

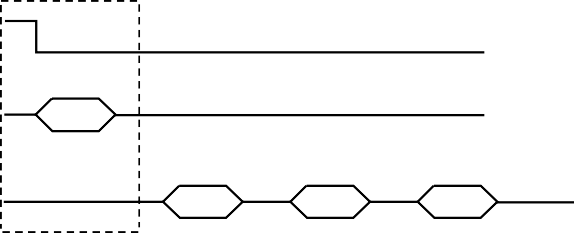


**CS**

**SCLK**

**SDIO**

|  |  |  |
| --- | --- | --- |
|  |  |  |
| **SYMBOL** | **MIN** | **DEFINITION** |
| **tPRE** | **30ns** | **CS SETUP TIME** |
| **tSCLK** | **100ns** | **PERIOD OF SERIAL DATA CLOCK** |
| **tDSU** | **30ns** | **SERIAL DATA SETUP TIME** |
| **tSCLKPWH** | **40ns** | **SERIAL DATA CLOCK PULSE WIDTH HIGH** |
| **tSCLKPW L** | **40ns** | **SERIAL DATA CLOCK PULSE WIDTH LOW** |
| **tDHLD** | **0ns** | **SERIAL DATA HOLD TIME** |

*Figure 56. Timing Diagram for Data Write to AD9854*

**INSTRUCTION BYTE**

**INSTRUCTION DATA TRANSFER**

**CYCLE DATA BYTE 1 DATA BYTE 2 DATA BYTE 3**

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**CS**

**SDIO**

**SDO**

00636-057

**DATA TRANSFER**

*Figure 57. Timing Diagram for Read from AD9854*

**MSB/LSB TRANSFERS**

The AD9854 serial port can support MSB- and LSB-first data formats. This functionality is controlled by Bit 1 of Serial Register Bank 20 hex. When this bit is set active high, the AD9854 serial port is in LSB-first format. This bit defaults low, to the MSB-first format. The instruction byte must be written in the format indicated by Bit 1 of Serial Register Bank 20 hex.

Therefore, if the AD9854 is in LSB-first mode, the instruction byte must be written from least significant bit to most significant bit.

**CONTROL REGISTER DESCRIPTION**

The control register is located in the shaded portion of [Table 8](#_bookmark43) at Address 1D to Address 20 hex. It is composed of 32 bits.

Bit 31 is located at the top left position, and Bit 0 is located in the lower right position of the shaded portion. In the text that follows, the register descriptions have been subdivided to make it easier to locate the text associated with specific control categories.

CR [31:29] are open.

CR [28] is the comparator power-down bit. When this bit is set (Logic 1), its signal indicates to the comparator that a power- down mode is active. This bit is an output of the digital section and is an input to the analog section.

CR [27] must always be written to Logic 0. Writing this bit to Logic 1 causes the AD9854 to stop functioning until a master reset is applied.

CR [26] is the Q DAC power-down bit. When this bit is set (Logic 1), it indicates to the Q DAC that a power-down mode is active.

CR [25] is the full DAC power-down bit. When this bit is set (Logic 1), it indicates to both the I and Q DACs, as well as the reference, that a power-down mode is active.

CR [24] is the digital power-down bit. When this bit is set (Logic 1), its signal indicates to the digital section that a power- down mode is active. Within the digital section, the clocks are forced to dc, effectively powering down the digital section. In this state, the PLL still accepts the REFCLK signal and continues to output the higher frequency.

CR [23] is reserved. Write to 0.

CR [22] is the PLL range bit, which controls the VCO gain. The power-up state of the PLL range bit is Logic 1; a higher gain is required for frequencies greater than 200 MHz.

CR [21] is the bypass PLL bit, active high. When this bit is active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1 with PLL bypassed.

CR [20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

CR [15] is the Clear Accumulator 1 bit. This bit has a one-shot type of function. When this bit is written active (Logic 1), a Clear Accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to 0. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a sawtooth frequency sweep pattern with minimal intervention. This bit is intended for chirp mode only, but its function is still retained in other modes.

CR [14] is the clear accumulator bit. When this bit is active high, it holds both the Accumulator 1 and Accumulator 2 values at 0 for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR [13] is the triangle bit. When this bit is set, the AD9854 automatically performs a continuous frequency sweep from F1 to F2 frequencies and back. This results in a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR [12] is the source Q DAC bit. When this bit is set high, the Q path DAC accepts data from the Q DAC register.

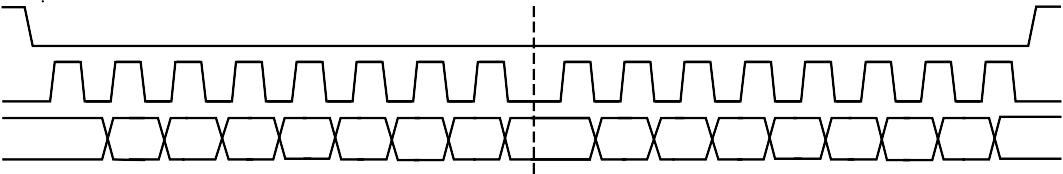
CR [11:9] are the three bits that describe the five operating modes of the AD9854:

0x0 = single-tone mode 0x1 = FSK mode

0x2 = ramped FSK mode 0x3 = chirp mode

0x4 = BPSK mode



**CS**

**INSTRUCTION CYCLE**

**DATA TRANSFER CYCLE**

**I7**

**I6 I5 I4 I3 I2 I1 I0**

**D7 D6**

**D5**

**D4 D3 D2 D1 D0**

**SCLK**

**SDIO**

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*Figure 58. Serial Port Write Timing Clock Stall Low*



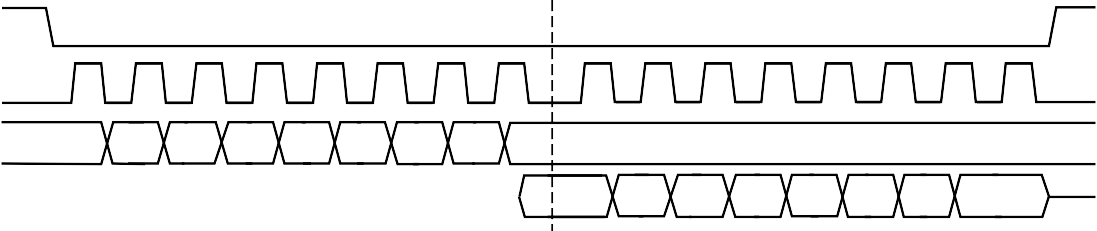
**CS**

**SCLK**

**SDIO**

**SDO**

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*Figure 59. 3-Wire Serial Port Read Timing Clock Stall Low*

**INSTRUCTION CYCLE**

**DATA TRANSFER CYCLE**

**I7**

**I6 I5 I4 I3 I2 I1 I0**

**DON'T CARE**

**DO7**

**DO6 DO5 DO4 DO3 DO2 DO1 DO0**

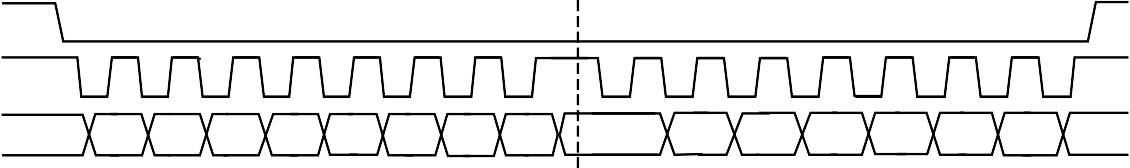


**CS**

**SCLK**

**SDIO**

00636-060

*Figure 60. Serial Port Write Timing Clock Stall High*

**INSTRUCTION CYCLE**

**DATA TRANSFER CYCLE**

**I7 I6 I5 I4 I3 I2 I1 I0**

**D7 D6 D5 D4 D3 D2 D1 D0**

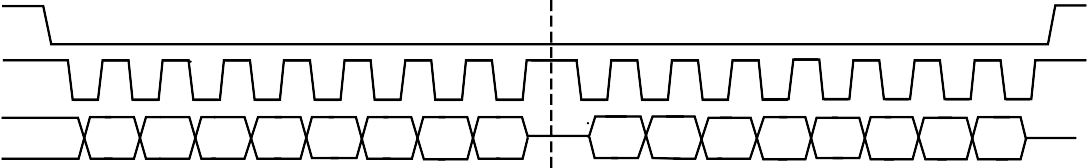


**CS**

**SCLK**

**SDIO**

00636-061

*Figure 61. 2-Wire Serial Port Read Timing Clock Stall High*

**INSTRUCTION CYCLE**

**DATA TRANSFER CYCLE**

**I7 I6 I5 I4 I3 I2 I1 I0**

**DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0**

CR [8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD CLK pin is an output and the AD9854 generates the I/O UD CLK signal. When this bit is set to Logic 0, external I/O UD CLK functionality is performed and the I/O UD CLK pin is configured as an input.

CR [7] is reserved. Write to 0.

CR [6] is the inverse sinc filter bypass bit. When this bit is set, the data from the DDS block goes directly to the output shaped keying logic, and the clock to the inverse sinc filter is stopped. Default is clear with the filter enabled.

CR [5] is the shaped keying enable bit. When this bit is set, the output ramping function is enabled and is performed in accordance with the CR [4] bit requirements.

CR [4] is the internal/external output shaped keying control bit. When this bit is set to Logic 1, the output shaped keying factor is internally generated and applied to both the I and Q paths.

When this bit is cleared (default), the output shaped keying function is externally controlled by the user, and the ouput shaped keying factor is the value of the I and Q output shaped keying factor register. The two registers that are the output shaped keying factors also default low such that the output is off at power-up until the device is programmed by the user.

CR [3:2] are reserved. Write to 0.

CR [1] is the serial port MSB-/LSB-first bit. Default is low, MSB first.

CR [0] is the serial port SDO active bit. Default is low, inactive.

**POWER DISSIPATION AND THERMAL CONSIDERATIONS**

The AD9854 is a multifunctional, high speed device that targets a wide variety of synthesizer and agile clock applications. The numerous innovative features contained in the device each consume incremental power. If enabled in combination, the safe thermal operating conditions of the device may be exceeded.

Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9854. However, in most cases, disabling the inverse sinc filter prevents exceeding the maximum die temperature, because the inverse sinc filter consumes approximately 30% of the total power.

The AD9854 is specified to operate within the industrial tem- perature range of −40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

Many variables contribute to the operating junction temperature within the device, including

* Package style
* Selected mode of operation
* Internal system clock speed
* Supply voltage
* Ambient temperature

The combination of these variables determines the junction temperature within the AD9854 for a given set of operating conditions.

The AD9854 is available in two package styles: a thermally enhanced surface-mount package with an exposed heat sink and a standard (nonthermally enhanced) surface-mount package. The

thermal impedance of these packages is 16.2°C/W and 38°C/W, respectively, measured under still air conditions.

**THERMAL IMPEDANCE**

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance is determined by the package material and the physical dimensions of the package. The dissipation of the heat from the package is directly dependent on the ambient air conditions and the physical connection made between the IC package and the PCB.

Adequate dissipation of heat from the AD9854 relies on all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9854ASVZ has an exposed paddle on the bottom of the package that must be soldered to a large copper plane, which, for convenience, can be the ground plane. Sockets for either package style of the device are not recommended.

**JUNCTION TEMPERATURE CONSIDERATIONS**

The power dissipation (PDISS) of the AD9854 in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with PDISS, such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device and its effect on the junction temperature must be considered when using the device. The junction temperature of the device is given by

(*Thermal Impedance × Power Consumption*) +

*Ambient Temperature*

The maximum ambient temperature combined with the maximum junction temperature establishes the following power consumption limits for each package: 4.06 W for ASVZ models and 1.71 W for ASTZ models.

***Supply Voltage***

The supply voltage affects power dissipation and junction temperature because *PDISS* = *V* × *I*. Users should design for 3.3 V nominal; however, the device is guaranteed to meet specifications over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

***Clock Speed***

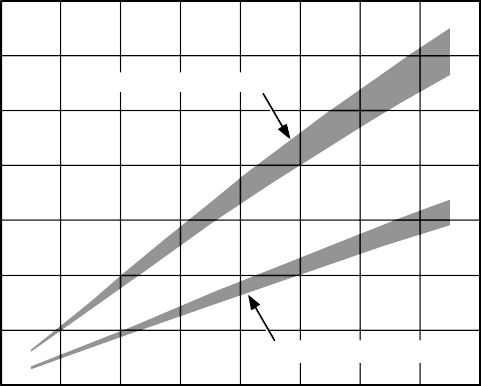
Clock speed directly and linearly influences the total power dissipation of the device and therefore the junction temperature. As a rule, to minimize power dissipation, the user should select the lowest possible internal clock speed to support a given application. Typically, the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to ensure that the requirements of the output low-pass filter are reasonable. For a typical DDS application, the system clock frequency should be 2.5 times the highest desired output frequency.

***Mode of Operation***

The selected mode of operation of the AD9854 significantly influences the total power consumption. Although the AD9854 offers many features targeting a wide variety of applications, the device is designed to operate with only a few features enabled at once for a given application. If multiple features are enabled at higher clock speeds, the maximum junction temperature of the die may be exceeded, severely limiting the long-term reliability of the device. [Figure 62](#_bookmark57) and [Figure 63](#_bookmark58) show the power requirements associated with each feature of the AD9854. These graphs should be used as a guide in determining power consumption for specific feature sets.

[Figure 62](#_bookmark57) shows the supply current consumed by the AD9854 over a range of frequencies for two possible configurations. All circuits enabled means that the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are enabled. Basic configuration means that the output scaling

multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are disabled.

**1400**

**ALL CIRCUITS ENABLED**

**BASIC CONFIGURATION**

**1200**

**1000**

**SUPPLY CURRENT (mA)**

**800**

**600**

**400**

**200**

**EVALUATION OF OPERATING CONDITIONS**

The first step in applying the AD9854 is to select the internal clock frequency. Clock frequency selections greater than

200 MHz require the use of the thermally enhanced package (AD9854ASVZ); other clock frequencies may allow the use of the standard plastic surface-mount package, but more information is needed to make that determination.

The second evaluation step is to determine the maximum required operating temperature for the AD9854 in a given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9854. For the extended industrial temperature range, the maximum operating temperature is 85°C, which results in a difference of

**0**

**20**

**NOTES**

**60 100 140 180 220 260 300**

**FREQUENCY (MHz)**

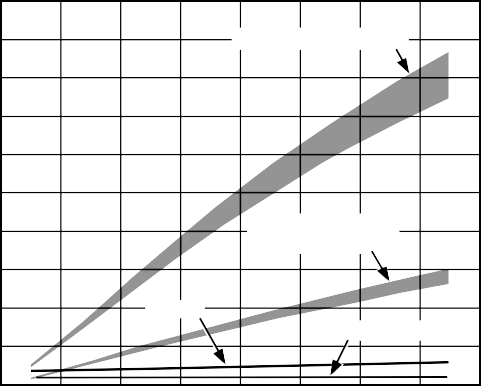
65°C. This is the maximum temperature gradient that the device can experience due to power dissipation.

**THIS GRAPH ASSUMES THAT THE AD9854 DEVICE IS SOLDERED TO A MULTILAYER PCB PER THE RECOMMENDED BEST MANUFACTURING PRACTICES AND PROCEDURES FOR THE GIVEN PACKAGE TYPE.**

00636-062

*Figure 62. Current Consumption vs. Clock Frequency*

[Figure 63](#_bookmark58) shows the approximate current consumed by each of four functions.

**500**

**INVERSE SINC FILTER**

**OUTPUT SCALING MULTIPLIERS**

**Q DAC**

**COMPARATOR**

**450**

**400**

**350**

**SUPPLY CURRENT (mA)**

**300**

**250**

**200**

**150**

**100**

**50**

**0**

**20 60 100 140 180 220 260 300**

**FREQUENCY (MHz)**

**NOTES**

**THIS GRAPH ASSUMES THAT THE AD9854 DEVICE IS SOLDERED TO A MULTILAYER PCB PER THE RECOMMENDED BEST MANUFACTURING PRACTICES AND PROCEDURES FOR THE GIVEN PACKAGE TYPE.**

00636-063

*Figure 63. Current Consumption by Function vs. Clock Frequency*

The third evaluation step is to divide the maximum temper- ature gradient by the thermal impedance to determine the maximum power dissipation allowed for the application.

For example, 65°C divided by the thermal impedance of the package being used yields the total power dissipation limit (4.06 W for the ASVZ models and 1.71 W for the ASTZ models).

Therefore, for a 3.3 V nominal power supply voltage, the current consumed by the device with full operating conditions must not exceed 515 mA for the standard plastic package and 1242 mA for the thermally enhanced package. The total set of enabled functions and operating conditions of the AD9854 application must support these current consumption limits.

To determine the suitability of a given AD9854 application in terms of the power dissipation requirements use [Figure 62](#_bookmark57)

and [Figure 63](#_bookmark58). These graphs assume that the AD9854 device is soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications are achieved.

**THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES**

Refer to the [AN-772 Application Note](http://www.analog.com/AN-772) for details on mounting devices with an exposed paddle.

**EVALUATION BOARD**

An evaluation board package is available for the AD9854 DDS device. This package consists of a PCB, software, and documentation to facilitate bench analysis of the device’s performance. To ensure optimum dynamic performance from the device, users should familiarize themselves with the operation and performance capabilities of the AD9854 with the evaluation board and use the evaluation board as a PCB reference design.

**EVALUATION BOARD INSTRUCTIONS**

The AD9852/AD9854 Revision E evaluation board includes either an AD9852ASVZ or AD9854ASVZ IC.

The ASVZ package permits 300 MHz operation by virtue of its thermally enhanced design. This package has a bottom-side heat slug that must be soldered to the ground plane of the PCB directly beneath the IC. In this manner, the evaluation board PCB ground plane layer extracts heat from the AD9852 or AD9854 IC package. If device operation is limited to 200 MHz or less, the ASTZ package can be used without a heat slug in customer installations over the full temperature range.

Evaluation boards for both the AD9852 and AD9854 are identical except for the installed IC.

To assist in proper placement of the pin header shorting jumpers, the instructions refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin 1 for each 3-pin header is marked on the PCB corresponding with the

schematic diagram. When following these instructions, position the PCB so that the PCB text can be read from left to right. The board is shipped with the pin headers configuring the board as follows:

* REFCLK for the AD9852 or AD9854 is configured as differential. The differential clock signals are provided by the MC100LVEL16D differential receiver.
* The input clock for the MC100LVEL16D is single ended via J25. This signal may be 3.3 V CMOS or a 2 V p-p sine wave capable of driving 50 Ω (R13).
* Both DAC outputs from the AD9852 or AD9854 are routed through the two 120 MHz elliptical LP filters, and their outputs are connected to J7 (Q, or control DAC) and J6 (I, or cosine DAC).
* The board is set up for software control via the printer port connector.
* The output currents of the DAC are configured for 10 mA.

**GENERAL OPERATING INSTRUCTIONS**

Load the CD software onto your PC’s hard disk. The current software (Version 1.72) supports Windows® 95, Windows 98, Windows 2000, Windows NT®, and Windows XP.

Connect a printer cable from the PC to the AD9854 evaluation board printer port connector labeled J11.

***Hardware Preparation***

Use the schematics (see [Figure 64](#_bookmark65) and [Figure 65](#_bookmark66)) in conjunction with these instructions to become acquainted with the electrical functioning of the evaluation board.

Attach power wires to the connector labeled TB1 using the screw-down terminals. This connector is plastic and press-fits over a 4-pin header soldered to the board. [Table 11](#_bookmark60) lists the connections to each pin.

**Table 11. Power Requirements for DUT Pins**[**1**](#_bookmark61)

|  |  |  |  |
| --- | --- | --- | --- |
| **AVDD 3.3 V** | **DVDD 3.3 V** | **VCC 3.3 V** | **Ground** |
| For all DUT analog pins | For all DUT digital pins | For all other devices | For all devices |

1 DUT = device under test.

***Clock Input, J25***

Attach REFCLK to the clock input, J25. This is a single-ended input that is routed to the MC100LVEL16D for conversion to differential PECL output. This is accomplished by attaching a 2 V p-p clock or sine wave source to J25. Note that this is a 50 Ω impedance point set by R13. The input signal is ac-coupled and then biased to the center-switching threshold of the MC100LVEL16D. To engage the differential clocking mode of the AD9854, Pin 2 and Pin 3 (the bottom two pins) of W3 must be connected with a shorting jumper.

The signal arriving at the AD9854 is called the reference clock. When engaging the on-chip PLL clock multiplier, this signal is the reference clock for the PLL and the multiplied PLL output becomes the system clock. If the PLL clock multiplier is to be bypassed, the reference clock supplied by the user directly operates the AD9854 and is therefore the system clock.

***Three-State Control***

The W9, W11, W12, W13, W14, and W15 switch headers must be shorted to allow the provided software to control the AD9854 evaluation board via the printer port connector, J11.

***Programming***

If programming of the AD9854 is not to be provided by the user’s PC and Analog Devices software, the W9, W11, W12, W13, W14, and W15 headers should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows J10 (the 40-pin header) and J1 to assume control without bus contention. Input signals on J10 and J1 going to the AD9854 should be 3.3 V CMOS logic levels.

***Low-Pass Filter Testing***

The purpose of the 2-pin W7 and W10 headers (associated with J4 and J5) is to allow the two 50 Ω, 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. Typically, a shorting jumper is

attached to each header to allow the DAC signals to be routed to the filters. If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50 Ω test signals should be applied at the J4 and J5 inputs to the 50 Ω elliptic filters. Users should refer to the schematic provided and to the following sections to properly position the remaining shorting jumpers.

***Observing the Unfiltered IOUT1 and the Unfiltered IOUT2 DAC Signals***

The unfiltered DAC outputs can be observed at J5 (the I, or cosine DAC, signal) and J4 (the Q, or control DAC, signal). Use the following procedure to route the two 50 Ω terminated analog DAC outputs to the SMB connectors and to disconnect any other circuitry:

1. Install shorting jumpers at W7 and W10.
2. Remove the shorting jumper at W16.
3. Remove the shorting jumper from the 3-pin W1 header.
4. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W4 header.

The raw DAC outputs may appear as a series of quantized (stepped) output levels that may not resemble a sine wave until they are filtered. The default 10 mA output current develops a

0.5 V p-p signal across the on-board 50 Ω termination. If the observation equipment offers 50 Ω inputs, the DAC develops only 0.25 V p-p due to the double termination.

If using the AD9852 evaluation board, the user can control IOUT2 (the control DAC output) by using the serial or parallel ports. The 12-bit, twos complement value(s) is/are written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum), with all 0s being midscale. Rapidly changing the contents of the control DAC register (up to 100 MSPS) allows IOUT2 to assume any waveform that can be programmed.

***Observing the Filtered IOUT1 and the Filtered IOUT2***

The filtered I (cosine DAC) and Q (control DAC) outputs can be observed at J6 (for the I signal) and J7 (for the Q signal). Use the following procedure to route the 50 Ω (input and output Z) low-pass filters into the pathways of the I and Q signals to remove images, aliased harmonics, and other spurious signals that are greater than approximately 120 MHz:

1. Install shorting jumpers at W7 and W10.
2. Install a shorting jumper at W16.
3. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W1 header.
4. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W4 header.
5. Install a shorting jumper on Pin 2 and Pin 3 (bottom two pins) of the 3-pin W2 and W8 headers.

The resulting I and Q signals appear as nearly pure sine waves and 90° out of phase with each other. These filters are designed with the assumption that the system clock speed is at or near its maximum speed (300 MHz). If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible, or inevitable, that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

If the AD9852 evaluation board is used, any reference to the Q signal should be interpreted as meaning the control DAC.



***Observing the Filtered IOUT1 and the Filtered IOUT1***

The filtered I DAC outputs can be observed at J6 (the true signal) and J7 (the complementary signal). Use the following procedure to route the 120 MHz low-pass filters in the true and complementary output paths of the I DAC to remove images, aliased harmonics, and other spurious signals that are greater than approximately 120 MHz:

1. Install shorting jumpers at W7 and W10.
2. Install a shorting jumper at W16.
3. Install a shorting jumper on Pin 2 and Pin 3 (top two pins) of the 3-pin W1 header.
4. Install a shorting jumper on Pin 2 and Pin 3 (top two pins) of the 3-pin W4 header.
5. Install a shorting jumper on Pin 2 and Pin 3 (bottom two pins) of the 3-pin W2 and W8 headers.

The resulting signals appear as nearly pure sine waves and 180° out of phase with each other. If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible, or inevitable, that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

***Connecting the High Speed Comparator***

To connect the high speed comparator to the DAC output signals use either the quadrature filtered output configuration (for AD9854 only) or the complementary filtered output configuration outlined in the previous section (for both the AD9854 and the AD9852). Follow Step 1 through Step 4 in either the [Observing the Filtered IOUT1 and the Filtered](#_bookmark63) [IOUT2](#_bookmark63) section or the [Observing the Filtered IOUT1 and the](#_bookmark62) [Filtered](#_bookmark62) IOUT1 section. Then install a shorting jumper on Pin 1 and Pin 2 (top two pins) of the 3-pin W2 and W8 headers. This reroutes the filtered signals away from the output connectors (J6 and J7) and to the 100 Ω configured comparator inputs.

This sets up the comparator for differential input without affecting the comparator output duty cycle, which should be approximately 50% in this configuration.

The user can change the value of RSET Resistor R2 from 3.9 kΩ to 1.95 kΩ to receive more robust signals at the comparator

inputs. This decreases jitter and extends the operating range of the comparator. To implement this change install a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with that provided by R2. This boosts the DAC

output current from 10 mA to 20 mA and doubles the peak-to- peak output voltage developed across the loads, thus resulting in more robust signals at the comparator inputs.

***Single-Ended Configuration***

To connect the high speed comparator in a single-ended configuration so that the duty cycle or pulse width can be controlled, a dc threshold voltage must be present at one of the comparator inputs. The user can supply this voltage using the control DAC. A 12-bit, twos complement value is written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum), with all 0s being midscale. The IOUT1 channel continues to output a filtered sine wave programmed by the user. These two signals are routed to the comparator by using the 3-pin W2 and W8 header switches. Use of the configuration described in the [Observing the Filtered IOUT1 and the Filtered](#_bookmark63) [IOUT2](#_bookmark63) section is required. Follow Step 1 through Step 4 in this section, and then install a shorting jumper on Pin 1 and Pin 2 (top two pins) of the 3-pin W2 and W8 headers.

The user can change the value of RSET Resistor R2 from 3.9 kΩ to 1.95 kΩ to receive more robust signals at the comparator inputs. This decreases jitter and extends the operating range of the comparator. To implement this change install a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with that provided by R2.

**USING THE PROVIDED SOFTWARE**

The evaluation software is provided on a CD, along with a brief set of instructions. Use the instructions in conjunction with the AD9852 or AD9854 data sheet and the AD9852 or AD9854 evaluation board schematic.

The CD contains the following:

* The AD9852/AD9854 evaluation software
* AD9854 evaluation board instructions
* AD9854 data sheet
* AD9854 evaluation board schematics
* AD9854 PCB layout

Several numerical entries, such as frequency and phase infor- mation, require pressing **Enter** to register the information. For example, if a new frequency is input but does not take effect when **Load** is clicked, the user probably neglected to press **Enter** after typing the new frequency information.

Normal operation of the AD9852/AD9854 evaluation board begins with a master reset. After this reset, many of the default register values are depicted in the software control panel. The reset command sets the DDS output amplitude to minimum and 0 Hz, zero phase offset, as well as other states that are listed in the Register Layout table ([Table 8](#_bookmark43) for AD9854).

The next programming block should be the reference clock and multiplier because this information is used to determine the proper 48-bit frequency tuning words that are entered and later calculated.

The output amplitude defaults to the 12-bit, straight binary multiplier values of the I (cosine DAC) multiplier register of 000 hex; no output (dc) should be seen from the DAC. Set the

multiplier amplitude in the **Output Amplitude** dialog box to a substantial value, such as FFF hex. The digital multiplier can be bypassed by selecting **Output Amplitude is always Full Scale,** but this usually does not result in the best spurious-free dynamic range (SFDR). The best SFDR, achieving improvements of up to 11 dB, is obtained by routing the signal through the digital multiplier and then reducing the multiplier amplitude. For instance, FC0 hex produces less spurious signal amplitude than FFF hex. If SFDR must be maximized, this exploitable and repeatable phenomenon should be investigated in the given application. This phenomenon is more readily observed at higher output frequencies, where good SFDR becomes more difficult to achieve.

Refer to this data sheet and the evaluation board schematic to understand the available functions of the AD9854 and how the software responds to programming commands.

**SUPPORT**

Applications assistance is available for the AD9854, the AD9854 PCB evaluation board, and all other Analog Devices products. Call 1-800-ANALOGD or visit [www.analog.com/dds](http://www.analog.com/dds).

**Table 12. AD9854 Customer Evaluation Board (AD9854 PCB > U1 = AD9854ASVZ)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Qty** | **Reference Designator** | **Device** | **Package** | **Value** | **Min Tol** | **Manufacturer** | **Manufacturer Part No.** |
| 1 | 3 | C1, C2, C45 | Capacitor 0805 | 805 | 0.01 μF, | 10% | Kemet Corp. | C0805C103K5RACTU |
|  |  |  |  |  | 50 V, X7R |  |  |  |
| 2 | 21 | C7, C8, C9, C10, | Capacitor 0603 | 603 | 0.1 μF, | 10% | Murata | GRM188R71H104KA93D |
|  |  | C11, C12, C13, |  |  | 50 V, X7R |  | Manufacturing |  |
|  |  | C14, C16, C17, |  |  |  |  | Co., Ltd. |  |
|  |  | C18, C19, C20, |  |  |  |  |  |  |
|  |  | C22, C23, C24, |  |  |  |  |  |  |
|  |  | C26, C27, C28, |  |  |  |  |  |  |
|  |  | C29, C44 |  |  |  |  |  |  |
| 3 | 2 | C4, C37 | Capacitor 1206 | 1206 | 27 pF, | 5% | Yageo Corporation | CC1206JRNPO9BN270 |
|  |  |  |  |  | 50 V, NPO |  |  |  |
| 4 | 2 | C5, C38 | Capacitor 1206 | 1206 | 47 pF, | 5% | Yageo Corporation | CC1206JRNPO9BN470 |
|  |  |  |  |  | 50 V, NPO |  |  |  |
| 5 | 3 | C6, C21, C25 | Capacitor TAJC | TAJC | 10 μF, | 10% | AVX | TAJC106K016R |
|  |  |  |  |  | 16 V, TAJ |  |  |  |
| 6 | 2 | C30, C39 | Capacitor 1206 | 1206 | 39 pF, | 5% | Yageo Corporation | CC1206JRNPO9BN390 |
|  |  |  |  |  | 50 V, NPO |  |  |  |
| 7 | 2 | C31, C40 | Capacitor 1206 | 1206 | 22 pF, | 5% | Yageo Corporation | CC1206JRNPO9BN220 |
|  |  |  |  |  | 50 V, NPO |  |  |  |
| 8 | 2 | C32, C41 | Capacitor 1206 | 1206 | 2.2 pF, | 0.25 | Yageo Corporation | CC1206CRNPO9BN2R2 |
|  |  |  |  |  | 50 V, NPO | pF |  |  |
| 9 | 2 | C33, C42 | Capacitor 1206 | 1206 | 12 pF, | 5% | Yageo Corporation | 1206CG120J9B200 |
|  |  |  |  |  | 50 V, NPO |  |  |  |
| 10 | 2 | C34, C43 | Capacitor 1206 | 1206 | 8.2 pF, | 0.5 | Yageo Corporation | CC1206DRNPO9BN8R2 |
|  |  |  |  |  | 50 V, NPO | pF |  |  |
| 11 | 9 | J1, J2, J3, J4, J5, | SMB | STR-PC MNT | N/A | N/A | Emerson/Johnson | 131-3701-261 |
|  |  | J6, J7, J25, J26 |  |  |  |  |  |  |
| 12 | 1 | J10 | 40-pin header | Header 40 | N/A | N/A | Samtec, Inc. | TSW-120-23-L-D |
| 13 | 4 | L1, L2, L3, L5 | Inductor coil | 1008CS | 68 nH | 2% | Coilcraft, Inc. | 1008CS-680XGLB |
| 14 | 2 | L4, L6 | Inductor coil | 1008CS | 82 nH | 2% | Coilcraft, Inc. | 1008CS-820XGLB |
| 15 | 2 | R1, R5 | RES\_SM | 1206 | 49.9 Ω, | 1% | Panasonic-ECG | ERJ-8ENF49R9V |
|  |  |  |  |  | ¼ W |  |  |  |
| 16 | 2 | R2, R20 | RES\_SM | 1206 | 3.92 kΩ, | 1% | Panasonic-ECG | ERJ-8ENF3921V |
|  |  |  |  |  | ¼ W |  |  |  |
| 17 | 2 | R3, R7 | RES\_SM | 1206 | 24.9 Ω, | 1% | Panasonic-ECG | ERJ-8ENF24R9 |
|  |  |  |  |  | ¼ W |  |  |  |
| 18 | 1 | R4 | RES\_SM | 1206 | 1.3 kΩ, | 1% | Panasonic-ECG | ERJ-8ENF1301V |
|  |  |  |  |  | ¼ W |  |  |  |
| 19 | 4 | R6, R11, | RES\_SM | 1206 | 49.9 Ω, | 1% | Panasonic-ECG | ERJ-8ENF49R9V |
|  |  | R12, R13 |  |  | ¼ W |  |  |  |
| 20 | 1 | R8 | RES\_SM | 1206 | 2 kΩ, | 1% | Panasonic-ECG | ERJ-8ENF2001V |
|  |  |  |  |  | ¼ W |  |  |  |
| 21 | 2 | R9, R10 | RES\_SM | 1206 | 100 Ω, | 1% | Panasonic-ECG | ERJ-8ENF1000V |
|  |  |  |  |  | ¼ W |  |  |  |
| 22 | 4 | R15, R16, | RES\_SM | 1206 | 10 kΩ, | 1% | Panasonic-ECG | ERJ-8ENF1002V |
|  |  | R17, R18 |  |  | ¼ W |  |  |  |
| 23 | 1 | RP1 | Resistor | SIP-10P | 10 kΩ | 2% | Bourns | 4610X-101-103LF |
|  |  |  | network |  |  |  |  |  |
| 24 | 1 | TB1 | TB4 | 4-position | N/A | N/A | Wieland Electric, Inc. | Plug: 25.602.2453.0; |
|  |  |  |  | terminal |  |  |  | terminal strip: Z5.530.3425.0 |
| 25 | 1 | U1 | AD9854 | SV-80 | N/A | N/A | Analog Devices, Inc. | AD9854ASVZ |
| 26 | 1 | U2 | 74HC125D | 14 SOIC | N/A | N/A | Texas Instruments | SN74HC125DR |
|  |  |  |  |  |  |  | Incorporated |  |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Qty** | **Reference Designator** | **Device** | **Package** | **Value** | **Min Tol** | **Manufacturer** | **Manufacturer Part No.** |
| 27 | 1 | U3 | Primary | 8 SOIC | N/A | N/A | ON Semiconductor | Primary: MC10EP16DGOS |
|  |  |  | Secondary | 8 SOIC | N/A | N/A | ON Semiconductor | Secondary: |
|  |  |  |  |  |  |  |  | MC100LVEL16DGOS |
| 28 | 4 | U4, U5, U6, U7 | 74HC14 | 14 SOIC | N/A | N/A | Texas Instruments | SN74HC14DR |
|  |  |  |  |  |  |  | Incorporated |  |
| 29 | 3 | U8, U9, U10 | 74HC574 | 20 SOIC | N/A | N/A | Texas Instruments | SN74HC574DWR |
|  |  |  |  |  |  |  | Incorporated |  |
| 30 | 1 | J11 | C36CRPX | 36CRP | N/A | N/A | Tyco Electronics | 5552742-1 |
|  |  |  |  |  |  |  | Corporation |  |
| 31 | 6 | W1, W2, W3, W4, | 3-pin header | SIP-3P | N/A | N/A | Samtec, Inc. | TSW-103-07-S-S |
|  |  | W8, W17 |  |  |  |  |  |  |
| 32 | 10 | W6, W7, W9, | 2-pin header | SIP-2P | N/A | N/A | Samtec, Inc. | TSW-102-07-S-S |
|  |  | W10, W11, W12, |  |  |  |  |  |  |
|  |  | W13, W14, W15, |  |  |  |  |  |  |
|  |  | W16 |  |  |  |  |  |  |
| 33 | 6 | W1, W2, W3, W4, | Jumpers | N/A | Black | N/A | Samtec, Inc. | SNT-100-BK-G |
|  |  | W8, W17 |  |  |  |  |  |  |
| 34 | 10 | W6, W7, W9, | Jumpers | N/A | Black | N/A | Samtec, Inc. | SNT-100-BK-G |
|  |  | W10, W11, W12, |  |  |  |  |  |  |
|  |  | W13, W14, W15, |  |  |  |  |  |  |
|  |  | W16 |  |  |  |  |  |  |
| 35 | 2 | N/A | Self-tapping | 4–40, Phillips | N/A | N/A |  | 90410A107 |
|  |  |  | screw | pan head |  |  |  |  |
| 36 | 4 | N/A | Adhesive feet | N/A | Black | N/A | 3M | SJ-5518 |
| 37 | 1 | AD9852/54 PCB | N/A | N/A | N/A | N/A |  | GS02669 REV. E |
| 38 | 2 | R14, R19 | RES\_SM | 1206 | 0 Ω, | 5% | Panasonic-ECG | ERJ-8GEY0R00V |
|  |  |  |  |  | ¼ W |  |  |  |
| 39 | 4 | N/A | Pin socket |  |  |  | Tyco Electronics | 5-5330808-6 |
|  |  |  | (open end) |  |  |  | Corporation |  |
| 40 | 1 | Y1 | XTAL | COSC | N/A | N/A | Optional | Optional |

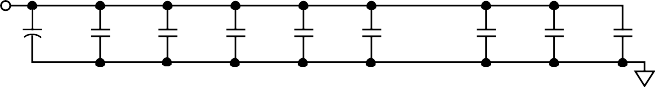
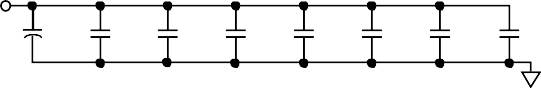
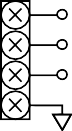
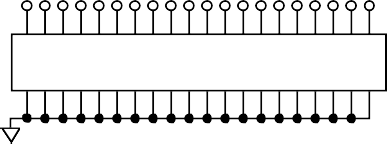
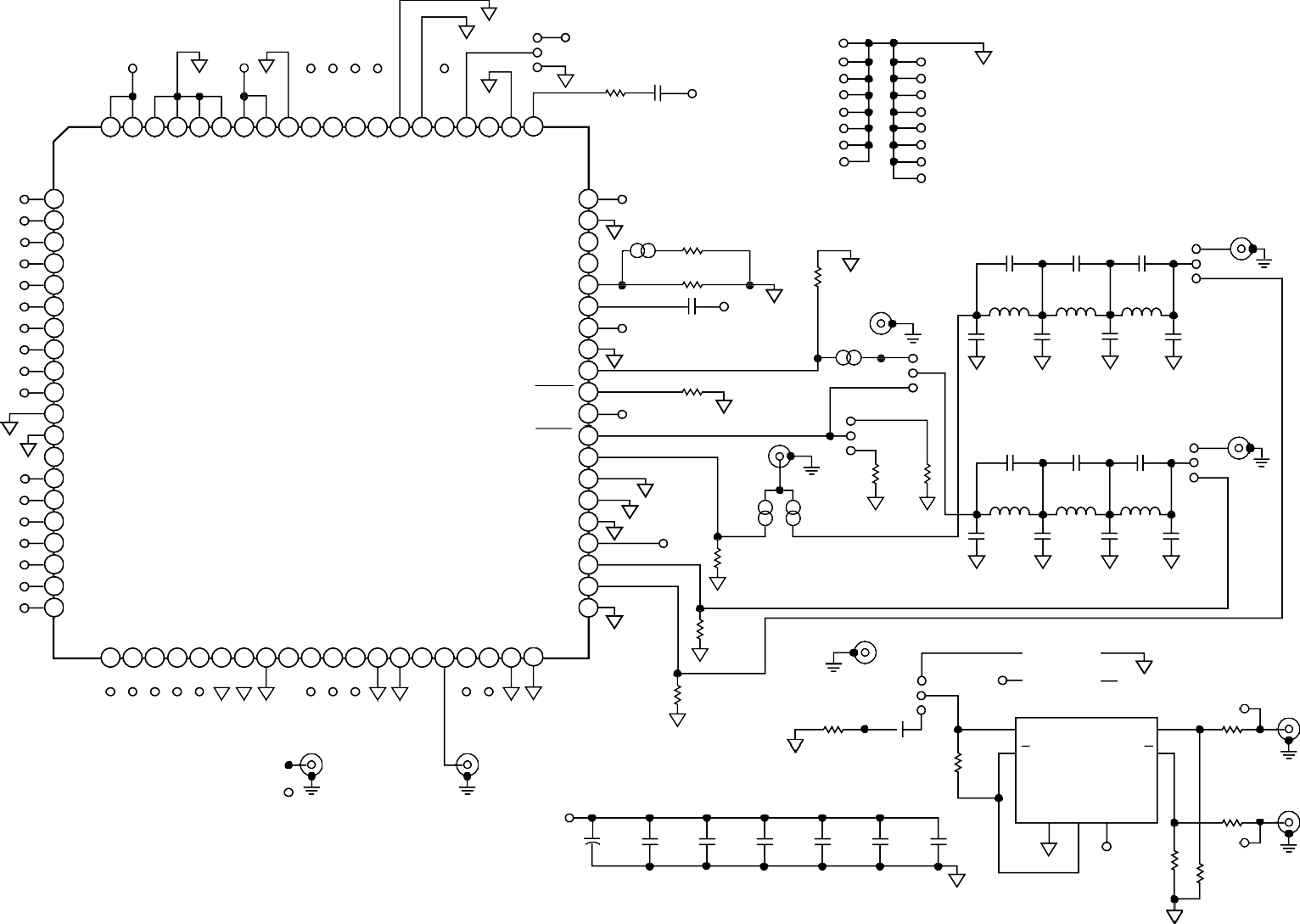
**GND**

**DVDD**

**GND**

**DVDD**

**GND GND**

**W3**

**RESET PMODE CLK**

**CLK8**

**AVDD**

**1**

**GND**

**DVDD GND**

**R4 C1**

**AVDD**

**J15**

**J16 J17 J18 J19**

**J8 J6 J11 J12**

**GND**

**80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61**

**DVDD9 DVDD8 DGND9 DGND8 DGND7 DGND6 DVDD7 DVDD6 OPTGND MRESET SPSELECT REFCLK REFCLK GND4 CLKGND CLKVDD DIFFCLKEN**

**NC5**

**GND3 PLLFLT**

**1.3kΩ 0.01µF**

**J20 J22 J24**

**J13**

**J14 J21 J23**

**D7 1 D7**

**PLLVDD 60**

**AVDD**

**120MHz LOW-PASS FILTER**

**D6 2 D6**

**D5 3 D5**

**PLLGND 59**

**NC4 58**

**GND**

**R20 3.92kΩ**

**C32 2.2pF**

**C33 12pF**

**C34 J6**

**8.2pF**

**D4 4 D4**

**D3 5 D3**

**D2 6 D2**

**NC3 57**

**RSET 56**

**DACBYPASS 55**

**W6 R2**

**3.92kΩ**

**AVDD**

**R1**

**49.9Ω GND**

**GND**

**J4**

**L4 82nH**

**L5 68nH**

**W2**

**L2 1**

**68nH**

**GND**

**D1 7 D1**

**D0 8 D0**

**U1**

**AD9854**

**AVDD2 54**

**AGND2 53**

**AVDD C45**

**0.01µF**

**GND**

**W7 GND**

**1**

**C4 27pF**

**C5 47pF**

**C30 39pF**

**C31 22pF**

**DVDD DVDD**

*Figure 64. Evaluation Board Schematic*

1. **DVDD1**
2. **DVDD2**
3. **DGND1**

**TOP VIEW**

**(Not to Scale)**

**IOUT2 52**

**IOUT2 51**

**AVDD 50**

**AVDD R3**

**GND**

**W1 GND GND GND GND**

**120MHz LOW-PASS FILTER**

**GND**

**GND**

**A5**

1. **DGND2**
2. **NC**
3. **ADDR5**

**IOUT1 49**

**IOUT1 48**

**AGND 47**

**24.9Ω**

**W4**

**J5 1**

**R7 R6**

**GND**

**C41 2.2pF**

**L6**

**C42 12pF**

**L3**

**C43 8.2pF**

**L1**

**J7**

**W8**

**1 GND**

**A4 15 ADDR4**

**GND2 46**

**GND GND**

**W10**

**24.9Ω**

**W16**

**49.9Ω**

**82nH**

**68nH**

**68nH**

**A3**

**A2/IO RESET**

**A1/SDO A0/SDIO**

1. **ADDR3**
2. **ADDR2**

**WR RD DVDD3 DVDD4 DVDD5**

**DGND3 DGND4 DGND5**

**FSK/BPSK/HOLD OSK**

**DACDVDD DACDVDD2 DACDGND DACDGND2 NC2**

**VOUT COUTVDD COUTVDD2 COUTGND**

**COUTGND2**

1. **ADDR1**
2. **ADDR0**

**COMPGND 45**

**COMPVDD 44**

**VINN 43**

**VINP 42**

**GND**

**AVDD**

**R5 49.9Ω**

**GND**

**GND**

**C37 27pF**

**GND**

**C38 47pF**

**GND**

**C39 39pF**

**GND**

**C40 22pF**

**GND**

**I/O UD CLK**

1. **UPDCLK**

**21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40**

**GND 41**

**GND**

**GND**

**R9 100Ω GND**

**J25 Y1**

**8 7**

**OUT GND**

**3.3V NC**

**NC = NO CONNECT**

**WR/SCLK RD/CS DVDD DVDD DVDD GND GND**

**GND**

**OSK AVDD AVDD GND**

**GND**

**AVDD AVDD GND**

**GND**

**R10 100Ω**

**GND**

**W17**

**1 DVDD 14**

**2**

**1**

**GND**

**U3**

**7**

**Q**

**Q**

**D**

**D**

**CLKB J3**

**FDATA**

**D7 D6 D5 D4 D3 D2 D1 D0 ADR5 ADR4 ADR3 ADR2 ADR1 ADR0**

**UDCLK WR**

**RD PMODE OSK RESET**

**J1 GND**

**J26 GND**

**DVDD**

**C25**

**C24**

**GND**

**C23**

**C22**

**R13 GND 49.9Ω**

**C27 C8**

**C2 0.01µF**

**C44**

**3**

**R8**

**2kΩ**

**5 4 8**

**VEE**

**6 R19**

**0Ω**

**MC100LVEL16DGOS**

**R14 0Ω**

**VBB**

**VCC**

**CLK**

**GND J2**

**J10**

**TB1**

**20**

**19**

**18**

**17**

**16**

**15**

**14**

**13**

**12**

**11**

**10**

**9**

**8**

**7**

**6**

**5**

**4**

**3**

**2**

**1**

**40**

**39**

**38**

**37**

**36**

**35**

**34**

**33**

**32**

**31**

**30**

**29**

**28**

**27**

**26**

**25**

**24**

**23**

**22**

**21**

**VCC**

**C21**

**10µF**

**C20**

**0.1µF**

**C19**

**0.1µF**

**C18**

**0.1µF**

**C17**

**0.1µF**

**C16**

**0.1µF**

**C14**

**0.1µF**

**C26**

**GND C28**

**GND**

**DVDD**

**R11**

**49.9Ω R12**

**49.9Ω**

**GND**

1. **AVDD**
2. **DVDD**

**10µF**

**0.1µF**

**0.1µF**

**0.1µF**

**0.1µF**

**0.1µF**

**0.1µF**

**0.1µF**

**0.1µF**

**GND**

**GND**

**GND**

1. **VCC 4**

**GND**

**AVDD**

**C6 10µF**

**C7 C29**

**0.1µF 0.1µF**

**C9 C10**

**0.1µF 0.1µF**

**C11 0.1µF**

**C12 0.1µF**

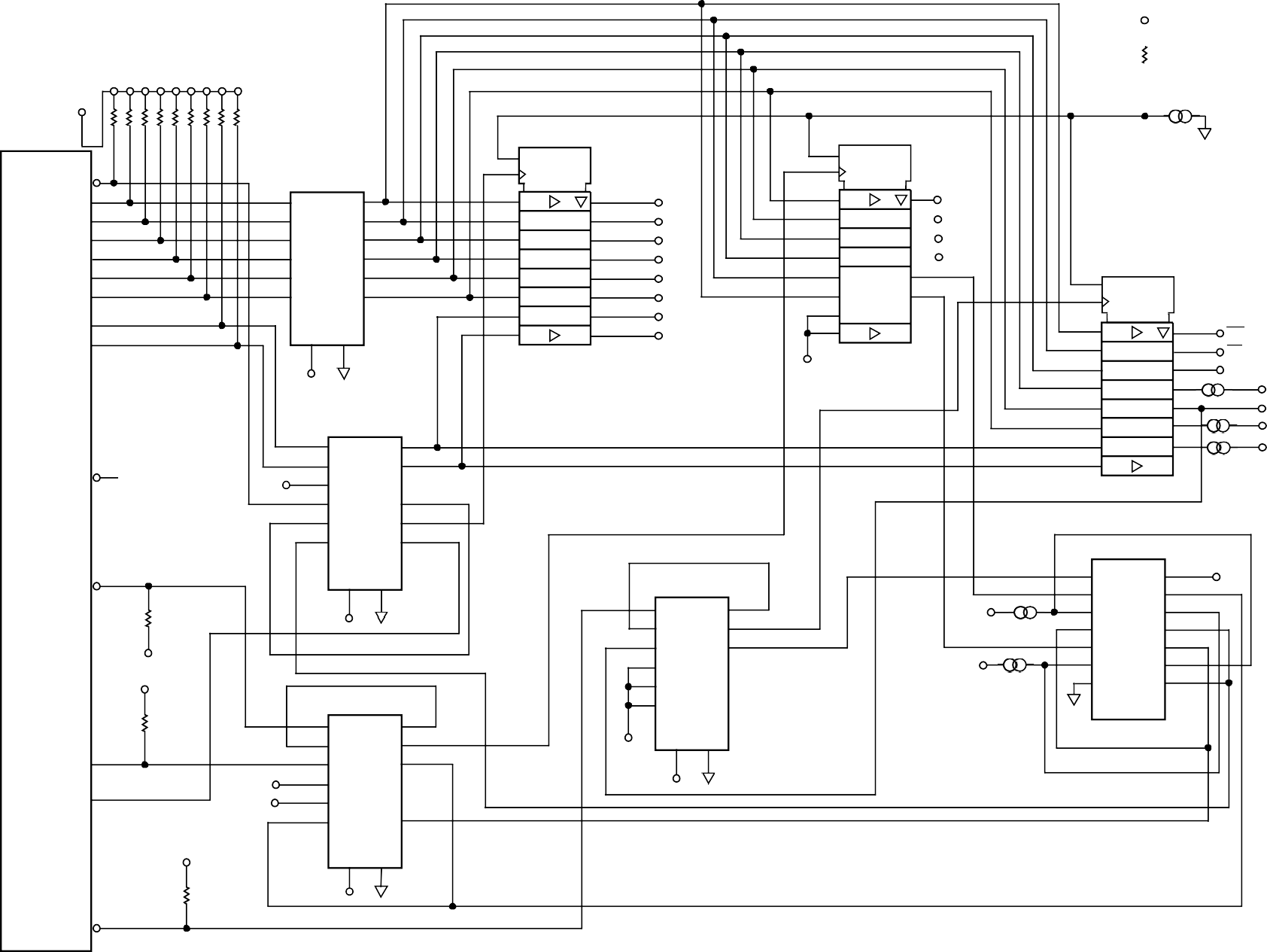
**C13 0.1µF**

**GND**

00636-068

**AD9854**

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**VCC**

**R18 10kΩ**

**VCC**

**1 2 3 4 5 6 7 8 9 10**

**RP1 10kΩ**

**U8**

**1 EN**

**VCC: 20**

**U9**

**1 EN**

|  |  |  |
| --- | --- | --- |
| **9** | **8D** | **12** |
| **8** |  | **13** |
| **7** |  | **14** |
| **6** |  | **15** |
| **5** |  | **16** |
|  |  |  |
|
| **4** |  | **17** |
|  |  |  |
| **3** |  | **18** |

**VCC: 20**

**W15**

**GND**

**C0 1**

**11 C1**

**U5 74HC574**

**GND: 10**

**11 C1 74HC574**

**GND: 10**

**A0 2**

**A1 3**

**A2 4**

**A3 5**

**A4 6**

**7**

**1 1A**

**3 2A**

**5 3A**

**9 4A**

**11 5A**

**13 6A**

**1Y 2**

**2Y 4**

**3Y 6**

**4Y 8**

**5Y 10**

**6Y 12**

**9 8D 12 D0**

**8 13 D1**

**7 14 D2**

**6 15 D3**

**5 16 D4**

**4 17 D5**

**ADDR5 ADDR4 ADDR3 ADDR2**

1. **EN**

**11**

**U10**

**VCC: 20**

**A5**

**A6 8**

**74HC14**

**3 18 D6**

**2 19**

**2 19**

**C1 74HC574**

**9**

**GND: 10**

**12**

**A7 9**

**VCC GND**

**1D D7 1D**

**8D WR**

**8**

**J11 36PINCONN**

**GND:[19:30]**

**10**

**14 7**

**VCC GND**

**U6**

**1 1A 1Y 2**

**VCC**

**13**

**7 14**

**6 15**

**5 16**

**4 17**

**3 18**

**RD RESET**

**W12**

**W13**

**UDCLK**

**PMODE ORAMP**

**FDATA**

**B6 11 3 2A**

**2Y 4**

1. **1D**

**19 W9**

**B7**

**B5 12**

**13**

**VCC**

**5 3A**

**9 4A**

**3Y 6**

**4Y 8**

**B4 11 5A 5Y 10**

**13 6A 6Y 12 U2**

**74HC14**

**14 VCC GND**

**1 1G**

**VCC 14**

**VCC**

**C1**

**R15 10kΩ**

**VCC**

**14 7**

**VCC GND**

**U4**

**1 1A 1Y 2**

**3 2A 2Y 4**

**5 3A 3Y 6**

**ADDR1**

**W11**

1. **1A**
2. **1Y**
3. **2G**
4. **2A**

**4G 13**

**4A 12**

**4Y 11**

**3G 10**

**VCC**

**9 4A**

**11 5A 13**

**4Y 8**

**5Y 10**

**6Y 12**

**ADDR0 W14**

1. **2Y**
2. **GND**

**3A 9**

**3Y 8**

**R16 10kΩ**

**U7**

**1 1A 1Y 2**

**3 2A 2Y 4**

**6A**

**74HC14**

**VCC GND**

**GND 74HC125D**

**C2 31**

**B3 32**

**VCC VCC**

**5 3A**

**9 4A**

**11 5A**

**13 6A**

**3Y 6**

**4Y 8**

**5Y 10**

**6Y 12**

**VCC**

**14 7**

**VCC GND**

**VCC**

**74HC14**

**VCC GND**

**R17 10kΩ**

**36**

**C3**

**14**

**VCC**

**7**

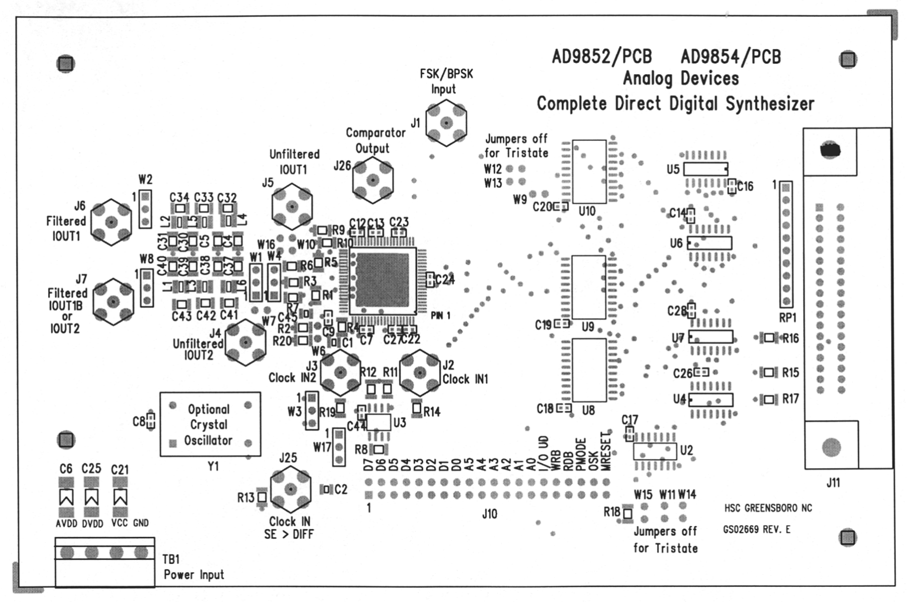
**GND**

00636-069

**AD9854**

*Figure 65. Evaluation Board Schematic*

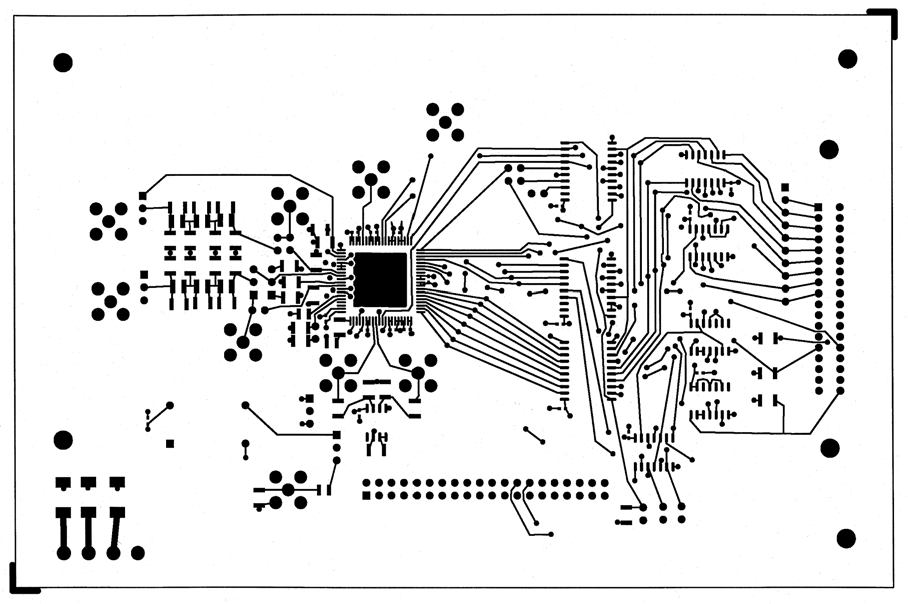
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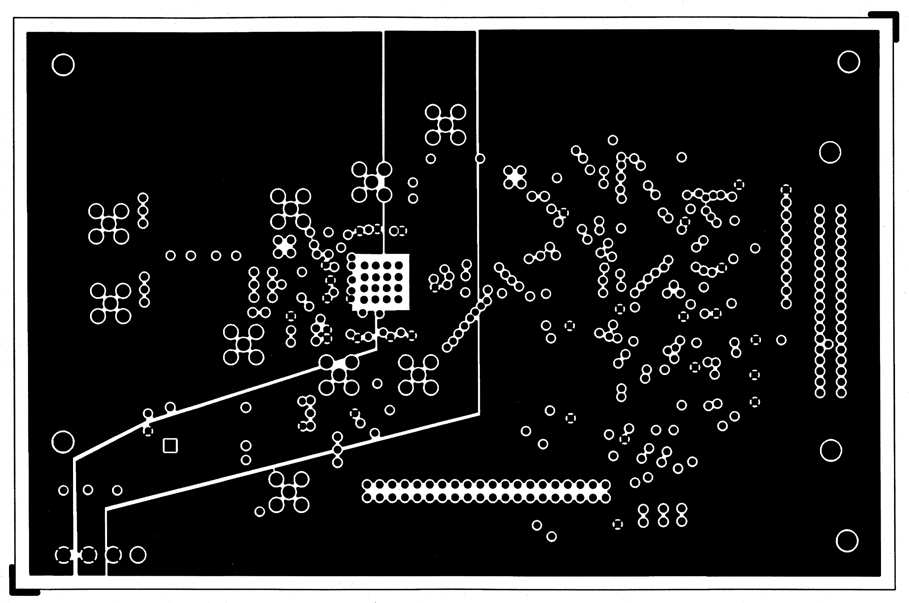
*Figure 66. Assembly Drawing*

00636-071

00636-070



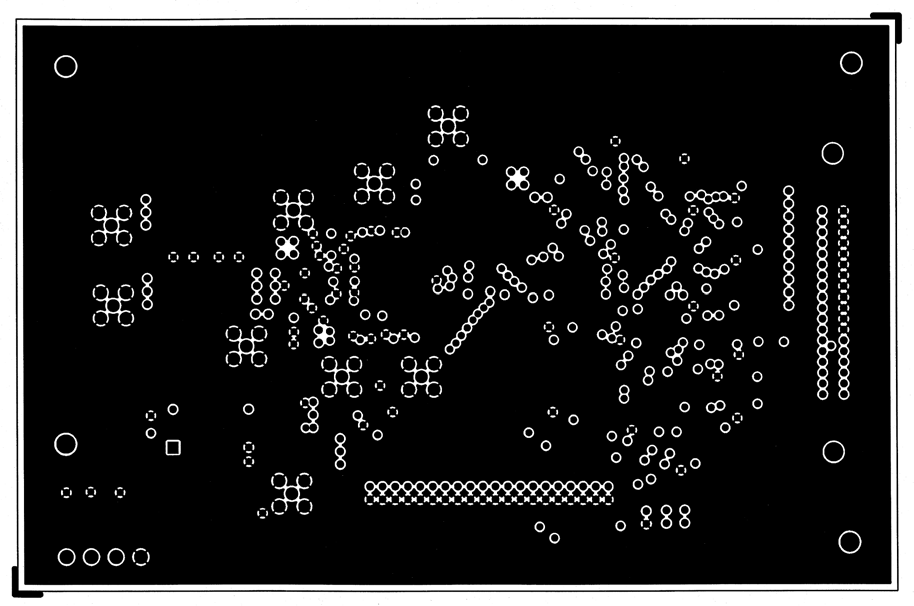
*Figure 67. Top Routing Layer, Layer 1*



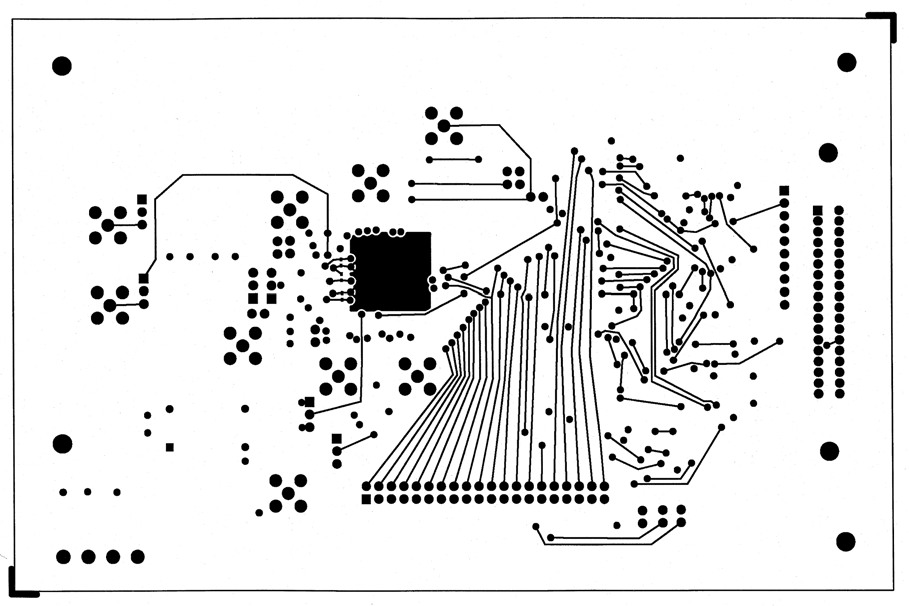
*Figure 68. Power Plane Layer, Layer 3*

00636-072

00636-073



*Figure 69. Ground Plane Layer, Layer 2*



*Figure 70. Bottom Routing Layer, Layer 4*

00636-074

**OUTLINE DIMENSIONS**

**1.05**

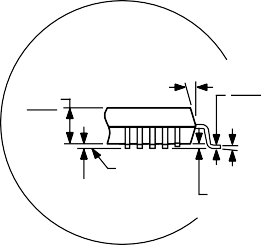
**1.00**

**0.95**

**0.75**

**0.60**

**0.45**

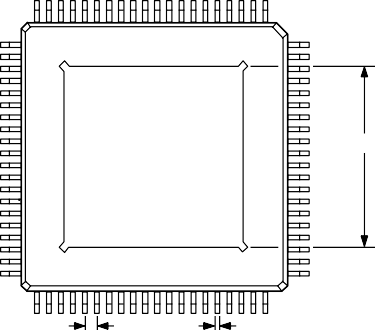
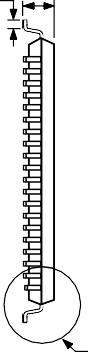
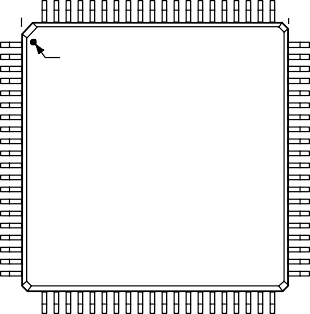
**0° MIN**

**0.20**

**0.09**

**7° 3.5°**

**1.20**

**MAX**

**16.20**

**16.00 SQ 15.80**

**14.20**

**14.00 SQ 13.80**

**80 61**

**1 60**

**PIN 1**

**TOP VIEW**

**(PINS DOWN)**

**20**

**41**

**21 40**

**61**

**80**

**60 1**

**EXPOSED PAD**

**9.50 SQ**

**BOTTOM VIEW (PINS UP)**

**41**

**20**

**40 21**

**0.15**

**0.05**

**SEATING PLANE**

**0°**

**0.08 MAX COPLANARITY**

**VIEW A**

**0.65 BSC LEAD PITCH**

**0.27**



**0.22**

**0.17**

**VIEW A**

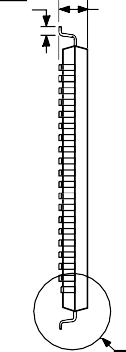
**ROTATED 90° CCW**

**091506-A**

**COMPLIANT TO JEDEC STANDARDS MS-026-AEC-HD**

*Figure 71. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP\_EP] (SV-80-4)*

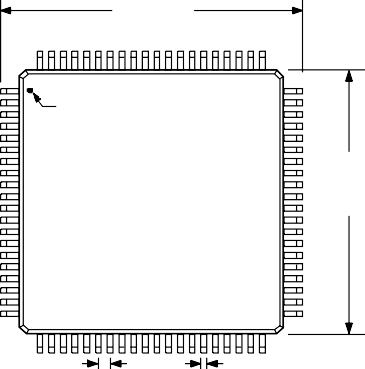
*Dimensions shown in millimeters*

**0.75**

**0.60**

**0.45**

**1.60**

**MAX**

**16.20**

**16.00 SQ 15.80**

**80**

**61**

**1 60**

**PIN 1**

**TOP VIEW (PINS DOWN)**

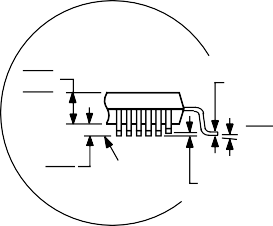
**14.20**

**14.00 SQ 13.80**

**20**

**41**

**21 40**

**VIEW A**

**1.45**

**1.40**

**1.35**

**0.15**

**0.05**

**SEATING PLANE**

**0.20**

**0.09**

**7°**

**3.5°**

**0°**

**0.10**

**COPLANARITY**

**ROTATED 90° CCW**

**VIEW A**

**0.65**

**BSC LEAD PITCH**

**0.38**

**0.32**



**0.22**

**ORDERING GUIDE**

**COMPLIANT TO JEDEC STANDARDS MS-026-BEC**

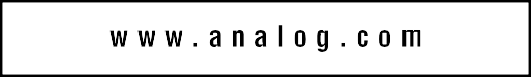
*Figure 72. 80-Lead Low Profile Quad Flat Package [LQFP] (ST-80-2)*

**051706-A**

*Dimensions shown in millimeters*

|  |  |  |  |
| --- | --- | --- | --- |
| **Model** | **Temperature Range** | **Package Description** | **Package Option** |
| AD9854ASVZ[1](#_bookmark69) | −40°C to +85°C | 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP\_EP] | SV-80-4 |
| AD9854AST | −40°C to +85°C | 80-Lead Low Profile Quad Flat Package [LQFP] | ST-80-2 |
| AD9854ASTZ[1](#_bookmark68) | −40°C to +85°C | 80-Lead Low Profile Quad Flat Package [LQFP] | ST-80-2 |
| AD9854/PCB |  | Evaluation Board |  |

1 Z = RoHS Compliant Part.

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**C00636-0-7/07(E)**