x	Initial submission		Modification request

Short description of the project	The LSQ project aims at building a portfolio of HW and SW technologies enabling the control at large scale of emerging solid state qubits technologies e.g. Superconducting cat qubits, semiconductor qubits (carbon nanotubes, spin qubits) and photonic qubits in development by emerging industrial actors. The project will cover a large span of technologies ranging from cryo-electronics to real time error correction under a system approach encompassing the development of models for control chains enabling the exploration of various architectures and leading to demonstration of solutions representative of future scaling requirements. The project will involve actors along the value chain including the main French research institutes in the domain, a CAD tools vendor, a CMOS chips manufacturer, and will welcome the inclusion of national startups specialized in qubits technologies for quantum computing processors.
Key words	Quantum computing, Qubit, cryo-electronics, cryoCMOS, Quantum error code correction, control chain, 3D stacking, silicon photonics, system architecture, modeling, CAD tools.

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Revision	Date	Comments	Budget File
1.0	27/02/2023	First version for partners approbation	
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Executive summary

This document has been prepared as an answer to the mission letter sent by the French public authorities and received by CEA has holder of IRT Nanoelec. The letter requests Nanoelec to build a 6 years research program that addresses some of the key challenges of bringing fault tolerant quantum processors to scale, including QEC and its impact on programming stack, at a 10 years horizon. IRT Nanoelec is a consortium of 22 partners specialized in semiconductor technologies. The consortium gathers key actors (CNRS, INRIA, CEA, UGA, SIEMENS EDA and STMicroelectronics) of the French ecosystem, which are in a position to contribute to quantum technologies.

In response to the expectations of the French Public Authorities, the project is addressing three main ambitions to support the scaling of solid-state qubit technologies such as superconducting cat qubits, silicon spin qubits and photonic qubits.

1. Developing and setting up tools and methodologies for a system approach covering all stages of a qubits control chain from electronics to error code correction including technology bricks ranging from cryo-electronics to silicon photonics and 3D/packaging technologies;
2. Validate the approach through the technology demonstration of full control chain architectures that can scale up to the future requirements of quantum processors;
3. Build a solid IP portfolio that helps our French and European ecosystems compete with international ones.

We propose a program with a statement of work covering all aspects of the required activities including the development of building blocks (cryo electronics, photonic components, 3D stacking and packaging technologies, quantum error code correction), the elaboration of software and test environments to model the control chain and evaluate building blocks as well as functional control chain demonstrators. The core of the program will consist in coordinating and integrating all the previous key elements to explore and implement innovative architectures through demonstrations of control chains at intermediary scale that will serve as proof of concept for further scaling when qubit technologies mature and become available.

Research and engineering teams from each partner's organization will carry out the programs. At the time of the proposal preparation and not withstanding future opportunities, teams from the following institutes were identified as research partners: CNRS/NEEL, CNRS/C2N, INRIA/Qinfo, INRIA/Qantic, INRIA/Loria, INIRA/QuaCS, INRIA/Cosmiq, UGA/IMEP-LaHC, CEA/IRIG, CEA/LETI and CEA/LIST. As far as industrial players are concerned Siemens EDA, STMicroelectronics, Silent Waves, Alice & Bob, Siquance and Quandela have confirmed their interest in the program and/or their willingness to contribute. As a result, the program has already reached a critical mass of expertise and resources to cope with the ambition of the French public authorities.

The program coordination and governance will notably include a scientific and strategic advisory board with three main missions:

1. Advising the program management team on the main objectives of the state of work and on potential evolutions of the project roadmap;
2. Coordinating with the other programs of the French national strategy on quantum technologies,
3. Identifying opportunities for collaborations with other teams to build on useful or necessary expertise whether it is available in academic laboratories or industrial organizations.

In parallel to addressing technical roadmaps, the consortium will set up an ambitious organization to monitor innovations in the field (publications, patents, fundraising…). Through analysis with the pool of experts and contributors, this will serve as a basis for expanding collaborations to research laboratories and teams from other ecosystems. The main objective being to gain access to critical know-how and related IPs to maximize the freedom to operate of the LSQ project partners that will industrialize the results of the program. Together with the background brought by each partner, the creation of IP during the program and new collaborations with other partners, the ambition is to build a portfolio of up to 120 accessible patents and know-how. IRT Nanoelec will also build on its record of accomplishment in transferring technologies to industry and supporting the creation of startups to drive an ambitious dissemination plan for the program development. Dissemination strategies will encompass opportunities with other actors in the industry whether they bring specific activities (materials, equipment, hardware or software platforms), or they are positioned in other application sectors such as space, instrumentation and communications.

Resources for the program will come from funds brought in by the national authorities, but also by the European Commission in the framework of the flagship program and from the industrial partners. The latter will also bring in their own resources to contribute to the project tasks.

The ambition of the program, at the end of the six-year plan is to validate a portfolio of technologies that will accelerate the ability of quantum processors manufacturers and vendors to scale their solutions for the advent of fault tolerant quantum computers at a ten-year horizon.

1. INTRODUCTION/ CONTEXT

1.1. IRT Nanoelec in a nutshell

Nanoelec is one of the 16 institutes for technological research (IRT) and for energy transition (ITE) set up by the French government and financed by the PIA to bring together academic and industrial players on R&D and innovation projects for the competitiveness. The Nanoelec technological research institute is a consortium of actors from the private and public sectors, supported by CEA. Its mission is to help companies create value and differentiate their technology & product portfolio in the areas of digital transition. IRT Nanoelec runs multi-partner technology development and dissemination programs to help its partners from the electronic sector gain competitiveness. It is located in Grenoble, a world-class hub for research, innovation and production in this field. Its R&D programs, related to the design and development of new processes, systems and components are built jointly with representatives of academic laboratories and industry.

1.2. Quantum computing context

1.2.1. Disruptive technology: toward quantum computer

Thanks to ever-increasing computing power and cost reductions offered by Moore's law, electronic systems are now so pervasive that novel applications account for the biggest part of the value share of information technologies. Yet, an important range of applications remain unfeasible on modern classical computing due to their algorithmic complexity with respect to problem size. This is the case for a large category of optimization algorithms who fall in the NP-complexity[1] category for which there is no known polynomial time solution. Hence the practical execution of such algorithms on large inputs is intractable on existing high-performance computer, and will remain so even if Moore's law is able to keep its 20th century pace.

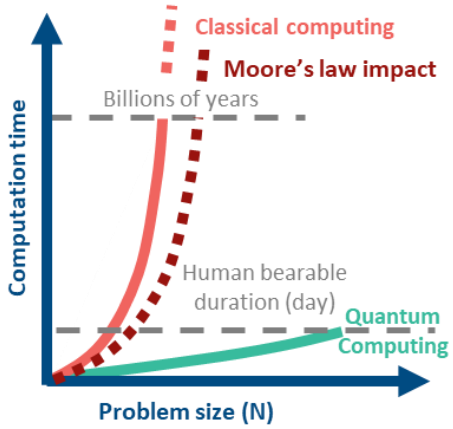


Figure 1 - Illustration of potential impact of quantum computing for complex problems

By carrying out operations on qubits with 2 superposed quantum states, quantum computers would be able to represent a large number of possible states on a limited number of qubits. It would thus be possible to simultaneously process several possible values and therefore significantly speed up certain processing operations as compared with a "classical" computer as depicted Figure 1. This is the property used by Shor's algorithm for polynomial time processing of numbers factorization whereas its complexity (sub-exponential) on a classical computer is one of the pillars of RSA type asymmetrical encryption approaches. Therefore, the ability of quantum computers to decrypt the ciphered data at the heart of modern information systems makes this a real challenge for State sovereignty, both technological and strategic. Over and above security issues, quantum

[1] NP is the set of decision problems for which the problem instances are verifiable in polynomial time by a deterministic Turing machine

acceleration could be of benefit for numerous application areas, notably resolving widespread combinatorial optimization problems.

To achieve such a paradigm shift in computing, one would need quantum computers with a large number of entangled qubits and in which the computing error for each basic operation is low. The accumulation of errors during execution of an algorithm can bury the measured result in noise. For an error rate of about 10^{-3}, Quantum Error Correction (QEC) solutions exist, but imply a significant increase in the number of noisy gates used per ideal logic gate. For example, for this same error rate, Shor's algorithm applied to factorization of numbers of 2048 bits requires 4098 qubits for quasi-ideal gates, but requires 20 million once the error has been corrected[2].

As such, only Noisy Intermediate Scale Quantum (NISQ) computing solutions exist to this date. These approaches exhibit fewer qubits and cope with their inherent errors by identifying quantum algorithm more robust to noise. Making the shift from NISQ to Large Scale Quantum Computing (LSQ) requires to address several challenges that the program supervised by IRT Nanoelec aims to tackle in close articulation to the research work conducted in other pillars of the French national strategy for quantum computing. In particular the proposed project will focus on the scalability of the solid-state qubit control chain and will rely on work conducted in the French priority research programs and equipment (Programme d'Equipement Prioritaire de Recherche, PEPR) for the definition of high quality and reproducible qubits solutions.

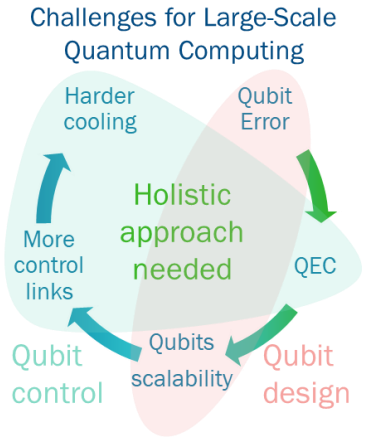


Figure 2 - Challenges for Large-Scale Quantum Computing

1.2.2. International overview

Due to its expected ability to render some complex computing problem feasible, the advent of Quantum Computing could disrupt the existing technological leaderships. This could grant a competitive edge to companies embracing the technology ahead of their counterparts in several applications domains from biology and chemistry to transport, including energy and finance. This is also an opportunity to reduce the dominion of the Silicon Valley on IT technologies through the advent of novel players of the quantum computing domain, which nations aim to attract. One stronger area of Interest is the defense sector, as the processing power gain could significantly imbalance the technological advantages of some nations, especially in the cyphering domain.

As a direct consequence, nations that aim to play a first-rank role in the definition of tomorrow's world from its defense and economic standpoint, are all investing significant amount of funding to spur the emergence of universal quantum computers on their soil. As of 2022, international government investments in quantum computing research totaled 30 Billion USD. The European countries are playing a significant part of this effort with 9 Billion USD, significantly ahead

[2] https://arxiv.org/abs/1905.09749v3

of USA 1.2 Billion USD National Quantum Initiative. France on its own is investing 2.2 Billion USD in its National Strategy for Quantum Computing. One must also notice the tremendous investments announced by The Popular Republic of China whose 15 Billion USD investments linked with the creation of Hefei's *National laboratory for quantum information sciences* account for 40% of worldwide investments[3]. Figure 3 summarizes global public investments in quantum research.

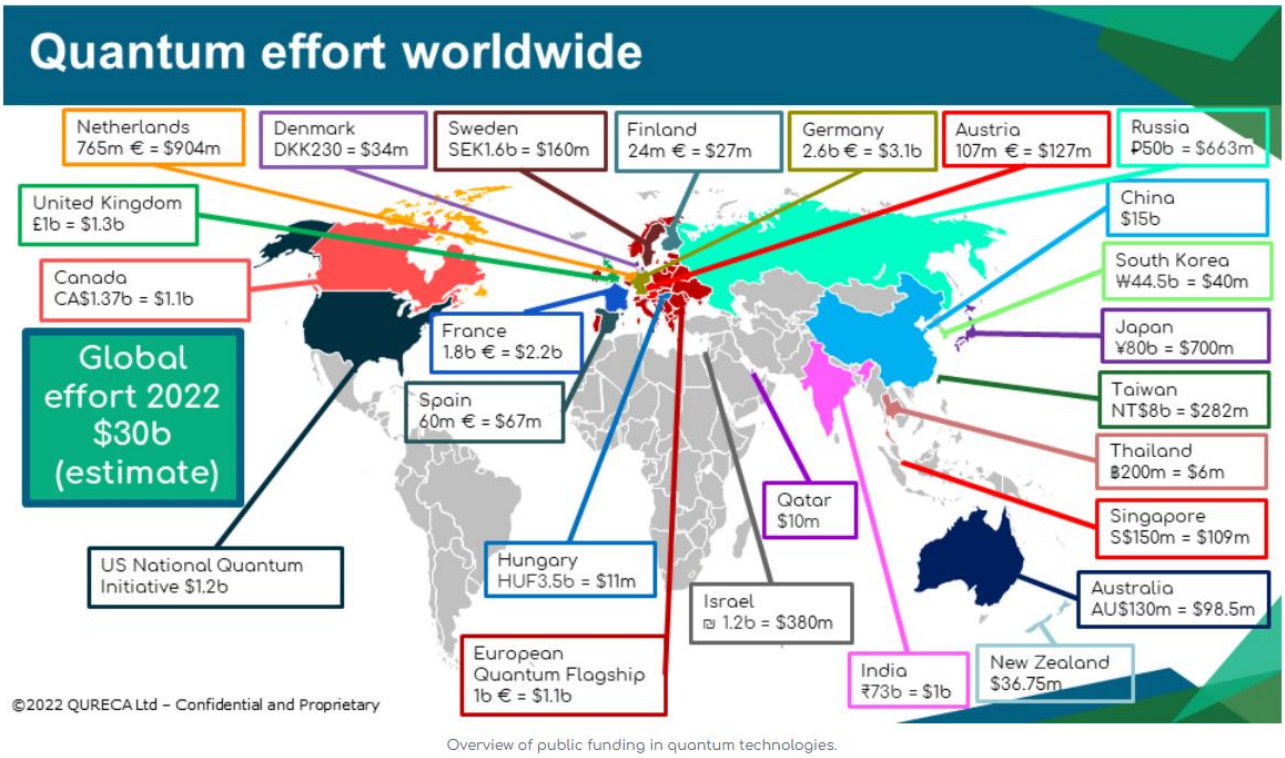


Figure 3 - Worldwide quantum research public funding

(source https://qureca.com/overview-on-quantum-initiatives-worldwide-update-2022/)

1.2.3. Promising qubit technologies

At the forefront of quantum computing technologies, lie qubits. Several technologies have emerged to implement superposed and entangled states on different elementary elements whether they are atoms, ions, photons or electrons as summarized in Figure 4. Photons technologies have shown a high potential as they can theoretically work at higher temperatures, however unique photon detectors usually require ~10K to perform correctly. Trapped Ions and cold atoms can also work at higher temperature, as local cooling is achieved by means of Doppler techniques. However the mass production of such particles is hard to achieve and often exhibit topological constraints limiting qubit interactions.

[3] https://english.ckgsb.edu.cn/knowledges/quantum-wars/

Both Photon qubits and Solid-state qubits, namely superconducting qubits and semiconducting spin qubits, differ from the previous solutions in that they use more classical microelectronic design processes. The potential use of 2D or even 3D meshes makes them good candidates for scaling up the number of qubits.

Historically, superconducting qubits have been the focus of fundamental research in physics. Exploiting the non-linear response of the Josephson junction in order to define the two states, they have led to the first demonstrations of quantum computers. Initial encouraging results triggered the emergence of industrial roadmaps lead by big players in the computing ecosystem such as IBM and Google whose current quantum computers achieve respectively 433 and 72 qubits with plans to push forward their scaling. However quantity is not quality, and emerging startups also focus on improving the qubits quality to ease their usefulness at scale. Among French players, *Alice and Bob* targets significant error reduction thanks to the definition of *cat qubits* that can exhibit exponential reduction of bit flip errors [1].

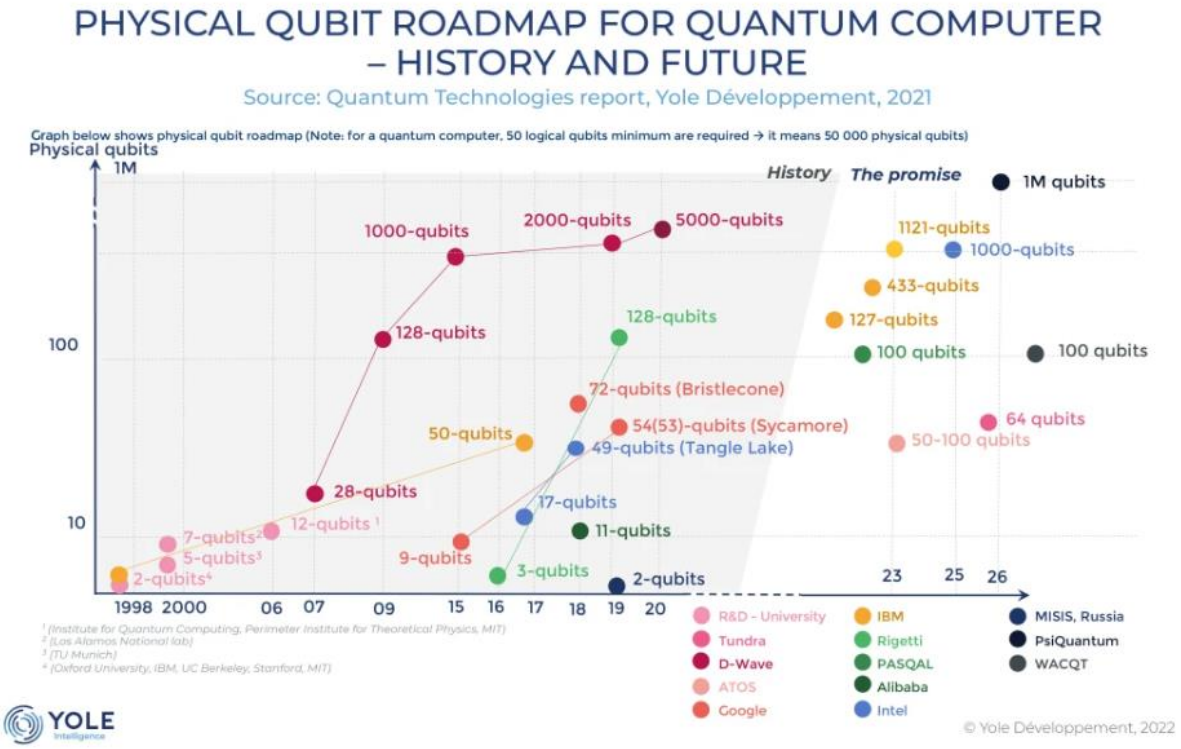


Figure 4 - Qubit technologies, demonstrated scaling and roadmaps

Silicon spin qubits have a more recent track record and have therefore been demonstrated at a limited scale. However, by relying on mature robust and scalable technology processes that demonstrate their capacity to produce billions of high quality transistors, they have high qubit scalability perspectives. Different strategies can be exploited to address individual qubits, within a large matrix of qubits with the same physical properties. These qubits have been demonstrated on systems of a few qubits by various international research teams: 2 qubits by the University of New South Wales (UNSW) [2] using silicon technologies, 3 qubits for SiGe technologies by the RIKEN [3] (Princeton, QuTech) and QuTech recently demonstrated 4 qubits with a Ge channel [4], and even more recently the control of a six-qubits quantum processor in silicon (SiGe/Si/SiGe) [5]. The QLSI European Quantum Flagship project is aiming for 16 qubits by 2025. Aiming for high-quality spin qubits, the French start-up C12 Quantum Electronics, proposes to exploit electron

spin maintained in carbon nanotubes suspended over a wafer incorporating the qubit coupling control and read-out functions.

Both superconducting and spin qubit technologies face similar challenges to their scalability: multiplexing several qubit control signals into limited communication channels (to reduce coldsink) and ensuring real-time error correction. No matter the solid-state technology that emerges, the definition of generic control chain technologies that scale beyond today's NISQ solutions will become an essential part of tomorrow's universal quantum computing. Based on qubit maturity roadmaps, now is the time to create these enabling technologies to support the future quantum computing champions.

Closer to the qubit, specific control is needed in-line with the underlying physics, these specificities need to be taken into account as soon as information is available in the system analysis, and shall be specifically addressed with complementary projects when qubit technologies mature.

1.2.4. French national quantum strategy

In order to support the excellence of French research towards the emergence of industrial champions, key to Europe's economic and strategic independence, France has adopted an ambitious 2-Billion-dollars *National Strategy for Quantum Technologies*[4], coordinated with complementary European initiatives. This strategy is structured in several layers[5] to best accompany the technologies according to their various level of readiness.

The French priority research programs and equipment (PEPR, Programme d'équipement prioritaire de recherche), started on January 1st 2022, targeting low TRL research on all aspects of the quantum technologies spectrum.

Currently, the program has been structured around 10 targeted projects. The first call for projects on the theme of 'quantum computing in flight' was launched in February 2022. Other more generic calls involving breakthrough concepts and talents will be launched soon. The PEPR is structures around four axes:

- Axis 1 – robust solid-state qubits, with target projects on Spin qubits (CMOS) & Superconducting qubits, as well as flying qubits for quantum computing (photons / electrons)
- Axis 2 – cold-atomic qubits for computing & sensing, with target projects on quantum simulation with large number of atoms and quantum sensing
- Axis 3 – quantum algorithms, with target projects on NISQ to LSQ error-correction, quantum-software/stack, post-quantum cryptography

[4] Stratégie nationale pour les technologies quantiques, as part of several Strategie nationales d'acceleration or SNA- we will refer to this strategy as SNAQ in the remainder of this document

[5] https://www.enseignementsup-recherche.gouv.fr/fr/strategie-nationale-sur-les-technologies-quantiques-faire-de-la-france-un-acteur-majeur-de-ces-49233

- Axis 4 – quantum communication, with target projects on quantum cryptography, quantum memories, and quantum communication operational testbeds

Work conducted within the program supported by Nanoelec shall be conducted in close relationship with advances in the PEPR.

The NISQ Grand Challenge is a second layer of the strategy that covers the definition of Noisy Intermediate Scale Quantum Computing (NISQ) solutions. It targets more mature technologies able to be demonstrated in advanced research computing facilities. The challenge encompasses both NISQ machine investments and research program to define adapted algorithms and software stacks to better exploit them. GENCI (*Grand Équipement National De Calcul Intensif*) was appointed to acquire novel QPU to be integrated by CEA, who will manage them, in its existing shared HPC computing infrastructure. The resulting infrastructure, coined *HPC Quantum Iniative* (HQI) platform (formerly Plateforme Nationale de Calcul Quantique Hybride[6] or PNCQH), will benefit to all academic and RTO actors. The funding schemes target successive investment plan to account for the maturation of promising qubit technologies and the expected emergence of industrial players. The project officially started retroactively in April 2022 but the official kick-off occurred in February 2023. First acquisitions of QPUs were conducted with the support of HPCQS European program that conducted European public tenders leading to the installation of Pasqal 100 qubit QPU, by the end of 2023, at CEA's TGCC (Très Grand Centre de Calcul, Very Large Computing Centre).

The LSQ Grand Challenge, targets the innovations that are required to enable the advent of Large Scale universal Quantum computing (LSQ). The program addresses the challenge brought by the implementation, at scale, of the control chain and error correction of solid-state qubits. It will leverage work conducted on qubits and QEC within the PEPR, and will aim at providing a generic interface for LSQ control to ease the industrialization of emerging qubit solutions and their potential inclusion in HPC centers akin to the HQI infrastructure. This is the part of the National Quantic Strategy (SNAQ) that the letter of mission entrusts IRT Nanoelec to carry out.

The Technology Maturation Plan (PMT – Plan de Maturation Technologique), addresses the funding of emerging industrial actors in their first phase of developments. It targets direct participation in key companies by the means of public equity, as well as innovation partnership public tenders to sustain the emerging QPU market. This aspect of the strategy will ensure that competition is fierce between QPU vendors, while securing their cash flow and capacity to develop necessary technologies. The PMT and LSQ program are intended to work in a complementary fashion so as to separate common technologies, to be developed by the LSQ program so as to avoid double funding, and the vendor specific ones, that shall be supported by the PMT terms. In order to reach this goal, regular updates on LSQ progress shall be shared with the entity in charge of the PMT. In addition, it is expected that industrial QPU vendors, will seek to adapt the common technologies developed by the LSQ program to their specific needs in their strategies to meet the PMT tenders performance milestones. This will ensure that technologies developed within the LSQ project are disseminated to industry, and will increase global IRT industrial funding.

[6] https://www.gouvernement.fr/france-2030-strategie-quantique-lancement-d-une-plateforme-nationale-de-calcul-quantique

Due to their above-mentioned complementary nature, the LSQ and PMT projects are part of a broader vision to reach large-scale quantum computing named Proqcima.

The Industrial development of enabling technology program (Programme de développement Industriel relatif aux technologies capacitantes) targets the funding of technologies mature enough to hit market but with too high technology risk to be industrialized without accompanying public funding. Such technologies are analyzed with respect to strategic assets for the European independence in the quantum domain. One of such project of interest deals with the development of future cryogenic solutions, as its outcome can impact power consumption budget in next generation cryostat. Reversibly, the LSQ program could help size requirements for future cryogenic system based on control electronics power dissipation needs. Several meetings with coordinators of this project took place in building this proposal, and it is intended to reinforce exchanges as the projects advance.

MetriQs-France is the national program on measurements, standards, test & evaluation of quantum technologies. With the ambition to support innovation and establishment of a sound, thriving and sustainable quantum industry, the program aims at developing, exploiting and promoting reference measurement means for reliable, comparable, and impartial characterizations and performance evaluations of these emerging technologies. Such information is required to demonstrate indisputably the possible advantage of quantum technologies (QT) over existing ones and to enable their adoption by industry and markets. Coordinated by the LNE (the French national metrology and testing laboratory) the 5-year program, which started in 2022, addresses the measurement needs on the priority topics of the National Quantum Strategy: quantum computing, quantum sensing, quantum communication, and importantly, enabling technologies. The program comprises two complementary parts: (i) a main operating part, with all the actors of the ecosystem (academia, industry, standardization bodies…), dedicated to R&D on the measurement means, evaluation, promotion, and coordination actions, and (ii) the deployment of a quantum metrology infrastructure based on the French metrology network led by LNE and linked to other test and characterization platforms.

2. PROGRAM OBJECTIVES AND ROADMAP

2.1. Main Scientific and technical objectives

By using proven industrial technological processes – such as CMOS technologies for silicon spin qubit – solid-state qubit technologies aim to scale the number of qubits by reproducing them in large-sized matrices. A quantum dot for a spin qubit in silicon has a size of about 100 nm². Fabricating a matrix of 10^8 qubits of this type would then require a silicon surface of 1 mm². However, utilizing such a large number of qubits must overcome several technological obstacles, which are described below.

The quantum effect of these technologies only appears in specific temperature conditions [10mK-1K], depending on the technologies, and over a short coherence time. Achieving such cryogenic temperatures (called Ultra-Low Temperature or ULT) is only possible with optimized management of the volume to be cooled and of heat insulation. The external communication interfaces between the quantum computer and its classical control system must thus be as compact as possible to avoid creating a thermal bridge and unreasonably increasing the volume to be cooled. In addition, a quantum calculation systematically involves (1) an initialization phase for all the qubits in a known state, (2) computation phases where several operations over the qubits are performed to apply quantum gates, (3) measure phases of the quantum states. Performing these steps in a scalable fashion that additionally supports QEC requires to define a multi-constrained control chain. The required components and associated constraints are summarized in Figure 5.

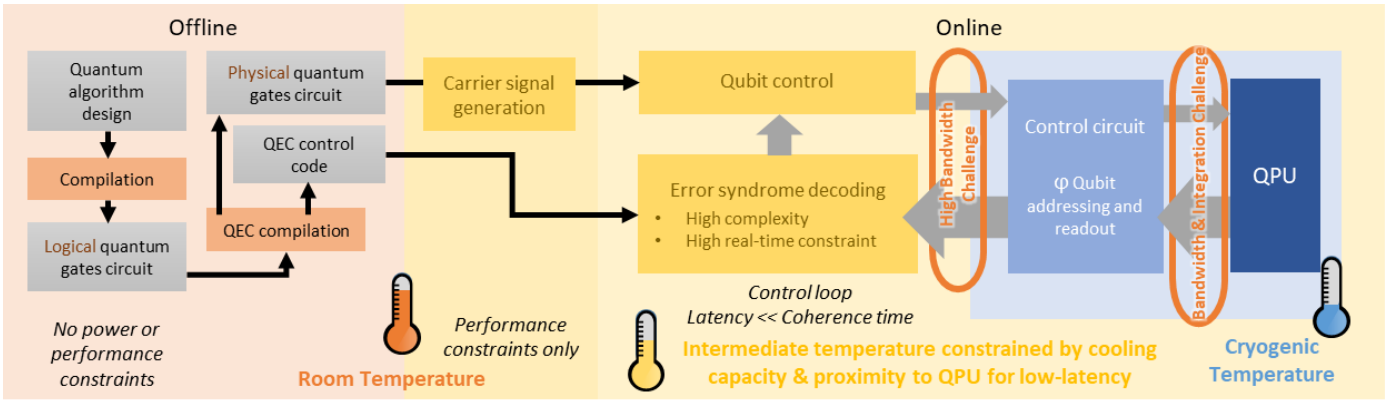


Figure 5 - Schematic of a fault-tolerant control chain for solid-state qubit, and associated constraints

This, results in a serious constraint on the design of the nearby control electronics for the quantum chip, which must on the one hand address large arrays of qubits and, on the other, communicate with the rest of the control system via a small number of links, while operating at ULT within a limited energy budget. This requires the design of CryoCMOS control circuits operating at temperatures below 4K and capable of communicating via high-speed links with the rest of the control chain.

The use of QEC solutions requires additional control as execution progresses. This involves the measurement of qubits called *ancillas* which collectively constitute a computing error syndrome the analysis of which allows feedback to

correct the rest of the execution. This analysis must take place within a period constrained by the coherence time of the qubits (which varies according to the technologies). It therefore requires the design of dedicated real-time hardware solutions for which the energy budget also remains limited owing to the temperature. The consideration of error correction thus becomes a dimensioning factor for the control chip next to the qubit.

The challenge of defining a qubit control chain, taking QEC into consideration and communicating with the user at ambient temperature is thus common to all the solid-state qubit technologies. The strategies of the qubit designers are very similar in many ways, hence the need to have CryoCMOS control circuits (see architectures proposed by QuTech, Berkeley on superconducting SFQ, Google) and high-speed links (state-of-the art optical solutions being explored by Berkeley and NIST). The solutions designed by the Great LSQ Challenge could thus be applied to various promising qubit technologies.

Taking up this challenge implies defining design methodologies suitable for cryogenic temperatures. This entails controlling the behavior of standard transistors in these temperature ranges by characterizing and modeling them before performing combined analog-digital functions. The 3D design challenges are also considerable, with mechanical expansion stresses and differences in thermal behavior in these cryogenic and vacuum conditions (e.g. absence of convection, limited thermal diffusion outside the metal traces). The construction of dedicated models able to analyze these behaviors during the design phases would thus appear to be essential. The data rates involved between the cryogenic environment and the ambient temperature will likely require fiber optic communications which demand expertise in silicon photonics technology and its packaging as well as the design of fibers dedicated to this type of thermal gradient. Finally, the design of processing control channels will be accelerated by the use of models such as digital twins to assess the target performance and energy consumption and allow architectural choices to be made in accordance with the QEC constraints.

These obstacles must be overcome in order to develop all the technological building blocks leading to control of an LSQ computer.

2.2. Key challenges and technology leads

To tackle the challenges of scaling solid-state quantum machines, IRT Nanoelec will set up and manage an ambitious LSQ Program as part of the Great LSQ Challenge, which will aim to develop the technological value chain for control and programming of qubits in cryogenic conditions. The development of solid-state qubit solutions is not covered by the Program, but by other complementary actions within the national quantum strategy and in particular the French priority research programs and equipment (PEPR).

Based on the expertise developed with previous IRT Nanoelec programs on 3D integration and silicon photonics, along with the expertise of the quantum technology research players (CNRS, INRIA, CEA), the IRT proposes a unique program designed to overcome the 7 challenges to the arrival of LSQ for solid-state qubit technologies:

Challenge 1– Digital model of the quantum control chain: The first challenge aims to define a functional digital twin type model for the control chain, from the logical qubit up to the matrix of imperfect solid state qubits, taking account of the error correction code. This digital model will enable designers to explore architectural solutions for the complete control chain, taking account of needs in terms of computing, throughput and impacts in terms of dissipation budget consumption for the processing chains. It will be used to define the first technology demonstrators and to define the architecture of the future generation, with the aim of producing an integrated demonstrator. This model will allow the

evaluation of different options to facilitate architecture design choice by taking account of multi-criteria constraints and thus selecting the best solutions in order to save time in the design/production processes. This digital model will take account of the control constraints of the various qubit technologies (subject to the availability of information from the project stakeholders). The experimental results obtained during the course of the program will feed the model with experimental data.

Challenge 2 – System architecture: The second challenge is tightly linked with the difficulty to build a system vision for the control architecture. Redefining control chain in a scalable fashion, requires to question all choices made at a smaller scale and making a decision on one component can directly impact the applicability of the remainder of the chain. Consequently, the first architectural challenge will consist in bringing together expertise from different fields, through the system modeling approach, and with direct involvement of the project stakeholders, to lay down the foundations for scalability. This will enable achieving high optimization of the overall system control for both performance and energy efficiency. As many quantum technology are being developed, the architecture work will target to encompass the external technological evolution on the scalability roadmaps. Another challenge that will need to be addressed is the lack of a full understanding of component behaviors in cryo conditions that can hinder the capacity to understand and debug experimental demonstrators. Therefore, a specific attention to find novel design for cryo-testing methodology will need to be sought out. Finally the most impacting challenge comes from the dual target of realizing a generic control chain for several qubit types while optimizing it at the same time. Arbitration towards performance or genericity will be required in the project.

Challenge 3 – Optical links: Faced with the considerable challenges of rate and latency needed for qubit control and error correction codes, the third research challenge will address the design of a fiber optic communication chain. The thermal stresses on such a chain and the design of special optical fibers in a thermal gradient ranging from ULT to ambient temperature will be investigated. According to the chosen target technologies, the project will investigate the issues of silicon photonics at ULT and its specific packaging problems. Signal conversion solutions in cryogenic conditions will also be studied.

Challenge 4 – Real-time QEC: In order to provide data required to overcome the above mentioned challenge, this research challenge will study the error mitigation and correction chain, as a dimensioning parameter of the control chain for known algorithms in the literature. This challenge will also aim to define the real-time hardware processing chain for analysis of surface code syndromes and feedback decision-making. To a certain extent, the technologies developed will be generic and modular, so as to address the various constraints of solid-state qubit technologies (coherence time, error rate). Once QEC comes into play, operations must be realized among logical qubits, which drastically increases the complexity of the execution patterns. Compilation approaches will be investigated to provide necessary programmability.

Challenge 5 – Cryo electronics: The fifth research challenge aims to develop CMOS design libraries and electronics components in cryogenic conditions suitable for the definition of AMS circuits. This will involve work to characterize and model transistor behavior at these temperatures. This work could lead to the definition and production of minimal subsets of characterized components leading to a design using a traditional design flow. It is here important to note the full potential of FDSOI technologies in cryogenic conditions thanks to the possibility of back-biasing the substrate to compensate for certain behavioral drifts. The scaling up challenge is to enabling a French/European robust industrial supply chain for cryo-electronic devices and superconducting quantum circuits.

Challenge 6 – 3D Integration and Packaging: Over and above the behavior of the transistors, the design of a control chain next to the qubit requires the use of advanced 3D integration technologies for which it is important to evaluate the applicability at low temperatures (mechanical stresses, differential expansion, and behavior of materials). Thermal dissipation behavior also differs at these temperatures. The sixth research challenge will therefore aim to establish a 3D design and packaging stream compatible with very low temperatures, on the basis of the existing streams. Additional tools capable of assessing behaviors below a temperature of 4K could be defined for this purpose.

Challenge 7 - Cryogenic Tests: The technical challenges above, will need test capacities and capabilities at cryogenic temperatures to be addressed. But characterization protocols themselves need to be improved or developed: current means and methods are academic grade and not adapted to systematic and statistical tests, devices self-heating phenomena impact on large scale electronic have to be evaluated.

These 7 challenges, supported in the operational phase by as many WPs, will be articulated together toward a common goal of achieving an integrated control chain demonstrating the relevance of the building blocks created and validated by the project. One key aspect for this ultimate challenge will consist in defining adapted testing methodologies to validate correct functioning. Especially the fact that qubit resources may not be immediately available abundantly shall be considered while providing confidence in the overall chain. Smaller scale testing might prove necessary as well as the use of more mature qubit control technologies to provide high-quality measure of the achieved communication links. This work will also target integration into the software stack developed within HQI. This demonstrator will be the root for ever more integrated FTQC (Fault Tolerant Quantum Computation) demonstrations with potentially several types of qubits with the definition of complimentary *Associated Projects* to the core IRT one.

A detailed review of the state of the art for the above-mentioned challenges can be found in appendix section 5.1.

2.3. Work methodology

Above all, the work conducted directly within the scope of the project shall target the definition of generic building blocks for the control chain. Genericity will be key to find applications for a variety of solid-state qubits and accelerate the maturation of most promising qubit technologies through the maturation plan. It is also a necessity to provide a fair development path for all the technologies. Thus the identification of common requirements from various qubit makers will be sought to refine the scope of the actions.

If the communication and error correction chains are inherently generic in terms of technological solutions, functioning point will likely differ. For instance, significant differences in qubit physics induce orders of magnitude of difference in the coherence time which definess both the communication bandwidth and QEC performance needs. Qubits errors as well as interconnection topologies will also likely differ impacting the whole control. To cope with this, the project will target generic hardware implementation of QEC methods that shall support various power/area/performance tradeoffs. Communication techniques investigated shall provide the necessary performance for the various qubit needs. To project system performance at scale, simulation of the complete control chain will be sought to help system decision for all qubit technologies which would likely yield to different setups based on the generic building blocks.

Part of the control chain are however very specific to some qubit technologies. This will likely be the case for the qubit control circuit which shall perform gate application through the emission of very specific RF signals as well as the

readout of the qubits. Part of this cryo-electronics can be seen as generic. For instance parametric amplifier for the readout will be needed no matter the technology. However, they will likely need optimization to a given signal range to be exploited, and their operating conditions are expected to significantly differ. Other IPs, such as signal multiplexing, or encoding/decoding shall be more generic but may also need significant adaptation to cope with various qubit addressing strategies. Consequently, deeper analysis, with contributions from the qubit players, must be conducted as part of the project work plan to clarify the project boundaries closest to the qubits. The rationale that will guide decision during this phase will be to address all generic work in the Grand LSQ Challenge and keep all optimization for a given qubit for the maturation plan. Qubit control features not considered as generic will gracefully benefit from the cryo characterization work that will accelerate the design of qubit specific control circuits in the future.

Last but not least, the project will target the integration of the control chain in HPC infrastructure. Reaching this goal would permit various qubit technology to rapidly be exploited by infrastructures such as the one setup in the HQI project. The programming interface of the control chain shall be kept unified no matter the qubit technology. Ideally this unified interface would be built on available standards developed at the national or European level or become one *de facto*. In doing so, work on the universal QPU API, the QEC compilation & mapping, and the transpilation for RT-QEC control will be required. This line of work will be very dependent on both the hardware QEC design (which depends on the QEC scheme itself), and the qubit technologies (which exhibit various error rates, and can handle some gates better than other). Consequently this line of work will start with limited activities to survey existing software stacks and evolutions of the HQI platform and will gain importance as the definition of the control hardware including QEC becomes mature enough.

To validate the key control building blocks built in the project, significant efforts will be spend on setting up an adapted test plan. Due to dependency to the availability of qubits for complete control chain validation, the program will be built considering their lack, and will provide unit testing strategies. This will require to leverage all existing expertise in (non-scalable) qubit control to perform validation measures of the communication chain in cryogenic conditions. This approach of unit testing will therefore be conducted in each WP of the program, and will make use of common measurement expertise and infrastructure shared by Nanoelec partners. Time sharing of these facilities will be needed among all quantum computing projects of the SNAQ. Tight supervision of the measure needs will be performed at the program level in close interaction with equipment's owners to ensure efficient usage of these resources.

2.4. Actions and Work packages organization

The Work Breakdown Structure is made of 7 technical Work Packages in addition to the WP Management as depicted in Figure 6 - LSQ program work package organization:

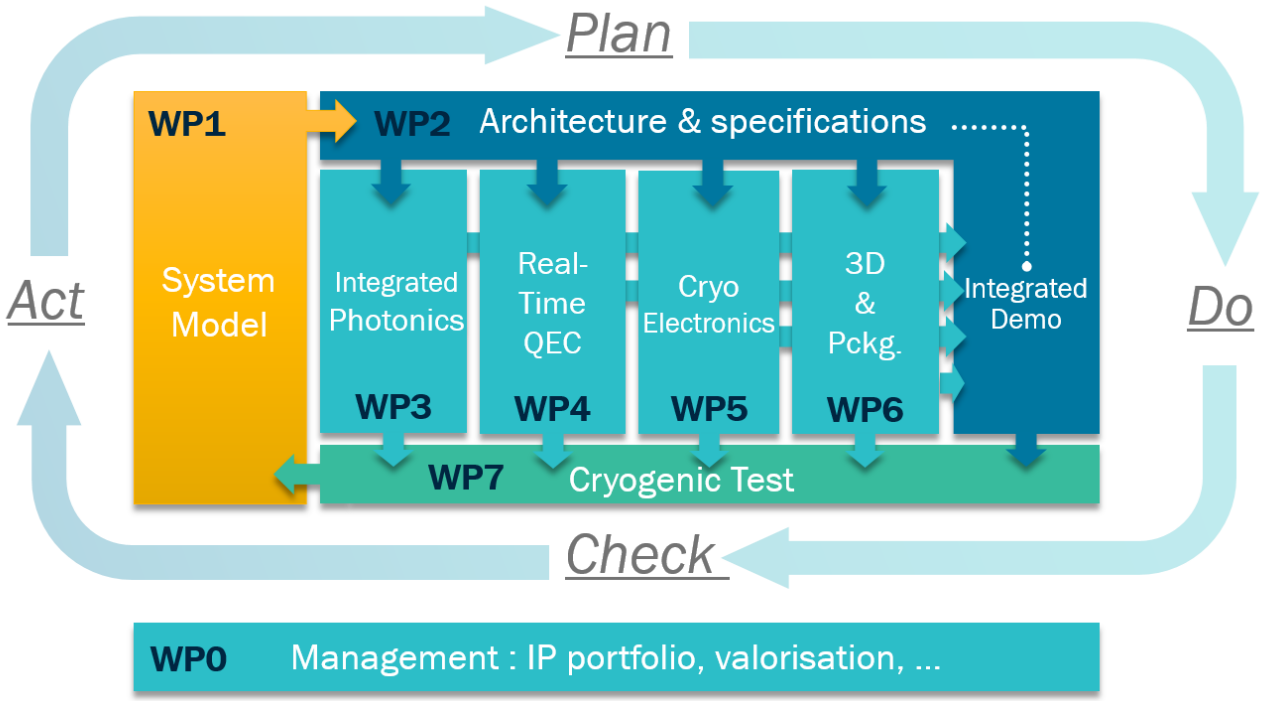


Figure 6 - LSQ program work package organization

- WP0: Project management: This WP is in charge of project management, ensuring reporting, dissemination, and IP management.

-**WP1- Digital models and EDA tools for quantum control chain system design exploration:** This work package consists in enabling the design of a scalable control chain by analyzing possible gaps of electronic design tools to comply with novel cryogenic constraints, and defining a novel system modeling solution for quantum control chains. Dedicated actions in WP1 will seek to provide applicative resource constraints, while technology WP3, 4, 5 and 6 will help populate the system model by providing hardware components constraints and performance figures.

- **WP2- Architecture specification towards integrated demonstrator**: This work package will centralize all design decisions regarding system design of an integrated control chain. It is in charge of gathering intelligence from the system modeling in WP1 to identify enabling technologies for the scalability of the control, and take design decisions for the project demonstrators.

- **WP3- Integrated photonics**: WP3 will study how integrated photonics can be leveraged to allow for increased scalability of the communication links between the cryo-stated qubits and the likely more power consuming error estimation hardware developed in WP4.

- WP4- Real-Time quantum error correction: the ambition of WP4 is to design real-time QEC solutions that scale with the number of qubits. To reach this goal, software and hardware implementations of QEC decoders will be

investigated, based either on existing decoding algorithms, or under development within the PEPR project NISQ2LSQ. Acquired knowledge will be fed back to the system modeling in WP1 for the complete control chain design.

- **WP5- Cryogenic electronic**: Solid-state circuits operating at cryogenic temperature requires classical electronic controllers operating at cryogenic temperatures. This work package aims at developing CMOS model & design-blocks in cryogenic conditions, at evaluating and maturing electronic devices technologies, and at developing a superconducting quantum circuit industrial sector to enable a French and European robust supply chain.

- WP6 - 3D integration and packaging: The aim of work package 6 is to validate the complete communication chain in terms of cryogenic electro-thermal behavior by developing 3D interconnection and packaging solutions which optimally manage heat flux and high-frequency signals that will propagate in the final demonstrator. Starting from WP2 recommendations, system architecture hypotheses will be investigated regarding interconnections key technologies, parasitics and power dissipation.

- WP7- Cryogenic characterization: This work package aims at addressing the cryogenic characterization needs of the other work packages. CEA, CNRS, UGA already have cryogenic characterizations capabilities, but our first analysis highlights that the LSQ program will need additional testing resources since existing facilities workload is already high. In addition, the scaling naturally calls for statistical characterizations, which in turn requires tools and characterization methods industrialization.

2.5. Technological Roadmap

To give an overall vision of the technical work envisioned in the project, Figure 7 summarizes the planning of key milestone of the project.

WP1 will address the challenge of spanning the expertise from several domains within a single simulation environment. First stages will therefore focus on laying the infrastructure for a first system model then populate it with control chain components and quantum application requirements data. Then the work will be focused on continuous evolution of the models with project and international state of art evolutions. A last line of work will be started in the last part of the project to provide a programmer's view of the QEC hardware interface for validation of its integration in hybrid HPC-quantum environments

WP2 that will supervise the architectural decision will first detail specification for the system modeling approach developed within WP1. Then based on its availability, will start projecting scalability routes leading to the definition of the demonstrator spec. The work package will thereafter supervise the demonstrator work up to its final testing since it will require developments from all technological WPs 3-6.

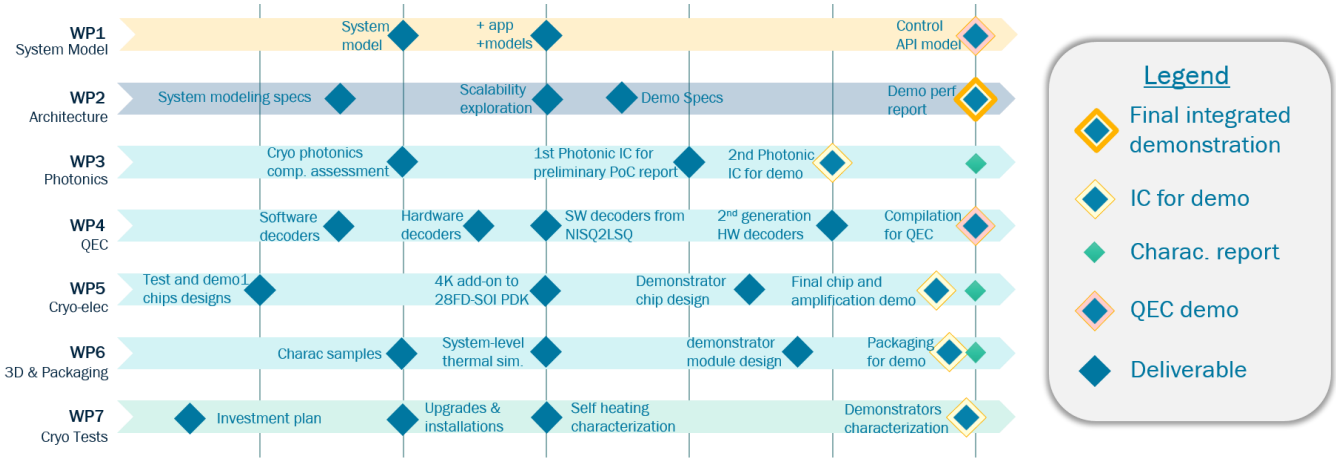


Figure 7 - Key milestones of the LSQ program technological roadmap

WP3: The WP will start with the cryogenic evaluation of existing photonics components, so as to focus design efforts on key missing functions. Then two photonic integrated components designs will be done, one preliminary proof of concept and then the final demonstrator. Synchronously CMOS ICs for the photonic drivers will be designed, so as to build a complete communication photonic subsystem.

WP4 will initially be focused on existing QEC decoder software and hardware implementation, then will study in a second stage novel codes impact on performance. Last stage of the program will address compilation issues with QEC to better integrate QEC in the software stack.

WP5 first major milestone will be the design of the first test chips for CMOS FDSOI cryogenic evaluation. In the meantime, characterizations and model enrichment will lead to the second milestone: 4K add-on to 28FD-SOI technology. Then final chip design and fabrication for the demonstrator and pre-industrial amplification demonstration will be the two last milestones

WP6 will start by developing samples for material testing that will help populate datasets for thermal simulation and 3D interconnection in cryo-condition. Specific tests and software developments shall lead to the definition of a system level thermal simulation methodology accounting for the photonic transport of heat at small scale and low temperature. Based on this knowledge, the work will then focus on the definition of the thermally and electrically efficient 3D integration scheme for the final demonstrator, and will ensure its packaging.

WP7 will start with the definition (first milestone) and the execution (second milestone) of the investment plan needed to be able to characterize the program work packages evaluations and demonstrators. In the meantime, self-heating effect will be evaluated (third milestone), and the WP will end with the demonstrators characterization as the fourth milestone.

Due to the disruptive research nature of the work conducted in the program, the project may encounter technological roadblocks or promising alternative technologies leading to evolution in the program's actions. To cope with this *de facto* situation, IRT bring the necessary flexibility in the program definition through annual revision of the action plan, validated by its program committee then by its steering committee and supported by ANR. To address such technical difficulties, the program will also rely on a specific Scientific and Strategic Advisory Board that will help in identifying solutions outside of the initial project scope. In particular fundamental research institutions are rich with expertise

that could not be all reached out to during the build-up phase. A specific budget reserve was set aside to accompany these changes without impacting the course of other necessary works.

2.6. Link and coordination with other projects

The LSQ project will be tightly linked with other projects in the SNAQ as depicted in Figure 8. With its unique position on technological transfer, IRT Nanoelec is naturally leveraging technologies developed in lower TRL projects. Indeed, the LSQ project will directly leverage research performed within the PEPR program that started ahead of it. In particular, results from directed projects developing qubits -- such as Presquile for quantum-dots based spin-qubits and RobustSuperQ for superconducting qubits – will be used to populate system models for qubits and help project scaling roadmaps for these technology.

These projects also fund technological developments necessary for qubit designs that can have a broader impact on the control chain development, and require further investigation within the LSQ program. One can mention 3D integration at low temperature or superconducting fabrication process that are also used for TWPAs. Even more crucial, the error correction algorithms developed in NISQ2LSQ will be studied for hardware decoding implementation within the LSQ program's WP4, making it a valorization vector for these technologies. Links with other PEPR program will be further investigated during the project execution, to benefit for instance from evolutions on the applicative side with programs such as EPIQ.

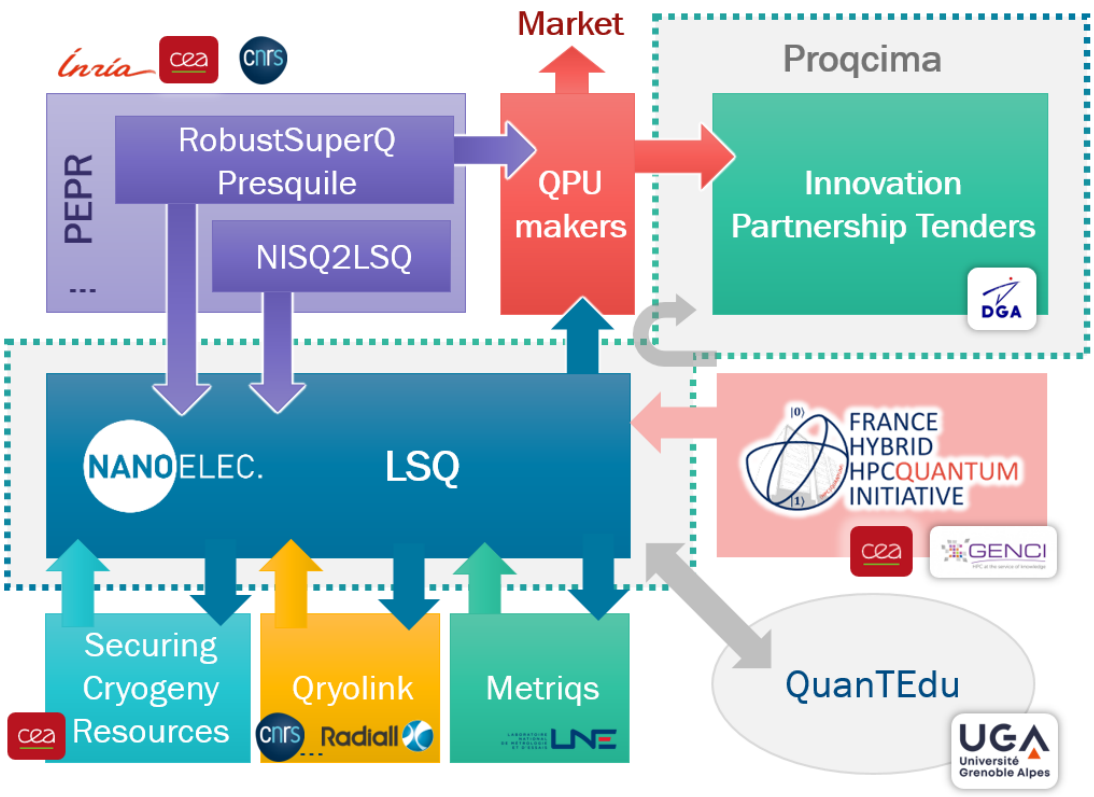


Figure 8 - Interdependence of the project with complementary projects in the SNAQ

Another source of strong link with other projects in the SNAQ lie in the control chain system modeling approach sought in WP1. Indeed, the project will use reference data stemming from the "Cryogenic Engineering" project as constraints for the cooling capacities that can be expected when the scaling of the control chain will be required. Reciprocally, the LSQ program will provide requirements for future cryo-systems. Similarly, the Qryolink project, that develops novel generation of control chains for experimental and NISQ setups, will be a source of data for state-of-art components. The open cryogenic platforms that the project also aims to develop, could also be leveraged for the LSQ program test needs. Early discussion with Qryolink partners also stressed their interest for a system vision and projection of the market needs. They could therefore directly benefit from the system model set up in WP1. Last but not least, the Metriqs project supervised by LNE (Laboratoire National de métrologie et d'Essais – French National Metrology and Testing Laboratory) will target the definition of key characteristics, the reference methods to measure them, and their reliable evaluation, for a variety of quantum technologies. Defining the parameters of the system model components in agreement with the measurements of such key characteristics with reference methods would help populating the models in the long run. Reversibly, should a parameter be critical for system analysis, it shall be part of the component properties assessed in Metriqs methodology. Therefore bridges will be built with the Metriqs project as both program make progress.

As previously mentioned future QPUs will likely be integrated within HPC centers similarly to the approach conducted with the HQI platform. Therefore quantum control chains need to interoperate with ease with such environment. In order to address this aspect, the LSQ program will rely on developments in the scope of the HQI program that will lead to the definition of standardized interfaces with QPUs. It was secured during the project build-up phase that such interfaces will be made public, and therefore exploitable by the LSQ program developments. In addition CEA teams involved on the QEC hardware definition – and therefore programming interfaces -- will also be involved in HQI for NISQ solution integration. This will ensure proper understanding and early access to this critical interface. This interface will also likely be part of the requirements of future provision of next generation QPU by the DGA's innovation partnership tenders, easing the way to valorization of the LSQ developments.

The LSQ program will also require the involvement of well-trained researchers that are becoming a scarce resource with the growing importance of industrial actors, and the steep acceleration of the research project in the past years. To cope with this issue, the program will seek to strengthen its links with the QuanTEdu France project to ensure its training needs are well covered by the courses set up and get a privileged access to first-rank students. This link will naturally grow with the involvement of QuanTEdu's pilot (UGA/CNRS) in the program.

Finally the last link with SNAQ projects is indirect and is in fact one aspect of the dissemination strategy. Indeed the innovation achieved within the project will be exploited by quantum industrial partners in their route towards LSQ. One of their first commercial target is therefore likely to be the innovation partnership public tenders that are envisioned to be setup by the DGA. Consequently, in the State's vision, the LSQ program and this public tenders approach are part of a broader ensemble named Proqcima.

As the national quantum project landscape is evolving with changes in the international environment, one can foresee that other projects in the SNAQ will rise by the end of the program's execution. The program will therefore seek to continue developing links with these project to come, whenever it serves its objectives or valorization strategies.

3. IRT FRAMEWORK & CONSIDERED PARTNERSHIP

3.1. IRT Nanoelec overview and presentation

Nanoelec is one of the 16 institutes for technological research (IRT) and for energy transition (ITE) set up by the French government and financed by the PIA to bring together academic and industrial players on R&D and innovation projects for competitiveness. Their mission is to bring out innovations in future economic sectors through balanced public-private strategic partnerships. IRTs are by definition multi-partners: their members are public RTOs and research laboratories as well as private industries, manufacturers, SMEs and start-ups.

The Nanoelec technological research institute is a consortium of actors from the private and public sectors, supported by CEA. Its mission is to help companies create value and gain competitive advantages in the areas of digital transition. IRT Nanoelec runs multi-partner technology development and dissemination programs to make the electronics sector more competitive. Its R&D programs, jointly built with academic organizations and industrial actors, relate to the design and development of new processes, components and systems. Historically, Nanoelec conducted programs along three main axis: (i) technologies along the "more-than-moore" roadmaps of the microelectronics industry (3D stacking, silicon photonics and more recently GaN/Si for energy conversion, nano-characterization), (ii) technology dissemination and user centric design, and (iii) human capital and training design. In 2020, Nanoelec technology roadmaps evolved to address more specific applications reflecting the priorities of its industrial members:

- **Imaging** through a program call Smart Imager that aims at paving the way for three layer imagers
- **Displays** through a program called Displed that aims at preparing technologies for new micro-led displays based on the innovative concept of Smart pixel that benefit from 3D stacking techniques
- **Photonic Sensors** to take advantage of silicon photonics technologies for applications such as Lidar that require new functionalities such a high power lasers and OPAs
- **Digital trust** with the consolidation of a program on technologies for connected objects including the development of cybersecurity solutions for components and embedded systems,
- **Characterization** activities that are now encompassing a roadmap on radiation proof components and systems through the use of large instruments.

IRT Nanoelec also conducts a training design program in partnership with Grenoble INP and Grenoble Ecole de Management as well as a technology dissemination programs for SMEs. Supported by the AURA region, the latter implements open innovation methods as well as more conventional methods of technological development. Given the disseminating nature of digital technologies, Nanoelec deals with a large number of industrial sectors, from industry and infrastructure to consumer products, including those of transport, environment and health.

3.2. Governance of IRT Nanoelec

IRT Nanoelec is not a legal entity but a consortium led by CEA. CEA, as the holder of IRT Nanoelec, handles the administrative and financial management as well as the coordination of the institute, in interaction with the French National Research Agency (ANR), on the one hand, and, on the other, with regards to the other Partners. CEA signed with ANR the Bilateral Agreement for the execution of IRT Nanoelec Programs.

The *Consortium Agreement* defines the general procedures governing the relations between the Partners of the IRT, and in particular between CEA, as Holder of the IRT, and the other Partners, as well as the rights and obligations of the

Partners on the basis of the commitments CEA has taken as Holder of the IRT, in the framework of the Financing Agreement. This agreement defines operating rules for the institute, the obligations of the partners, the rules of confidentiality, and those for the attribution of intellectual property rights and the exploitation of results. As such the present program will comply with the pre-existing rules that were established in 2012.

This *Consortium Agreement* is supplemented by *Specific Agreements* between CEA as Holder of the IRT and the Partners to define the procedures specific to each of them and/or to each of the Programs to which they contribute. These *Specific Agreements* essentially specify the financial elements applicable to the partners.

As presented in the diagram Figure 9, the governing structure of Nanoelec is based on 4 bodies. The Main one is the *Steering Committee*. It has 13 members with voting rights, as requested by the public authorities. 7 from private entities, and 6 from public organizations. Among the partners identified as future participants to the LSQ program: CEA, CNRS, INRIA, UGA, Minalogic, STMicroelectronics, and Siemens EDA are members of the *Steering Committee*. The missions of the *Steering Committee*, conducted in compliance with the commitments between CEA, as Holder of the IRT, and the National Research Agency, are listed below:

- Build and consolidate the IRT's general plurennial orientations and the IRT's annual program of action in accordance with the commitments signed with ANR;
- Examine and approve the IRT's development strategy and see to its execution thereof;
- Monitor the execution of the Consortium Agreement and the Particular Agreements;
- Monitor the progress of the IRT's various programs;
- Examine and validate budgets, staff forecasts, the means allocated to the various Programs and monitor the commitment of partners;
- Propose or examine solutions for solving, when necessary, the problems encountered in executing the IRT's Programs;
- Decide on the admission of new Partner(s) in the IRT and approve the conditions to their admission.

The *Steering Committee* also constitutes a privileged communication body between the Partners, and it is attentive to all the parties involved so as to take account of the community's needs and to constitute a proposing force for preparing the future. The Steering Committee is also the forum for consultation among the Partners in the case of difficulties. The management of IRT Nanoelec consists of the director and his team. The IRT Programs are conducted by Directors appointed by the Steering Committee (hereinafter the "Program Directors"). An *Operational Committee* gathers the Program Directors and the general representative of MINALOGIC, under the direction of the *IRT Director*. This *Operational Committee* implements the strategy and Programs approved by the Steering Committee. It is responsible for collecting data and monitoring all IRT indicators.

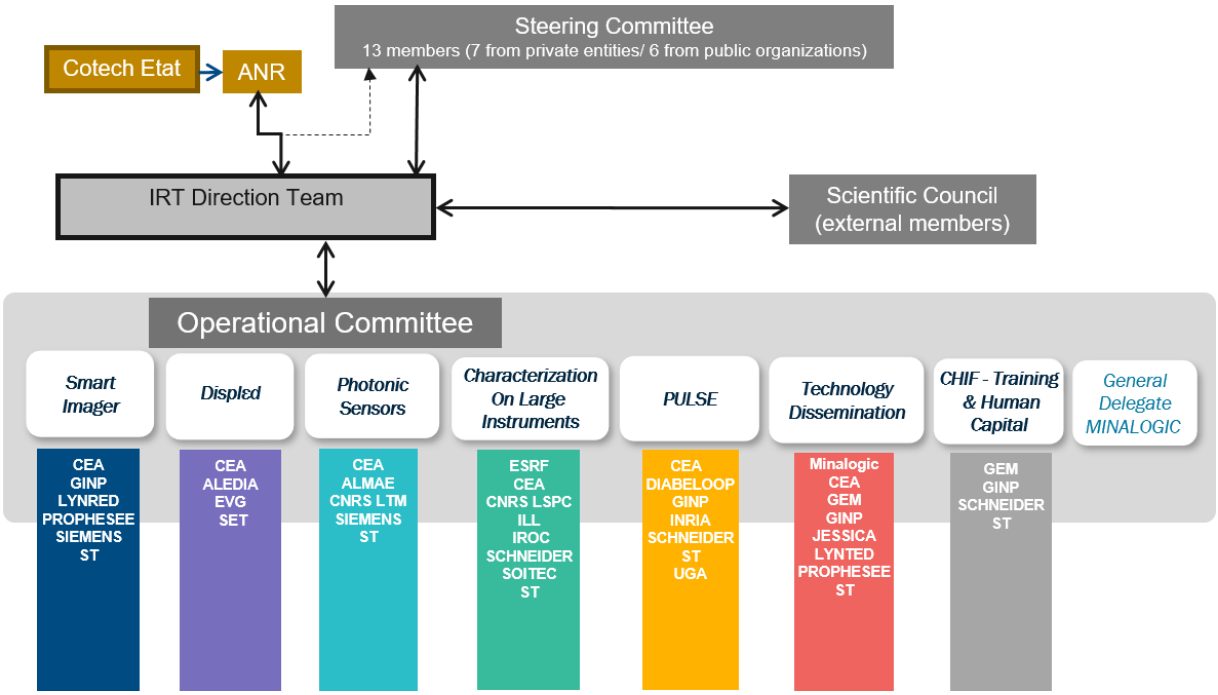


Figure 9 - IRT Nanoelec's existing organization diagram

Concerning the choice for the organization of IRT Nanoelec management team, it was initially decided to rely as much as possible on the existing CEA functions (legal teams, finance and accounting) rather than duplicate and create from scratch entities within the IRT. Nanoelec direction is therefore small in size (about 5 persons full time equivalent). This approach is very pragmatic and one could describe as lean and has been used successfully until now.

A *Program Committee* has been set up for each IRT Program, the composition of which reflects the various players involved in said Program. This committee is placed under the direction of the corresponding *Program Director*(s) and is responsible for defining the Work Program precisely, for monitoring its execution and development, including the examination of the admission into the Program of Partners not initially members of the said Program and/or of new Partners of the consortium. It also decides on the relevance of launching in the program associated partnerships by verifying the consistency of these actions with the Program (providing skills not available, results dissemination ...). The governance also includes a *Scientific Council* composed of French and/or foreign experts representative of the domain, outside of the Partners of the IRT. This Scientific Committee meets once per year. It is consulted regarding

- strategic orientations in the domain of nano electronics and related fields defined by the IRT's Steering Committee
- results obtained by the Programs, taking account of the strategic orientations established by the Steering Committee and the means attributed for each Program.

3.3. Proposed governance and structure evolution for the LSQ program

IRT Nanoelec intends to address all three actions of the LSQ program (system model and exploration, demonstration, IP strategy) entrusted by the SGPI into a single IRT-Nanoelec program. The objective of this approach is to keep an efficient interoperability of the actions and a single reporting view encompassing all aspects.

This structure has proven to be effective and successful in previous programs conducted within Nanoelec. The evaluation recently conducted by the funding agency (ANR) highlighted the high level of impact of the Nanoelec programs as well as their scientific and technical excellence.

This single program structure will also help keep the visibility of other key Nanoelec research programs. The proposed governing scheme, seamlessly integrated in Nanoelec's current governing structure (see Figure 9, §3.2) is depicted in Figure 10. The scheme is built on three main bodies:

- A ***LSQ Deputy Director*** dedicated to the program and integrated in the IRT Direction team, bringing a broader vision with an internationally recognized background in processor architecture and HPC.
- A ***program direction team*** with two co-directors bringing different backgrounds in technologies, system architecture and design,
- An ***advisory board*** specific to the LSQ program that will support the governing structure on scientific and strategic issues.

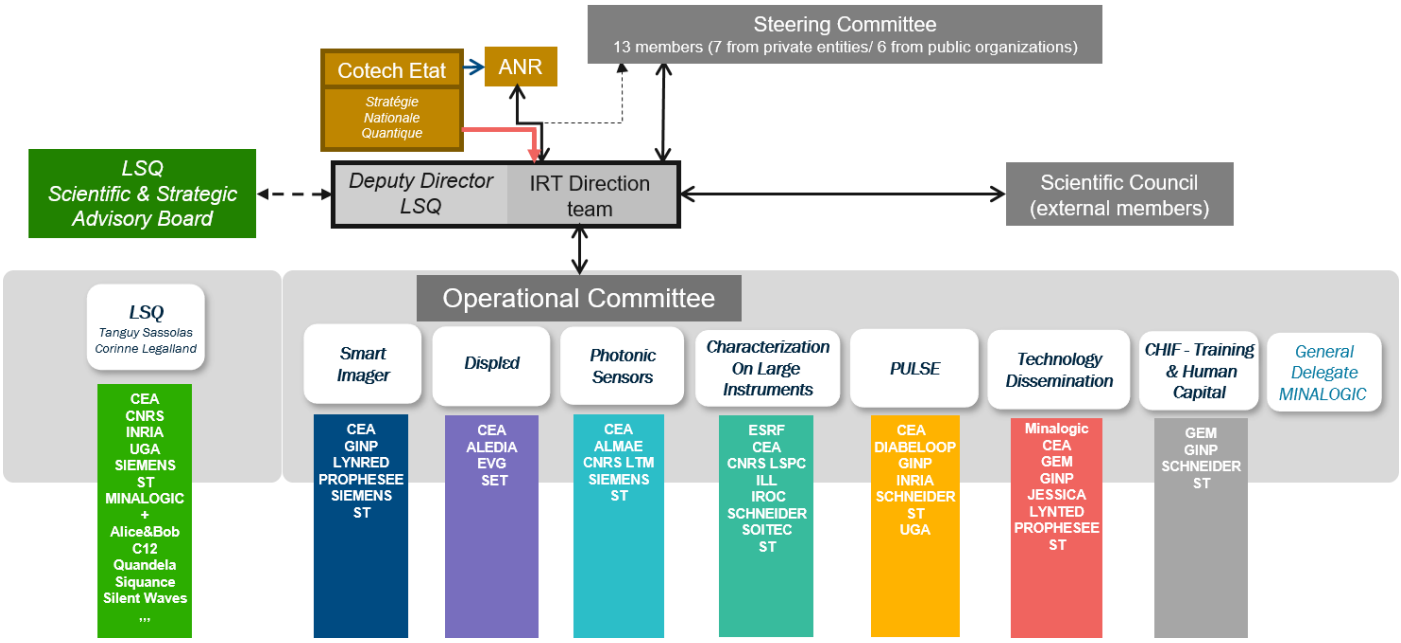


Figure 10 - Proposal of Quantum Computing Program's governing structure within Nanoelec

First of all, to better address this strategic challenge, and the significant increase of activities it represents for Nanoelec, we propose to strengthen the IRT direction team with a deputy director in charge of the quantum computing program, named *QC Deputy Director*.

The main objective of this QC deputy director is to keep a strategic view on the program in close interaction with the dedicated Program management structure that will be more dedicated to program execution. The QC deputy director thanks to its visibility would also seek international collaborations for the project and would suggest evolutions of the program to better align with a moving ecosystem. Specific survey of interactions with advances in HPC and Quantum communications will also be sought to integrate the work in a more global ecosystem.

The QC deputy director will also be in charge of animating and managing the *Scientific and Strategic Advisory Board* that will be set up during the first year of the program. This board will be led by a director chosen in the scientific quantum computing community and will have a twofold mission:

- Advising Nanoelec program managers and IRT direction team on the key orientations of the project in terms of scientific and technological choices and helping analyze threats and opportunities arising from advances and innovation in the field. This mission will be filled in by building a team of 4 to 8 scientists whose expertise encompass the technical activities of the program
- Contributing to the interactions with the various initiatives of the National Strategy for Quantum Technologies, to position the LSQ program with regards to national and international HPC programs and ecosystems.
- Highlighting potential contributions from the academic community or the industrial ecosystem to help the program build on existing resources, expertise and technologies.

Finally, due to the diversity of the challenges on the road to reaching LSQ control, Nanoelec intends, in compliance with the program governing framework, to build a team based on two project leaders with complementary backgrounds to lead the project and conduct operating management : Corinne Legalland, stemming from CEA-LETI[7], experienced in CMOS and semiconductor technology, and Tanguy Sassolas, coming from CEA LIST[8], experienced in system architecture ; this will ensure correct execution of the program on a daily basis. The Nanoelec Quantum Computing Program itself will be structured in eight work packages to address the 3 ambitions stated in the mission letter. Each work package will be led by one or two leaders coming from the different partners of the program.

3.4. Considered partnership

The project will bring together current partners form Nanoelec together with new actors that are specialized in the field of quantum technologies. At the time of the proposal submission the program is expected to gather contribution from 12 members as described in the figure below.

7 CEA-Leti, a technology research institute at CEA Tech, in micro and nanotechnologies

8 CEA_LIST, a technology research institute at CEA Tech, and specializes on digital systems.

3.4.1. Current Members of Nanoelec involved in the program buildup

STMicroelectronics will contribute to the development, characterization and industrialization of cryo electronics and cryoCMOS technologies. The objective is to establish a process flow and its related PDK (Design Kit) to build the control layers of the physical qubits in a range of temperatures that has not been explored today by such technologies essential to scaling. In addition, STMicroelectronics will bring a potential path towards industrialization for 3D integration and packaging solutions as well as silicon photonics devices.

Siemens EDA and Siemens ISS will provide CAD tools and software suites required for the design of key elements of the control chain with exploratory work to be performed on specific models and data collection with a particular focus on materials and devices behavior at Ultra Low Temperatures.

CNRS will contribute in several fields : Instrumentation and Tests at Cryogenic temperatures for both Silicon and Superconducting device , tools and framework for system models , innovative photonic devices at low temperatures , Cryoelectronics .

UGA will contribute, together with INRIA on quantum error code correction. One ambition of the program is to establish a common team specialized on real time quantum error code algorithms and their implementation on digital or mix signal architectures.

CEA will be involved in system level and IC design as well as all technology developments (CryoCMOS design, Superconducting technologies for TWPAs, photonic links, 3D stacking and packaging technologies) and will therefore be coordinating the final demonstration.

Minalogic[9] will help disseminate and build momentum in the regional and national ecosystem. Minalogic has already initiated the organization of workshops and seminars in the quantum computing field helping build a community of scientists, business professionals coming from laboratories, large companies as well as SMES.

3.4.2. Potential new members of the consortium

The 4 startups, Alice & Bob, C12, Siquance and Quandela will bring some resources to support the development of generic elements of common interest. They have planned to dedicate resources for the design and tests of the functions of interest to them e.g. cryo-electronic building blocks, 3D assemblies, low temperature models, error code which can differ from one another depending on their roadmaps.

In coordination with their developments of prototypes in the framework of the Technology Maturation Plan, they will express to Nanoelec, the requirements for specific developments, designs and demonstrations that will be carried out as associated projects by Nanoelec teams when relevant. These projects will be fully funded by cash coming from the industrial partners.

[9] Minalogic is the digital technology cluster for France's Auvergne-Rhône-Alpes region.

Finally, another emerging player has expressed a strong interest in the program. Silent Waves develops and commercializes a TWPA technology which is a key component of the control chains of potential interest for many qubits platforms. Future generations of TWPAs will require collective manufacturing technologies.

3.4.3. National and international ecosystem collaborations

Although Nanoelec is strongly embedded in its local ecosystem, the proposal has been built in coordination with some of the national key players and academic teams. Through the large organizations (CNRS / INRIA / CEA) and their network of common labs (Equipes Mixtes de recherche), connections to many of the main players in the academic field, whether they belong to Universities or Engineering, have been established during the preparation of this proposal. Collaborations will be possible through members of the consortium but R&D collaboration contracts can be set up when relevant. This is a practice that has already been implemented within Nanoelec with partnerships with CNRS-C2N in Saclay and Ampere Laboratory in Lyon.

The connection to ecosystems will be further reinforced by the choice of the members for the *Scientific and Strategic Advisory Board* whose members will be selected so that the program network is also expanded to non-members of Nanoelec. As far as international collaborations are concerned two main thrusts will be pursued:

- Assessment of opportunities through European Funding scheme. The consortium will benefit from an existing network of partnerships at the European level with Universities and other RTOs to build projects benefiting from European programs. This will allow bring leverage to the national funding of the program but also build partnerships to access specific know-how or help develop access to pilot lines or industrialized platforms benefiting our industrial members. Opportunities within the KDT scheme are already under exploration for Cryo-CMOS developments. The consortium will also build on the pre-existing works conducted in the framework of European projects. CEA & CNRS are involved in the Coordination and Support Action (CSA) European project QUCATS started in 2022 to coordinate quantum initiatives in Europe with the European Quantum Flagship. The Strategic Research to Industry Agenda (SRIA), under CEA's coordination, has already published a preliminary roadmap, with a final document expected by December 2023. It will include specific chapters on quantum computing, engineering and enabling technologies, with recommendations for the development of the control electronics to implement quantum error correction. This will be useful to identify opportunities to leverage European Funding for some of the LSQ program tasks. CEA is also involved in the CSA InCoqFlag which aims at providing a roadmap toward international partnerships that are beneficial to the European ecosystem. For the LSQ program, this will serve as an input data for the launch of international cooperation initiatives as part of the third axis of the program. CEA is also a key contributor to European projects addressing technology roadmaps: the projects QLSI, launched in 2020 and QuCube, initiated in 2019 are addressing the development of silicon spin qubits technologies that are integrating work on cryo-electronics and 3D assembly techniques. In this latter field, the project SEQUENCE, focusing cryogenic electronics, ended recently. INRIA is involved in several projects as well. Q-FEEDBACK and DANCINGFOOL are addressing the control techniques for Superconducting Qubits. EQUALITY is a project launched in November 2022 that aims at developing cutting-edge quantum algorithmic primitives relevant for various industry-specific workflows. Coordinating and participating to European projects is part of Nanoelec dissemination and program management strategy. Since 2012, Nanoelec has been involved in more than 30 European projects. In the case of the LSQ program, the partners will build proposals to leverage European funding on technology intensive hardware roadmaps such as cryo-electronics, silicon photonics, 3D packaging at cryogenic

temperatures or other fabrication techniques. Other programs will target cooperation in the field of software and IP design and implementation. The European framework will serve as a platform to build partnerships with key players outside France including the Netherlands and Germany to position the LSQ program as a key element of the QT Flagship.

- In parallel and in coordination with these European initiatives, opportunities for international partnerships will be assessed :
    - With universities that are already connected to the network of the program members,
    - New academic teams when unique expertise, know-how have been identified through scientific and technology watch.
    - Industrial players if the program members, and the governance of the LSQ program are considering that such a partnership will benefit the National Strategy. This can be easily done with specific players such as material providers or equipment manufacturers but may also be the case with other actors whose contributions might benefit our ecosystem (acceleration, cross-technologies development or licencing, …)

Nanoelec has already been involved in such international collaborations with leading material suppliers (Nagase, JSR) and equipment manufacturers (AMAT, LAM Research, EVG, SPTS,…) and academic labs in Canada and the US for instance (Sherbrooke University, University of Minnesota).

4. DETAILED WORK DESCRIPTION

4.0. WP0 Operational management, intellectual property capitalization and valorization

4.0.1. Work package objectives

This work package aims at the global management and work-package coordination, intellectual properties management, dissemination and valorization of the work and communication. It will also provide scientific and technical watch, and generate possible synergies with other domains (as spatial…).

4.0.2. Partners Role

Entity	Role
IRT/DIR	Due to the importance of the program in IRT Nanoelec actions, IRT will dedicate resources to the program for financial, legal, communication and scientific actions.
CEA	As major provider of research works conducted in the project, CEA with its institutes CEA and CEA will lead the project operational execution. CEA's marketing analysis office has developed key competences in market and patent survey for a wide range of technology. It will drive actions regarding access to IP rights and freedom to operate.
All partners	All partners in the project will be involved in the access IP strategy, by sharing on their own research and patent watch. They will also be in charge of the scientific dissemination of the works conducted in the program.

Additional contributions from industrial partners joining the program may be added during the project execution.

4.0.3. Detailed work description

T0.1 Operational Management
Description: T0.1 will be in charge of the supervision of technical actions conducted in the WP1 to7 and will ensure correct flow of information in between work packages. The program directors will report to the IRT COPIL significant evolution of the program execution and will propose corrective actions whenever necessary. In order to achieve the necessary steering of actions the task will organize monthly WP leaders meetings, as well as regular Program Committee meetings. Task T0.1 will update risk assessment analysis, manage interactions with other French quantum strategy programs and European calls, and identify potential synergies with, for example, space domain applications. It will drive the interactions with the advisory board, consolidate annual ANR reports on achieved works and dedicated efforts. Task T0.1 will also monitor the worldwide publications to benchmark the program objectives and results.
T0.2 Intellectual property management
Description: The main objective of T0.2 is to ensure the freedom to operate of developed IPs in the program. In order to achieve that, the task will focus on performing active watch of external IPs evolution. Specific search patterns will be setup for both OSINT (short for Open-Source INTelligence) analysis as well as closed publications and patent databases. Adapted filtering and data analysis will target to cluster retrieved information to assess IP generated by third parties. Then further analysis will be handed over to researchers with the correct background. The capacity to provide the good level of filtering will be critical to request analysis from researchers only when necessary.

Complementary analysis will seek to identify ecosystem links for concurrent IP portfolio, to identify market opportunities.

T0.3 Dissemination, valorization, and communications

Description:

The task will coordinate all communication and dissemination actions in the program. It will ensure scientific communications shed good light on the project by including proper references to the source of the research. To ease communications in all context, the task will prepare public communication documents for all supports whether digital (logo, slide decks, LinkedIn posts) and physical (kakemonos, posters, sustainable accessories).

Both know-how and patents are an important production issued from the project and this is reported in this task. Publications, patents are all reported in each annual report.

Additionally, economic and social valorization by industrial partners are also key success indicators of the project and will be highlighted in annual reports and specific reporting.

Initial dissemination and valorization plan will be updated on regular bases taking into account technical results, IP portfolio evolutions, changes in the ecosystem landscape.

Work package deliverables

D0.1 Annual reports (M12-M72)
D0.2 Intermediate report on identified IP threats and opportunities and related actions (M36)
D0.3 Summary report on identified IP threats and opportunities and related actions (M72)
D0.4 Synthesis of communication actions (M72)
D0.5 Valorisation plan update (M36)
D0.6 Final valorization plan (M72)

4.1. WP1 Digital models and EDA tools for quantum control chain system design exploration

4.1.1. Work package objectives

The ambition of WP1 is to enable the design of a scalable control chain by analyzing possible gaps of electronic design tools to comply with novel cryogenic constraints, and defining a novel system modeling solution for quantum control chains. Gap analysis will support design works from WP3-6, while system modeling will be core to the architecture exploration and definition conducted in WP2-Architecture.

To provide relevant analysis the system model will be enriched from hardware and software data. Dedicated actions in WP1 will seek to provide applicative resource constraints, while technology WP3-6 will help populate the system model by providing hardware components constraints and performance figures. To ensure a holistic vision, the WP will develop strong interaction with other projects in the national strategy to encompass for instance RF links properties or cryogenic power.

At a later stage of the program, based on WP4-QEC developments, functional model of the programming interface of the control chain including error-correction will also be addressed to ease quantum software development and allow applicative performance evaluation.

4.1.2. Partners Role

Entity	Role
CNRS	With its expertise in quantum system modeling encompassing energetic issues, CNRS will provide the initial shared system modeling infrastructure and will extend knowledge databases with state of art review of technologies out of the scope of the program
CEA	Together with CNRS, CEA will bring the system model setup by CNRS for superconducting QPUs to a higher maturity level by defining a generic system modeling approach taking its roots from MBSE and ESL simulation. CEA will also enrich the applicative aspect by providing dimensioning application use cases, and will provide models build on acquired data in WP3-6. In later project stages, CEA will conceived programmer's view models for error-corrected quantum computers
Siemens	Work Package Leader As a major player in EDA and system simulation, Siemens will evaluate its tool applicability to cryo system design and support design work in WP3-6.
Inria	Inria will provide dimensioning use-cases for numerical simulation such as HHL and will also provide hardware constraints and information flow structure for architectures based on stabilized bosonic qubits
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, industrial QPU makers would provide dimensioning data on qubits properties for system modeling (error model, connection topology)
Silent Waves	Upon joining the program, SilentWaves would provide data on TWPA

Additional contributions from industrial partners joining the program may be added during the project execution.

4.1.3. Detailed work description

T1.1 Gap analysis for EDA tools evolutions for quantum computing

Description:

The target of this task is to identify for EDA tools involved in classical electronic design the specific evolutions needed to address the challenge of quantum computing. In particular, the impact of change of material behaviors at low/cryogenic temperature is expected to push the tools to their limits; this includes thermal phenomena at small scale and superconducting behavior. This task will gather feedback from CEA experts involved in WP3-WP6 on existing tools and specific design needs. Siemens will identify to what extent their current offer can meet the project needs, or possibly devise evolution plans depending upon evaluation of business case.

T1.2 System modeling

Description:

Bringing the gap between many expertise domains (application, QEC, 3D integration, integrated photonics, cryo-electronics, cryogenics…) is critical to the definition of innovative control chains for qubits that shall reach a global optimum rather than local ones. The following tasks together aim at defining a novel system approach for quantum control electronics.

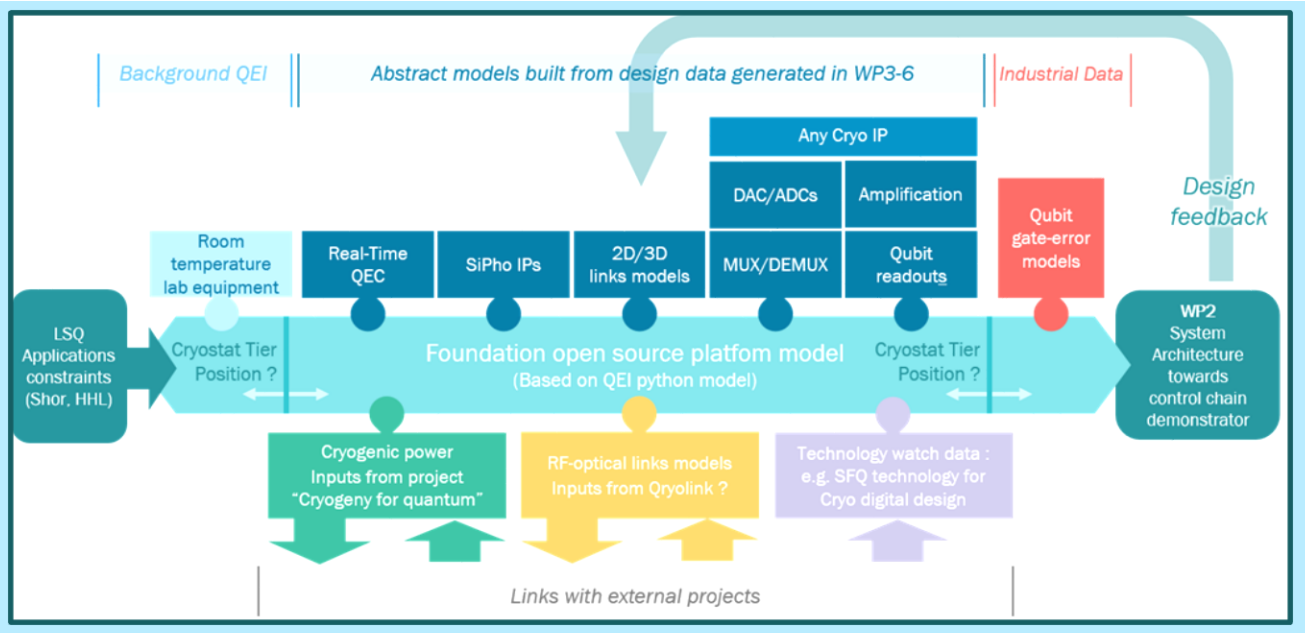


Figure 11 - System modeling approach

T1.2.1 Shared System Infrastructure

Description:

The goal of this task is to define an infrastructure for system modeling of the control chain that is able to encompass every IPs constraints and requirements and will therefore help system architect understand how each component can impact the system as a whole. To reach this objective, experts from different backgrounds will first be gathered to define the adapted data structure of the models. CNRS will bring its expertise in superconducting qubits control modeling, associated with a first python codebase used in http://dx.doi.org/10.48550/arXiv.2209.05469. CEA will bring its expertise in ESL simulation based on SystemC and FMI simulation as well as MBSE (Model-Based System Engineering). Siemens will bring its expertise in building holistic digital twins and tools like Veloce System Interconnect enabling multi-domain, multi-fidelity system simulation.

Involved personal will lead interviews from every stakeholder in the control chain to reach the definition of an infrastructure specification compatible with every element of the system and in capacity to assess their overall impact. Analytical performance models are envisioned whenever applicable, but simulation that is more complex may prove necessary for some components, or even co-simulation with existing domain specific tools.

Then efforts will be spent in implementing the specified framework infrastructure, including components templates (to be populated by experts in T1.2.2). Open-source opportunities for the infrastructure will be investigated from day one to allow for adoption of a broader maintenance community. Additionally, automated analysis services will be added to help architecture decision in WP2-Architecture. After a strong initial development phase up to M42, the task will focus on evolving maintenance required by the project

T1.2.2 Key Component models

Description:

This goal of this task is to create models for each components of the control chain. IPs developed within the project in WP3-6 will be modelled by the teams, directly involved in their developments, and may be refined as the project progresses: CEA will provide CryoCMOS IP models; CNRS will provide TWPA models; INRIA together with CEA and CNRS will build QEC models; CEA and CRNS will provide optical links models; and CEA will provide 3D links models. CNRS, which is implicated in other SNAQ projects such as Qryolink will be in charge of building models from external data (HEMTs, RF links ...). INRIA will provide hardware constraints and descriptions of the informational flow extracted from stabilized bosonic qubits (noise-biased Schrödinger cat qubit and unbiased GKP qubits).

Additional qubits data is expected to be provided from industrial actors with in-kind contributions. Due to their critical intelligence value, qubit models may remain proprietary to their developers. To cope with this risk, approximate qubit models (representative of realistic performance bounds) may be used for architecture analysis in WP2-Architecture.

This task will seek to develop symmetric cooperation with the SNAQ Metriqs project that is expected to provide characterization of quantum components, so as to (1) share invaluable data for system architects that characterization shall address, and (2) gather additional components data for modeling.

T1.2.3 Applicative constraints

Description:

As for classical architecture, to correctly size quantum systems, one needs to consider target applicative constraints. In order to achieve that, the task will consider application use-cases at different scales to pave the way to industrialization.

CEA will provide application constraints by means of cryptanalysis, including declinations of Shor's algorithms for hacking various classical cryptosystems. A co-design approach will be pursued aiming to find shortcuts in the implementation of cryptanalysis algorithms from hardware specificities, to identify resource efficient implementations of quantum computers but also to offer a guidance for the whole control chain

Inria will provide application constraints in the field of numerical simulation with algorithms dedicated to resolution of systems of equations. A first candidate is the HHL algorithm and its refinements, but other algorithms for working with EDP will also be considered.

These various applicative constraints, together with QEC properties coming from WP4-QEC will be central to the overall control architecture scaling analyses performed in WP2-Architecture.

T1.3 QPU functional models

Description:

In order to validate that the control chain architecture will be able to connect to existing HPC architecture, task T1.3 would build a functional view of the quantum system encompassing QEC hardware. The intent is to represent the programming interface offered by the QEC hardware and potential room temperature equipment.

This model with then be used to define additional software steps to convert operations from the "Quantum HW Specification Standard" defined by Atos in the HQI project and the interfaces made available by the QEC hardware(s). This shall allow to project performances for real-case full stack programming of error corrected QPUs.

Work package deliverables

D1.1 Reference system model infrastructure implementation (M24)
D1.2 Report on first system model encompassing components models and application constraints (M36)
D1.3 Report on API model for integration in computing platforms (M72)

4.2. WP2 Architecture specification towards integrated demonstrator

4.2.1. Work package objectives

This work package will centralize all decisions regarding system design of an integrated control chain. It is in charge of gathering intelligence from the system modeling in WP1-System model to identify enabling technologies for the scalability of the control, and take design decisions for the final project demonstrator. To achieve this goal the work package will gather expertise from many entities, including the ones from industrial quantum players joining the program. The work package is expected to get a growing importance as the project moves forward, starting with a prescriptive role for enabling technologies, to initial system specification and finally to reach final demonstrator supervision.

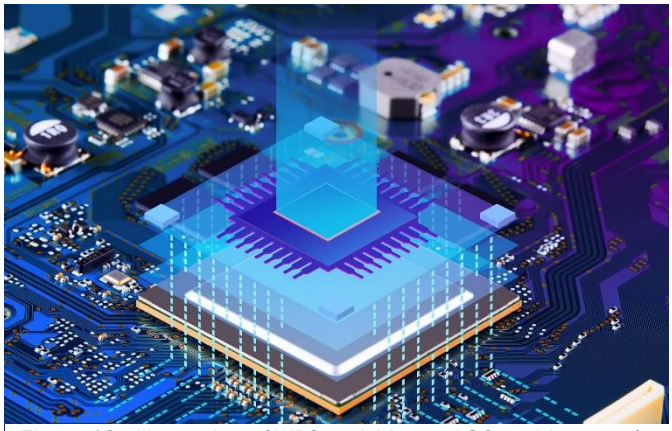


Figure 12 - Illustration of WP2 activities on LSQ architecture from state-of-art specifications to system exploration by means of simulation, towards final demonstrator implementation supervision

4.2.2. Partners Role

Entity	Role
CEA	Work Package Leader With its expertise and background in complex integrated architecture (e.g. EPI processor architecture) and system design (e.g. Renault FACE industrial project), CEA will lead the architecture specification work package, and contribute to it with its knowledge in WP3-6 technologies.
CNRS	At the root of the Quantum energy initiative, CNRS will focus its work on evaluating the energetic implication of the scaling of the control chain depending on used technologies and QEC schemes.
Inria	With a central program role on the definition of QEC schemes, Inria will mainly participate in WP2-Architecture to get better grips at how hardware constraints (topology, control multiplexing…) can affect applicability of proposed QEC schemes solutions.
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, QPU vendors will leverage the system tools analysis from WP1-System model to devise their own scalability roadmap, and will help define needed system demonstrator needs to derisk their scalability roadmap.
SilentWaves	Upon joining the program, SilentWaves will contribute to specify co-integration strategy applicable to their amplification solutions

Additional contributions from industrial partners joining the program may be added during the project execution.

4.2.3. Detailed work description

T2.1 Expression of requirements for developed technologies
Description: Based on prior knowledge acquired on namely (1) the state-of-the art of quantum control electronics, (2) high-performance computing electronics such as high-speed IOs for data communications, (3) energetic issues stemming from quantum noise and cryogenic power and (4) quantum error correction, CEA and CNRS will define the target figure of merit for technologies investigated by the project in WP3-6.

T2.2 Expression of requirements for system model analyses
Description: In order to ensure the system model will be in capacity to address questions raised in defining the system architecture, T2.2 will specify the expected exploration capacities required from the toolset developed in WP1-System model. In particular, capacity to perform evaluation of environmental impacts with the system tool in conjunction with existing solutions will be dealt with.
T2.3 Evaluation of scalability strategies for performance and energy efficiency
Description: Starting with the availability of first system models the task will evaluate different scalability strategies for the control chain of various qubits technologies from a pure performance driven perspective (CEA) and from an energetic one (CNRS). Leveraging the holistic system model build in WP1-System model, will enable system-scale optimizations for the control chain. A refined evaluation will be performed based on updated models available later in the project. Scalability scenario may encompass *what-if* analysis considering the advent of quantum technologies outside of the project scope, such as quantum communications or quantum memories. Most promising scalability routes will be assessed in terms of environmental impacts possibly leading to simplified life-cycle analysis (LCA).
T2.4 Specification for the control chain demonstrator
Description: Based on partial scalability evaluations from T2.3, the task will focus on defining concrete specifications for a demonstrator in capacity to demonstrate the scaling potential of involved technologies. In particular, structuring choices such as I/0 methods need to be made early enough in the project to allow for their development. As scalability routes may differ from one qubit technology to another, the demonstrator may require a certain level of versatility that will need to be put in adequacy with available design resources.
T2.5 Control chain demonstrator supervision and integration
Description: This task will be in charge of ensuring good cooperation between developments conducted in each WP3-6. A particular area of focus will lie in the definition of interfaces at all scales, be it 3D integration, packaging I/O, or board design, cryostat I/O, or QEC syndrome decoding accelerator I/Os and protocols. In order to achieve that, the task will centralize refined specifications of each subcomponent and keep a reference specification up to date with required adjustments for each subcomponent. In particular, to allow the demonstrator to be plugged with actual qubits that are not designed in the project, interfaces towards qubits will be defined with participating industrial players, to ensure the capacity to implement QPUs through associated projects.
T2.6 Specifications for future generation of scalable control chain
Description: The goal of this task is to prepare a second generation for the control chain demonstration based on results accumulated in the project. Having such specifications as starting point for a follow-up Nanoelec program would avoid work interruptions that could lead to loss of momentum. The second generation would prepare industrialization by demonstrating control at larger scale; it will also likely extend the scope of the program to scale-out strategies depending on results from PEPR actions.
Work package deliverables
D2.1 Requirements for system modeling analyses (M18) D2.2 Partial report on scalability strategies (M36)

D2.3 Specification report for the control chain demonstrator (M42)
D2.4 Performance report on the demonstrator (M72)

4.3. WP3 Integrated Photonics

4.3.1. Work package objectives

WP3-Integrated Photonics will study how integrated photonics can be leveraged to allow increased scalability of the communication links between the cryostated qubits and the likely more power consuming error estimation hardware developed in WP4-QEC. Indeed, optical fibers offer higher bandwidth than RF cables and also provide good thermal isolation. The challenge for WP3-Integrated Photonics is thus to ensure proper functionality of integrated photonics in cryogenic conditions while keeping a constrained power dissipation budget and good Signal-Noise Ratio.

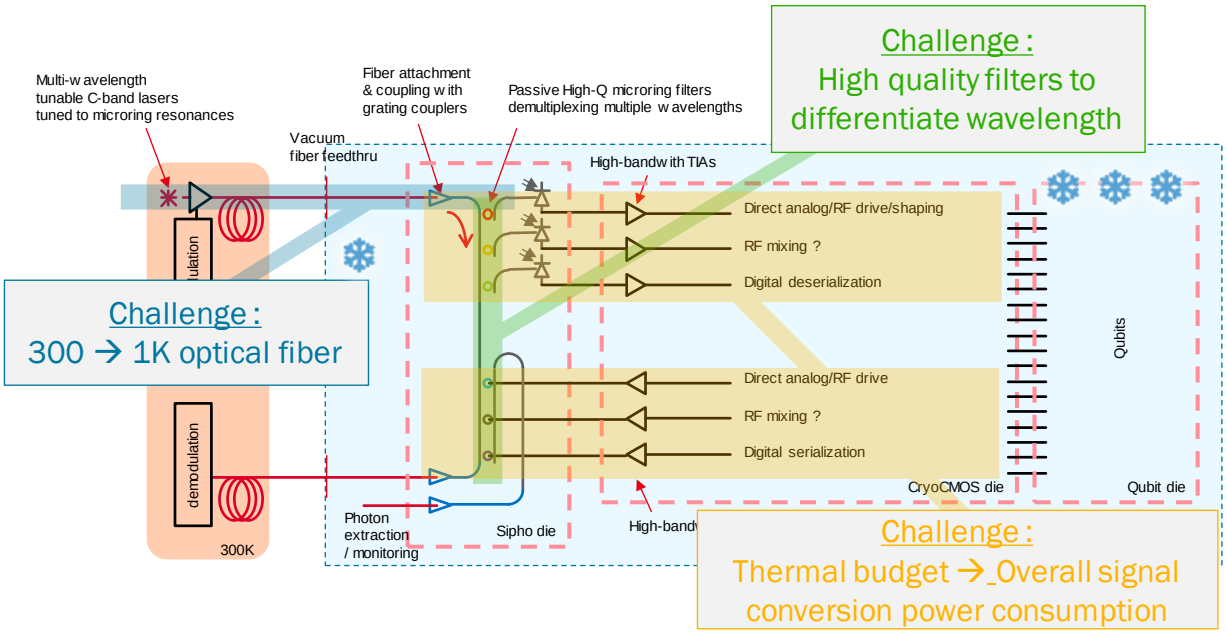


Figure 13 - Proposed solution for optical communication at cryo temperatures

WP3-Integrated Photonics will begin with an exploration phase to identify which existing integrated photonics do work in cryo-conditions, and which of them are the most promising to reach the expected performances. Then design of integrated photonics will start based on validated components, while design of advanced, high performances, key components will be investigated. As a starting point, integrated photonics use will be evaluated for both analog and digital output to provide data for system modeling in WP1-System model, while its use for ingress and the final subsystem design specification for egress (analog or digital) will be dependent on system architecture decision conducted in WP2-Architecture. Considered integrated photonics technologies may be based on either glass or SOI substrates or encompass both using 3D integration.

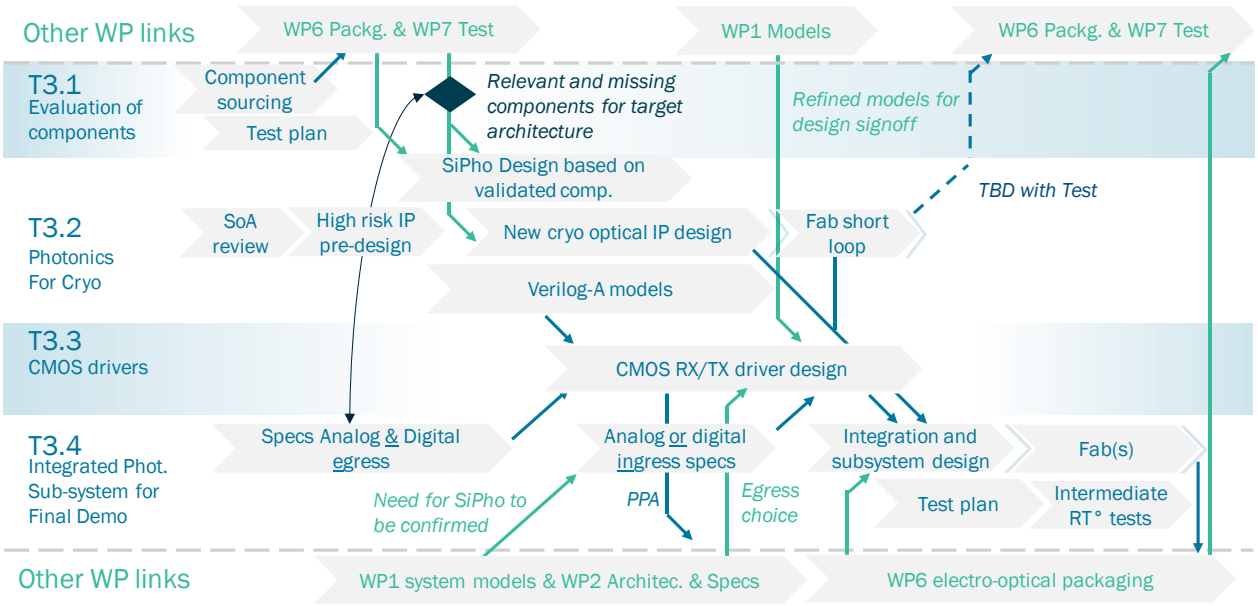


Figure 14 - WP3 PERT Chart showing intra & inter WP synergies

Another key aspect is the co-design and the assembly of the CMOS driver providing the appropriate bandwidth, voltage-swing and power supply at cryo conditions, and while keeping a limited heat dissipation. Thus, photonic and electronic IC packaging and 3D integration will be investigated, in relationship with WP6-3D&packaging. Discrete components will be evaluated at first in cryo conditions inside this WP and using the tools available/under development in WP7-Cryogenic tests. A proof-of-concept cryo-compatible transceiver will be designed after this assessment, while the final demonstrator is likely to require advanced photonics devices in order to reach the overall specifications (mostly regarding speed, heat dissipation, and compliance with drivers).

4.3.2. Partners Role

Entity	Role
CNRS	CNRS has a strong expertise in integrated photonics design. Contributions could encompass specific integrated photonics device design as well as provide characterization environments in cryo-conditions.
CEA	WP leader. As an RTO, CEA has developed a strong expertise in integrated photonics architecture design, more specifically using Silicon-Photonics processes, It will lead the architecture definition of the photonic integrated circuits necessary to provide a scalable communication between cryostat and room temperature
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design teams with its design tools and expertise (e.g. Lightsuite Photonic Compiler).
ST	ST would support actions by providing SiPho device samples to be tested in cryo conditions and will also evaluate applicability of newly developed SiPho designs to other application domains
UGA	UGA has a strong expertise in integrated photonics design, especially over glass. Contributions could encompass specific passive integrated photonics device design as well as provide characterization environments in cryo-conditions.

Additional contributions from industrial partners joining the program may be added during the project execution.

4.3.3. Detailed work description

T3.1 Evaluation of existing components

Description :

This task is devoted to the assessment of existing photonics passive and active devices in cryogenic environment, in relationship with WP6-3D & Packaging and WP7-Cryogenic tests. CEA and CNRS will be mainly focused on Silicon-based and Silicon Nitride-based components, while UGA will be centered on Glass-based structures. For passive devices, insertion losses, spectral responses, and propagation losses will be evaluated, while for actives devices, speed, energy consumption, thermal dissipation, and compliance with Driver voltage limitation will be assessed, offering early inputs for T3.2.

In this task, CNRS proposes to participate to the determination of the limit of Si and SiN photonics devices in Cryo environment. That includes (i) the determination of the limit of plasma dispersion (electro-optics effect currently used in Si) effect as a function of the temperature, (ii) the determination of the temperature limit of germanium waveguide detectors and avalanche photodetectors in terms of speed and responsivity and noise and the validation of passive photonic structures.

UGA will contribute by providing its expertise and facilities in evaluating the performances of existing passive devices made on glass and pigtailed to optical fibers operated at cryogenic temperatures. It will provide with low-loss waveguides (<0.1 dB/cm at ambient temperature) connected with optical fibers (insertion losses < 2dB) and will evaluate the potential loss of transmission quality when the devices is brought to cryogenic temperatures (~4K). Cycled measurements to evaluate the aging of the fiber-waveguide connection could be carried-out if needed thanks to our new cryogenic bench test that is operating in a close-loop configuration. Once the connection between the waveguides and the fiber is validated, the behavior of wavelength multiplexing and de-multiplexing functions (typically AWG) will be performed in order to document the expected shift of their spectral response when cooled down from room temperature to cryogenic ones. During this assessment task, we could also perform measurements on photodiodes at the wafer layer (top illumination) thanks to the microwave and electric probes that complete the optical line of our cryogenic bench. Si-waveguides based functions like high-speed modulators or grating coupler-based devices could eventually be tested on our bench but it would require some developments.

In this task, CEA will provided passive and active devices based its 300mm SOI and 200mm SiN photonic platforms. Electro-Absorption modulator (SiGe, III-V/Silicon), or Polymer-based modulators might be added to the study, providing a first comparison with plasma dispersion-based modulators. For each device, room temperature characterization will be performed prior to the packaging and cryogenic tests. Cryo tests will be performed by other partners participating in this WP and WP7-Cryogenic tests, depending on the requirements (purely optical, electrical, DC, and RF measurements). It is worth noting that additional devices could be added in the test plan on the fly (phase change material, others…), relying on inputs from T3.2 and T3.4 that will precise further the system to circuits and devices specifications.

T3.2 Photonics for Cryo

Description:

This task is focalized on the design and fabrication of high-speed photonic integrated circuits operating at cryogenic temperature. While passive devices evaluated in T3.1 may require 'only' some adaptations/customizations, high performances active devices at cryo temperature appear to be more challenging, especially when considering other constraints such as energy efficiency, temperature dissipation, and low swing voltage. Thus, this task will anticipate the need for disruptive modulation and photo-detection solutions. After an in-depth state of the art review together with a device to system level analysis, high-risk designs will be proposed and evaluated. Short-loop of fabrication on small wafer format will be employed to accelerate the assessment of the new design, prior to circuit demonstrators to be manufactured on larger wafer scale (200/300mm). A relatively high level of synergy and coordination between the three other tasks of this WP will be required to ensure that the

high-risk design will be validated within the appropriate timeline for the demonstrators. Two demonstrators will be planned, the first one being anticipated as a proof of concept (POC) that may not reach the full specifications, while the final demonstrator should aggregate the best developments available at the time.

The first goal is to be able to select the best candidates for high performance modulation and photo-detection, but not only taking into account the performances at cryo temperature but also the manufacturability on large wafer scale, thus minimizing the risks in term of integration when the fabrication of the demonstrators will start. CEA will participate to the state-of-the art review as well as the co-development of the PIC (Photonic Integrated Circuit) in regard with T3.3 and T3.4 related to the drivers and system integration. CEA will contribute also to prototyping of advanced devices emerging from either existing solutions assessed in T3.1 and/or disruptive approaches found during the review process (which take into account not only the performances but also manufacturing concerns as mentioned above). Depending on the technological solutions that will emerge from D3.2.4, CEA will lead the realization of the photonics chips for a 1st POC (simplified transceiver operating at cryo temperature) and next the photonics chips for the final demonstrator, both in direction to T3.4 (Photonics sub-system merging the PIC and its driver).

CNRS will design new silicon photonics devices adapted to cryo temperature. In particular, electro-optics effects at such a temperature require intrinsic electronic properties, e.g. Kerr and Pockels effect. CNRS, in collaboration with CEA and STM propose to study different photonic structures and exploit different effect. First DC Kerr will be considered and study in cryo environment. Such effect has already demonstrated promising results and requires a complete optimization and characterization. In parallel, CNRS propose to study Pockels based photonic devices by the hybridization of ferroelectric materials (Lithium Niobate and Barium Titanate) on silicon and silicon nitride photonics platforms. CNRS has also a strong expertise in the development of fiber couplers (grating and inverted tapers), efficient wavelength filters with high power rejection (>100dB) and passive photonic devices (waveguides, ring resonators, Mach-Zehnder interferometer....). CNRS has also all the necessary facilities to rapidly fabricate passive photonic devices using ebeam lithography to validate certain concepts before larger-scale fabrication at CEA and STM.

UGA contribution for this task will be to design and provide a glass-based solution for interfacing the PIC made on silicon with optical fibers. This solution could contain wavelength multiplexing and demultiplexing functions if required. UGA will collaborate with CNRS and CEA to design and chose the most appropriate solution for this interfacing interposer, and will manufacture it before assembling it with the silicon PIC . UGA will rely on its state-of-the-art in-house simulation tools and its technology line dedicated to glass to perform these tasks. Depending on the determined test plan, our cryogenic bench will be part of the PIC qualification plan.

Siemens EDA will contribute to task 3.2 actions by providing access to its available industrial design tools (such as S-edit, L-edit, and LightSuite) and may allocate resources to support research and development work that would be performed when it is relevant.

T3.3 CMOS driver

Description :

This task aims to design the appropriate CMOS drivers for the selected active photonic devices (modulation, demodulation). Considering a diversity of potential candidate physical phenomena used for these photonic devices, the task will be phased in steps from generic functions to co-designed electronics in interaction with the maturation of the photonic devices.

This task will have a high level of interactions with T3.2 and T3.4. It will start with device-independent functions, such as high-speed serializer and deserializer, to focus then on preliminary driver design with voltage or current modulation, with full-swing or low-swing signaling. Once the milestone for photonic device selection is reached, the next step is to specialize the drivers and to integrate all functions. Based on the milestone/deliverable D3.2.4 regarding the evaluation of the first generation of the photonics components for Cryo, a first simplified CMOS driver may be designed in order to qualify the photonic and electronic IC together at cryogenic temperature with reduced

specifications as a proof of concept. Alternatively, external driver will be used, prior to the final driver design work that will be conducted for the Co-design of the demonstrator expected to start M48. The fabrication of the drivers, mostly through foundry runs, and subsequent post-processing is included in this task.

In the longer perspective, analog/RF signaling over photonic links will be studied, and tentative drivers will be designed.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

T3.4 Integrated photonic sub-system for final demonstrator

Description :

This task covers the cryo-compatible transceivers sub-system specifications, from the architecture to the device. One of the main challenge will be adjust the sub-system specification with the inputs from T3.1 on the photonics device assessment, together with the inputs of the other WP that will provide insights on the total power dissipation acceptance, the number of I/Os, or other constraints on the system (density/footprint, packaging, materials…).

In this task, In the first years of the program, CEA will provide system-level specification for ingress and egress needs through an optical cryo-photonic link, and iterate with T3.1/T3.2 to refine requirements in terms of bandwidth, integration, power consumption, interfaces between CMOS and photonics.

In a second phase of the program, CEA will coordinate the integration of the selected photonic devices and drivers in an electro-optical link architecture will be carried out , with potential integration on an optical interposer. This task will involve the interactions with WP6-3D&Packaging for the EIC – PIC assembly/packaging/3D integration and WP7-Cryogenic tests for the Cryogenic equipment for both the 1st POC and the Final demonstration.

Here, for the POC expected at M48 and for the Final demo expected at M72, the Photonic IC fabricated in T3.2 and the associated CMOS Drivers designed in T3.3 and fabricated in WP5-Cryo electronic must be assembled together through Packaging/3D integration in WP6-3D&Packaging (depending on the specs). Subsequently, the transceivers performances will be assessed by CEA in this task at Cryo temperature by coupling the equipment from WP7-Cryogenic tests with high-speed communication setup corresponding to the specifications at both device and system levels.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools as described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

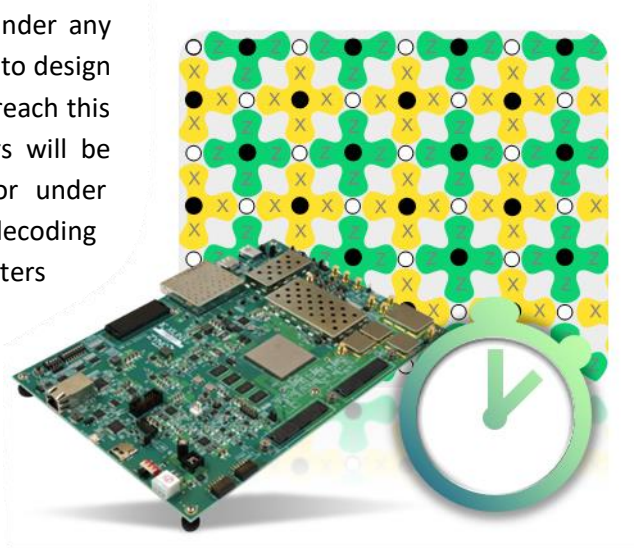
Work package deliverables

D3.1 Final report on Si and glass-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M24)
D3.2 Report on 1st Photonic IC for preliminary POC (M48)
D3.3 Characterization report on integrated cryo-photonic IC for final Demo (M72)

4.4. WP4 Real-Time quantum error correction

4.4.1. Work package objectives

Quantum error correction (QEC) is key to the development of a large-scale, fault-tolerant quantum computer, achieving the full computational power of quantum computing. However, the efficacy of a QEC solution is heavily dependent on its decoder: a classical algorithm that processes the extracted error syndrome to determine appropriate corrections. Previous research essentially focused on the accuracy (i.e., error correction capability) of the decoder, mostly ignoring scalability and real-time implementation constraints (critically, the decoding must be faster than the syndrome generation rate, otherwise it will introduce an exponential time overhead – in the number of non-Clifford gates – which will hinder any quantum advantage). In this context, the ambition of WP4-QEC is to design real-time QEC solutions that scale with the number of qubits. To reach this goal, software and hardware implementations of QEC decoders will be investigated, based either on existing decoding algorithms, or under development within the PEPR project NISQ2LSQ. For each decoding algorithm, a design space exploration will be performed for parameters of interest, to identify best tradeoffs in terms of accuracy, latency, power, and scalability. Acquired knowledge will be fed back to the system modeling in WP1-System model for the complete control chain design. To ensure fast exploration, and increase the adaptability of the design to QEC evolutions, hardware implementation will leverage High-Level Synthesis tools.



4.4.2. Partners Role

Entity	Role
Inria	WP Co-leader Algorithmic Leader Expertise in QEC algorithms and compilation for quantum computing using logical gates
CEA	WP Co-leader Hardware design leader CEA will bring expertise from several teams, from QEC expertise to hardware acceleration design applied to error syndrome decoding and quantum circuit compilation and optimization
Siemens EDA	High Level Synthesis and EDA tool supplier and expertise support to the hardware design teams

Additional contributions from industrial partners joining the program may be added during the project execution.

4.4.3. Detailed work description

T4.1 Software implementation of topological codes decoders
Description: Topological codes (e.g., surface or color codes) are currently seen as the main and most promising approach to fault-tolerant quantum computing, for a wide range of quantum technologies. The prevalent decoding solution is based on the minimum-weight perfect matching (MWPM) algorithm, commonly used to assess the error correction thresholds of topological codes, due to its superior error correction capability (accuracy). However, its complexity scales cubically with the number of qubits, which may prevent its use in practical applications, especially for large

scale systems. Thus, a number of alternative solutions have been proposed in the literature, including greedy or approximate versions of the MWPM decoder, renormalization group based decoding, machine learning techniques based on neural networks, or the so-called union-find decoder.

In this context, the goal of this task is to uncover bottlenecks and identify decoding solutions that lend themselves to low-complexity and high speed hardware. CEA will contribute to the development and the software implementation of decoding algorithms for topological codes. Specific C/C++ coding style required for HLS will be used for the decoder implementation.

The proposed contribution will build upon existing decoding solutions, while proposing further adaptations and/or simplifications, in order to bridge the critical gap between the algorithmic solution and the latency-power-scalability constrained hardware design.

T4.2 Hardware implementation of topological codes decoders

Description:

CEA will design a hardware implementation of topological code decoders provided by T4.1. Typical hardware conception flows augmented with High Level Synthesis (HLS) brought by Siemens will be used to produce the Register Transfer Level (RTL) model implementing this algorithm. Then, exploration of the design space to find good tradeoffs between performance and complexity will be conducted by CEA with Siemens support. Physical synthesis for FPGA and advanced CMOS technologies will be performed to assess the interest of such an accelerator in a large scale QPU and assess power, performance and area.

Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant.

T4.3 Software implementation of decoders from PEPR NISQ2LSQ

Description:

Quantum low-density parity-check (QLDPC) codes are a generalization of topological codes. Similar to topological constructions, QLDPC codes are defined by low (constant) weight generators, which allows simple fault-tolerant syndrome extraction and logical state preparation. Moreover, the QLDPC family has been recently shown to yield good asymptotic codes, with linear minimum distance and constant rate, which augurs for practical constructions with increased error correction capacity or reduced qubit overhead. However, decoding QLDPC codes is in general a difficult problem, constituting a very active field of research, and a number of decoding solutions are currently being developed within the PEPR project NISQ2LSQ.

The goal of tasks T4.3 and T4.4 is to take the developed solutions from the algorithmic level to respectively the software and the hardware implementation stages. INRIA will perform the implementation and benchmarking of the parallel decoders for QLDPC codes having large encoding rate and good error correction capacities , and will further investigate rapid decoding algorithms and provide support for their implementation . Inria will also investigate new LDPC codes designed for biased noise cat-qubits as the absence of one error component could significantly simplify the decoding requirements, and will also study cellular-automaton based decoders for topological codes designed for extremely biased noise qubits.

CEA will focus on message-passing decoding algorithms, for a class of QLDPC codes having the single-shot error correction property. Similarly to T4.1 coding style required for HLS will be used for the decoder implementation.

T4.4 Hardware implementation of decoders from PEPR NISQ2LSQ

Description:

Similarly to the approach taken in T4.2, CEA will study in T4.4 hardware implementation of a selection of decoders from T4.3. Again, HLS will be used for early-stage exploration and then for the identification of performance-tradeoffs. Commonalities between the decoders of various codes will be studied to identify, where applicable, core

IPs that could benefit from more optimization efforts. Finally physical synthesis for FPGA and advanced CMOS technologies will be performed.

Specific hardware implementation for cellular-automaton based decoders for topological codes may also be investigated by INRIA/Quantic as they may be integrated closer to the qubit using similar technologies. Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant

T4.5 Exploration of error correction tradeoffs (correction rate, latency, power, complexity)

Description:

Exploring the design space for efficient error correction requires to challenge its impact at all level, from the qubit topology constraints to the error decoding. Teams with complementary backgrounds will therefore conduct the exploration.

Having performed the hardware implementation of codes, CEA will focus is action on assessing the performance of decoding algorithms in terms of latency, power and resource usage (gates or mm^2); as well as precision, since some codes, such as Edmond's MWPM algorithm, allow to trade latency for decoding accuracy by taking into account error locality.. As achieved precision shall be appreciated depending on the qubit properties, decoding procedure will be evaluated using Monte-Carlo simulations of error propagation for syndrome generation. Several aspects of the QPUs will be taken into account provided that input data is made available by partners developing qubit technologies (qubit connectivity, addressability and intrinsic parallelism, specific gate and qubit error models).

Inria/QInfo will study the limitations the geometry of the physical qubits imposes on the fault-tolerance memory and time overhead. In particular, the maximum encoding rate that can be obtained as well as the best error correction capacity will be determined. Additional work will focus on the efficiency of the standard algorithms for error correction: this includes runtime, latency, communication between the different parts of the processor and power consumption.

Generated data in T4.5 will be integrated in the system model in T1.2.2.

T4.6 Hardware aware compilation of universal set of logical gates

Description:

To exploit the benefits brought by the QEC, one must be able to perform quantum operations over logical gates composed of several physical qubits. Specific computation schemes must be sought out to do so. Task T4.6 will investigate several compilation approaches to provide efficient computing with error-corrected qubits :

(A) When using quantum error correcting block codes, encoding several logical qubits in one block, the set of fault-tolerant quantum gates accessible can be very different from standard gate sets Indeed cases arise where one can have access to a few easy (transversal) gates acting on all logical qubits at once. For instance, in some situations, one can obtain a large circuit of CCZ or CZ on the logical level obtained from a transversal T gate on the physical level. While on the contrary being able to implement targeted single or two qubit gates within the code block is more difficult. Circumventing this often resort to using some tricks such as teleportation, code deformation or Pauli measurements all with additional auxiliary qubits needed making these gates more costly. Inria/Loria will develop compilers able to handle these constrained gate sets will allow to take advantage of the higher encoding rates of block codes without paying too much price in gate implementations.

(B) As the choice of error correcting scheme imposes strong constraints on the computational framework, possibly very distinct from the usual Clifford+T formalism, Inria/QuaCS will study various models of execution and the such as Measurement-based Computation (MBQC), Quantum Cellular Automata (QCA), and exotic gate-sets such as Clifford+Toffoli. The work conducted with the help of graphical languages such as ZX or ZH calculi could lead to the definition of transpilation or code optimization strategies.

(C) As magic state distillation is one of the most resource-consuming primitives in surface code-based quantum architectures, CEA will develop a hardware-agnostic tool that will translate a logical circuit for state distillation into

a sequence of physical gates. Established techniques in quantum circuit optimization will be implemented. Then, a secondary goal will be to adapt this approach to specific architectures whose properties could be shared by industrial partners joining the program.

(B)To further reduce the overhead of error correction CEA/IPhT will develop a systematic numerical method to optimize low-depth circuits working on a limited set of qubits, and will seek to exploit it to optimize stabilizer measurements for different codes, and assess the impact on their correction thresholds.

T4.7 Final Demonstrator

Description :

Concerning the final project demonstrator, options for the QEC contributions are very open at this stage. Indeed, it is yet to be confirmed that large enough qubit resources could be developed by industrial players to allow for their integration in complementary projects leveraging the final LSQ demonstrator. In addition, works conducted in T4.2 and T4.3 may conclude on the need for ASIC implementation of decoders, which is not in the scope of the project to date. Consequently, the practical validation of an error correction loop may be out of reach of the project.

Still, the final demonstrator shall seek to be able to prove correct interoperability between all elements of the control chain. Hence, in a pessimistic scenario, this task will focus on the definition, and implementation of interfaces to the remainder of the control chain for future QEC integration. In an optimistic scenario, the task will aim to provide inclusion of FPGA decoders and practical validation of QEC loop.

Work package deliverables

D4.1 Report on software implementation of adapted QEC decoders with increased scalability potential (M18)
D4.2 Report on refined hardware implementation of error estimator for generic topological code (M30)
D4.3 Report on soft decoders from NISQ2LSQ (M36)
D4.4 Report on hardware implementation of decoders for specific codes (M60)
D4.5 Report on demonstration for quantum error correction (M72)

4.5. WP5 Cryogenic electronic

4.5.1. Work package objectives

Solid-state circuits operating at cryogenic temperature are more and more critical to address the challenges related to quantum computing applications. Indeed, performing operations on quantum bits (qubits) like control and read out, requires classical electronic controllers. As soon as quantum processors become more complex, classical electronic control approaches, requiring multiple RF and DC cables per qubit and each connected to room-temperature instruments, are no longer a sustainable way.

A promising approach consists in considering the integration of read-out and control circuitry in standard CMOS technologies operating at cryogenic temperatures. In such a way, significant form factor is reachable, enabling more qubit control complexity while limiting power consumption and being a cost-effective solution. This work package aims at developing CMOS model & 4K add-on to FD-SOI PDK to enable design-blocks in cryogenic conditions, and at evaluating and maturing electronic amplification devices technologies.

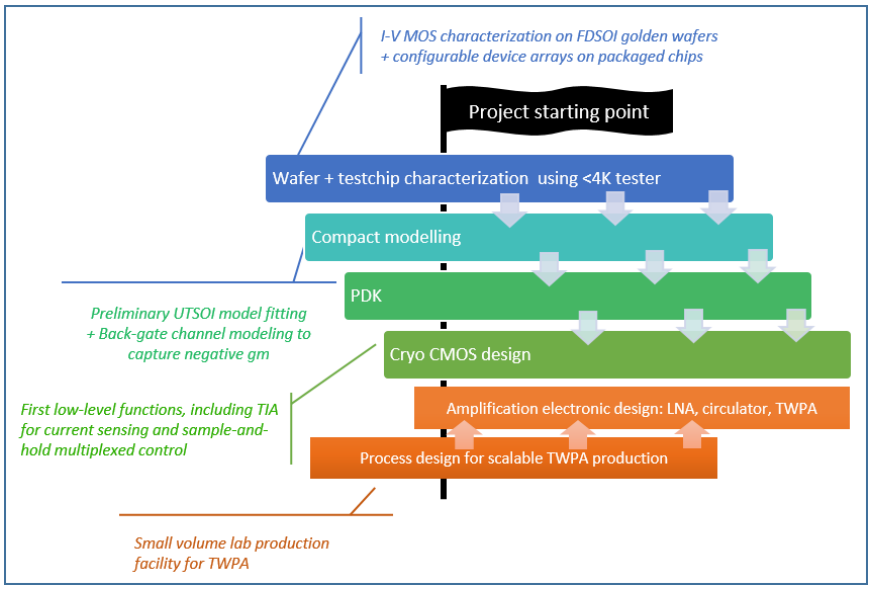


Figure 15 - Logical diagram of WP5 actions for CryoCMOS design

Beside the CMOS circuitry, solid-state qubits read-out and control often use circulators, low noise amplifier (LNA), and several superconducting electronic devices like specific very low power and very low noise amplifiers (known as Traveling-Wave Parametric Amplifiers, TWPA). The project will evaluate BiCMOS and LNA integration together with circulators, and investigate the scaling of production by industrialization of the fabrication process to increase yield. CMOS circuits and electronic components developed in this WP will be integrated in the demonstrator.

4.5.2. Partners Role

Entity	Role
ST MICROELECTRONICS	Work Package Leader Will give access to the FD-SOI technology to update the 28FD PDK for 4K (and possibly 77K) applications.
CEA	Will characterize devices, develop models, and implement designs for cryogenic electronics. Will evaluate electronics devices.
UGA	Will characterize devices (noise and 77K), contribute to models development and to self-heating study. Will contribute to design model evaluations
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design and modeling work in T5.2 and T5.4 tasks.
CNRS	Will contribute to TWPA developments

Additional contributions from industrial partners joining the program may be added during the project execution.

4.5.3. Detailed work description

T5.1 Devices characterizations at 4K (and 77K sampling) for PDK Add-On
Description: This task is very dependent of characterization means availabilities, capabilities and capacities (WP7-Cryogenic tests, T7.1 and T7.2.1). The tasks can start with manual and none statistical characterizations but the full task execution supposes strong amplification and industrialization of characterization means.
T5.1.1 FEOL devices characterization at 4K (and 77K sampling)
Description: To enable circuits 28nm FD-SOI circuits design at cryogenic temperatures especially at 4K, several FEOL devices such as NMOS and PMOS transistors, (if possible according to WP7-Cryogenic tests, resistors, decoupling capacitors, junction diodes) must be modeled. To do so, those devices must first be characterized in various domains, including DC, AC and noise (LFN / RTN for UGA). Then, to address RF applications, extra HF characterization based on S-parameter and possibly Noise Figure (NF) measurements may be needed, coming with their own challenges in terms of calibration procedure (either on-wafer or based on external substrate standards) and linear (small-signal) device operation at cryogenic temperatures 4K (and 77K sampling). According to the previous results and output of WP7-Cryogenic tests T7.2.1, it could be interesting to investigate the statistical approach and measurement strategies in the framework of the pre-industrialization of cryogenic PDK. As a perspective for Year 4 to Year 6, we can consider next FD-SOI generation node characterizations at cryogenic temperature. And for Year 6, high frequency noise measurement at cryogenic temperature.
T5.1.2 BEOL interconnect and RF passives models
Description: Qubits control and read-out require the generation and acquisition of specific RF signals, leading to the need of several RF blocks that could be assimilated as wireless RF transceiver. To enable electromagnetic RF passives modeling and dimensioning at cryogenic temperatures, we have to implement the accurate extraction of BEOL physical values. In addition to low frequency physical parameters, a validation of the above-calibrated stack will be mandatory versus frequency up to 30 GHz if possible according to WP7-Cryogenic tests T7.2.1. The technology considered for BEOL interconnect model and RF passives devices enablement will be the 28nm FDSOI node from STMicroelectronics. Cryogenic temperature of interest will be 4°K (and 77°K by sampling).

As a perspective for Year 4 to Year 6, we can consider next FD-SOI generation node characterizations at cryogenic temperature.

T5.1.3 Reliability tests

Description:

The specific simulation models for the Cryo modeling is planned to be available using a PDK add-on on the existing PDK release. This will require cryogenic environment reliability tests and collection of reliability data. The set-up of wafer level tests at cryogenic temperatures, should allow reliability testing to cover:

(1) gate dielectric and inter-metal dielectric breakdown

(2) NBTI/PBTI aging and

(3) HCI aging in “on” and “off” state mode.

Measurements protocol will first have to be adapted and applied to cryogenic environment.

Based on experimental results, existing reliability models will then be extended down to 4K.

T5.2 Compact model developments for FD-SOI transistors and diode at cryogenic temperatures

Description:

The first year will be dedicated to the improvement of the core’s model. Indeed, at cryogenic temperatures several effects appear such as the observed double kink effect on the drain current in inversion regime and a specific linear-saturation transition. In addition, a first model library containing NMOS and PMOS transistors models in typical case will be implemented in PDK environment. These models will reproduce DC and CV characteristics.

The low frequency noise (LFN) modeling and the substrate modeling will done in the second year. An update of the model library will use the results of these last works. In parallel, a dedicated parameter extraction flow will be optimized for cryogenic temperatures.

During the third year, new MOSFET models for RF applications and models for diodes will be developed always for typical case. They will be implemented in the PDK. The MOSFET model will include the effect of multi-finger layout.

The variability modeling will be done during the fourth year, depending on data availability (WP7-Cryogenic tests industrialization). The goal will be to update the model library by introducing corners and Monté Carlo simulation capabilities.

The 2 last years will be focused on the implementation of reliability models in PDK and several updates of model library by introducing the best experimental data. Finally, during the last year of this project, high frequency noise (HFN) modeling will be covered to improve the RF MOSFET models.

Siemens EDA, will contribute to the actions by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre…) and needed support.

T5.3 First 28FD-SOI PDK 4K (and 77K) add-on implementations

Description:

The specific simulation models for the Cryo modeling is planned to be available using a PDK Add On to the existing 28FD-SOI PDK release. This will require the development of cryogenic models with the constraints of fitting to the PDK model interfaces. This will ease the development and ensure the alignment with the standard PDK for designer community. The Focus will be done on 4K model encapsulations (77K should be an extrapolation and option; not be consider as target for this study) compliant with the process and tools flow in industrial environment.

As a perspective for year 4 to year 6, we can consider a new FD-SOI PDK add-on with variabilities.

T5.4 Cryo CMOS design

In this program, following the analysis performed in WP2-Architecture, CEA will specify and design generic integrated functions for scalability and dynamic control and read-out and exploring FD-SOI capabilities in cryogenic interface electronic for large scale quantum computing.

Because design at cryogenic temperature is not yet possible with appropriate process design kit, CEA will work the methodology to accomplish a valuable design process in the task T5.4.1. In the meantime, UGA propose to work on design modeling.

Task T5.4.2 will aim at designing control, readout and digital communication functions with, if possible, 3 loops of learning.

On both tasks, Siemens EDA, will contribute by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre…) and needed support.

T5.4.1 Cryo CMOS design methodology and PDK evaluation 28nm

Description:

Design oriented models allow simple but efficient analytical design method based on gm/ID or IC parameters. These models are based on charge modeling and use a very small set of parameters (between 3 to 7). Recent works show how such models are well suited to advanced nodes and to low and week inversion regime, where region-based models are limited. In addition, these works show that non-linearities or bandwidth limitation can be captured. The model parameters can be extracted based on few DC measurements which are accessible in cryogenic frameworks.

In this context, UGA propose three research lines:

- Using the models already developed, UGA propose to investigate how these models are suited to cryogenic devices and which parameters are required to capture the MOS behavior in cryogenic environment.
- Based on a design-oriented model and a set of extracted parameters for MOS transistors in cryogenic environment, design methods will be investigated for readout devices.
- The issue of testing cryogenic devices can be investigated through the correlation that could exist between the model parameters at cryogenic temperature and room temperature. Testing methods could be investigate based on this approach allowing the screening out of devices at higher temperatures leaving only good candidates for cryogenic temperatures.

Design learning (CEA): because design at cryogenic temperature is not yet possible with appropriate process design kit, this task is focused on the methodology to accomplish a valuable design process. The objectives are

- to set up a proper asic design and tests flow, based on partial cryogenic PDK
- to design cryogenic benchmarck circuits, analog and digital (e.g. amplifier and integrated logic characterization circuits for flip-flop and combinational gates)
- to benchmark and conclude on design rules and test practices thanks to characterizations results.

First year will be devoted on designing cryogenic test chip analog and digital: schematics design based on gm/id approach (tentative models), simulations at room temperature and approximate projection to cryogenic results, tape out preparation.

Depending on process cycle time, second year will deal with test chip characterizations, retrofit analysis, methodology refinement, and benchmarking of available cryogenic compact models based on circuit simulation vs circuit characterization. Optimized benchmark circuits could be proposed if necessary, depending on results and models development.

During the following years, CEA will continue the evaluations of the PDK add-on upgrades from WP5-Cryo electronic T5.3 through designs and characterizations loops.

T5.4.2 Generic design for demonstrator: Qubit control and readout and digital control, processing and communication functions.

Description:

This task aims at designing ultralow power consumption, Qubit control and readout functions (IP targeted could be: CMOS-based dynamic digital-to-analog converter, analog buffers, high-speed mux and demux, CMOS-based amplifiers and analog-to-digital converter for qubits readout, biasing circuits and oscillators) as well as digital functions for communication interfaces.

The task goes from blocks architecture study to design, and test and characterizations at cryogenic temperature. Different test chips are planned to be fabricated, and some will be designed to be embedded in 3D and supra demonstrators of WP3-Integrated Photonics.

During the 6 years of the program, CEA aims at performing 3 loops of design learning with new functions implementation for each loop.

T 5.5 Amplification devices evaluations at cryogenic temperatures

Description:

The amplification chain requires parametric amplifiers (like TWPAs) and LNA, specified and designed for cryogenic applications.

TWPA: Currently, J-TWPA are being manufactured in academic-grade clean room facilities and rely on fabrication processes that are not scalable nor reproducible enough for the anticipated volumes of TWPA necessary for the future solid-state quantum computing architectures. The development of a CMOS-like fabrication process for reliable and reproducible way to manufacture Josephson junctions is crucial for European Sovereignty. Such process can be developed in the CEA. Furthermore, this development could not only benefit the TWPA manufacturing process, but also laboratories and companies related to quantum information with superconducting circuits.

This task goes from the design of the Josephson junctions (CEA) to their characterization (CNRS-Neel), both at room temperature and at sub-kelvin temperatures (10mK). It could include the design and the characterization of short Josephson junction arrays working as resonant parametric amplifiers as a proof of concept.

Low Noise Amplifiers: current available LNA power consumption is above 20mW. The quantum needs are to reduce from one decade (around 1 mW). This task aims at evaluating ST B55x technology, understanding the limitations, and through integrated design, improving the performance.

Circulators are "must-have" cryogenic components for the most advanced quantum experiments. They are necessary to avoid the noise from the front-end low noise amplifier (LNA) to radiate onto the sample. So far the only available cryogenic circulators which use a local static magnetic field are very bulky (typ. 2x2x1cm3) and they work only at high frequency (several GHz). Recent works using CMOS technology demonstrated that circulators based on transistors can be realized. This tasks aims first at evaluating and characterizing ST CMOS technology to realize circulators. CEA then propose to go beyond the state of the art by combining the best of both worlds thanks to the complementary aspect of BiCMOS technology: using the CMOS part for the circulator and the bipolar (HBT) transistor technology for the best LNA.

Components developed in this task will be implemented in the demonstrators.

Work Packages deliverables:

D5.1 Report on benchmark test and demo1 chip design (M12)
D5.2 Report on Cryo CMOS characterizations report (M36)
D5.3 Report on PDK add-on (M36)
D5.4 Report on demonstrator chip design (M54)
D5.5 Final chip and amplification demonstration (M72)

4.6. WP6: 3D integration and packaging

4.6.1. Work package objectives

The aim of work package 6 is to validate the complete communication chain in terms of cryogenic electro-thermal behavior. As illustrated in Figure 16, the scope of the study ranges from the qubits to the outside of the cryostat. Starting from WP2-Architecture recommendations, system architecture hypotheses will be investigated regarding interconnections key technologies, parasitic and power dissipation. To achieve this goal, low temperature characterizations of raw materials and elementary integrated modules will feed simulation and modeling. A schematic view of the work package is introduced in Figure 17. Task T6.1 will be in charge of the fabrication of test vehicles that will be packaged within T6.2 (it will also include photonics packaging issues stemming from WP3-Integrated Photonics). Experimental characterizations of these packaged test vehicles will be performed in T6.3 and the output data will be used to feed modeling and simulation task T6.4 that will also seek to define a thermal simulation methodology allowing to interoperate low-level simulations in cryogenic conditions with thermal simulation tools already qualified for standard temperature ranges. The methodology will be used to define specifications for the test vehicles of T6.1. Based on the acquired knowledge of T6.1, T6.2, T6.3 and T6.4 outputs, task T6.5 will develop 3D interconnection and packaging solutions to manage optimally heat fluxes and high-frequency signals that will propagate in the final demonstrator.

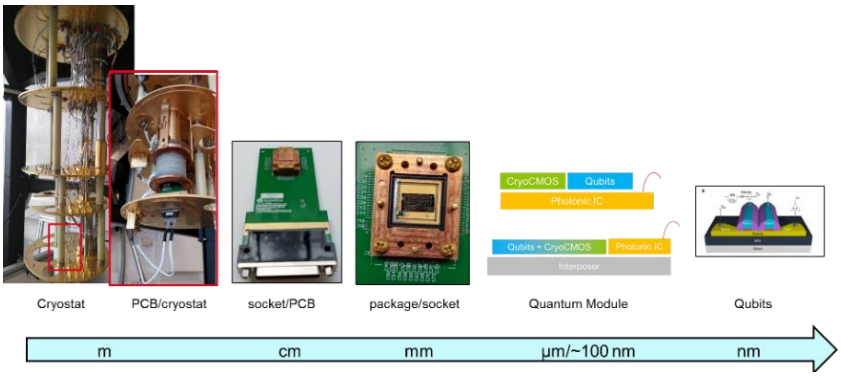


Figure 16 - Scope and range of interconnections of a qubit control chain (Quantum Silicon Grenoble)

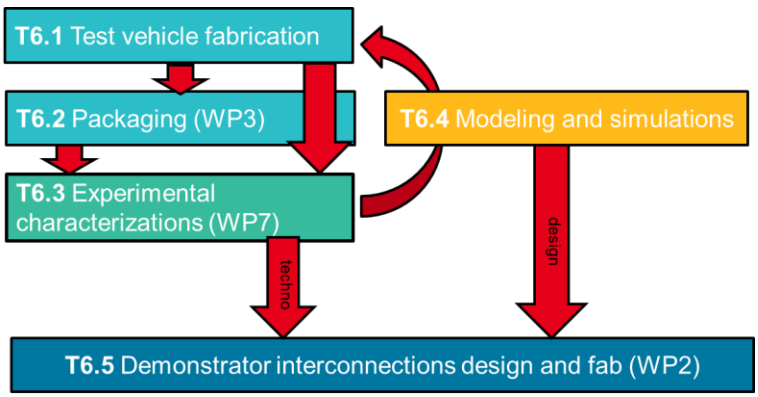


Figure 17 - WP6: 3D & packaging –task chart

4.6.2. Partners Role

Entity	Role
CEA	Work package leader With its expertise in 3D integration technology, demonstrator assembly (e.g. P. Coudrain *et al.*, ECTC (2019)) and superconductor integration (C. Thomas *et al.*, *Mater. Quantum. Technol.*, (2022)), CEA will lead the 3D and Packaging work package.
CNRS	With its expertise in thermal characterization at low temperatures, CNRS will support the work of WP6 through the low temperature tests conducted in T6.3, and will therefore participate in the specification definition and design of the test vehicles in T6.1.
Siemens EDA	Siemens will provide the required support to assess their simulation tools applicability to cryogenic thermal conditions especially in T6.4.
STM	STM would support the work of WP6 by providing short loop BEOL samples for interconnection characterizations at low temperatures, as well as partial MPW wafers (with WP2-Architecture, WP3-Integrated Photonics and WP5-Cryo electronic) for specific CEA post-process for bumps and potential superconducting integration.

Additional contributions from industrial partners joining the program may be added during the project execution.

4.6.3. Detailed work description

T6.1 Test vehicle fabrication
Description: Test vehicles made from, first, raw materials deposited on blanket wafers and then, patterned materials, forming simple structures such as lines and bumps, will be fabricated to build a material and interconnection property database. During a second phase, elementary technological modules (daisy chain assemblies, superconducting multilayer stacks) will also be processed to complete the database and feed the model and simulations tools (T6.3). Process developments will involve superconducting material integration. Post-processing of Cryo elctronic (WP5), Photonic IC (WP3) or Interposer wafers, will be envisioned with respect to developments conducted in the WP2-architecture.
T6.2 Packaging of test vehicles and demonstrator
Description: While Printed Circuit Board (PCB) design & fabrication will be included in WP7-Cryogenic tests, the other packaging items and tasks will be addressed here. It includes the optical fiber attachment (Pig-tailing) in close collaboration with WP3-Integrated Photonics and qualification of the connectors and sockets (with PCB design inputs from WP7-Cryogenic tests). A dedicated study will be conducted on the behavior of co-packaged optics/electronics at low temperature and specifically on Ball Grid Array (BGA) or Quad Flat No lead (QFN) type of packages and their sockets, which will need engineering. Each of the investigated packaging solutions will be evaluated in terms of parasitic and thermal propagation properties.
T6.3 Experimental characterizations
Description: The experimental characterizations will be divided in 3 main families as described below. a) Mechanical and electrical characterizations. This will include the tests of different materials and technological bricks, such as 2D routing lines and 3D interconnects, to extract the following parameters: electrical resistance and capacitance @ 300K, electrical resistance at cryogenic temperatures, superconducting properties (Tc, Jc, Bc) when applicable, Coefficient of Thermal Expansion (CTE) between 300K and 77K (methods to be developed) and E (Young Modulus) @ 300K.

b) Thermal characterizations. This will comprise the experimental measurements in cryostat to extract the thermal conductivities of materials and technological bricks as well as fundamental thermal behavior characterizations for tool/model assessment of T6.4.

c) RF and photonic characterizations. The first objective will be to extract the RLCG parameters of simple structures at 7K using a dedicated VNA and cryo-prober set up. Concurrently, RF characterizations of the packaging environment will be carried out to evaluate signal bandwidth and losses through the packaging supports and sockets with WP7-Cryogenic tests. The second objective will be the elaboration and qualification of the optical test set up and measurement protocol at low temperatures to characterize photonic passive devices and then active ones.

T6.4 Modelling and simulations

Description:

As thermal behavior, drastically changes at low temperatures and small scales, advanced thermal simulations will need to be carried out based on expected behavior of phonon transport. Thermal exchange at small length scale and below 4K, with specific attention to interfaces phenomenon will be explored thanks to dedicate experiments and samples design. Dedicated expert softwares such as Non-equilibrium Green's Function based FeNEGF will be exploited to this end. Adapted strategies for interoperations between low-level (FeNEGF) and system-level thermal simulation (Flotherm) tools will then be investigated in synergy between institutional and industrial actors. This shall enable the definition of a system-level thermal model methodology for cryogenic temperatures that will also be completed with a system-level RF modeling. Depending on software development and Task 6.3 test results , RF simulations will be carried out with the full control chain perspective

T6.5 Control Chain Demonstrator

Description:

The first part of the task will concentrate on the delivery of an optimized design of the control chain interconnections based on thermal, RF and photonic data and models at all scales: integrated photonics, 3D integration, packaging I/O, PCB design, cryostat cables in close link with WP2-Architecture, WP3-Integrated Photonics and WP7-Cryogenic tests. The second part of the task will address the demonstrator module fabrication itself with incoming components such as photonic dies form WP3-Integrated Photonics, CryoCMOS dies or wafers from WP5-Cryo electronic and PCB from WP7-Cryogenic tests.

Work package deliverables

D6.1 Report on first samples characterization (M24)
D6.2 Report on system-level thermal model (M36)
D6.3 Report on control chain demonstrator module design (M54)
D6.4 Report on control chain demonstrator module fabrication (M72)

4.7. WP7 Cryogenic characterization

4.7.1. Work package objectives

This work package aims at addressing the cryogenic characterization needs of the other work packages. CEA, CEA, CNRS, UGA already have cryogenic characterizations capabilities, but our first analysis highlights that the LSQ program will need additional testing resources since existing facilities workload is already high. In addition, the scaling naturally calls for statistical characterizations, which in turn require tools and characterization methods industrialization.

First actions in Task 7.1 will then aim at evaluating missing capabilities and capacities to address the program needs, defining the specifications, acquiring and installing needed tools and upgrades.

Besides the hardware needs, characterization methods, both at wafer level and at system level, need to be developed and improved. Task 7.2 will address these actions.

Task 7.3 will implement appropriate automation and systems to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

Finally, as required for nowadays qubit control, we expect that room temperature electronics will be needed using either RF signal sources as well as optical ones. Signal shaping solutions, adapted to the scaling, and able to interoperate with QEC may also be required for test and demonstration purposes and task 7.4 will address these points. As all work packages will need access to characterization tools, last task is the coordination and scheduling of these accesses.

4.7.2. Partners Role

Entity	Role
CEA	Expertise and infrastructures for cryogenic test and room temperature electronic
CNRS	Work Package Leader Expertise and infrastructures for cryogenic test
UGA	Expertise on Self-heating phenomena

Additional contributions from industrial partners joining the program may be added during the project execution.

4.7.3. Detailed work description

T7.1 Equipment needs identification & equipment acquisition

Description:

Our first analysis highlights that the LSQ program will need statistical characterizations, which require tools and characterization methods industrialization. Typically, WP5-Cryo electronic requires strong amplification and industrialization of characterization means for DC, RF and aging: 28FD PDK 4K add-on needs statistical wafer level characterization.

Statistical test required (wafer level)	**Availibility (CEA or CNRS or UGA)**
DC	Die only. Cryogenic prober available but strong need of industrialization.
RF	Die only. Cryogenic prober retrofit needed and probe card concept at cryogenic temperature to be evaluated: Instrumentation for MOS characterization (DC up to 1MHz) may be needed. Cabling for RF measurements up to few tenth of GHz
Aging	Die only. Cryogenic prober available but strong need of industrialization.

CEA manual cryogenic prober (Lakeshore CPX) are currently working with open loops cooling systems. To limit the project environmental footprint and reduce operation expenditures that would spur with test industrialization, we will plan the necessary upgrades. Some may also need an upgrade of RF probes for more reliable measurements. UGA's 6 arms prober is DC only and RF upgrades on 2 arms would add some capacity for RF characterizations.

Besides tools capabilities and industrialization needs, we suspect that scaling up will increase the need for statistical wafer level characterizations and therefore may require supplying a second cryogenic prober, and some manual probers.

For single transistors or devices characterizations (WP5-Cryo electronic), RF and photonic characterizations (WP3-Integrated photonics & WP6-3D&Packaging), new cryostat and control electronics capacities may be needed both at CEA et CNRS.

This task aims at evaluating the exact needs of the program to define the investment plan for upgrades, or new tools supply, in coherence with 'Cryogenic Plan'. An in-depth analysis of characterization volumes, put in perspective with existing equipment workload and productivity ramp-up, will be conducted to assess the benefits of such investments.

T7.2 Characterization methods developments

Description:

Besides the hardware needs, characterization methods, at all levels (from transistor to system) and scales (from single device to wafer), need to be developed and improved. Task 2 will address these actions.

T7.2.1 DC, RF and Aging Cryogenic wafer level probing pre-industrialization

Description:

Due to cryogenic conditions, the cryogenic wafer level prober needs specific designs on the last metal levels: pad pitches need to be relaxed compared to standard 28FD technologies and additional alignment structures are required in each die.

The first part of this task aims at specifying the last metal levels dimensions and structures required to speed up and improve the cryogenic characterization at wafer level. These specifications will apply to all wafers requesting cryogenic probing. Some wafers already available may need post processing (2 mask levels) to fit in the cryogenic probing specifications.

In the second and third part of this task, after the appropriate upgrades for RF measurement, RF probe cards will be evaluated to assess the RF characterization capability (frequency level) at wafer level at 4K. If some relevant conditions can be obtained, RF test protocols will be implemented.

In parallel those two phases, depending on tool workload, some DC and/or RF and/or Aging tests methodologies will be evaluated/optimized:

Example for DC: statistical measurement through addressable transistor arrays

Example for RF: impact mitigation of self-heating

T7.2.2 RF cryogenic characterization process development.

Description:

To evaluate RF performances and acquire data for a future RF cryogenic compact model, specific RF structures that can be measured on manual cryogenic prober with 2 RF pads (GSG) are needed, with various dimensions (W, L, number of finger gates…) oxide thicknesses (GO1, GO2),... New RF design with access to the back gate is required to fully take advantage of FDSOI capability at low T.

RF test protocol down to 4K need to be optimized as well.

M1-M24 : specification and evaluation of FDSOI test structures required to perform RF measurements at cryogenic temperature.

M1-M72 : all along the project, improvement of the test protocol, including optimization of the calibration and de-embedding procedure. Development of new characterization methods if needed.

T7.2.3 Self-heating phenomena evaluation and impact simulation on cryogenic characterizations

Description:

In FDSOI devices, the outflow of the heat generated at the drain side is impeded due to the low thermally conductive materials constituting the channel. Therefore, self-heating effects (SHEs) lead to a significant increase in the channel temperature when the device is tested. This temperature increase can severely affect the characterization results one intends to upload in the cryogenic models.

This task aims at evaluating the self-heating impact on characterization results compared to real operating conditions to adapt the characterization protocols if needed (to be done in task 7.2.1 and/or 7.2.2).

T7.3 Characterization PCB and systems design.

Description:

In relation to WP5-Cryo electronic tasks 5.4.1, 5.4.2, but also from WP3-Integrated Photonics, WP6-3D&Packaging and for program demonstrators, tests methodologies have to be developed to reduce test setup in cryostat environment, to implement appropriate automation and hardware equipment to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

First year will be devoted to a diagnostic on existing hardware and software equipment, and to the evaluation of the constraints of multi-site cryostats settlement. On this basis, a new test board architecture, as generic as possible to cover all WP needs will be proposed and designed.

Second year will be focused on fabrication, debug of the test bench (at room temperature and then cryogenic temperature), and application to the different WP samples.

The following years will be an iterative process to adapt test methodologies and design test boards and the task will be conclude by a proposal of system designs strategies for the scaling up.

T7.4 Room temperature electronics for test and demonstration

Description:

Current Qubit control uses lab equipment leveraging FPGA for signal generation as it provides more flexibility for signal shaping feedback than traditional AWG. Industrial vendors such as Quantum Machines, QBlox or Zurich Instruments, market such devices, but they come with a consequent price and cannot be easily extended due to their closed source nature.

With the technologies envisioned for the scaling up of the control, such equipment's will face significant evolutions depending on the selected technology path. The use of optical channels, or the interactions with QEC decoders, may structurally modify their requirements.

Consequently, to provide the flexibility needed for the program tests and demonstrators, task 7.4 will initially seek to design signal generation solutions able to adapt to the project needs. Then, drastic evolutions may be required to cope with system design decisions for the demonstrator. This task would leverage existing competences both at CEA in target specific signal generation using commercial FPGA. Should these pieces of equipment be proven as a limit to the scaling, this task may also address their ASIC performance projection to provide necessary insight for system analysis.

Another development is envisioned on FPGAs: the high-speed link (whether copper or fiber) between cryo chips and room-temperature control electronics will require IPs for handling up and down-link communications. Presently a SerDes is developed as a primary brick in this scheme and the higher layers of protocol will have to follow.

T7.5 Characterization coordination and scheduling

Description:

Most of the work packages will need cryogenic characterizations: each work package will be in charge of its measurements in the cryostats or on the Lakeshores. This task aims at organizing the tools accesses, at CEA, CEA and CNRS facilities.

Work package deliverables

D7.1 Report on needs evaluation and investment plan (M6)
D7.2 Final report on tools upgrade and installations (M24)
D7.3 Report on self-heating impact on characterization results (M36)
D7.4 Final report on demonstrator characterizations (M72)

5. APPENDIX

5.1. State of Art review

To put in perspective the proposed work plan, the following section aims at providing a synthetic positioning of the technologies at the heart of the proposal with respect to the state of the art, with key references in the domain.

When considering the new field of system modeling for quantum computing, most works either (i) model the hardware in detail [6], [7] but not the quantum operations that enable the computer to function, or (ii) provide simulators that model the quantum operations [8]–[10] without considering the hardware resources that they require. These two aspects were combined in a new full-stack approach by the CNRS team [11], which exhibited intricate feedback loops between hardware (e.g. cryogenics, control electronics, …) and software (the choice of quantum operations that implement an algorithm, quantum error correction, etc). It showed how to optimize, and find the sweet spot where the computer functions as desired, while having technologically accessible specifications for each hardware and software component, and a sober use of physical resources. To provide ever more intelligence to the system designers, this full-stack model needs to integrate the evolution of the control electronics and more specifically the ones developed in the project.

As for the control architecture, approaches in the state of the art are most often focusing on key elements in the chain than on the overall system architecture. Indeed, the notion of large-scale architecture in quantum computing may cover very different areas, from base arrangement of qubits [12], [13], to software stack [14]. In terms of hardware control chain, after decades of few-qubit physics experiments, multiplexing has been considered since 2015 [15], [16]. Hardware in the loop with dedicated controllers has been originally proposed by Delft and QuTech in 2016 with a digital-intensive architecture [17]. Multiple-layered architectures with intermediate temperatures for CryoCMOS were proposed in 2018 [18], and first small-scale realizations in line with qubit specifications [19] originated from the main early solid-state qubit actors, Intel [20], IBM [21], Google [22], followed by academia [23], pushing new concepts such as single-flux quantum logic [24].

One key aspect that the control architecture must address lies in the extraction of data processed in the quantum domain inside a cryostat. In particular the LSQ will focus on how optical communications can be leveraged to meet the bandwidth called by the scaling. Indeed, we find in the literature some significant works [25], [26] that highlight the added value of optical links to provide a high-speed transduction able to channel the large amount of information to room temperature servers, but also to provide a solution that will limit the heating in the cryostat and the thermal exchanges by replacing the coaxial cables by fewer optical fiber(s). This approach requires a number of developments in order to realize transceivers meeting all the presupposed specifications of the system. In particular, these transceivers will have to operate at high speed at cryogenic temperature, and although the passive routing and coupling components can be adapted from known components at room temperature, the active components will have to be largely revised. Their specifications in terms of bandwidth (modulators, photodiodes), energy balance (to limit heating), or driving voltage will be challenged compared to the existing ones at room temperature [27], [28]. In this respect, several technologies stand out in the literature, such as Pockels effect modulators, inorganic [29]–[31] or hybrid [32], plasma effect modulators [33], or Germanium [34] and III-V [35] photodetectors. *In fine*, additional criteria of co-integration with the driving electronics, packaging of the circuits to the cryo constraints (cf WP6), or manufacturability must also be taken into account. We can also add the optimization of circuit calibration to the list of issues [36]. As classical optical phase shifters consume and dissipate a lot of energy, recent works in the field of AI

photonics and quantum photonics draw interesting alternatives, with for instance the emerging of non-volatile chalcogenide phase shifters [37]. All of this work at the scale of transceiver components will be critical – together with CEA's expertise in the field of photonic interposers for disaggregated computing architectures [38] – in meeting the challenges at the circuit and system levels

Aside from the issue of extracting significant amount of readout data from the cryostat, comes the issue of being able to identify error sources and correct them by means of QEC. In a fault-tolerant quantum computer, the QEC decoder design faces significant challenges, with major implications on the control electronics of the quantum system. These challenges arise from the need to integrate into the QEC decoder design various system constraints, such as accuracy, bandwidth, latency, power-consumption, or scalability [39]–[41]. At the algorithmic level, QEC decoding solutions usually focus on the accuracy constraint, with the latter constraints being only considered from the limited perspective of the time/space algorithmic complexity. For topological quantum codes, a number of decoding algorithms have been proposed in the literature, including the minimum-weight perfect matching (MWPM) [42], greedy or approximate versions of the MWPM [41], [43], renormalization group based decoding [44], machine learning techniques based on neural networks [45], union-find decoding [46], or trimming decoding [47]. Significant advances have also been made over the last years for the general case of quantum LDPC codes, e.g., [47]–[50]. Recent research has focused on the design of hardware architectures capable of efficiently implementing QEC solutions, e.g. [51]–[56], however, real hardware implementation results have hardly been reported so far in the literature.

Being able to provide integrated electronics capable of performing the qubit operations as well as readout is key to reach scalability of the control. Several technologies will be investigated in the project from CMOS to specific parametric amplifiers for readout. CMOS based circuits in cryogenic conditions (Cryo-CMOS) have been firstly discussed during the 60's [57], [58]. At the time, the interest was justified by the increased speed, steeper switching, reduced noise and study of temperature dependent physical mechanisms such as, intensification of interface states and quantum effects [59] . Nowadays, Cryo-CMOS technology gains attention rapidly for its compatibility and excellent properties as control circuits at low temperature environments. The attention is mostly focused on quantum computing applications [60]–[62] where qubits [63] requires a readout unit operating in close proximity to avoid long cables and latency. Fully depleted Silicon On Insulators (FD-SOI) MOSFETs, except the improved electrostatic control and reduced floating effects at room temperature [64], show also some excellent characteristics at cryogenic conditions [65]. For this reason, a wide range of reports is oriented towards the understanding of the mobile charge [66] transport mechanisms [67], [68], switch characteristics [69], identification of zero temperature coefficient [70] , self-heating effects [71] of FD-SOI at approximately 4K. Regardless of the extensive reports on FD-SOI and similar CMOS devices [72], [73], there are still several difficulties on the development of a compact model accurate and robust in the full range of temperatures, with a few attempts on implementing corrections to existing models [74], [75]. On this basis, a physics based Cryo-CMOS compact model that incorporates the low temperature effects is required to drive the design and development of cryogenic circuits.

Looking into usage of CMOS technology for cryogenic quantum IP design, one can observe that research efforts for the control and reading of qubits have steadily increased since 2017. EPFL has proposed several chips permitting the simultaneous reading of quantum dots [76], [77]. Intel has designed "horseridge" chip using a 22 nm FinFet technology [78]. As of today, it is the most advanced SOC that allows the control, manipulation and reading of 6 Qubits. Google has proposed a control chip for superconducting qubits with a power consumption of 4mW per qubit which is the best power consumption so far [22], [79]. CEA has designed several chips for the reading (Transimpedance Amplifier[80]),

and for the static control of small matrix of QuBits (DACs)[81]–[84]. So far, the proposed solutions lack in scalability, because of their under-optimized bandwidth, area and power consumption per qubit that is still several of magnitude order greater than needed to address large matrices. Getting accurate models of passive and active components is a key towards the design of optimized and reliable cryogenic circuits and architectures, and is therefore a key target of the LSQ program.

High-fidelity qubit readout requires amplifiers with added noise near the quantum limit of noise. These amplifiers – called quantum-limited amplifiers – must be made of superconducting materials, either high kinetic inductance materials or Josephson junctions, to guaranty the lowest loss possible.

The first Traveling-Wave Parametric Amplifier based on superconducting material was initially implemented in 2012 with high kinetic inductors by the Jet Propulsion Laboratory, in California [85]. They kept working on this technology over the year and recently published [86].

Three years later, in 2015, the first TWPA based on Josephson junctions was implemented by a collaboration between two US based laboratories (Berkeley and the MIT Lincoln Lab) [87]. This project is now mainly carried out now by the MIT Lincoln Lab and it works on improving this technology [88]. To be noted that on the same year (2015), Google Lab also published a paper based on the same architecture [89].

One of the most promising architectures is the traveling-wave architecture, which either needs millimeter long high kinetic inductance strip lines or long arrays of Josephson junctions. The latter option, a Josephson-based traveling-wave amplifier (J-TWPA), allows to have near-quantum limited amplifiers with very low power consumption (less than a nanowatt). In Europe, several experimental research teams are working on Josephson TWPA. The PTB in Germany worked on a three-wave mixing TWPA [90], Néel Institute in France has implemented a four-wave mixing TWPA based on a standard scheme (dispersion engineering) [91] and on an original scheme (nonlinearity engineering) [92]. Chalmers University in Sweden has worked on TWPAs since 2016 [93], and recently published a new work on three-wave mixing TWPA [94]. Finally, a consortium of teams in Italy are currently working on Josephson TWPAs [95].

In Israel, an experimental research team from the Hebrew University of Jerusalem has recently published their work on a TWPA based on a high kinetic inductor material [96]. The NIST in the USA is also working on high kinetic inductor TWPA [97] and recently published their work [98].

Finally, three European-based companies are selling JTWPAs: Silent Waves, in France; their product is based on the work done at the Néel Institute. The VTT, an RTO in Finland; work with their device has been published [99]. QuantWare, a startup in the Netherlands; no published work.

All of the above-mentioned cryogenic components rely on different technology process that will need to be tightly co-integrated to ensure a high connection density while minimizing signal loss and thermal conduction towards the qubits. Large-scale integration of qubits makes packaging more and more complex especially due to an increasing number of input and output signals to carry along the different stages of a cryostat. Three-dimensional (3D) architectures comprising qubits and their associated control electronics are thus envisioned [100] [101] and recently, the first multi-chip assemblies hosting superconducting or spin qubits were fabricated [102]–[105]. Within the full qubit control chain, ranging from the cryostat cables to the multi-chip assemblies, careful designs, sizing and material choices are required at all stages to optimize the whole system operation. The following aspects are particularly important: thermal management, reduction of parasitics signals and improvement of passive compound

performances. To the authors' knowledge, little to no experimental data are available on the electrical, thermal and radio-frequency properties of the different bricks forming the control chain. For example, at the scale of the multi-chip assemblies and close to the cryostat base temperature, only a few data are available on the electrical properties of interconnects (routing lines [106], [107], through-silicon vias (TSV) [108], under bump metallizations and microbumps [109], [110]) and on the radio-frequency [111] and thermal properties [112]–[115] of compounds made from such technologies. Acquiring more data is essential to help developing modeling and simulation tools, especially concerning heat transfer [116] [117] along the control chain as this can directly affect the qubit coherence. In addition, even if some multi-fiber optical packaging examples at low temperature were reported [118]–[120] , mechanical failures occurred and the overall approach needs to be tailored to improve yield.

The development of the technologies investigated by the project will require innovative test bed to address measure requirements in stringent conditions. Indeed, RF characterization at low temperature is not straightforward due to the experimental environment (He cryostat, limited sample size,..) [121]–[124]. Improvement are still required to perform reliable measurements down to 4K and up to 40GHz on both transistors and passive components [125]. All reliability procedures also need to be revisited [126], [127]. High throughput DC measurements, needed to acquire large statistics and build compact models, remain to be addressed using different strategies both at circuit level [128]–[131], and at wafer level using a 300mm wafer prober [132], [133]. For now, only few works have addressed the self-heating effect in CMOS transistors down to 4K [115], [133]–[136]. A high temperature rise can be observed during low temperature operation, which needs to be accounted for in other electrical characterization methods (DC and RF).

Another major issue when implementing LSQ is the scalability of room temperature control, measurement and feedback. Since quantum feedback must answer three major constraints of latency, flexibility and scalability, current architectures use networks of FPGA to implement room temperature electronic. Major projects in the domain comprises open-source academic systems [137], [138], scalable academic systems [139]–[141], industrial projects [142], [143] or systems already available on the market like 'Quantum-Machines'. Those architectures focus on superconducting qubits extensively using AWGs, which does not scale. Two main platforms focus on spin qubits: one still using AWGs [144] and another one from Intel using on-the fly generation with better scalability [145].

5.2. Scientific excellence

5.2.1. Involved laboratories research institutions

CNRS

The French National Centre for Scientific Research is among the world's leading research institutions. .The National Centre for Scientific Research is an interdisciplinary public research organisation under the administrative supervision of the French Ministry of Higher Education and Research. (More 1 100 research laboratories in France and abroad, 33 000 people dedicated to research).

CNRS, Néel Institut, UGA-G-INP / QuantECA

The research activities of the Néel Institut cover a wide range of scientific fields: superconductivity, quantum fluids, new materials, and crystallography, surface science, quantum nanoelectronics, nano-mechanics, nonlinear and quantum optics, spintronics, magnetism. The 450 members of the laboratory are partitioned into research teams and technology support groups according to their common goals of sharing, concerns, expertise.

In the QuantECA research team, specialized in superconducting and spin qubits (Quantum Electronic Circuits Alps, 14 permanents, more than 35 non permanents), members share common research interests and develop original experimental techniques for electronic transport measurements and microwave techniques to observe and control quantum effects in various different materials. To have access to quantum coherence effects in electronic systems and to their coherent manipulation, very stringent experimental conditions are required such as very low temperature, very low noise and weak measurement signals, microwave techniques as well as high quality nano-fabricated samples. The team is strongly involved in building novel experimental set-ups to control multi-qubit systems, to develop quantum-limited amplifiers, to develop opto-electronic techniques compatible with cryogenic environment and to develop cryogenic refrigerators.

CNRS C2N

The Centre for Nanoscience and Nanotechnology (C2N) is a joint research unit between the CNRS and Université Paris-Saclay. The C2N develops research in the field of material science, nanophotonics, nanoelectronics, nanobiotechnologies and microsystems, as well as in nanotechnologies. In all these fields, its research activities cover all the range from basic physics to applied science. The C2N Technological Facility are hosted in a clean room of 2 900 sqm, dedicated to nanofabrication processes, to the growth, the epitaxy and the characterization of materials. C2N cleanroom is part of the French network of large high-end facilities (RENATECH) coordinated by the CNRS. The MINAPHOT team at C2N has extensive expertise in integrated photonics. The leadership of the group is composed of international renowned researchers in the field, including Dr. Alonso-Ramos (ERC consolidator 2022), Dr. Vivien (ERC consolidator 2015), Dr Melati (ERC Starting 2021), Prof. Cassan and Prof. Marris-Morini (ERC Starting 2015). Their research expertise covers a wide range of silicon photonics topics ranging from high-speed optoelectronic devices, on-Si hybrid integration, mid-IR and near-IR photonics, quantum well nanostructures, to nonlinear applications (including Brillouin interactions). All their knowledge combined with the experience of the more than 15 Ph.D. students and postdoctoral researchers in the group create a unique environment for the successful development of the project and the transfer of knowledge.

CEA

The CEA, (French Atomic Energy Commission) is a Governmental Research Organization (15000 employees) devoted to both fundamental and industrial R&D in three main areas: energy, technologies for information, and defense and security. Within CEA, several institutes and technology platforms have been involved in the research and development of quantum technologies for more than 10 years.

CEA LETI

The Laboratory for Electronics & Information Technology **(CEA-LETI)** is focused on micro and nanotechnologies and their applications, from wireless devices and systems to photonics, biology and healthcare. Founded in 1967, CEA-LETI is a French technology research institute that pioneers micro / nanotechnologies, with 11 000 m2 of cleanroom space, 160 M€ of 200 and 300 mm wafer processing equipment, 1900 research engineers. CEA-LETI is strongly committed to industry and puts a strong emphasis on technology transfers and innovation. Strongly focused on value creation for its industrial partners, LETI puts a strong emphasis on intellectual property and owns more than 3200 patent families.

The Silicon **Technology Division** (about 600 research engineers) is in charge of all the technological steps execution, necessary to manufacture devices (lithography, implantation, stripping, etching, deposition, thermal treatments, CMP, metrology, process development and tool maintenance, etc.). The level of skills of the engineers, the wealth of equipment places this technological platform at the forefront of Europe and very competitive at the world level.

Silicon components teams who are designing new devices and their fabrication process flows in areas such as substrate engineering, MEMS, CMOS, RF components, power devices, memories and quantum technologies. This division also has a strong expertise in 3D stacking technologies. Many projects are build and carried out in partnership with industrial partners coming from France, Europe, the US and Asia.

The photonic division has developed solid expertise in imaging information displays solid-state lighting, optical communications and optical sensors. The activities are based on a wide range of materials, from III-V and II-VI and process technologies compatible with 200 and 300 mm silicon wafers. CEA-Leti's photonic platform developing optical components and systems in a diversity of application from telecommunications, cybersecurity, health to augmented reality. It covers every aspect of their development: device design, semiconductor technologies, component manufacturing, system integration, and packaging.

CEA LIST

A leader in research, development and innovation, the CEA, French Alternative Energies and Atomic Energy Commission (Commissariat à l'énergie atomique et aux énergies alternatives), is active in four main areas: low-carbon energies, information technologies and health technologies, Large Research Instruments, defense and global security. In each of these domains, the CEA relies on a high-level fundamental research and ensures a role of support to the industry.

Within the CEA Technological Research Division, the CEA LIST institute carries out research on intelligent digital systems. Its R&D programs, all with potentially major economic and social implications, focus on advanced manufacturing (robotics, virtual & augmented reality, non-destructive testing, vision), embedded systems (computing architectures, software and systems engineering, security & safety), and ambient intelligence (sensors, instrumentation & metrology, communication & sensory interfaces, data processing & multimedia). By developing cutting-edge technological research with applications in the industrial markets of transports, defense and security,

manufacturing, energy and health, the CEA LIST helps its partners to enhance their industrial competitiveness thanks to innovation and technology transfer (https://list.cea.fr).

UGA:

A multidisciplinary institution located in the heart of the French Alps, Université Grenoble Alpes (UGA) is renowned for its scientific and technological research activities, aimed at providing essential training to students and faculty and at addressing societal issues. In a unique partnership with national research institutions (CEA, CNRS, Inria, Inserm and Inrae) and in association with the major international instruments (ESRF, ILL, EMBL, IRAM, GHML) present on its territory, UGA is building its research and innovation policy on a global scale. UGA's strategic ambition is to strengthen its leadership in research and education in order to build a major international, eco- and socio-responsible university. (73 research Units, 124 ERC since 2007, 10 400 staff)

UGA- IMEP-LaHC

IMEP-LaHC laboratory is a joint research unit based in Grenoble and Le Bourget-du-lac, whose activities are based on three main themes: microelectronic devices, photonics and electromagnetism. Two transverse axes have recently emerged, due to strong collaborations between the teams on common themes on sensors and opto-electronics applications. Research of IMEP-LaHC is dedicated to the understanding, development, fabrication and characterization of devices for a wide range of applications, such as the environment, health and information and communication technologies. In this framework, and using its known expertise, IMEP-LaHC is currently involved in the new field of quantum technologies, especially dedicated to Cryo-CMOS and quantum photonics applications.

UGA-TIMA laboratory

The TIMA laboratory has been for almost 3 decades a major academic actor in the French and Grenoble landscape. It addresses the fields of integrated circuit design, MEMS, analog circuits, digital circuits, CAD tools and multiprocessor integrated systems. Among the 4 research teams that compose the laboratory, RMS team focuses on the design and reliability of analog RF, mmWave and mixed circuits. For 6 years, the RMS team works on design-oriented MOS model suited for several applications such as early design with non-mature PDK as it is the case in cryogenic applications. RMS team expertise in circuit design (RF and BF) using such design-oriented model is a strong advantage for the project. In addition, TIMA lab is strongly involved in the CIME nanotech which operates HOG facilities for measurement and the CONCEPTION facilities for CAD tools which will be accessible in IRT framework.

INRIA

Inria is the French national research institute for digital science and technology. World-class research, technological innovation and entrepreneurial risk are its DNA. In 215 project teams, most of which are shared with major research universities, more than 3,900 researchers and engineers explore new paths, often in an interdisciplinary manner and in collaboration with industrial partners to meet ambitious challenges. As a technological institute, Inria supports the diversity of innovation pathways: from open source software publishing to the creation of technological startups.

Inria was a pioneer on the quantum computing scene, at both a French and European level. The Institute first began research on the subject back in 2001 and now has a clear ambition with regard to quantum computing, which was outlined as a priority in its Objectives and Performance Contract 2019-2023.

In the context of the LSQ program, 5 Inria Teams focusing on quantum technologies will contribute to project' success by bringing their complementary expertise:

- The activities of the QUANTIC (QUANTum Information Circuits) team are defined at the theoretical and experimental border of the emerging field of quantum engineering with an emphasis on the applications in quantum information, computation and communication. The main objective of this interdisciplinary team, formed by experimental physicists and applied mathematicians, is to develop both theoretical methods and experimental devices ensuring a robust processing of quantum information. The research work within COSMIQ (Code-based Cryptology, Symmetric Cryptology and Quantum Information) is mostly devoted to the design and analysis of cryptographic algorithms, in the classical or in the quantum setting. The team mixes fundamental aspects and practical aspects of information protection (cryptanalysis, design of algorithms, implementations).
- The goal of the Mocqua team is to tackle challenges coming from the emergence of new or future computational models. The team investigates these new models and tries to solve their intrinsic problems by computational and algorithmic methods. These models includes programs working with qubits (quantum computing), programs working with functions as inputs (higher-order computation) and programs working in infinite precision (real numbers, infinite sequences, streams, coinductive data ...).
- The QuaCS team is specialized in languages and formal methods dedicated to quantum computation. The tools considered by the team members involves domain-specific abstract models, graphical and programming languages, type systems, and dedicated logical systems.
- The QInfo team focuses on various aspects of quantum information theory. In particular, it aims at developing mathematical and algorithmic methods to analyse the behaviour of noisy quantum devices and to reduce the undesirable effected caused by noise on quantum information processing tasks.

5.2.2. Key Involved scientists

Olivier Bourgeois, CNRS Institut Néel

Dr. Olivier Bourgeois (OB) is currently a Research Director of CNRS in Institut NEEL. He is the head of the TPS group, co-director of the GDR NAME. He obtained his PhD in Condensed Matter Physics from UGA (Grenoble, France) in 1999. He was a post-doctoral fellow in the lab of Prof. Dynes at UCSD California. He has directed fifteen PhD students and ten postdoctoral researchers, and was involved in 5 EU projects and 10 ANR national projects (as leading coordinator or as partners), raising more than 5 M€ in grants. He has also published more than 80 peer-reviewed articles in high-impact journals obtaining 2000 citations. He has developed an internationally recognized expertise in nanothermal physics from very low temperature phonon physics, materials science for energy. Olivier Bourgeois is strongly involved in industrial innovations coming from the results of fundamental science (4 patents). He is co-founder of the MOïZ start-up with D. Tainoff.

Nicolas Roch, CNRS Institut Néel

Nicolas Roch is a Permanent staff researcher at CNRS-Néel Institut since 2013. After graduating in Physics at Joseph Fourier University of Grenoble in 2006, he obtained his Ph.D. at University of Grenoble in 2010 and worked at Ecole Normal Supérieure (ENS) under the supervision of B. Huard and M. Devoret from 2010 to 2012 and at UC Berkeley

under the supervision of I. Siddiqi from 2012-2013 as Post Doc. He was among the firsts to design, build and operate quantum-limited Josephson parametric amplifiers and to integrate them into microwave measurement chains for advanced quantum experiments. His main research interests are now focused on many-body quantum optics, quantum-limited parametric amplifiers, Josephson junction meta-materials for high impedance quantum circuits and QND measurement in quantum mechanics. He received an ERC CoG grant in 2021 and several scientific prizes: Saint-Gobain Prize of the French Physical Society, Prix Hugot du Collège de France, Nanoscience Thesis Award.

Robert Whitney, CNRS LPMMC

Robert Whitney is a CNRS researcher at the Laboratoire de Physique et Modélisation des Milieux Condensés (LPMMC) of the Université Grenoble Alpes and CNRS. He is a specialist in dissipation in quantum physics, and the quantum thermodynamics of nanoscale electronic circuits. He has been working with Alexia Auffèves on quantum computing energetics since 2019. They recently formed the Quantum Energy Team (QET) together to continue this work. He is a cofounder of the Quantum Energy Initiative (QEI), which is creating a world-wide interdisciplinary community to address the energy consumption of quantum technologies. He is the quantum engineering representative in the Grenoble quantum ecosystem (QuantAlps), and is on the steering committee of a project to facilitate linking quantum physics to social sciences and humanities within the University Grenoble Alpes (CDTools project: TiQuA).

Alexia Auffèves, CNRS Majulab

Alexia Auffèves is a CNRS research director, heading the International Research Lab MajuLab in Singapore. After an experimental PhD with Serge Haroche, she joined the CNRS in 2005, doing research on the theory of quantum optics and quantum thermodynamics, in strong interaction with experimentalists. She promotes the physics-philosophy interface, and coordinated it within the Grenoble quantum ecosystem (2017-2022). In 2022, she created the Quantum Energy Team (QET) with R. Whitney; which is an international CNRS research team (Singapore-Grenoble) working on energy in quantum systems. At the same time, she saw the need for a world-wide interdisciplinary community to address the energy consumption of quantum technology, and so she founded the Quantum Energy Initiative (QEI) with Robert Whitney, Olivier Ezratty and Janine Splettstoesser. She chairs a new IEEE working group (also called “Quantum Energy Initiative”) to establish standards for the energy efficiency of quantum technologies.

Laurent Vivien, CNRS C2N

Dr Vivien is a CNRS Director at the Centre for Nanoscience and Nanotechnology (C2N) on the development of innovative concepts for Si photonics including optoelectronic and hybrid photonic devices. Dr Vivien has also been at the forefront of the development of Pockels effect in strained silicon and c-oxide integration on Si photonics. Since 2016, he has served as Deputy Director of C2N and Director of the Photonics Department. In 2021, he cofounded the start-up company InSpek-solution for the development of Integrated sensors (J. Michon as CEO)). He also received a Consolidator European Research Council (ERC) grant. Dr Vivien has published over 510 international papers (H-index of 49 from isi WoS), holds 8 patents, 9 book chapters and 1 handbook. He is regularly invited to conferences (> 180 invited talks). He is also elected Fellows of Optica, EOS and SPIE. He regularly serves as a Chair of EOS, OSA, IEEE and SPIE conferences.

Franck Balestro, UGA, CNRS, Néel Institut

Franck Balestro is a Professor at University Grenoble Alps, researcher at the CNRS Néel Institut. He is an experimentalist, specialist in, mesoscopic physics, superconducting qubits, quantum manipulation of single electronic

and nuclear spin for quantum algorithm. Since 2012, he is in charge of scientific teams, since 2018, he is in charge of the QuantECA research team, specialized in superconducting and spin qubits. He is deputy director of QuantAlps, the research federation in quantum sciences and technologies in Grenoble, coordinator of the QuanTEdu-France program, a national ANR project gathering 21 Universities and Schools for Education in Quantum Technologies, the French representative in EQN-Edu, the European Quantum Network on Education, in charge of the Master 2 program Quantum Information Quantum Engineering, in the steering comittee of TiQuA, a project to facilitate linking quantum physics to social sciences and humanities within the UGA.

Maryline Bawedin, UGA IMEP-Lahc

Maryline Bawedin received her Ph.D. degree jointly from the Université Catholique de Louvain and from the National Polytechnics Institute of Grenoble, France, in 2007. From 2002 to 2007, her main research field was the electrical characterization and modeling of floating-body effects (FBEs) in SOI technology for memories applications and DC performance of very-thin film SOI power devices. From 2008 to 2010, she worked at the Centre for Advanced Photonics and Electronics (CAPE), Cambridge UK, where she was involved in the development of III-V hetero-structures on alternative substrate like diamond for high power and RF applications. She is now Associate Professor at Grenoble INP. She is author or co-author of over 200 scientific papers and communications in the field of Silicon-on-Insulator (SOI) devices.

Jean-Emmanuel Broquin, UGA IMEP-Lahc

Jean-Emmanuel Broquin received an Engineering Degree in the Physics of Microelectronic devices and a Master degree in Optics Electromagnetism and Optoelectronics from the Institut National Polytechnique de Grenoble (France) in 1993. Since the completion of his PhD on Erbium-Doped Waveguide amplifiers in 1997, he has been working on both active and passive integrated optics devices (mainly realized on glass substrate). In 1999, he has been appointed Associate Professor at the Grenoble Institute of Technology (G-InP, France) and became a Full Professor in 2007. His main teaching activities are microtechnology, optoelectronics and integrated optics. After having been in charge of the Photonics group of the IMEP (Institute for Microelectronics, Electromagnetism and Photonics), he has been the the Director of this 140 people research institute from 2014 to 2021. In 2020, Jean-Emmanuel Broquin has been awarded the Nokia Foundation-IFF distinguished chair.

Christoforos Theodorou, UGA IMEP-Lahc

Christoforos Theodorou received his B.S. degree in Physics(2006), M.S. degree in electronic circuit technologies (2008), and Ph.D. degree (2013) from Aristotle University of Thessaloniki, Greece. He is currently a CNRS Researcher with the IMEP-LAHC Laboratory (MINATEC Center), GrenobleINP in France. His main research focuses on the characterization, modeling and simulation of noise and fluctuations phenomena (LFN/RTN), as well as noise-induced dynamic variability in novel nano-scale devices and the development of new methods of circuit noise simulations. His recent interests cover the experimental study of cryogenic electronic devices: electrical characterization, new methods of parameter extraction, benchmarking of emerging technologies and understanding of low temperature conduction. He is the author/co-author of 60 publications in peer-reviewed journals, 36 international conference papers and 1 book chapter.

Sylvain Bourdel, UGA TIMA

Sylvain Bourdel received the Ph. D in microelectronics from the National Institute of Applied Science (INSA) of Toulouse in 2000. He was with the LAAS laboratory of Toulouse where he was involved on radiofrequency systems modeling and he was especially focused on spread spectrum techniques applied to 2.45GHz transceivers. In 2002 he joined the

IM2NP in Marseille where he headed the Integrated Circuit Design team. Meanwhile, he was expert for the SCS world-class clusters and the ARCSIS cluster and member of the National Council of Universities (CNU). He joined in 2013 the IMEP-LaHC laboratory and Grenoble-INP as a full Professor. From 2018 to 2021, he led the RFIC-Lab laboratory of Grenoble, France. He is now with the TIMA laboratory. He was involved in the steering committees of several CAS conferences and he is actually the secretary of the French CAS chapter. He works on RF and mmW IC design and integration. He particularly focuses on low cost and low power applications. His area of interest also includes design oriented MOS modeling, UWB and RFID systems. He is the author and co-author of about 150 referenced IEEE publications.

Nicolas Sangouard, CEA IPhT

Nicolas Sangouard studied physics at the Université de Brougogne where he did a PhD in the framework of coherent control. He did a postdoc in quantum optics with M. Fleischhauer in Kaiserslautern in 2005 and also with N. Gisin in Geneva in 2006. In 2007, he obtained a Maitre de Conferences position at the University Paris VII. Returning to Geneva in 2009, he headed the theoretical activities related to quantum optics in N. Gisin's group. He received a professorship from the Swiss National Foundation in 2014, which he used to run an independent research group at the University of Basel. Since 2020, he is a senior CEA researcher at the Institut de Physique Théorique in Paris-Saclay where he co-leads a research group working on quantum optics and quantum information. Notable research results include theoretical proposals related to quantum networks. He contributed for exemple to lay the mathematical groundwork needed for the first implementation of device-independent quantum key distribution. On the fundamental side, he made proposals to create and detect quantum features in macroscopic systems, which led for exemple to the first detection of Bell correlations in a many-body system. He is the recipient a Carnot Foundation Fellowship in 2004 and the co-recipient of the Paul Ehrenfest Best Paper Award for Quantum Foundations in 2017.

Marc Duranton, CEA LIST

Dr. Marc Duranton is Senior Fellow of CEA and member of the Digital Systems and Integrated Circuits Division of CEA, where he is involved in realizations for Artificial Intelligence, for Cyber Physical Systems and for distributed systems from IoT to Cloud.He previously spent more than 23 years in Philips where he led the development of the family of L-Neuro chips, digital processors using artificial neural networks. He also worked on several video coprocessors for the VLIW processor TriMedia and for various Nexperia platforms. In NXP Semiconductors, he was in charge of Ne-XVP project that targeted the design of the hardware and software of a multi-core processor for real-time applications and for consumer video processing.He is in charge of the roadmap activities of the HiPEAC community (High Performance and Embedded Architecture and Compilation), freely available at https://www.hipeac.net/vision/ and is also involved in the Strategic Research and Innovation Agenda of the Electronics Components and Systems (*ECS SRIA)* and in the Strategic Research Agenda of the European Technology Platform for High Performance Computing (*ETP4HPC SRA*).

Eric Guthmuller, CEA LIST

Eric Guthmuller graduated from Ecole Polytechnique and received the MS degree from Telecom Paris, France in 2009. He received his Ph.D in computer science from the University Pierre & Marie Curie (UPMC, Paris, France) in 2013. He then joined the Technological Research Division of CEA, the French French Alternative Energies and Atomic Energy Commission, within the CEA-Leti institute as a full-time researcher until 2019, then within the CEA-List institute. He is now expert in processor architectures and quantum computer architectures. His main research interests include

processor architectures and their memory hierarchy, cache coherency, heterogeneous architectures and control electronics for quantum computers. He is author or co-author of 18 publications and 5 patents.

Yvain Thonnart, CEA LIST

Yvain Thonnart received the MS degree from Ecole Polytechnique and an engineering diploma from Telecom Paris, France in 2005. He then joined the Technological Research Division of CEA, the French French Alternative Energies and Atomic Energy Commission, within the CEA-Leti institute until 2019, then within the CEA-List institute. He is now senior expert on communication and synchronization in systems on chip, and scientific advisor for the mixed-signal design lab. His main research interests include asynchronous logic, networks on chip, physical implementation, emerging technologies integration such as photonics, cryoelectronics and interposers, leading to more than 70 publications and 10 patents. He is currently serving in the technical program committee of the ISSCC.

Franck Badets, CEA LETI

Franck Badets earned an engineering degree from ENSERB in 1995, a PhD degree in electronics from University of Bordeaux in 2000 and an accreditation to direct research (HDR) in 2012. From 2000 to 2011 he was with STMicroelectronics where he was involved in the design of RF frequency synthesizers and RF transmitters. In 2012 he joined CEA Leti as Researcher Engineer in an analog design team dedicated to sensor interface. Currently, his research focus on the design of Ultra-Low Power sensor interfaces, analog computing and cryogenic IC design dedicated to quantum computing. He has supervised 10 PhD students, he is author or co-author of more than 50 conference and journal papers and holds 18 patents.

Mikael Cassé, CEA LETI

Dr. Mikael Cassé received the Ph.D. degree in physics from the Institut National des Sciences Appliquées, Toulouse, France, in 2001. He studied quantum effects at low temperature in semiconductor systems. Since 2001, he is working as a Research Staff Member at CEA-Leti, Grenoble. His current research interests include DC / RF electrical characterization and modeling of advanced CMOS devices (with novel channel and dielectrics materials…), cryoCMOS, novel CMOS device architectures and devices for quantum computing. He has been involved in several EU and French projects acting as task leader (including PullNano, ASCENT, Sequence) and he is the actual CEA representative of MATQu ECSEL project. He is/was involved in industrial collaborations with STMicroelectronics, IBM, and Globalfoundries. He authored and co-authored more than 200 international communications in peer-reviewed journals and conference proceedings, and 2 book chapters.

Karim Hassan, CEA LETI

Karim HASSAN received the Ph.D. degree in physics from the University of Burgundy, Dijon, France, in 2013 on the development of thermo-optical plasmonic routers for telecom applications, in the framework of the European project FP7-PLATON. Since 2014, he has been with the CEA-Leti (France) as a Research Fellow. He has been involved in both industrial R&D projects and collaborative projects either as a technical contributor (H2020-COSMICC) or as WP Leader and Project Board member (FP7-SEQUOIA, H2020-PICTURE). His research interests include the design, fabrication, and characterization of photonics integrated circuits, hybrid III-V on silicon laser sources, and topological optimization for nanophotonics. He has authored or co-authored more than 100 journal publications, conference papers, and patents. Since 2022, Karim HASSAN is the Head of Silicon Photonics Laboratory under the Optics and Photonics Division at CEA-Leti.

Valentin Savin, CEA LETI

Valentin Savin received the M.S. degree in mathematics from the École Normale Supérieure, Lyon, and Joseph Fourier University, Grenoble, in 1997, and the Ph.D. degree in mathematics from Joseph Fourier University, in 2001. From 2002 to 2004, he was a Post-Doctoral Researcher with the Institute of Mathematics of the Romanian Academy. Since 2005, he has been with CEA-LETI, first as a two-year Post-Doctoral Researcher, and then as a Permanent Researcher. Currently, he is a Senior Researcher at CEA, with more than 15 years of research experience in the field of classical and quantum error correction, for reliable communication and fault-tolerant information storage and processing. Over the last years, he has been coordinating several French and European research projects on the analysis and design of iterative decoders running on faulty hardware, the design of fault-tolerant circuits from unreliable components, and advanced error correction techniques for quantum information processing.

Candice Thomas, CEA LETI

Candice Thomas received her Ph.D. degree from University Grenoble Alpes (France) in 2016, focusing on the material and low temperature electrical characterizations of topological insulators. Between 2017 and 2019, she was a postdoctoral research associate at Microsoft Quantum Purdue in the USA, where she designed and fabricated hybrid superconductor-semiconductor hetero-structures by molecular beam epitaxy for topological quantum computation. She then joined CEA-Leti in 2019, where she is now focusing on 3D integration and cryo-packaging solutions for silicon spin qubits. She has a total of 38 publications in peer-reviewed journals.

Xavier Jehl, CEA Pheliqs

Xavier Jehl earned his PhD in 1999 in the fundamental physics department CEA-Grenoble on shot noise in superconducting junctions. He then moved to NIST in Boulder, Colorado, to work as a postdoctoral researcher on electron pumps for quantum metrology. With the Lateqs team (www.lateqs.fr) since 2002, he started investigating silicon-on-insulator nanowire transistors at very low temperatures. Since the first demonstration of a hole spin quantum bit in 2016 in such structures, our group focuses on the physics of spin-orbit coupling and the opportunities it opens for quantum information processing. His activity is centered on the measurement techniques of these qubits in their cryogenic environment, including the fridges themselves, the fast electronics and reflectometry techniques, as well as cryogenic electronics

Mazyar Mirrahimi, INRIA Quantic

MM is an expert of quantum information theory with superconducting circuits. This expertise includes feedback control of quantum systems, quantum error correction, preparing non-classical states of microwave radiation with superconducting circuits, and stabilizing such non-classical states with quantum reservoir engineering. He is a senior researcher (DR1) at Inria Paris. He is the scientific leader of the joint Inria-Mines-ENS-CNRS QUANTIC team (team of about 30 permanent and non-permanent researchers), and a part-time professor of Applied Mathematics at Ecole Polytechnique. From 2011 to 2020, he also held a visiting scientist position at Yale University. He is also on the scientific board of the startup Alice and Bob. He has authored/co-authored about 60 peer reviewed journal papers around these topics and has been cited over 9000 times. In 2017, he won «Inria-Academy of Science young researcher award».

Omar Fawzi, INRIA QInfo

Omar Fawzi is an Inria research director hosted at ENS Lyon. He obtained his PhD from McGill University in 2012 on quantum information theory and spent two years at ETH Zurich as a postdoctoral researcher. He has worked on

quantum Shannon theory, quantum error correction and fault tolerance and quantum cryptography. He received a CNRS Bronze Medal in 2019 and an ERC Starting Grant in 2019.

Benoît Valiron, INRIA QuaCS

Benoît Valiron is a teacher-researcher at CentraleSupelec, attached to the Formal Methods Laboratory (LMF) for research within the QuaCS team. He obtained a PhD from the University of Ottawa in 2008 under the supervision of Peter Selinger. As a continuation of his thesis work, he participated in the development of the theory and semantics of quantum programming languages. In particular, he is one of the main developers of the Quipper language. His current research covers quantum compilation and formal methods to analyze quantum programs.

Benoît Valiron is co-coordinator of the ANR SoftQPro project, WP leader for the Quantum PEPR, and is participating in in the European project EuroHPC HPCQS as well as in the HQI project. He has published more than 50 scientific papers and has been in charge of the organization of several international conferences (POPL 2017, QPL and MFPS 2020, QPL 2022).

Anthony Leverrier, INRIA Cosmiq

Anthony Leverrier received his PhD from Telecom ParisTech in 2009 and his HdR from UPMC in 2017. After two postdocs at ICFO (Barcelona) and ETH (Zürich), he joined Inria in 2012 and is currently working in the team COSMIQ. His current research activities are mainly focused on quantum error correcting codes, and more particularly on quantum LDPC codes that promis to achieve fault tolerance with minimal redundancy. He has published more than 50 scientific papers, including more than 15 in leading physics journals (PRL, PRX, Nature Photonics, Nature Communications) or computer science conferences (FOCS, STOC,SODA). He is currently coordinating the project NISQ2LSQ from the PEPR, dedicated to bosonic codes and quantum LDPC codes.

Christophe Vuillot, INRIA Mocqua

Christophe Vuillot obtained his PhD from TU Delft University, Netherlands in 2020. After a postdoc at Inria Paris he joined in 2021 Inria Nancy as permanent junior researcher (CR). His research focuses on fault-tolerant quantum computing using discrete as well as continuous quantum systems.

5.3. Program Management Team

Corinne Legalland, CEA LETI

Corinne Legalland received the engineering degree from INP-Toulouse in 1995. From 2002 to 2011, she managed several technical teams (process engineering, parametric test, defect density) at Altis Semiconductor (now XFab France at Corbeil Essonnes – France). In 2012, she joined CEA-Leti as Silicon Technologies Division deputy manager, in charge of clean rooms operations (8000m^2 clean rooms, serving 250 projects 200 and 300 mm, delivering 100 wafer lots per week). In 2018, she became key account manager for a major CEA-Leti industrial partner, managing a technical program of more than 200 researchers covering Image sensors, nonvolatile memories, RF components, photonic and 3D technologies. Today, she is charge of quantum program direction at CEA-Leti, and lead, together with Tanguy Sassolas and IRT Nanoelec, the buildup of the LSQ program.

Tanguy Sassolas, CEA LIST

Tanguy Sassolas is high-performance and quantum computing program manager at CEA LIST. He received a M.Sc. and a M.Eng. in Electronics from ENSEEIHT, Toulouse in 2008 with a specialty in computing architecture. Since then his architectural work focused on the design of manycore architectures. In particular, he was deeply involved in the conception of the SESAM multiprocessor architecture simulation and exploration environment. To address the design of hardware support for efficient performance, power and thermal management, he conceived novel methods for joint functional/thermal co-simulation and co-emulation. To cope with simulation performance bottlenecks of VP simulation he investigated parallelization strategies leading to the definition of the SCale parallel SystemC kernel (5 patents). He lead CEA's EDA and Architecture Lab that performed the virtual prototyping and exploration of the European Processor Initiative, designed the embedded neural network processor PNeuro® and developed the Leaf formal framework for the analysis of processor temporal behavior for both safety and security. Today, he is deeply involved in the definition of major research in the field of quantum computing, and lead, together with Corinne Legalland and IRT Nanoelec, the buildup of the LSQ program.

5.4. Acronyms and definitions

Acronym	Signification	Comment
ANR	Agence Nationale pour la Recherche National Research Agency	French National research agency
APP	Agence de Protection des Programmes Program protection agency	The APP is a European organization for the protection of authors and publishers of digital creations. Its solutions enable the deposit of all types and all size of content as software, mobile applications, databases, websites and strategic contents.
CSA	Coordination and Support Action	European project structuring academic and industrial ecosystems by funding training, conference and gatherings as well as technological roadmap definitions
EDA	Electronic Design Automation	Refers to the domain addressing the automation of electronic design. EDA tools are software used in this automation often using an EDA methodology to ensure several tools interoperation to achieve design goals
ESL	Electronic System Level	Electronic system level (ESL) design and verification is an electronic design methodology, focused on (higher) appropriate abstractions in order to increase comprehension about a system, and to enhance the probability of a successful implementation of functionality in a cost-effective manner.
FMI	Fonctional Mockup Interface	A standard for the cosimulation of numerical models https://fmi-standard.org/
FTQC	Fault-Tolerant quantum Computing	Refers to a universal quantum computer that can provide error correction mechanisms. One must bear in mind that FTQC will still exhibit a remaining quantum error. To the author's knowledge there is no formal definition of FTQC in terms of remaining error probability
HPC	High-Performance Computing	HPC uses supercomputers and computer clusters to solve advanced computation problems.
HQI	HPC Quantum Initiative	A research and investment project part of the SNAQ whose goal is to setup an HQI platform.

HQI Platform		National computing equipment shared between research entities own by GENCI and managed by CEA, aiming to operate quantum computer accelerators within the HPC infrastructure in a NISQ then LSQ approach
IP	Intellectual Property	By extension in the electronic design domain, a functional block implemented by means of a hardware description language or its physical implementation on a given technology is referred as an IP, due to the fact that there use can be licensed to third parties that build system composed of several such IPs.
JJ	Josephson junction	
LNE	Laboratoire National D'essai National Laboratory of Metrology and Testing	
LNA	Low-noise amplifier	
LCA	life-cycle analysis (LCA)	
LSQ	Large-Scale Quantum Computing	Refers to a universal quantum computer (gate based) who exhibits hundreds of error-corrected qubits, and therefore provides quantum supremacy
MBSE	Model-based system engineering	Model-based systems engineering (MBSE) is a formalized methodology that is used to support the requirements, design, analysis, verification, and validation associated with the development of complex systems. In contrast to document-centric engineering, MBSE puts models at the center of system design.
NISQ	Noisy Intermediate Scale Quantum	Quantum computers that exhibit few qubits with quantum error that limit the depth of computation that they can be used for.
OSINT	short for open-source intelligence	
PIA	Programme d'Investissement d'Avenir Investment program for the future	Type of national funding that co- finances the IRT programs.
PNCQH	Plateforme Nationale de Calcul Quantique Hybride (France Hybrid Quantum HPC Initiative)	

QEC	Quantum Error Correction	Refers to solutions developed to reduce the quantum error of qubits by means of control feedback occuring during the processing
SNA	Stratégie Nationale d'Accélération National acceleration strategy	French Investment programs for several strategic technology domain
SNAQ or SNQ	Stratégie Nationale (d'Accélération) pour les technologies quantiques National Strategy for Quantum Technologies	The French investment program dedicated to quantum technologies as part of all SNA
TEF	Testing and Experimentation Facilities	TEFs are specialised large-scale reference sites open to all technology providers across Europe to test and experiment at scale state-of-the art AI solutions, including both soft-and hardware products and services, e.g. robots, in real-world environments.
TDP	thermal design power	The maximum amount of heat generated by a computer chip or component that the cooling system in a computer is designed to dissipate under any workload
TWPA	Traveling Waves Parametric Amplifier	High quality LNA based on JJ used as first stage of qubit readout for superconducting qubits. Due to their use of JJ they must be used in cryogenic conditions

5.5. References

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