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## 4. DETAILED WORK DESCRIPTION

### 4.0. WPO Operational management, intellectual property capitalization and valorization

#### 4.0.1. Work package objectives

This work package aims at the global management and work-package coordination, intellectual properties management, dissemination and valorization of the work and communication. It will also provide scientific and technical watch, and generate possible synergies with other domains (as spatial...).

#### 4.0.2. Partners Role

Entity	Role
IRT/DIR	Due to the importance of the program in IRT Nanoelec actions, IRT will dedicate resources to the program for financial, legal, communication and scientific actions.
CEA	As major provider of research works conducted in the project, CEA with its institutes CEA-list and CEA-leti will lead the project operational execution. CEA's marketing analysis office has developed key competences in market and patent survey for a wide range of technology. It will drive actions regarding access to IP rights and freedom to operate.
All partners	All partners in the project will be involved in the access IP strategy, by sharing on their own research and patent watch. They will also be in charge of the scientific dissemination of the works conducted in the program.

Additional contributions from industrial partners joining the program may be added during the project execution.

#### 4.0.3. Detailed work description

T0.1 Operational Management
<b>Start: M1</b>
<b>End: M72</b>
<b>Contributors: CEA</b>
<p><b>Description:</b></p> <p>T0.1 will be in charge of the supervision of technical actions conducted in the WP1 to7 and will ensure correct flow of information in between work packages.</p> <p>The program directors will report to the IRT COPIL significant evolution of the program execution and will propose corrective actions whenever necessary. In order to achieve the necessary steering of actions the task will organize monthly WP leaders meetings, as well as regular Program Committee meetings.</p> <p>Task T0.1 will update risk assessment analysis, manage interactions with other French quantum strategy programs and European calls, and identify potential synergies with, for example, space domain applications. It will drive the interactions with the advisory board, consolidate annual ANR reports on achieved works and dedicated efforts.</p> <p>Task T0.1 will also monitor the worldwide publications to benchmark the program objectives and results.</p> <p><b>Deliverables (due month/lead):</b></p> <ul style="list-style-type: none"> <li>ID0.1.1 Annual report 1 (M12)</li> <li>ID0.1.2 Annual report 1 (M24)</li> <li>ID0.1.3 Annual report 1 (M36)</li> <li>ID0.1.4 Annual report 1 (M48)</li> <li>ID0.1.5 Annual report 1 (M60)</li> </ul>

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## ID0.1.6 Annual report 1 (M72)

### T0.2 Intellectual property management

**Start: M1**      **End: M72**      **Lead: CEA/SBEM**

**Contributors: CEA/SBEM + All partners**

#### Description:

The main objective of T0.2 is to ensure the freedom to operate of developed IPs in the program. In order to achieve that, the task will focus on performing active watch of external IPs evolution. Specific search patterns will be setup for both OSINT (short for Open-Source INTElligence) analysis as well as closed publications and patent databases. Adapted filtering and data analysis will target to cluster retrieved information to assess IP generated by third parties. Then further analysis will be handed over to researchers with the correct background. The capacity to provide the good level of filtering will be critical to request analysis from researchers only when necessary.

Complementary analysis will seek to identify ecosystem links for concurrent IP portfolio, to identify market opportunities.

**Deliverables (due month/lead):**

**ID0.2.1 Report on search request definitions (M24)**

**ID0.2.2 Intermediate report on identified IP threats and opportunities (M36)**

**ID0.2.3 Summary report on identified IP threats and opportunities (M72)**

### T0.3 Dissemination, valorization, and communications

**Start: M0**      **End: M72**      **Lead: CEA**

**Contributors: CEA/IRT**

#### Description:

The task will coordinate all communication and dissemination actions in the program. It will ensure scientific communications shed good light on the project by including proper references to the source of the research. To ease communications in all context, the task will prepare public communication documents for all supports whether digital (logo, slide decks, LinkedIn posts) and physical (kakemonos, posters, sustainable accessories).

Both know-how and patents are an important production issued from the project and this is reported in this task. Publications, patents are all reported in each annual report.

Additionally, economic and social valorization by industrial partners are also key success indicators of the project and will be highlighted in annual reports and specific reporting.

Initial dissemination and valorization plan (cf Section 3.5) will be updated on regular bases taking into account technical results, IP portfolio evolutions, changes in the ecosystem landscape.

**Deliverables (due month/lead):**

**ID0.3.1 Communication kit (M12)**

**ID0.3.2 Synthesis of communication actions (M72)**

**ID0.3.3 Valorisation plan update (M36)**

**ID0.3.4 Final valorization plan (M72)**

### Work package deliverables

**D0.1 Annual reports (M12-M72)**

**D0.2 Intermediate report on identified IP threats and opportunities and related actions (M36)**

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D0.3 Summary report on identified IP threats and opportunities and related actions (M72)

D0.4 Synthesis of communication actions (M72)

D0.5 Valorisation plan update (M36)

D0.6 Final valorization plan (M72)

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#### 4.1. WP1 Digital models and EDA tools for quantum control chain system design exploration

##### 4.1.1. Work package objectives

The ambition of WP1 is to enable the design of a scalable control chain by analyzing possible gaps of electronic design tools to comply with novel cryogenic constraints, and defining a novel system modeling solution for quantum control chains. Gap analysis will support design works from WP3-6, while system modeling will be core to the architecture exploration and definition conducted in WP2-Architecture.

To provide relevant analysis the system model will be enriched from hardware and software data. Dedicated actions in WP1 will seek to provide applicative resource constraints, while technology WP3-6 will help populate the system model by providing hardware components constraints and performance figures. To ensure a holistic vision, the WP will develop strong interaction with other projects in the national strategy to encompass for instance RF links properties or cryogenic power.

At a later stage of the program, based on WP4-QEC developments, functional model of the programming interface of the control chain including error-correction will also be addressed to ease quantum software development and allow applicative performance evaluation.

##### 4.1.2. Partners Role

Entity	Role
CNRS	With its expertise in quantum system modeling encompassing energetic issues, CNRS will provide the initial shared system modeling infrastructure and will extend knowledge databases with state of art review of technologies out of the scope of the program
CEA	Together with CNRS, CEA will bring the system model setup by CNRS for superconducting QPUs to a higher maturity level by defining a generic system modeling approach taking its roots from MBSE and ESL simulation. CEA will also enrich the applicative aspect by providing dimensioning application use cases, and will provide models build on acquired data in WP3-6. In later project stages, CEA will conceive programmer's view models for error-corrected quantum computers
Siemens	Work Package Leader As a major player in EDA and system simulation, Siemens will evaluate its tool applicability to cryo system design and support design work in WP3-6.
Inria	Inria will provide dimensioning use-cases for numerical simulation such as HHL ( <b>QuaCS</b> ) and will also provide hardware constraints and information flow structure for architectures based on stabilized bosonic qubits ( <b>Quantic</b> )
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, industrial QPU makers would provide dimensioning data on qubits properties for system modeling (error model, connection topology)
Silent Waves	Upon joining the program, SilentWaves would provide data on TWPA

Additional contributions from industrial partners joining the program may be added during the project execution.

##### 4.1.3. Detailed work description

###### T1.1 Gap analysis for EDA tools evolutions for quantum computing

**Start: M0**      **End: M12**      **Lead: Siemens**

**Contributors: Siemens, CEA**

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#### Description:

The target of this task is to identify for EDA tools involved in classical electronic design the specific evolutions needed to address the challenge of quantum computing. In particular, the impact of change of material behaviors at low/cryogenic temperature is expected to push the tools to their limits; this includes thermal phenomena at small scale and superconducting behavior. This task will gather feedback from CEA experts involved in WP3-WP6 on existing tools and specific design needs. Siemens will identify to what extent their current offer can meet the project needs, or possibly devise evolution plans depending upon evaluation of business case.

#### Deliverables (due month/lead):

##### ID1.1 Report on needed EDA tool evolutions (M12)

#### T1.2 System modeling

#### Description:

Bringing the gap between many expertise domains (application, QEC, 3D integration, integrated photonics, cryo-electronics, cryogenics...) is critical to the definition of innovative control chains for qubits that shall reach a global optimum rather than local ones. The following tasks together aim at defining a novel system approach for quantum control electronics.

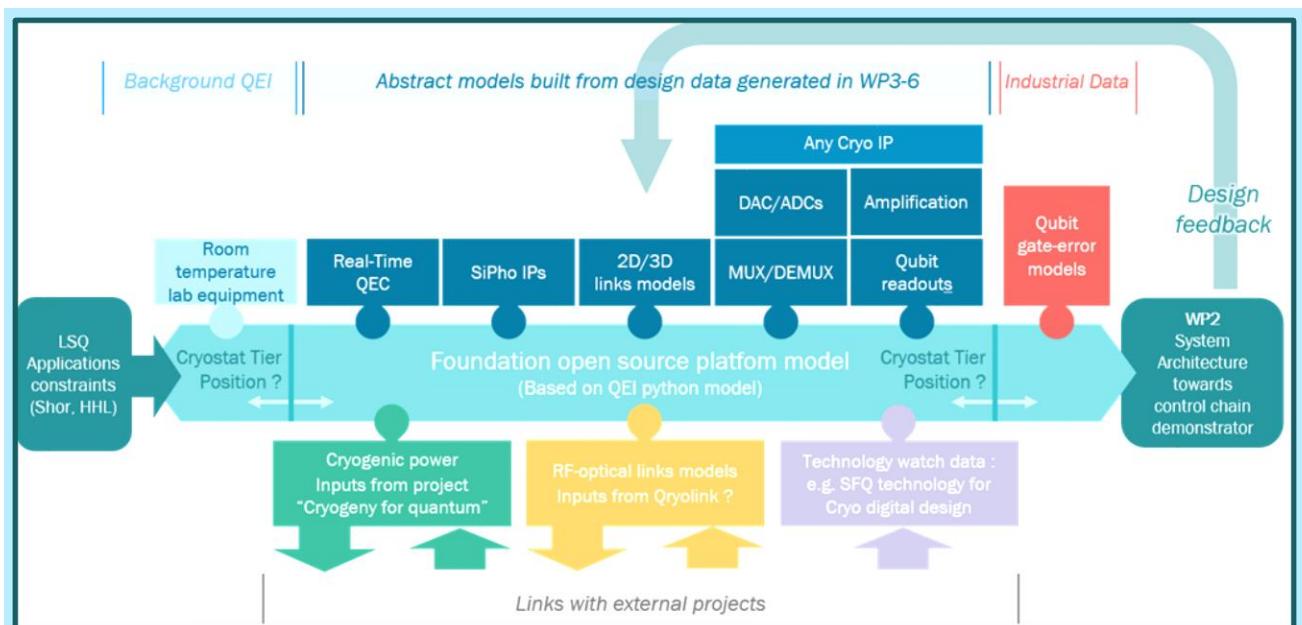


Figure 15 - System modeling approach

#### T1.2.1 Shared System Infrastructure

Start: M0	End: M72	Lead: CEA
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Contributors: CNRS, CEA, Siemens

#### Description:

The goal of this task is to define an infrastructure for system modeling of the control chain that is able to encompass every IPs constraints and requirements and will therefore help system architect understand how each component can impact the system as a whole. To reach this objective, experts from different backgrounds will first be gathered to define the adapted data structure of the models. CNRS will bring its expertise in superconducting

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qubits control modeling, associated with a first python codebase used in <http://dx.doi.org/10.48550/arXiv.2209.05469>. CEA will bring its expertise in ESL simulation based on SystemC and FMI simulation as well as MBSE (Model-Based System Engineering). Siemens will bring its expertise in building holistic digital twins and tools like Veloce System Interconnect enabling multi-domain, multi-fidelity system simulation.

Involved personal will lead interviews from every stakeholder in the control chain to reach the definition of an infrastructure specification compatible with every element of the system and in capacity to assess their overall impact. Analytical performance models are envisioned whenever applicable, but simulation that is more complex may prove necessary for some components, or even co-simulation with existing domain specific tools.

Then efforts will be spent in implementing the specified framework infrastructure, including components templates (to be populated by experts in T1.2.2). Open-source opportunities for the infrastructure will be investigated from day one to allow for adoption of a broader maintenance community. Additionally, automated analysis services will be added to help architecture decision in WP2-Architecture. After a strong initial development phase up to M42, the task will focus on evolving maintenance required by the project

#### Deliverables (due month/lead):

**ID1.2.1.1 Specification of the system infrastructure and template components (M8)**

**ID1.2.1.2 Reference infrastructure implementation (M24)**

**ID1.2.1.3 Report on analysis services (M36)**

**ID1.2.1.4 Report on infrastructure maintenance updates (M72)**

#### T1.2.2 Key Component models

<b>Start: M12</b>	<b>End: M60</b>	<b>Lead: CNRS</b>
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**Contributors: CEA, CNRS**

#### Description:

This goal of this task is to create models for each components of the control chain. IPs developed within the project in WP3-6 will be modelled by the teams, directly involved in their developments, and may be refined as the project progresses: CEA will provide CryoCMOS IP models; CNRS will provide TWPA models; INRIA together with CEA and CNRS will build QEC models; CEA and CRNS will provide optical links models; and CEA will provide 3D links models. CNRS, which is implicated in other SNAQ projects such as Qryolink will be in charge of building models from external data (HEMTs, RF links ...). INRIA/Quantic will provide hardware constraints and descriptions of the informational flow extracted from stabilized bosonic qubits (noise-biased Schrödinger cat qubit and unbiased GKP qubits).

Additional qubits data is expected to be provided from industrial actors with in-kind contributions. Due to their critical intelligence value, qubit models may remain proprietary to their developers. To cope with this risk, approximate qubit models (representative of realistic performance bounds) may be used for architecture analysis in WP2-Architecture.

This task will seek to develop symmetric cooperation with the SNAQ Metriqs project that is expected to provide characterization of quantum components, so as to (1) share invaluable data for system architects that characterization shall address, and (2) gather additional components data for modeling.

#### Deliverables (due month/lead):

**ID1.2.2.1 Report on initial component models (M36)**

**ID1.2.2.2 Report on refined component models (M60)**

#### T1.2.3 Applicative constraints

<b>Start: M0</b>	<b>End: M36</b>	<b>Lead: CEA</b>
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**Contributors: CEA, INRIA**

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#### Description:

As for classical architecture, to correctly size quantum systems, one needs to consider target applicative constraints. In order to achieve that, the task will consider application use-cases at different scales to pave the way to industrialization.

CEA will provide application constraints by means of cryptanalysis, including declinations of Shor's algorithms for hacking various classical cryptosystems. A co-design approach will be pursued aiming to find shortcuts in the implementation of cryptanalysis algorithms from hardware specificities, to identify resource efficient implementations of quantum computers but also to offer a guidance for the whole control chain

Inria/[QuaCS](#) will provide application constraints in the field of numerical simulation with algorithms dedicated to resolution of systems of equations. A first candidate is the HHL algorithm and its refinements, but other algorithms for working with EDP will also be considered.

These various applicative constraints, together with QEC properties coming from WP4-QEC will be central to the overall control architecture scaling analyses performed in WP2-Architecture.

#### Deliverables (due month/lead):

**ID1.2.3.1 Report on resources, runtime and constraints for performing cryptanalysis with distributed quantum computations (M12)**

**ID1.2.3.2 Report on the generic toolbox for cryptanalysis constraints at various scales (M36)**

**ID1.2.3.3 Report on algorithms for numerical simulation at various scales (M36)**

T1.3 QPU functional models (**to be started in second project phase**)

Start: M48	End:M72	Lead: CEA
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**Contributors: CEA, INRIA (TBC)**

#### Description:

In order to validate that the control chain architecture will be able to connect to existing HPC architecture, task T1.3 would build a functional view of the quantum system encompassing QEC hardware. The intent is to represent the programming interface offered by the QEC hardware and potential room temperature equipment.

This model will then be used to define additional software steps to convert operations from the "Quantum HW Specification Standard" defined by Atos in the HQI project and the interfaces made available by the QEC hardware(s). This shall allow to project performances for real-case full stack programming of error corrected QPUs.

#### Deliverables (due month/lead):

**ID1.3.1 Programmer's view model of the QEC hardware (M60)**

**ID1.3.2 Report on software passes for QEC Hardware code generation (M72)**

Work package deliverables

D1.1 Reference system model infrastructure implementation (M24)
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D1.2 Report on first system model encompassing components models and application constraints (M36)
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D1.3 Report on API model for integration in computing platforms (M72)
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## 4.2. WP2 Architecture specification towards integrated demonstrator

### 4.2.1. Work package objectives

This work package will centralize all decisions regarding system design of an integrated control chain. It is in charge of gathering intelligence from the system modeling in WP1-System model to identify enabling technologies for the scalability of the control, and take design decisions for the final project demonstrator. To achieve this goal the work package will gather expertise from many entities, including the ones from industrial quantum players joining the program. The work package is expected to get a growing importance as the project moves forward, starting with a prescriptive role for enabling technologies, to initial system specification and finally to reach final demonstrator supervision.



Figure 16 – Illustration of WP2 activities on LSQ architecture from state-of-art specifications to system exploration by means of simulation, towards final demonstrator implementation supervision

### 4.2.2. Partners Role

Entity	Role
CEA	Work Package Leader With its expertise and background in complex integrated architecture (e.g. EPI processor architecture) and system design (e.g. Renault FACE industrial project), CEA will lead the architecture specification work package, and contribute to it with its knowledge in WP3-6 technologies.
CNRS	At the root of the Quantum energy initiative, CNRS will focus its work on evaluating the energetic implication of the scaling of the control chain depending on used technologies and QEC schemes.
Inria	With a central program role on the definition of QEC schemes, Inria will mainly participate in WP2-Architecture to get better grips at how hardware constraints (topology, control multiplexing...) can affect applicability of proposed QEC schemes solutions.
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, QPU vendors will leverage the system tools analysis from WP1-System model to devise their own scalability roadmap, and will help define needed system demonstrator needs to derisk their scalability roadmap.
SilentWaves	Upon joining the program, SilentWaves will contribute to specify co-integration strategy applicable to their amplification solutions

Additional contributions from industrial partners joining the program may be added during the project execution.

### 4.2.3. Detailed work description

T2.1 Expression of requirements for developed technologies		
Start: M1	End: M6	Lead: CEA
Contributors: CEA, CNRS, INRIA		

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#### Description:

Based on prior knowledge acquired on namely (1) the state-of-the art of quantum control electronics, (2) high-performance computing electronics such as high-speed IOs for data communications, (3) energetic issues stemming from quantum noise and cryogenic power and (4) quantum error correction, CEA and CNRS will define the target figure of merit for technologies investigated by the project in WP3-6.

#### Deliverables (due month/lead):

**ID2.1 Report on target technology figure of merit (M6)**

T2.2 Expression of requirements for system model analyses

**Start: M1**

**End: M18**

**Lead: CEA**

#### Contributors: All partners

#### Description:

In order to ensure the system model will be in capacity to address questions raised in defining the system architecture, T2.2 will specify the expected exploration capacities required from the toolset developed in WP1-System model. In particular, capacity to perform evaluation of environmental impacts with the system tool in conjunction with existing solutions will be dealt with.

#### Deliverables (due month/lead):

**ID2.2.1 First Requirements for system modeling analysis (M6)**

**ID2.2.2 Requirements for system modeling analyses (M18)**

T2.3 Evaluation of scalability strategies for performance and energy efficiency

**Start: M25**

**End: M42**

**Lead: CEA**

#### Contributors: CEA, CNRS

#### Description:

Starting with the availability of first system models the task will evaluate different scalability strategies for the control chain of various qubits technologies from a pure performance driven perspective (CEA) and from an energetic one (CNRS). Leveraging the holistic system model build in WP1-System model, will enable system-scale optimizations for the control chain. A refined evaluation will be performed based on updated models available later in the project. Scalability scenario may encompass *what-if* analysis considering the advent of quantum technologies outside of the project scope, such as quantum communications or quantum memories. Most promising scalability routes will be assessed in terms of environmental impacts possibly leading to simplified life-cycle analysis (LCA).

#### Deliverables (due month/lead):

**ID2.3.1 Partial report on scalability strategies (M36)**

**ID2.3.2 Final report on scalability strategies (M42)**

T2.4 Specification for the control chain demonstrator

**Start: M37**

**End: M42**

**Lead: CEA**

#### Contributors: All partners

#### Description:

Based on partial scalability evaluations from T2.3, the task will focus on defining concrete specifications for a demonstrator in capacity to demonstrate the scaling potential of involved technologies. In particular, structuring choices such as I/O methods need to be made early enough in the project to allow for their development. As scalability routes may differ from one qubit technology to another, the demonstrator may require a certain level of versatility that will need to be put in adequacy with available design resources.

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**Deliverables (due month/lead):**

**ID2.4 Specification report for the control chain demonstrator (M42)**

T2.5 Control chain demonstrator supervision and integration

Start: M43	End: M72	Lead: CEA
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**Contributors:** CEA

**Description:**

This task will be in charge of ensuring good cooperation between developments conducted in each WP3-6. A particular area of focus will lie in the definition of interfaces at all scales, be it 3D integration, packaging I/O, or board design, cryostat I/O, or QEC syndrome decoding accelerator I/Os and protocols. In order to achieve that, the task will centralize refined specifications of each subcomponent and keep a reference specification up to date with required adjustments for each subcomponent. In particular, to allow the demonstrator to be plugged with actual qubits that are not designed in the project, interfaces towards qubits will be defined with participating industrial players, to ensure the capacity to implement QPUs through associated projects.

**Deliverables (due month/lead):**

**ID2.5 Performance report on the demonstrator (M72)**

T2.6 Specifications for future generation of scalable control chain

Start: M60	End: M72	Lead: CEA
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**Contributors:** CEA, CNRS

**Description:**

The goal of this task is to prepare a second generation for the control chain demonstration based on results accumulated in the project. Having such specifications as starting point for a follow-up Nanoelec program would avoid work interruptions that could lead to loss of momentum. The second generation would prepare industrialization by demonstrating control at larger scale; it will also likely extend the scope of the program to scale-out strategies depending on results from PEPR actions.

**Deliverables (due month/lead):**

**ID2.6 Specifications for potential LSQ program phase 2 (M72)**

Work package deliverables

D2.1 Requirements for system modeling analyses (M18)

D2.2 Partial report on scalability strategies (M36)

D2.3 Specification report for the control chain demonstrator (M42)

D2.4 Performance report on the demonstrator (M72)

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### 4.3. WP3 Integrated Photonics

#### 4.3.1. Work package objectives

WP3-Integrated Photonics will study how integrated photonics can be leveraged to allow increased scalability of the communication links between the cryostated qubits and the likely more power consuming error estimation hardware developed in WP4-QEC. Indeed, optical fibers offer higher bandwidth than RF cables and also provide good thermal isolation. The challenge for WP3-Integrated Photonics is thus to ensure proper functionality of integrated photonics in cryogenic conditions while keeping a constrained power dissipation budget and good Signal-Noise Ratio.

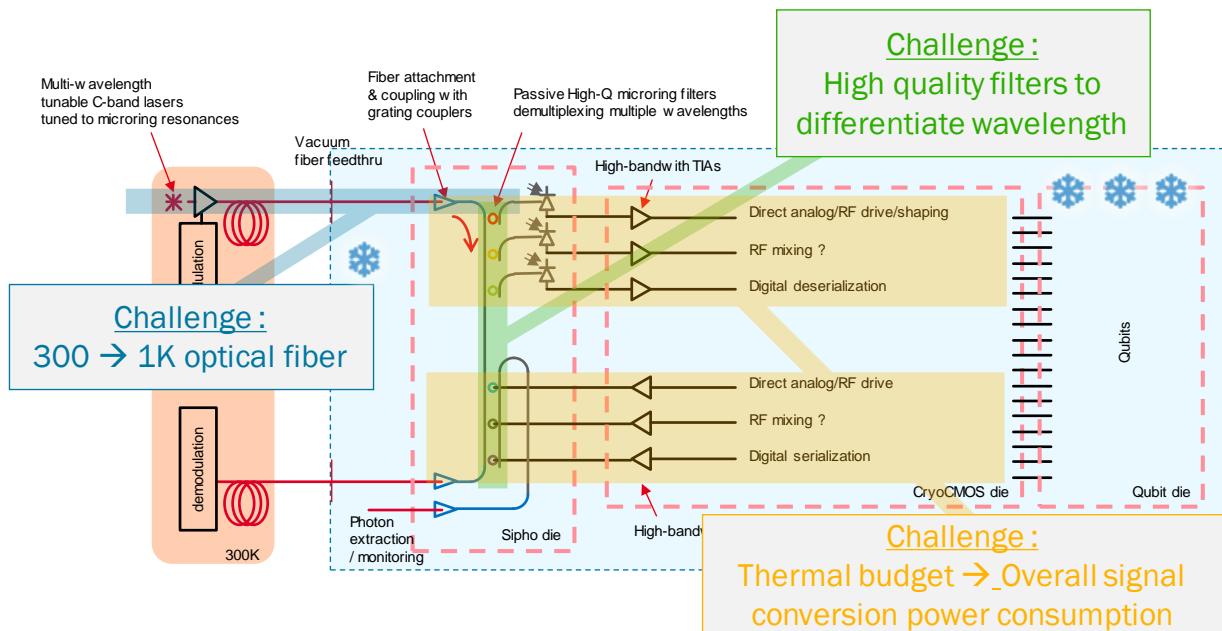


Figure 17 - Proposed solution for optical communication at cryo temperatures

WP3-Integrated Photonics will begin with an exploration phase to identify which existing integrated photonics do work in cryo-conditions, and which of them are the most promising to reach the expected performances. Then design of integrated photonics will start based on validated components, while design of advanced, high performances, key components will be investigated. As a starting point, integrated photonics use will be evaluated for both analog and digital output to provide data for system modeling in WP1-System model, while its use for ingress and the final subsystem design specification for egress (analog or digital) will be dependent on system architecture decision conducted in WP2-Architecture. Considered integrated photonics technologies may be based on either glass or SOI substrates or encompass both using 3D integration.

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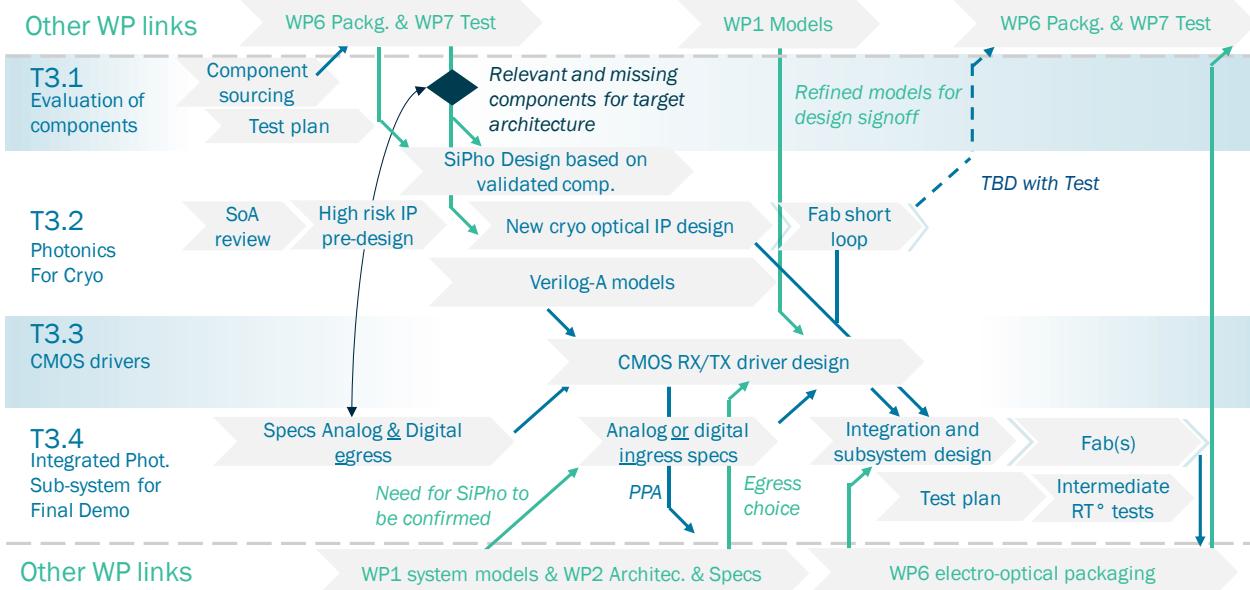
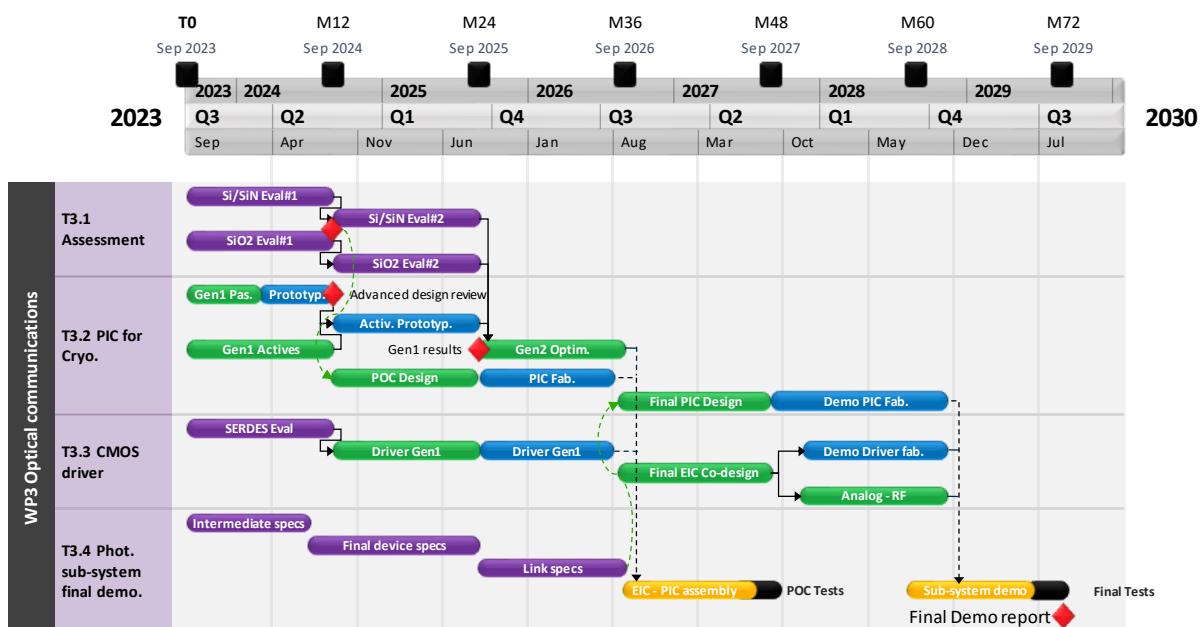


Figure 18 - WP3 PERT Chart showing intra & inter WP synergies

Another key aspect is the co-design and the assembly of the CMOS driver providing the appropriate bandwidth, voltage-swing and power supply at cryo conditions, and while keeping a limited heat dissipation. Thus, photonic and electronic IC packaging and 3D integration will be investigated, in relationship with WP6-3D&packaging. Discrete components will be evaluated at first in cryo conditions inside this WP and using the tools available/under development in WP7-Cryogenic tests. A proof-of-concept cryo-compatible transceiver will be designed after this assessment, while the final demonstrator is likely to require advanced photonics devices in order to reach the overall specifications (mostly regarding speed, heat dissipation, and compliance with drivers).



WP3 Gantt chart

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#### 4.3.2. Partners Role

Entity	Role
CNRS	CNRS has a strong expertise in integrated photonics design. Contributions could encompass specific integrated photonics device design as well as provide characterization environments in cryo-conditions.
CEA	WP leader. As an RTO, CEA has developed a strong expertise in integrated photonics architecture design, more specifically using Silicon-Photonics processes. It will lead the architecture definition of the photonic integrated circuits necessary to provide a scalable communication between cryostat and room temperature
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design teams with its design tools and expertise (e.g. Lightsuite Photonic Compiler).
ST	ST would support actions by providing SiPho device samples to be tested in cryo conditions and will also evaluate applicability of newly developed SiPho designs to other application domains
UGA-IMEP-LAHC	UGA-IMEP-LaHC has a strong expertise in integrated photonics design, especially over glass. Contributions could encompass specific passive integrated photonics device design as well as provide characterization environments in cryo-conditions.

Additional contributions from industrial partners joining the program may be added during the project execution.

#### 4.3.3. Detailed work description

T3.1 Evaluation of existing components		
Start: M1	End: M24	Lead: C2N
Contributors: CNRS-C2N, UGA-IMEP-LAHC, CEA		
<p>Description :</p> <p>This task is devoted to the assessment of existing photonics passive and active devices in cryogenic environment, in relationship with WP6-3D &amp; Packaging and WP7-Cryogenic tests. CEA and CNRS will be mainly focused on Silicon-based and Silicon Nitride-based components, while UGA-IMEP-LaHC will be centered on Glass-based structures. For passive devices, insertion losses, spectral responses, and propagation losses will be evaluated, while for actives devices, speed, energy consumption, thermal dissipation, and compliance with Driver voltage limitation will be assessed, offering early inputs for T3.2.</p> <p>In this task, CNRS proposes to participate to the determination of the limit of Si and SiN photonics devices in Cryo environment. That includes (i) the determination of the limit of plasma dispersion (electro-optics effect currently used in Si) effect as a function of the temperature, (ii) the determination of the temperature limit of germanium waveguide detectors and avalanche photodetectors in terms of speed and responsivity and noise and the validation of passive photonic structures.</p> <p>UGA-IMEP-LaHC will contribute by providing its expertise and facilities in evaluating the performances of existing passive devices made on glass and pigtailed to optical fibers operated at cryogenic temperatures. It will provide with low-loss waveguides (&lt;0.1 dB/cm at ambient temperature) connected with optical fibers (insertion losses &lt; 2dB) and will evaluate the potential loss of transmission quality when the devices are brought to cryogenic temperatures (~4K). Cycled measurements to evaluate the aging of the fiber-waveguide connection could be carried-out if needed thanks to our new cryogenic bench test that is operating in a close-loop configuration. Once the connection between the waveguides and the fiber is validated, the behavior of wavelength multiplexing and de-multiplexing functions (typically AWG) will be performed in order to document the expected shift of their spectral response when cooled down from room temperature to cryogenic ones. During this assessment task, we</p>		

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could also perform measurements on photodiodes at the wafer layer (top illumination) thanks to the microwave and electric probes that complete the optical line of our cryogenic bench. Si-waveguides based functions like high-speed modulators or grating coupler-based devices could eventually be tested on our bench but it would require some developments.

In this task, CEA will provided passive and active devices based its 300mm SOI and 200mm SiN photonic platforms. Electro-Absorption modulator (SiGe, III-V/Silicon), or Polymer-based modulators might be added to the study, providing a first comparison with plasma dispersion-based modulators. For each device, room temperature characterization will be performed prior to the packaging and cryogenic tests. Cryo tests will be performed by other partners participating in this WP and WP7-Cryogenic tests, depending on the requirements (purely optical, electrical, DC, and RF measurements). It is worth noting that additional devices could be added in the test plan on the fly (phase change material, others...), relying on inputs from T3.2 and T3.4 that will precise further the system to circuits and devices specifications.

#### Deliverables (due month):

**ID3.1.1 Intermediate report on Si-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M12/CNRS-C2N)**

**ID3.1.2 Intermediate report on Glass-based passive and active photonics devices assessment in Cryo conditions (M12/UGA-IMEP-LAHC)**

**ID3.1.3 Final report on Si-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M24/CNRS-CNRS-C2N)**

**ID3.1.4 Final report on Glass-based passive and active photonics devices assessment in Cryo conditions (M24/UGA-IMEP-LAHC)**

#### T3.2 Photonics for Cryo

<b>Start: M1</b>	<b>End: M60</b>	<b>Lead: CEA-Leti</b>
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**Contributors: CEA, CNRS-C2N, UGA-IMEP-LAHC, Siemens EDA**

#### Description:

This task is focalized on the design and fabrication of high-speed photonic integrated circuits operating at cryogenic temperature. While passive devices evaluated in T3.1 may require 'only' some adaptations/customizations, high performances active devices at cryo temperature appear to be more challenging, especially when considering other constraints such as energy efficiency, temperature dissipation, and low swing voltage. Thus, this task will anticipate the need for disruptive modulation and photo-detection solutions. After an in-depth state of the art review together with a device to system level analysis, high-risk designs will be proposed and evaluated. Short-loop of fabrication on small wafer format will be employed to accelerate the assessment of the new design, prior to circuit demonstrators to be manufactured on larger wafer scale (200/300mm). A relatively high level of synergy and coordination between the three other tasks of this WP will be required to ensure that the high-risk design will be validated within the appropriate timeline for the demonstrators. Two demonstrators will be planned, the first one being anticipated as a proof of concept (POC) that may not reach the full specifications, while the final demonstrator should aggregate the best developments available at the time.

The first goal is to be able to select the best candidates for high performance modulation and photo-detection, but not only taking into account the performances at cryo temperature but also the manufacturability on large wafer scale, thus minimizing the risks in term of integration when the fabrication of the demonstrators will start. CEA will participate to the state-of-the art review as well as the co-development of the PIC (Photonic Integrated Circuit) in regard with T3.3 and T3.4 related to the drivers and system integration. CEA will contribute also to prototyping of advanced devices emerging from either existing solutions assessed in T3.1 and/or disruptive approaches found during the review process (which take into account not only the performances but also

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manufacturing concerns as mentioned above). Depending on the technological solutions that will emerge from D3.2.4, CEA will lead the realization of the photonics chips for a 1<sup>st</sup> POC (simplified transceiver operating at cryo temperature) and next the photonics chips for the final demonstrator, both in direction to T3.4 (Photonics subsystem merging the PIC and its driver).

CNRS-C2N will design new silicon photonics devices adapted to cryo temperature. In particular, electro-optics effects at such a temperature require intrinsic electronic properties, e.g. Kerr and Pockels effect. CNRS-C2N, in collaboration with CEA-Leti and STM propose to study different photonic structures and exploit different effect. First DC Kerr will be considered and study in cryo environment. Such effect has already demonstrated promising results and requires a complete optimization and characterization. In parallel, CNRS-C2N propose to study Pockels based photonic devices by the hybridization of ferroelectric materials (Lithium Niobate and Barium Titanate) on silicon and silicon nitride photonics platforms. CNRS-C2N has also a strong expertise in the development of fiber couplers (grating and inverted tapers), efficient wavelength filters with high power rejection (>100dB) and passive photonic devices (waveguides, ring resonators, Mach-Zehnder interferometer....). CNRS-C2N has also all the necessary facilities to rapidly fabricate passive photonic devices using ebeam lithography to validate certain concepts before larger-scale fabrication at CEA-Leti and STM.

UGA-IMEP-LaHC contribution for this task will be to design and provide a glass-based solution for interfacing the PIC made on silicon with optical fibers. This solution could contain wavelength multiplexing and demultiplexing functions if required. UGA-IMEP-LaHC will collaborate with CNRS-C2N and CEA-LETI to design and chose the most appropriate solution for this interfacing interposer, and will manufacture it before assembling it with the silicon PIC (**TBC with CEA-LETI**). UGA-IMEP-LaHC will rely on its state-of-the-art in-house simulation tools and its technology line dedicated to glass to perform these tasks. Depending on the determined test plan, our cryogenic bench will be part of the PIC qualification plan.

Siemens EDA will contribute to task 3.2 actions by providing access to its available industrial design tools (such as S-edit, L-edit, and LightSuite) and may allocate resources to support research and development work that would be performed when it is relevant.

#### Deliverables (due month/lead):

**ID3.2.1 Design of passive photonics structures (fiber couplers and filters) (M9/UGA-IMEP);**

**ID3.2.2 Design of DC Kerr & hybrid Pockels-based active devices (M12/CNRS-C2N);**

**ID3.2.3 Review of high performance active devices solutions considering integration challenges and updated system specifications (M12/CEA);**

**ID3.2.4 Experimental results of the first run of photonic passive & active devices (M24/CNRS-C2N);**

**ID3.2.5 Optimized structures: electro-optics devices and passive devices) (M36/CNRS-C2N)**

**ID3.2.6 Delivery of 1<sup>st</sup> Photonic IC for preliminary POC (M42/CEA)**

**ID3.2.7 Delivery of 2<sup>nd</sup> Photonic IC for final Demo (M60/CEA)**

#### T3.3 CMOS driver

<b>Start: M1</b>	<b>End: M60</b>	<b>Lead: CEA-List</b>
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**Contributors: CEA-List, Siemens EDA**

#### Description :

This task aims to design the appropriate CMOS drivers for the selected active photonic devices (modulation, demodulation). Considering a diversity of potential candidate physical phenomena used for these photonic devices, the task will be phased in steps from generic functions to co-designed electronics in interaction with the maturation of the photonic devices.

This task will have a high level of interactions with T3.2 and T3.4. It will start with device-independent functions, such as high-speed serializer and deserializer, to focus then on preliminary driver design with voltage or current modulation, with full-swing or low-swing signaling. Once the milestone for photonic device selection is reached,

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the next step is to specialize the drivers and to integrate all functions. Based on the milestone/deliverable D3.2.4 regarding the evaluation of the first generation of the photonics components for Cryo, a first simplified CMOS driver may be designed in order to qualify the photonic and electronic IC together at cryogenic temperature with reduced specifications as a proof of concept. Alternatively, external driver will be used, prior to the final driver design work that will be conducted for the Co-design of the demonstrator expected to start M48. The fabrication of the drivers, mostly through foundry runs, and subsequent post-processing is included in this task.

In the longer perspective, analog/RF signaling over photonic links will be studied, and tentative drivers will be designed.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

**Deliverables (due month/lead):**

**ID3.3.1 Generic Serdes characterization at cryogenic temperatures (M12)**

**ID3.3.2 Preliminary driver design with tentative device specs (current/voltage, swing amplitude & bandwidth) (M24)**

**ID3.3.3 Co-designed CMOS drivers for the selected photonic devices (M48)**

**ID3.3.4 Driver adaptation for analog/RF signaling (M60)**

#### T3.4 Integrated photonic sub-system for final demonstrator

<b>Start: M1</b>	<b>End: M72</b>	<b>Lead: CEA-list</b>
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**Contributors: CEA, Siemens EDA**

**Description :**

This task covers the cryo-compatible transceivers sub-system specifications, from the architecture to the device. One of the main challenge will be adjust the sub-system specification with the inputs from T3.1 on the photonics device assessment, together with the inputs of the other WP that will provide insights on the total power dissipation acceptance, the number of I/Os, or other constraints on the system (density/footprint, packaging, materials...).

In this task, In the first years of the program, CEA-**LIST** will provide system-level specification for ingress and egress needs through an optical cryo-photonic link, and iterate with T3.1/T3.2 to refine requirements in terms of bandwidth, integration, power consumption, interfaces between CMOS and photonics.

In a second phase of the program, CEA-**List** will coordinate the integration of the selected photonic devices and drivers in an electro-optical link architecture will be carried out , with potential integration on an optical interposer. This task will involve the interactions with WP6-3D&Packaging for the EIC – PIC assembly/packaging/3D integration and WP7-Cryogenic tests for the Cryogenic equipment for both the 1<sup>st</sup> POC and the Final demonstration.

Here, for the POC expected at M48 and for the Final demo expected at M72, the Photonic IC fabricated in T3.2 and the associated CMOS Drivers designed in T3.3 and fabricated in WP5-Cryo electronic must be assembled together through Packaging/3D integration in WP6-3D&Packaging (depending on the specs). Subsequently, the transceivers performances will be assessed by CEA-**leti** in this task at Cryo temperature by coupling the equipment from WP7-Cryogenic tests with high-speed communication setup corresponding to the specifications at both device and system levels.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools as described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

**Deliverables (due month/lead):**

**ID3.4.1 Intermediate report on device requirements and specifications for an optical cryo-photonic link (after preliminary reports and iterations with T3.1/T3.2 (M9)**

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**ID3.4.2 Final report on device requirements and specifications for an optical cryo-photonic link (after preliminary reports and iterations with T3.1/T3.2) (M24)**

**ID3.4.3 Link architecture specifications (M36)**

**ID3.4.4 Characterization report of integrated cryo-photonic link final demonstrator (M72)**

#### Work package deliverables

D3.1 Final report on Si and glass-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M24)

D3.2 Report on 1st Photonic IC for preliminary POC (M48)

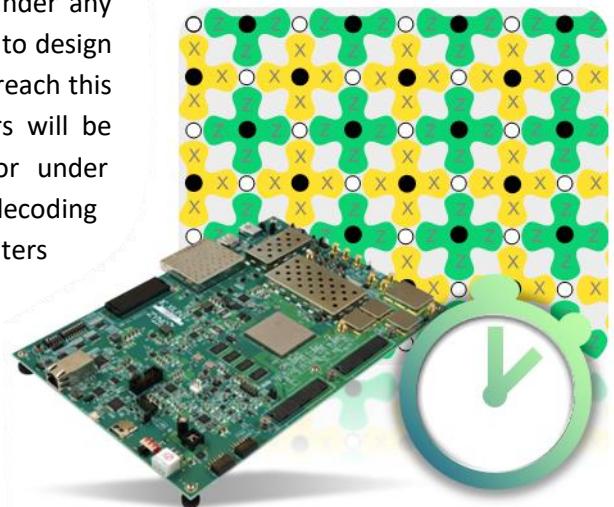
D3.3 Characterization report on integrated cryo-photonic IC for final Demo (M72)

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#### 4.4. WP4 Real-Time quantum error correction

##### 4.4.1. Work package objectives

Quantum error correction (QEC) is key to the development of a large-scale, fault-tolerant quantum computer, achieving the full computational power of quantum computing. However, the efficacy of a QEC solution is heavily dependent on its decoder: a classical algorithm that processes the extracted error syndrome to determine appropriate corrections. Previous research essentially focused on the accuracy (i.e., error correction capability) of the decoder, mostly ignoring scalability and real-time implementation constraints (critically, the decoding must be faster than the syndrome generation rate, otherwise it will introduce an exponential time overhead – in the number of non-Clifford gates – which will hinder any quantum advantage). In this context, the ambition of WP4-QEC is to design real-time QEC solutions that scale with the number of qubits. To reach this goal, software and hardware implementations of QEC decoders will be investigated, based either on existing decoding algorithms, or under development within the PEPR project NISQ2LSQ. For each decoding algorithm, a design space exploration will be performed for parameters of interest, to identify best tradeoffs in terms of accuracy, latency, power, and scalability. Acquired knowledge will be fed back to the system modeling in WP1-System model for the complete control chain design. To ensure fast exploration, and increase the adaptability of the design to QEC evolutions, hardware implementation will leverage High-Level Synthesis tools.



##### 4.4.2. Partners Role

Entity	Role
Inria	WP Co-leader Algorithmic Leader Expertise in QEC algorithms and compilation for quantum computing using logical gates
CEA	WP Co-leader Hardware design leader CEA will bring expertise from several teams, from QEC expertise ( <b>LETI</b> ) to hardware acceleration design ( <b>LST</b> ) applied to error syndrome decoding and quantum circuit compilation and optimization ( <b>IPhT</b> )
Siemens EDA	High Level Synthesis and EDA tool supplier and expertise support to the hardware design teams

Additional contributions from industrial partners joining the program may be added during the project execution.

##### 4.4.3. Detailed work description

T4.1 Software implementation of topological codes decoders		
Start: M1	End: M18	Lead: CEA
Contributors: CEA		

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#### Description:

Topological codes (e.g., surface or color codes) are currently seen as the main and most promising approach to fault-tolerant quantum computing, for a wide range of quantum technologies. The prevalent decoding solution is based on the minimum-weight perfect matching (MWPM) algorithm, commonly used to assess the error correction thresholds of topological codes, due to its superior error correction capability (accuracy). However, its complexity scales cubically with the number of qubits, which may prevent its use in practical applications, especially for large scale systems. Thus, a number of alternative solutions have been proposed in the literature, including greedy or approximate versions of the MWPM decoder, renormalization group based decoding, machine learning techniques based on neural networks, or the so-called union-find decoder.

In this context, the goal of this task is to uncover bottlenecks and identify decoding solutions that lend themselves to low-complexity and high speed hardware. CEA-leti will contribute to the development and the software implementation of decoding algorithms for topological codes. Specific C/C++ coding style required for HLS will be used for the decoder implementation.

The proposed contribution will build upon existing decoding solutions, while proposing further adaptations and/or simplifications, in order to bridge the critical gap between the algorithmic solution and the latency-power-scalability constrained hardware design.

#### Deliverables (due month/lead):

**ID4.1.1 Software implementation of QEC decoders from the literature (M6)**

**ID4.1.2 Software implementation of adapted QEC decoders with increased scalability potential (M18)**

#### T4.2 Hardware implementation of topological codes decoders

Start: M7	End: M30	Lead: CEA
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#### Contributors: CEA, Siemens

#### Description:

CEA-list will design a hardware implementation of topological code decoders provided by T4.1. Typical hardware conception flows augmented with High Level Synthesis (HLS) brought by Siemens will be used to produce the Register Transfer Level (RTL) model implementing this algorithm. Then, exploration of the design space to find good tradeoffs between performance and complexity will be conducted by CEA-list with Siemens support. Physical synthesis for FPGA and advanced CMOS technologies will be performed to assess the interest of such an accelerator in a large scale QPU and assess power, performance and area.

Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant

#### Deliverables (due month/lead):

**ID4.2.1 Report on first naive hardware implementation of error estimator for generic topological code (M20)**

**ID4.2.2 Report on refined hardware implementation of error estimator for generic topological code(M30)**

#### T4.3 Software implementation of decoders from PEPR NISQ2LSQ

Start:M12	End: M36	Lead: INRIA
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#### Contributors: INRIA, CEA

#### Description:

Quantum low-density parity-check (QLDPC) codes are a generalization of topological codes. Similar to topological constructions, QLDPC codes are defined by low (constant) weight generators, which allows simple fault-tolerant syndrome extraction and logical state preparation. Moreover, the QLDPC family has been recently shown to yield good asymptotic codes, with linear minimum distance and constant rate, which augurs for practical constructions

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with increased error correction capacity or reduced qubit overhead. However, decoding QLDPC codes is in general a difficult problem, constituting a very active field of research, and a number of decoding solutions are currently being developed within the PEPR project NISQ2LSQ.

The goal of tasks T4.3 and T4.4 is to take the developed solutions from the algorithmic level to respectively the software and the hardware implementation stages. INRIA will perform the implementation and benchmarking of the parallel decoders for QLDPC codes having large encoding rate and good error correction capacities (**QInfo**), and will further investigate rapid decoding algorithms and provide support for their implementation (**Cosmiq**). Inria (**Quantic**) will also investigate new LDPC codes designed for biased noise cat-qubits as the absence of one error component could significantly simplify the decoding requirements, and will also study cellular-automaton based decoders for topological codes designed for extremely biased noise qubits.

**CEA-list** will focus on message-passing decoding algorithms, for a class of QLDPC codes having the single-shot error correction property. Similarly to T4.1 coding style required for HLS will be used for the decoder implementation.

#### **Deliverables (due month/lead):**

#### **ID4.3 Software implementation of decoders for quantum LDPC codes and performance evaluation (M36)**

T4.4 Hardware implementation of decoders from PEPR NISQ2LSQ

<b>Start: M31</b>	<b>End: M54</b>	<b>Lead: CEA</b>
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**Contributors: CEA, INRIA, Siemens**

#### Description:

Similarly to the approach taken in T4.2, **CEA-list** will study in T4.4 hardware implementation of a selection of decoders from T4.3. Again, HLS will be used for early-stage exploration and then for the identification of performance-tradeoffs. Commonalities between the decoders of various codes will be studied to identify, where applicable, core IPs that could benefit from more optimization efforts. Finally physical synthesis for FPGA and advanced CMOS technologies will be performed.

Specific hardware implementation for cellular-automaton based decoders for topological codes may also be investigated by INRIA/Quantic as they may be integrated closer to the qubit using similar technologies. Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant

#### **Deliverables (due month/lead):**

#### **ID4.4 Report on hardware implementation of decoders for specific codes (M60)**

T4.5 Exploration of error correction tradeoffs (correction rate, latency, power, complexity)

<b>Start: M37</b>	<b>End: M60</b>	<b>Lead: CEA</b>
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**Contributors: CEA, INRIA**

#### Description:

Exploring the design space for efficient error correction requires to challenge its impact at all level, from the qubit topology constraints to the error decoding. Teams with complementary backgrounds will therefore conduct the exploration.

Having performed the hardware implementation of codes, CEA will focus is action on assessing the performance of decoding algorithms in terms of latency, power and resource usage (gates or mm<sup>2</sup>); as well as precision, since some codes, such as Edmond's MWPM algorithm, allow to trade latency for decoding accuracy by taking into account error locality.. As achieved precision shall be appreciated depending on the qubit properties, decoding procedure will be evaluated using Monte-Carlo simulations of error propagation for syndrome generation. Several aspects of the QPUs will be taken into account provided that input data is made available by partners developing qubit technologies (qubit connectivity, addressability and intrinsic parallelism, specific gate and qubit error models).

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Inria/QInfo will study the limitations the geometry of the physical qubits imposes on the fault-tolerance memory and time overhead. In particular, the maximum encoding rate that can be obtained as well as the best error correction capacity will be determined. Additional work will focus on the efficiency of the standard algorithms for error correction: this includes runtime, latency, communication between the different parts of the processor and power consumption.

Generated data in T4.5 will be integrated in the system model in T1.2.2.

#### Deliverables (due month/lead):

#### ID4.5 Report on QEC tradeoffs (M60)

T4.6 Hardware aware compilation of universal set of logical gates

Start: M31	End: M72	Lead: INRIA
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#### Contributors: CEA, INRIA

##### Description:

To exploit the benefits brought by the QEC, one must be able to perform quantum operations over logical gates composed of several physical qubits. Specific computation schemes must be sought out to do so. Task T4.6 will investigate several compilation approaches to provide efficient computing with error-corrected qubits :

(A) When using quantum error correcting block codes, encoding several logical qubits in one block, the set of fault-tolerant quantum gates accessible can be very different from standard gate sets. Indeed cases arise where one can have access to a few easy (transversal) gates acting on all logical qubits at once. For instance, in some situations, one can obtain a large circuit of CCZ or CZ on the logical level obtained from a transversal T gate on the physical level. While on the contrary being able to implement targeted single or two qubit gates within the code block is more difficult. Circumventing this often resort to using some tricks such as teleportation, code deformation or Pauli measurements all with additional auxiliary qubits needed making these gates more costly. Inria/Loria will develop compilers able to handle these constrained gate sets will allow to take advantage of the higher encoding rates of block codes without paying too much price in gate implementations.

(B) As the choice of error correcting scheme imposes strong constraints on the computational framework, possibly very distinct from the usual Clifford+T formalism, Inria/QuaCS will study various models of execution and the such as Measurement-based Computation (MBQC), Quantum Cellular Automata (QCA), and exotic gate-sets such as Clifford+Toffoli. The work conducted with the help of graphical languages such as ZX or ZH calculi could lead to the definition of transpilation or code optimization strategies.

(C) As magic state distillation is one of the most resource-consuming primitives in surface code-based quantum architectures, CEA will develop a hardware-agnostic tool that will translate a logical circuit for state distillation into a sequence of physical gates. Established techniques in quantum circuit optimization will be implemented. Then, a secondary goal will be to adapt this approach to specific architectures whose properties could be shared by industrial partners joining the program.

(B) To further reduce the overhead of error correction CEA/IPhT will develop a systematic numerical method to optimize low-depth circuits working on a limited set of qubits, and will seek to exploit it to optimize stabilizer measurements for different codes, and assess the impact on their correction thresholds.

#### Deliverables (due month/lead):

#### ID4.6 Compilation flow for error correction (M72)

T4.7 Final Demonstrator

Start: M49	End: M72	Lead CEA
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#### Contributors : CEA, INRIA

##### Description :

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Concerning the final project demonstrator, options for the QEC contributions are very open at this stage. Indeed, it is yet to be confirmed that large enough qubit resources could be developed by industrial players to allow for their integration in complementary projects leveraging the final LSQ demonstrator. In addition, works conducted in T4.2 and T4.3 may conclude on the need for ASIC implementation of decoders, which is not in the scope of the project to date. Consequently, the practical validation of an error correction loop may be out of reach of the project.

Still, the final demonstrator shall seek to be able to prove correct interoperability between all elements of the control chain. Hence, in a pessimistic scenario, this task will focus on the definition, and implementation of interfaces to the remainder of the control chain for future QEC integration. In an optimistic scenario, the task will aim to provide inclusion of FPGA decoders and practical validation of QEC loop.

**Deliverables (due month/lead):**

**ID4.7 Demonstration for quantum error correction (M72)**

Work package deliverables

- D4.1 Report on software implementation of adapted QEC decoders with increased scalability potential (M18)
- D4.2 Report on refined hardware implementation of error estimator for generic topological code (M30)
- D4.3 Report on soft decoders from NISQ2LSQ (M36)
- D4.4 Report on hardware implementation of decoders for specific codes (M60)
- D4.5 Report on demonstration for quantum error correction (M72)

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#### 4.5. WP5 Cryogenic electronic

##### 4.5.1. Work package objectives

Solid-state circuits operating at cryogenic temperature are more and more critical to address the challenges related to quantum computing applications. Indeed, performing operations on quantum bits (qubits) like control and read out, requires classical electronic controllers. As soon as quantum processors become more complex, classical electronic control approaches, requiring multiple RF and DC cables per qubit and each connected to room-temperature instruments, are no longer a sustainable way.

A promising approach consists in considering the integration of read-out and control circuitry in standard CMOS technologies operating at cryogenic temperatures. In such a way, significant form factor is reachable, enabling more qubit control complexity while limiting power consumption and being a cost-effective solution. This work package aims at developing CMOS model & 4K add-on to FD-SOI PDK to enable design-blocks in cryogenic conditions, and at evaluating and maturing electronic amplification devices technologies.

Beside the CMOS circuitry, solid-state qubits read-out and control often use circulators, low noise amplifier (LNA), and several superconducting electronic devices like specific very low power and very low noise amplifiers (known as Traveling-Wave Parametric Amplifiers, TWPA). The project will evaluate BiCMOS and LNA integration together with circulators, and investigate the scaling of production by industrialization of the fabrication process to increase yield. CMOS circuits and electronic components developed in this WP will be integrated in the demonstrator.

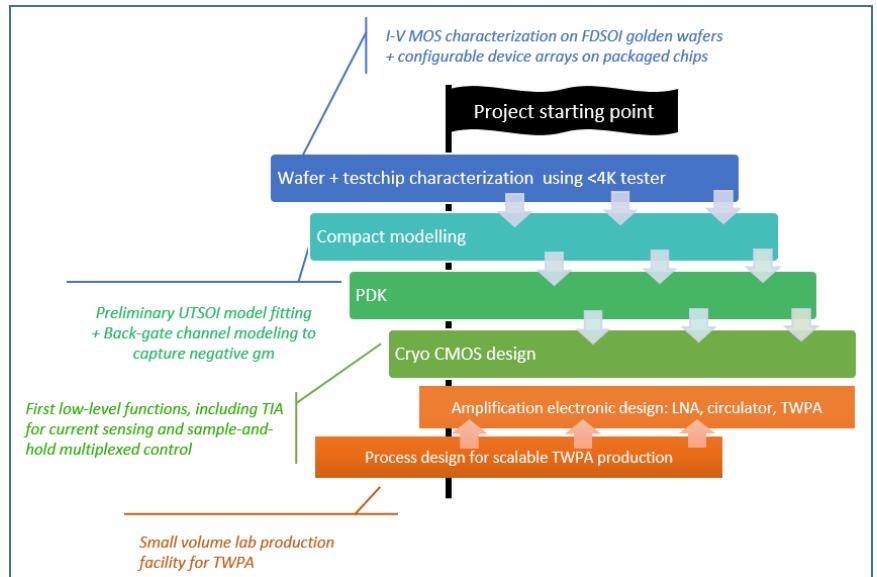


Figure 19 – Logical diagram of WP5 actions for CryoCMOS design

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#### 4.5.2. Partners Role

Entity	Role
ST MICROELECTRONICS	Work Package Leader Will give access to the FD-SOI technology to update the 28FD PDK for 4K (and possibly 77K) applications.
CEA	Will characterize devices, develop models, and implement designs for cryogenic electronics. Will evaluate electronics devices.
UGA-IMEP-Lahp UGA-TIMA	Will characterize devices (noise and 77K), contribute to models development and to self-heating study. Will contribute to design model evaluations
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design and modeling work in T5.2 and T5.4 tasks.
CNRS-Néel	Will contribute to TWPA developments

Additional contributions from industrial partners joining the program may be added during the project execution.

#### 4.5.3. Detailed work description

T5.1 Devices characterizations at 4K (and 77K sampling) for PDK Add-On		
<b>Description:</b> This task is very dependent of characterization means availabilities, capabilities and capacities (WP7-Cryogenic tests, T7.1 and T7.2.1). The tasks can start with manual and none statistical characterizations but the full task execution supposes strong amplification and industrialization of characterization means.		
T5.1.1 FEOL devices characterization at 4K (and 77K sampling)		
Start: M1	End: M36	Lead: CEA
<b>Contributors:</b> CEA / ST MICROELECTRONICS / UGA-IMEP		
<b>Description:</b> To enable circuits 28nm FD-SOI circuits design at cryogenic temperatures especially at 4K, several FEOL devices such as NMOS and PMOS transistors, (if possible according to WP7-Cryogenic tests, resistors, decoupling capacitors, junction diodes) must be modeled. To do so, those devices must first be characterized in various domains, including DC, AC and noise (LFN / RTN for UGA-IMEP). Then, to address RF applications, extra HF characterization based on S-parameter and possibly Noise Figure (NF) measurements may be needed, coming with their own challenges in terms of calibration procedure (either on-wafer or based on external substrate standards) and linear (small-signal) device operation at cryogenic temperatures 4K (and 77K sampling).		
According to the previous results and output of WP7-Cryogenic tests T7.2.1, it could be interesting to investigate the statistical approach and measurement strategies in the framework of the pre-industrialization of cryogenic PDK.		
As a perspective for Year 4 to Year 6, we can consider next FD-SOI generation node characterizations at cryogenic temperature. And for Year 6, high frequency noise measurement at cryogenic temperature.		
<b>Deliverables (due month/lead):</b> <b>ID5.1.1.1 Report on devices characterizations (M12)</b> <b>ID5.1.1.2 Report on devices characterizations (M24)</b> <b>ID5.1.1.3 Report on devices characterizations (M36)</b>		
T5.1.2 BEOL interconnect and RF passives models		
Start: M1	End: M36	Lead: CEA

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## Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP

### Description:

Qubits control and read-out require the generation and acquisition of specific RF signals, leading to the need of several RF blocks that could be assimilated as wireless RF transceiver.

To enable electromagnetic RF passives modeling and dimensioning at cryogenic temperatures, we have to implement the accurate extraction of BEOL physical values. In addition to low frequency physical parameters, a validation of the above-calibrated stack will be mandatory versus frequency up to 30 GHz if possible according to WP7-Cryogenic tests T7.2.1.

The technology considered for BEOL interconnect model and RF passives devices enablement will be the 28nm FDSOI node from STMicroelectronics. Cryogenic temperature of interest will be 4°K (and 77°K by sampling).

As a perspective for Year 4 to Year 6, we can consider next FD-SOI generation node characterizations at cryogenic temperature.

### Deliverables (due month/lead):

**ID5.1.2.1 Report on BEOL and RF characterizations (M12)**

**ID5.1.2.2 Report on BEOL and RF characterizations (M24)**

**ID5.1.2.3 Report on BEOL and RF characterizations and passive RF model (M36)**

### T5.1.3 Reliability tests

Start: M1	End: M36	Lead: CEA
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## Contributors: CEA / ST MICROELECTRONICS /UGA-IMEP

### Description:

The specific simulation models for the Cryo modeling is planned to be available using a PDK add-on on the existing PDK release. This will require cryogenic environment reliability tests and collection of reliability data. The set-up of wafer level tests at cryogenic temperatures, should allow reliability testing to cover:

- (1) gate dielectric and inter-metal dielectric breakdown
- (2) NBTI/PBTI aging and
- (3) HCl aging in “on” and “off” state mode.

Measurements protocol will first have to be adapted and applied to cryogenic environment.

Based on experimental results, existing reliability models will then be extended down to 4K.

### Deliverables (due month/lead):

**ID5.1.3.1 Report on measurement protocols (M12)**

**ID5.1.3.2 Report on aging characterization results (M36)**

### T5.2 Compact model developments for FD-SOI transistors and diode at cryogenic temperatures

Start: M1	End: M72	Lead: CEA
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## Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP / SIEMENS EDA

### Description:

The first year will be dedicated to the improvement of the core’s model. Indeed, at cryogenic temperatures several effects appear such as the observed double kink effect on the drain current in inversion regime and a specific linear-saturation transition. In addition, a first model library containing NMOS and PMOS transistors models in typical case will be implemented in PDK environment. These models will reproduce DC and CV characteristics.

The low frequency noise (LFN) modeling and the substrate modeling will be done in the second year. An update of the model library will use the results of these last works. In parallel, a dedicated parameter extraction flow will be optimized for cryogenic temperatures.

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During the third year, new MOSFET models for RF applications and models for diodes will be developed always for typical case. They will be implemented in the PDK. The MOSFET model will include the effect of multi-finger layout.

The variability modeling will be done during the fourth year, depending on data availability (WP7-Cryogenic tests industrialization). The goal will be to update the model library by introducing corners and Monté Carlo simulation capabilities.

The 2 last years will be focused on the implementation of reliability models in PDK and several updates of model library by introducing the best experimental data. Finally, during the last year of this project, high frequency noise (HFN) modeling will be covered to improve the RF MOSFET models.

Siemens EDA, will contribute to the actions by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre... ) and needed support.

**Deliverables (due month/lead):**

**ID5.2.1 Report on MOSFET model developments at cryo temperature and validation using experimental data (based on DC-CV present silicon data) (M12)**

**ID5.2.2 Report on MOSFET modeling for RF applications at cryo temperature and validation using experimental data (M36)**

**ID5.2.3 Report on variability modeling at cryo temperature including RF aspect (M48)**

**ID5.2.4 Report on model libraries update and HFN modeling (M72)**

T5.3 First 28FD-SOI PDK 4K (and 77K) add-on implementations

<b>Start: M1</b>	<b>End: M36</b>	<b>Lead: ST MICROELECTRONICS</b>
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**Contributors: ST MICROELECTRONICS**

**Description:**

The specific simulation models for the Cryo modeling is planned to be available using a PDK Add On to the existing 28FD-SOI PDK release. This will require the development of cryogenic models with the constraints of fitting to the PDK model interfaces. This will ease the development and ensure the alignment with the standard PDK for designer community. The Focus will be done on 4K model encapsulations (77K should be an extrapolation and option; not be consider as target for this study) compliant with the process and tools flow in industrial environment.

As a perspective for year 4 to year 6, we can consider a new FD-SOI PDK add-on with variabilities.

**Deliverables (due month/lead):**

**ID5.3.1 Report on PDK add-on (M36)**

T5.4 Cryo CMOS design

In this program, following the analysis performed in WP2-Architecture, CEA will specify and design generic integrated functions for scalability and dynamic control and read-out and exploring FD-SOI capabilities in cryogenic interface electronic for large scale quantum computing.

Because design at cryogenic temperature is not yet possible with appropriate process design kit, CEA will work the methodology to accomplish a valuable design process in the task T5.4.1. In the meantime, UGA-TIMA propose to work on design modeling.

Task T5.4.2 will aim at designing control, readout and digital communication functions with, if possible, 3 loops of learning.

On both tasks, Siemens EDA, will contribute by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre... ) and needed support.

T5.4.1 Cryo CMOS design methodology and PDK evaluation 28nm

<b>Start: M1</b>	<b>End: M72</b>	<b>Lead: CEA</b>
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**Contributors: CEA, Siemens EDA, UGA-TIMA**

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## Description:

Design oriented models allow simple but efficient analytical design method based on gm/ID or IC parameters. These models are based on charge modeling and use a very small set of parameters (between 3 to 7). Recent works show how such models are well suited to advanced nodes and to low and weak inversion regime, where region-based models are limited. In addition, these works show that non-linearities or bandwidth limitation can be captured. The model parameters can be extracted based on few DC measurements which are accessible in cryogenic frameworks.

In this context, UGA-TIMA propose three research lines:

- Using the models already developed, UGA-TIMA propose to investigate how these models are suited to cryogenic devices and which parameters are required to capture the MOS behavior in cryogenic environment.
- Based on a design-oriented model and a set of extracted parameters for MOS transistors in cryogenic environment, design methods will be investigated for readout devices.
- The issue of testing cryogenic devices can be investigated through the correlation that could exist between the model parameters at cryogenic temperature and room temperature. Testing methods could be investigated based on this approach allowing the screening out of devices at higher temperatures leaving only good candidates for cryogenic temperatures.

Design learning (CEA): because design at cryogenic temperature is not yet possible with appropriate process design kit, this task is focused on the methodology to accomplish a valuable design process. The objectives are

- to set up a properasic design and tests flow, based on partial cryogenic PDK
- to design cryogenic benchmark circuits, analog and digital (e.g. amplifier and integrated logic characterization circuits for flip-flop and combinational gates)
- to benchmark and conclude on design rules and test practices thanks to characterizations results.

First year will be devoted on designing cryogenic test chip analog and digital: schematics design based on gm/id approach (tentative models), simulations at room temperature and approximate projection to cryogenic results, tape out preparation.

Depending on process cycle time, second year will deal with test chip characterizations, retrofit analysis, methodology refinement, and benchmarking of available cryogenic compact models based on circuit simulation vs circuit characterization. Optimized benchmark circuits could be proposed if necessary, depending on results and models development.

During the following years, CEA will continue the evaluations of the PDK add-on upgrades from WP5-Cryo electronic T5.3 through designs and characterizations loops.

## Deliverables (due month/lead):

ID.5.4.1.1 Report on benchmark test chip design (M12)

ID.5.4.1.2 Report on benchmark test chip characterization (M30)

ID.5.4.1.3 Report on retrofit analysis, methodology refinement, and benchmarking (M36)

ID.5.4.1.4 Second report on retrofit analysis, methodology refinement, and benchmarking (M54)

ID.5.4.1.5 Final report on retrofit analysis, methodology refinement, and benchmarking (M72)

T5.4.2 Generic design for demonstrator: Qubit control and readout and digital control, processing and communication functions.

Start: M1	End: M72	Lead: CEA
<b>Contributors: CEA, Siemens EDA</b>		

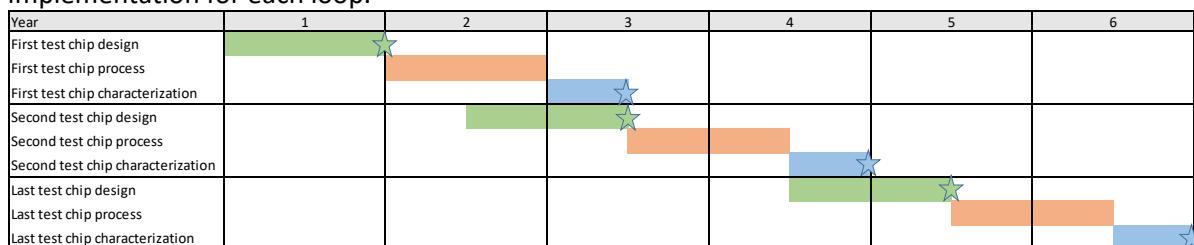
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## Description:

This task aims at designing ultralow power consumption, Qubit control and readout functions (IP targeted could be: CMOS-based dynamic digital-to-analog converter, analog buffers, high-speed mux and demux, CMOS-based amplifiers and analog-to-digital converter for qubits readout, biasing circuits and oscillators) as well as digital functions for communication interfaces.

The task goes from blocks architecture study to design, and test and characterizations at cryogenic temperature. Different test chips are planned to be fabricated, and some will be designed to be embedded in 3D and supra demonstrators of WP3-Integrated Photonics.

During the 6 years of the program, CEA aims at performing 3 loops of design learning with new functions implementation for each loop.



## Deliverables (due month/lead):

- ID5.4.2.1 Report on test chip1 design (M12)
- ID5.4.2.2 Report on test chip1 characterization (M30)
- ID5.4.2.3 Report on test chip2 design with more functions (M30)
- ID5.4.2.4 Report on Test chip2 characterization (M48)
- ID5.4.2.5 Report on demo chip design with more functions (M54)
- ID5.4.2.6 Report on demo chip characterization (M72)

T 5.5 Amplification devices evaluations at cryogenic temperatures

Start: M0	End: M72	Lead: CEA
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Contributors: CEA, STM, CNRS

## Description:

The amplification chain requires parametric amplifiers (like TWPs) and LNA, specified and designed for cryogenic applications.

TWPA: Currently, J-TWPA are being manufactured in academic-grade clean room facilities and rely on fabrication processes that are not scalable nor reproducible enough for the anticipated volumes of TWPA necessary for the future solid-state quantum computing architectures. The development of a CMOS-like fabrication process for reliable and reproducible way to manufacture Josephson junctions is crucial for European Sovereignty. Such process can be developed in the CEA-leti. Furthermore, this development could not only benefit the TWPA manufacturing process, but also laboratories and companies related to quantum information with superconducting circuits.

This task goes from the design of the Josephson junctions (CEA) to their characterization (CNRS-Neel), both at room temperature and at sub-kelvin temperatures (10mK). It could include the design and the characterization of short Josephson junction arrays working as resonant parametric amplifiers as a proof of concept.

Low Noise Amplifiers: current available LNA power consumption is above 20mW. The quantum needs are to reduce from one decade (around 1 mW). This task aims at evaluating ST B55x technology, understanding the limitations, and through integrated design, improving the performance.

Circulators are "must-have" cryogenic components for the most advanced quantum experiments. They are necessary to avoid the noise from the front-end low noise amplifier (LNA) to radiate onto the sample. So far the only

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available cryogenic circulators which use a local static magnetic field are very bulky (typ. 2x2x1cm3) and they work only at high frequency (several GHz). Recent works using CMOS technology demonstrated that circulators based on transistors can be realized. This task aims first at evaluating and characterizing ST CMOS technology to realize circulators. CEA then propose to go beyond the state of the art by combining the best of both worlds thanks to the complementary aspect of BiCMOS technology: using the CMOS part for the circulator and the bipolar (HBT) transistor technology for the best LNA.

Components developed in this task will be implemented in the demonstrators.

**Deliverables (due month/lead):**

**ID5.5.1 Report on the design of the first generation of test Josephson junctions for TWPA (M6)**

**ID5.5.2 Report on cryogenic and room-temperature characterization of the test Josephson junctions for TWPA (M24)**

**ID5.5.3 Report on the design of the second generation of test Josephson junctions for TWPA (M24)**

**ID5.5.4 Report on cryogenic and room-temperature characterization of the second generation of test Josephson junctions for TWPA (M42)**

**ID5.5.5 Report on the design of the first generation of short array resonant amplifier (M48)**

**ID5.5.6 Report on cryogenic and room-temperature characterization of short array resonant amplifier (M72)**

**ID5.5.7 Report on LNA characterization and development (M36)**

**ID5.5.8 Report on CMOS circulators characterization and development (M48)**

**ID5.5.9 Report on circulators and LNA co integration (M72)**

**Work Packages deliverables:**

D5.1 Report on benchmark test and demo1 chip design (M12)

D5.2 Report on Cryo CMOS characterizations report (M36)

D5.3 Report on PDK add-on (M36)

D5.4 Report on demonstrator chip design (M54)

D5.5 Final chip and amplification demonstration (M72)

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#### 4.6. WP6: 3D integration and packaging

##### 4.6.1. Work package objectives

The aim of work package 6 is to validate the complete communication chain in terms of cryogenic electro-thermal behavior. As illustrated in Figure 20, the scope of the study ranges from the qubits to the outside of the cryostat. Starting from WP2-Architecture recommendations, system architecture hypotheses will be investigated regarding interconnections key technologies, parasitic and power dissipation. To achieve this goal, low temperature characterizations of raw materials and elementary integrated modules will feed simulation and modeling. A schematic view of the work package is introduced in Figure 21. Task T6.1 will be in charge of the fabrication of test vehicles that will be packaged within T6.2 (it will also include photonics packaging issues stemming from WP3-Integrated Photonics). Experimental characterizations of these packaged test vehicles will be performed in T6.3 and the output data will be used to feed modeling and simulation task T6.4 that will also seek to define a thermal simulation methodology allowing to

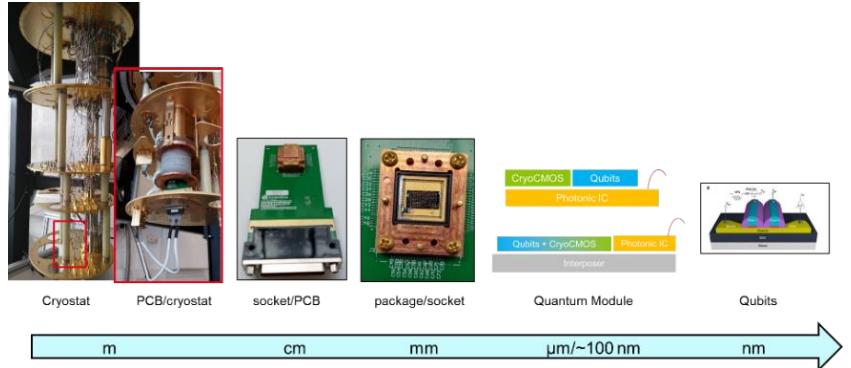


Figure 20 - Scope and range of interconnections of a qubit control chain  
(Quantum Silicon Grenoble)

interoperate low-level simulations in cryogenic conditions with thermal simulation tools already qualified for standard temperature ranges. The methodology will be used to define specifications for the test vehicles of T6.1. Based on the acquired knowledge of T6.1, T6.2, T6.3 and T6.4 outputs, task T6.5 will develop 3D interconnection and packaging solutions to manage optimally heat fluxes and high-frequency signals that will propagate in the final demonstrator.

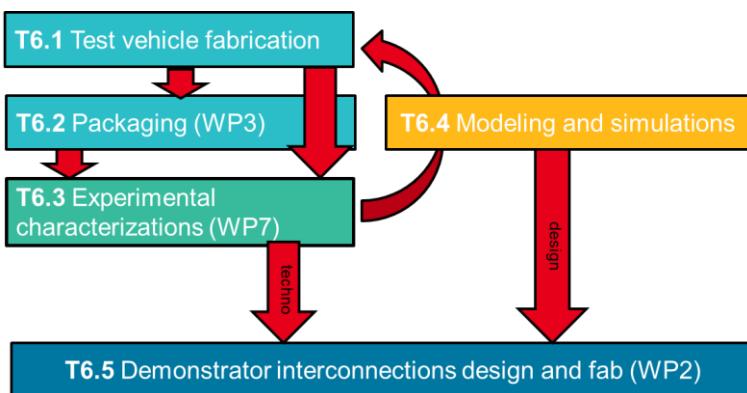


Figure 21 - WP6: 3D & packaging -task chart

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#### 4.6.2. Partners Role

Entity	Role
CEA	Work package leader With its expertise in 3D integration technology, demonstrator assembly (e.g. P. Coudrain <i>et al.</i> , ECTC (2019)) and superconductor integration (C. Thomas <i>et al.</i> , <i>Mater. Quantum. Technol.</i> , (2022)), CEA will lead the 3D and Packaging work package.
CNRS / Néel Institute	With its expertise in thermal characterization at low temperatures, CNRS will support the work of WP6 through the low temperature tests conducted in T6.3, and will therefore participate in the specification definition and design of the test vehicles in T6.1.
Siemens EDA	Siemens will provide the required support to assess their simulation tools applicability to cryogenic thermal conditions especially in T6.4.
STM	STM would support the work of WP6 by providing short loop BEOL samples for interconnection characterizations at low temperatures, as well as partial MPW wafers (with WP2-Architecture, WP3-Integrated Photonics and WP5-Cryo electronic) for specific CEA post-process for bumps and potential superconducting integration.

Additional contributions from industrial partners joining the program may be added during the project execution.

#### 4.6.3. Detailed work description

T6.1 Test vehicle fabrication		
Start: M1	End: M48	Lead: CEA
<b>Contributors:</b> CEA, CNRS, STM		
<p><b>Description:</b>            Test vehicles made from, first, raw materials deposited on blanket wafers and then, patterned materials, forming simple structures such as lines and bumps, will be fabricated to build a material and interconnection property database. During a second phase, elementary technological modules (daisy chain assemblies, superconducting multilayer stacks) will also be processed to complete the database and feed the model and simulations tools (T6.3). Process developments will involve superconducting material integration. Post-processing of Cryo electronic (WP5), Photonic IC (WP3) or Interposer wafers, will be envisioned with respect to developments conducted in the WP2-architecture.</p> <p><b>Deliverables (due month/lead):</b>  <b>ID6.1.1-2-3-4 Annual sample and module delivery report (M12-24-36-48/CEA)</b></p>		
T6.2 Packaging of test vehicles and demonstrator		
Start: M1	End: M72	Lead: CEA
<b>Contributors:</b> CEA		
<p><b>Description:</b>            While Printed Circuit Board (PCB) design &amp; fabrication will be included in WP7-Cryogenic tests, the other packaging items and tasks will be addressed here. It includes the optical fiber attachment (Pig-tailing) in close collaboration with WP3-Integrated Photonics and qualification of the connectors and sockets (with PCB design inputs from WP7-Cryogenic tests). A dedicated study will be conducted on the behavior of co-packaged optics/electronics at low temperature and specifically on Ball Grid Array (BGA) or Quad Flat No lead (QFN) type of packages and their sockets, which will need engineering. Each of the investigated packaging solutions will be evaluated in terms of parasitic and thermal propagation properties.</p> <p><b>Deliverables (due month/lead):</b>  <b>ID6.2.1 Report on packaging strategy for test vehicles (M24/CEA)</b></p>		

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## ID6.2.2 Report on optical fiber attachment for low temperature operations (M36/CEA)

### ID6.2.3 Report on demonstrator global packaging (M72/CEA)

#### T6.3 Experimental characterizations

Start: M1      End: M72      Lead: CEA

Contributors: CEA, CNRS Neel

##### Description:

The experimental characterizations will be divided in 3 main families as described below.

a) Mechanical and electrical characterizations. This will include the tests of different materials and technological bricks, such as 2D routing lines and 3D interconnects, to extract the following parameters: electrical resistance and capacitance @ 300K, electrical resistance at cryogenic temperatures, superconducting properties ( $T_c$ ,  $J_c$ ,  $B_c$ ) when applicable, Coefficient of Thermal Expansion (CTE) between 300K and 77K (methods to be developed) and E (Young Modulus) @ 300K.

b) Thermal characterizations. This will comprise the experimental measurements in cryostat to extract the thermal conductivities of materials and technological bricks as well as fundamental thermal behavior characterizations for tool/model assessment of T6.4.

c) RF and photonic characterizations. The first objective will be to extract the RLCG parameters of simple structures at 7K using a dedicated VNA and cryo-prober set up. Concurrently, RF characterizations of the packaging environment will be carried out to evaluate signal bandwidth and losses through the packaging supports and sockets with WP7-Cryogenic tests. The second objective will be the elaboration and qualification of the optical test set up and measurement protocol at low temperatures to characterize photonic passive devices and then active ones.

##### Deliverables (due month/lead):

ID6.3.1 Report on raw material and simple interconnection database (M24/CEA)

ID6.3.2 Report on 1st optical test set up and simple photonic passive devices tests (M24/CEA)

ID6.3.3 Report on thermal measurements for fundamental thermal behavior (M36/CEA)

ID6.3.4 Report on RF & Thermal measurements of interconnections including package & socket (M48/CEA)

ID6.3.5 Report on opto-electrical tests of active devices (M48/CEA)

#### T6.4 Modelling and simulations

Start: M1      End: M60      Lead: Siemens

Contributors: Siemens, CEA, CNRS Neel

##### Description:

As thermal behavior, drastically changes at low temperatures and small scales, advanced thermal simulations will need to be carried out based on expected behavior of phonon transport. Thermal exchange at small length scale and below 4K, with specific attention to interfaces phenomenon will be explored thanks to dedicate experiments and samples design. Dedicated expert softwares such as Non-equilibrium Green's Function based FeNEGF will be exploited to this end. Adapted strategies for interoperations between low-level (FeNEGF) and system-level thermal simulation (Flotherm) tools will then be investigated in synergy between institutional and industrial actors. This shall enable the definition of a system-level thermal model methodology for cryogenic temperatures that will also be completed with a system-level RF modeling. Depending on software development and Task 6.3 test results , RF simulations will be carried out with the full control chain perspective

##### Deliverables (due month/lead):

ID6.4.1 Report on low level thermal simulation of individual interconnections (M24/CEA)

ID6.4.2 Report on system-level thermal model (including optical compound) (M36/Siemens)

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### **ID6.4.3 Report on system-level RF and thermal models adapted to the architecture of control chain demonstrator (M60/CEA)**

T6.5 Control Chain Demonstrator

<b>Start: M37</b>	<b>End: M72</b>	<b>Lead: CEA</b>
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**Contributors: CEA**

**Description:**

The first part of the task will concentrate on the delivery of an optimized design of the control chain interconnections based on thermal, RF and photonic data and models at all scales: integrated photonics, 3D integration, packaging I/O, PCB design, cryostat cables in close link with WP2-Architecture, WP3-Integrated Photonics and WP7-Cryogenic tests. The second part of the task will address the demonstrator module fabrication itself with incoming components such as photonic dies from WP3-Integrated Photonics, CryoCMOS dies or wafers from WP5-Cryo electronic and PCB from WP7-Cryogenic tests.

**Deliverables (due month/lead):**

**ID6.5.1 Report on interconnection specifications for control chain demonstrator (M46/CEA)**

**ID6.5.2 Report on control chain demonstrator module design (M54/CEA)**

**ID6.5.3 Report on control chain demonstrator module fabrication (M72/CEA)**

Work package deliverables

D6.1 Report on first samples characterization (M24)

D6.2 Report on system-level thermal model (M36)

D6.3 Report on control chain demonstrator module design (M54)

D6.4 Report on control chain demonstrator module fabrication (M72)

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#### 4.7. WP7 Cryogenic characterization

##### 4.7.1. Work package objectives

This work package aims at addressing the cryogenic characterization needs of the other work packages. CEA-**leti**, CEA-**IRIG**, CNRS-**Neel**, UGA-**IMEP-Lahc** already have cryogenic characterizations capabilities, but our first analysis highlights that the LSQ program will need additional testing resources since existing facilities workload is already high. In addition, the scaling naturally calls for statistical characterizations, which in turn require tools and characterization methods industrialization.

First actions in Task 7.1 will then aim at evaluating missing capabilities and capacities to address the program needs, defining the specifications, acquiring and installing needed tools and upgrades.

Besides the hardware needs, characterization methods, both at wafer level and at system level, need to be developed and improved. Task 7.2 will address these actions.

Task 7.3 will implement appropriate automation and systems to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

Finally, as required for nowadays qubit control, we expect that room temperature electronics will be needed using either RF signal sources as well as optical ones. Signal shaping solutions, adapted to the scaling, and able to interoperate with QEC may also be required for test and demonstration purposes and task 7.4 will address these points. As all work packages will need access to characterization tools, last task is the coordination and scheduling of these accesses.

##### 4.7.2. Partners Role

Entity	Role
CEA	Expertise and infrastructures for cryogenic test and room temperature electronic
CNRS <b>Neel</b>	Work Package Leader Expertise and infrastructures for cryogenic test
UGA- <b>IMEP-Lahc</b>	Expertise on Self-heating phenomena

Additional contributions from industrial partners joining the program may be added during the project execution.

##### 4.7.3. Detailed work description

T7.1 Equipment needs identification & equipment acquisition		
Start:M1	End:M24	Lead: CEA
Contributors: CNRS-Neel, CEA, UGA-IMEP		

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#### Description:

Our first analysis highlights that the LSQ program will need statistical characterizations, which require tools and characterization methods industrialization. Typically, WP5-Cryo electronic requires strong amplification and industrialization of characterization means for DC, RF and aging: 28FD PDK 4K add-on needs statistical wafer level characterization.

Statistical test required (wafer level)	Availability (CEA or CNRS-Neel or UGA-IMEP)
DC	Die only. Cryogenic prober available but strong need of industrialization.
RF	Die only. Cryogenic prober retrofit needed and probe card concept at cryogenic temperature to be evaluated: Instrumentation for MOS characterization (DC up to 1MHz) may be needed. Cabling for RF measurements up to few tenth of GHz
Aging	Die only. Cryogenic prober available but strong need of industrialization.

CEA manual cryogenic prober (Lakeshore CPX) are currently working with open loops cooling systems. To limit the project environmental footprint and reduce operation expenditures that would spur with test industrialization, we will plan the necessary upgrades. Some may also need an upgrade of RF probes for more reliable measurements. UGA-IMEP's 6 arms prober is DC only and RF upgrades on 2 arms would add some capacity for RF characterizations.

Besides tools capabilities and industrialization needs, we suspect that scaling up will increase the need for statistical wafer level characterizations and therefore may require supplying a second cryogenic prober, and some manual probers.

For single transistors or devices characterizations (WP5-Cryo electronic), RF and photonic characterizations (WP3-Integrated photonics & WP6-3D&Packaging), new cryostat and control electronics capacities may be needed both at CEA-IRIG et CNRS-Neel.

This task aims at evaluating the exact needs of the program to define the investment plan for upgrades, or new tools supply, in coherence with 'Cryogenic Plan'. An in-depth analysis of characterization volumes, put in perspective with existing equipment workload and productivity ramp-up, will be conducted to assess the benefits of such investments.

#### Deliverables (due month/lead):

ID7.1.1 Report on needs evaluation and investment plan (M3),

ID7.1.2 Final report on tools upgrade and installations (M24)

#### T7.2 Characterization methods developments

##### Description:

Besides the hardware needs, characterization methods, at all levels (from transistor to system) and scales (from single device to wafer), need to be developed and improved. Task 2 will address these actions.

##### T7.2.1 DC, RF and Aging Cryogenic wafer level probing pre-industrialization

Start: M1

End: M72

Lead: CEA

Contributors: CEA

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#### Description:

Due to cryogenic conditions, the cryogenic wafer level prober needs specific designs on the last metal levels: pad pitches need to be relaxed compared to standard 28FD technologies and additional alignment structures are required in each die.

The first part of this task aims at specifying the last metal levels dimensions and structures required to speed up and improve the cryogenic characterization at wafer level. These specifications will apply to all wafers requesting cryogenic probing. Some wafers already available may need post processing (2 mask levels) to fit in the cryogenic probing specifications.

In the second and third part of this task, after the appropriate upgrades for RF measurement, RF probe cards will be evaluated to assess the RF characterization capability (frequency level) at wafer level at 4K. If some relevant conditions can be obtained, RF test protocols will be implemented.

In parallel those two phases, depending on tool workload, some DC and/or RF and/or Aging tests methodologies will be evaluated/optimized:

Example for DC: statistical measurement through addressable transistor arrays

Example for RF: impact mitigation of self-heating

#### Deliverables (due month/lead):

**ID7.2.1.1 Report on Cryo-prober industrialization for DC tests (M18)**

**ID7.2.1.2 Report on Cryo-prober evaluations for RF tests (M48)**

**ID7.2.1.3 Report on test protocols evaluations (M72)**

T7.2.2 RF cryogenic characterization process development.

**Start:M1**

**End:M72**

**Lead: CEA**

#### Contributors: CEA

#### Description:

To evaluate RF performances and acquire data for a future RF cryogenic compact model, specific RF structures that can be measured on manual cryogenic prober with 2 RF pads (GSG) are needed, with various dimensions (W, L, number of finger gates...) oxide thicknesses (GO1, GO2),... New RF design with access to the back gate is required to fully take advantage of FDSOI capability at low T.

RF test protocol down to 4K need to be optimized as well.

M1-M24 : specification and evaluation of FDSOI test structures required to perform RF measurements at cryogenic temperature.

M1-M72 : all along the project, improvement of the test protocol, including optimization of the calibration and de-embedding procedure. Development of new characterization methods if needed.

#### Deliverables (due month/lead):

**ID7.2.2.1 Report on RF measurements of dedicated FDSOI structures at cryogenic temperature (M24)**

**ID7.2.2.2 Report on RF measurement protocol at cryogenic temperature (M72)**

T7.2.3 Self-heating phenomena evaluation and impact simulation on cryogenic characterizations

**Start:M1**

**End:M36**

**Lead: CEA**

#### Contributors: CEA/UGA-IMEP

#### Description:

In FDSOI devices, the outflow of the heat generated at the drain side is impeded due to the low thermally conductive materials constituting the channel. Therefore, self-heating effects (SHEs) lead to a significant increase in the channel temperature when the device is tested. This temperature increase can severely affect the characterization results one intends to upload in the cryogenic models.

This task aims at evaluating the self-heating impact on characterization results compared to real operating conditions to adapt the characterization protocols if needed (to be done in task 7.2.1 and/or 7.2.2).

#### Deliverables (due month/lead):

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### ID7.2.3.1: Report on self-heating impact on characterization results (M36)

T7.3 Characterization PCB and systems design.

Start:M1

End:M72

Lead: CEA

Contributors: CEA, CNRS-Neel.

Description:

In relation to WP5-Cryo electronic tasks 5.4.1, 5.4.2, but also from WP3-Integrated Photonics, WP6-3D&Packaging and for program demonstrators, tests methodologies have to be developed to reduce test setup in cryostat environment, to implement appropriate automation and hardware equipment to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

First year will be devoted to a diagnostic on existing hardware and software equipment, and to the evaluation of the constraints of multi-site cryostats settlement. On this basis, a new test board architecture, as generic as possible to cover all WP needs will be proposed and designed.

Second year will be focused on fabrication, debug of the test bench (at room temperature and then cryogenic temperature), and application to the different WP samples.

The following years will be an iterative process to adapt test methodologies and design test boards and the task will be conclude by a proposal of system designs strategies for the scaling up.

Deliverables (due month/lead):

ID7.3.1 Report on new board and system test architecture proposal (M12)

ID7.3.2 Report on cryogenic test strategies for high speed and high scale integration (M72)

T7.4 Room temperature electronics for test and demonstration

Start:M1

End:M72

Lead: CEA

Contributors: CEA

Description:

Current Qubit control uses lab equipment leveraging FPGA for signal generation as it provides more flexibility for signal shaping feedback than traditional AWG. Industrial vendors such as Quantum Machines, Qblox or Zurich Instruments, market such devices, but they come with a consequent price and cannot be easily extended due to their closed source nature.

With the technologies envisioned for the scaling up of the control, such equipment's will face significant evolutions depending on the selected technology path. The use of optical channels, or the interactions with QEC decoders, may structurally modify their requirements.

Consequently, to provide the flexibility needed for the program tests and demonstrators, task 7.4 will initially seek to design signal generation solutions able to adapt to the project needs. Then, drastic evolutions may be required to cope with system design decisions for the demonstrator. This task would leverage existing competences both at CEA in target specific signal generation using commercial FPGA. Should these pieces of equipment be proven as a limit to the scaling, this task may also address their ASIC performance projection to provide necessary insight for system analysis.

Another development is envisioned on FPGAs: the high-speed link (whether copper or fiber) between cryo chips and room-temperature control electronics will require IPs for handling up and down-link communications. Presently a SerDes is developed as a primary brick in this scheme and the higher layers of protocol will have to follow.

Deliverables (due month/lead):

ID7.4.1 Report on flexible room temperature signal generation (M36)

ID7.4.2 report on room temperature equipment for final demonstrator (M72)

T7.5 Characterization coordination and scheduling

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<b>Start:M1</b>	<b>End:M72</b>	<b>Lead: CEA</b>
<b>Contributors: CEA, CNRS-Neel</b>		
<b>Description:</b> Most of the work packages will need cryogenic characterizations: each work package will be in charge of its measurements in the cryostats or on the Lakeshores. This task aims at organizing the tools accesses, at CEA- <b>IRIG</b> , CEA- <b>Leti</b> , UGA-IMEP-Lahc and CNRS- <b>Néel</b> facilities.		
<b>Deliverables (due month/lead):</b> <b>None.</b>		
<b>Work package deliverables</b> <ul style="list-style-type: none"> <li>D7.1 Report on needs evaluation and investment plan (M6)</li> <li>D7.2 Final report on tools upgrade and installations (M24)</li> <li>D7.3 Report on self-heating impact on characterization results (M36)</li> <li>D7.4 Final report on demonstrator characterizations (M72)</li> </ul>		