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X	Initial submission		Modification request
Short description of the project	<p>The LSQ project aims at building a portfolio of HW and SW technologies enabling the control at large scale of emerging solid state qubits technologies e.g. Superconducting cat qubits, silicon qubits (carbon nanotubes, spin qubits) and photonic qubits in development by emerging industrial actors. The project will cover a large span of technologies ranging from cryo-electronics to real time error correction under a system approach encompassing the development of models for control chains and the exploration of various architectures leading to demonstration of solutions representative of future scaling requirements. The project will involve actors along the value chain including the main French research institutes in the domain, a CAD tools vendor, a CMOS chips manufacturer, and will welcome the inclusion of national startups specialized in qubits technologies for quantum computing processors.</p>		
Key words	<p>Quantum computing, Qubit, cryo-electronics, cryoCMOS, Quantum error code correction, control chain, 3D stacking, silicon photonics, system architecture, modeling, CAD tools</p>		

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0. REVISION NOTES

Initial document submitted to IRT Nanoelec steering committee for validation on February 27th 2023.

0.4. Project evolution (major revisions)

0.5. Modifications (minor revisions)

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1. INTRODUCTION / CONTEXT

1.1. Key elements of the mission letter

The mission letter that was sent to the president of Nanoelec Steering committee requests a proposal from IRT Nanoelec, in the framework of the French National Strategy on Quantum Technologies, as part of the second Axis of the strategy that aims at developing a universal quantum computer through the use of error tolerant architectures. Two main objectives have been identified to enable such architectures: on one hand, maturing and industrializing solid state qubits technologies by supporting the roadmaps of the actors positioned in the field; on the other hand, preparing the technological environment to bring these technologies to scale as far as control electronics and error code correction are concerned. The focus of this proposal named Grand Défi LSQ – or Grand LSQ Challenge – deals with this latter point.

The mission letter defines a main objective: developing a framework that enables, at a ten year time horizon, the national ecosystem to develop one or several hardware architectures required to implement a quantum processor based on solid state technologies including the ones that are addressed in the first axis of the National Strategy (PEPR program). This ambition is three fold:

1. Developing and setting up tools and methodologies for a system approach covering all stages of qubits control chain from electronics to error code correction ;
2. Validate the approach through the technology demonstration of full control chain architectures that can scale up to the future requirements of quantum processors;
3. Build a solid IP portfolio that helps our French and European ecosystems compete with international ones.

This translates in expectations stated in the request to Nanoelec:

- Develop a tool to enable the exploration, the simulation and the design of hardware architectures to control solid state qubits including (i) a software environment taking into account the constraints brought by each part of the quantum computing architecture, (ii) the projection of performances of various envisioned technologies, (iii) one or several proofs-of-concept of fully functional architectures
- Implement and demonstrate one or several information processing and control system including (i) a proof of concept of a control chain at intermediary scale, (ii) an experimental validation of signal emission and reception for the control of qubits and (iii) a programming interface compatible with HPC environments
- Consolidate a portfolio of IP blocks through (i) the implementation of a scientific, technologic and economic watch and the exploration of resources and partnerships to enable access to a large (200) IP portfolio within and outside of the consortium.

Key requirements to carry out the program are to:

- Insure the interconnection with other projects of the National Strategy for quantum technologies,
- Take into account the mandatory cryogenic environments,
- Develop generic technology bricks,
- Build on existing solutions and know-how (including call for tenders) and build upon existing resources,
- Use the leverage effect of European projects,
- Favor the creation of national economic players,
- Provide solutions that minimize energy consumption and the project's environmental impact.

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The mission letter asks for a proposal that includes

- A framework proposal including a cartography of bricks, the organization of the program in projects/sub-projects, a state-of-the-art, the description of scientific and technology challenges as well as a technological roadmap together with a list of partners (including international ones),
- The description of the dissemination and exploitation strategy,
- The description of the proposed governance for the program,
- Letters of Intent for each of the partners with participation modalities,
- A risk analysis and action plan thereof,
- A financial appendix.

1.2. IRT Nanoelec overview and presentation

Nanoelec is one of the 16 institutes for technological research (IRT) and for energy transition (ITE) set up by the French government and financed by the PIA to bring together academic and industrial players on R&D and innovation projects for the competitiveness. IRTs are thematic and interdisciplinary technological research institutes set up by the French Government for industrial competitiveness. Their mission is to bring out innovations in future economic sectors through balanced public-private strategic partnerships. IRTs are by definition multi-partners: their members are public RTOs and research laboratories as well as private industries, manufacturers, SMEs and start-ups.

The Nanoelec technological research institute is a consortium of actors from the private and public sectors, supported by the CEA. Its mission is to help companies create value and differentiate their offer in the areas of digital transition. IRT Nanoelec runs multi-partner technology development and dissemination programs to make the electronics sector more competitive. It is based in Grenoble, a world-class hub for research, innovation and production in this field. Its R&D programs are built jointly by representatives from the academic and industrial worlds. They relate to the design and development of new processes, systems and components. Historically, Nanoelec conducted programs along three axis: (i) technologies along the “more-than-moore” roadmaps of the microelectronics industry (3D stacking, silicon photonics and more recently GaN/Si for energy conversion, nano-characterization), (ii) technology dissemination and user centric design, and (iii) human capital and training design. In 2020, Nanoelec technology roadmaps evolved to address more specific applications reflecting the priorities of its industrial partners:

- **Imaging** through a program call Smart Imager that aims at paving the way for three layer imagers
- **Displays** through a program called Displed that aims at preparing technologies for new micro-led displays based on the innovative concept of Smart pixel that benefit from 3D stacking techniques
- **Photonic Sensors** to take advantage of silicon photonics technologies for applications such as Lidar that require new functionalities such a high power lasers and OPAs
- **Digital trust** with the consolidation of a program on technologies for connected objects including the development of cybersecurity solutions for components and embedded systems,
- **Characterization** activities that are now encompassing a roadmap on radiation proof components and systems through the use of large instruments.

IRT Nanoelec also conducts a training design program in partnership with Grenoble INP and Grenoble Ecole de Management as well as a technology dissemination programs for SMEs. Supported by the AURA region, the latter implements open innovation methods as well as more conventional methods of technological development. Given the disseminating nature of digital technologies, Nanoelec is aimed at a large number of sectors of goods and services, from industry and infrastructure to consumer consumption, including those of transport, the environment and health.

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1.2.1. Governance of IRT Nanoelec

IRT Nanoelec is not a legal entity but consortium carried by CEA. CEA, as the holder of IRT Nanoelec, handles the administrative and financial management as well as the coordination of the IRT, in interaction with the French National Research Agency (ANR), on the one hand, and, on the other, with regards to the other Partners. With this same role, CEA signed with ANR the Bilateral Agreement for the execution of IRT Nanoelec Programs.

The *Consortium Agreement* defines the general procedures governing the relations between the Partners of the IRT, and in particular between CEA, as Holder of the IRT, and the other Partners, as well as the rights and obligations of the Partners on the basis of the commitments which CEA has made for the IRT, as Holder of the IRT, in the framework of the Financing Agreement. This agreement defined the functioning of the institute, the obligations of the partners, the rules of confidentiality, and those for the attribution of intellectual property rights and the exploitation of results. As such the present program will comply with the pre-existing rules it established.

This *Consortium Agreement* is supplemented by *Specific Agreements* between CEA as Holder of the IRT and the Partners to define the procedures specific to each of them and/or to each of the Programs to which they contribute. These *Specific Agreements* essentially specify the financial elements applicable to the partners: Cash and in-kind contributions from industrial partners and PIA funding amounts for academic partners. Industrial partners are not eligible to PIA funding.

Figure 1 summarizes the hierarchy of agreements that structure IRT Nanoelec's organization.

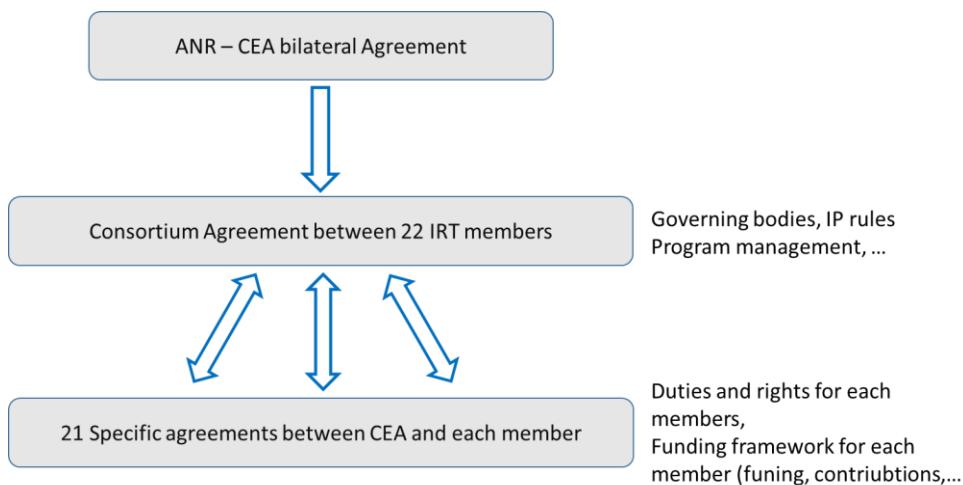


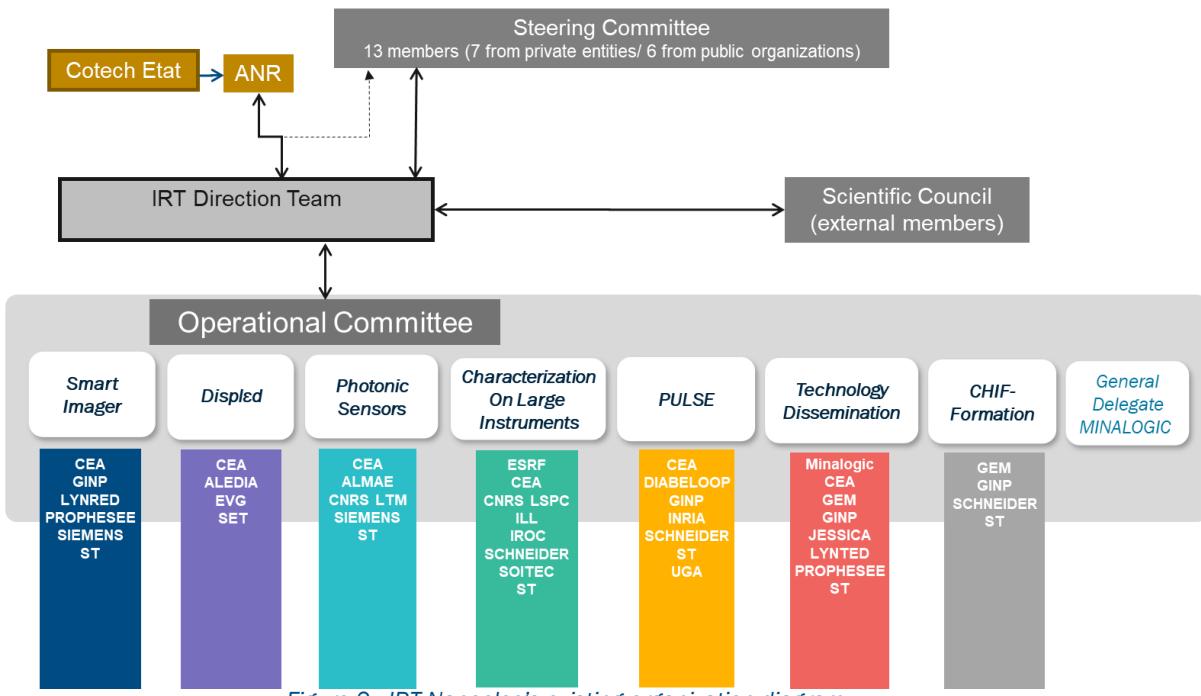
Figure 1 - IRT Nanoelec agreements structure and main roles

As presented in the diagram Figure 2, the governing structure of Nanoelec is based on 4 bodies. The Main one is the *Steering Committee*. It has 13 members with voting rights, as requested by the public authorities. 7 from private entities, and 6 from public organizations. Among the partners identified as future participants to the LSQ program: CEA, CNRS, INRIA, UGA, Minalogic, STMicroelectronics, and Siemens EDA are members of the *Steering Committee*. The missions of the *Steering Committee*, conducted in compliance with the commitments between CEA, as IRT Holder, and the National Research Agency, are listed below:

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- Build and consolidate the IRT's general pluriennial orientations and the IRT's annual program of action in accordance of the commitments signed with ANR;
- Examine and approve the IRT's development strategy and see to its execution thereof;
- Monitor the execution of the Consortium Agreement and the Particular Agreements;
- Monitor the progress of the IRT's various programs;
- Examine and validate budgets, staff forecasts, the means allocated to the various Programs and monitor the commitment of partners;
- Propose or examine solutions for solving, when necessary, the problems encountered in executing the IRT's Programs;
- Decide on the admission of new Partner(s) in the IRT and approve the conditions to their admission.

The *Steering Committee* also constitutes a privileged communication body between the Partners, and it is attentive to all the parties involved so as to take account of the community's needs and to constitute a proposing force for preparing the future. The Steering Committee is also the forum for consultation among the Partners in the case of difficulties. The management of IRT Nanoelec consists of the director and his team. The IRT Programs are conducted by Directors appointed by the Steering Committee (hereinafter the "Program Directors"). An *Operational Committee* gathers the Program Directors and the general representative of MINALOGIC, under the direction of the *IRT Director*. This *Operational Committee* implements the strategy and Programs approved by the Steering Committee. It is responsible for collecting data and monitoring all IRT indicators.



Concerning the choice for the organization of IRT Nanoelec management team, it was initially decided to rely as much as possible on the existing CEA functions (legal teams, finance and accounting) rather than duplicate and create from scratch entities within the IRT. Nanoelec direction is therefore small in size (about 5 persons full time equivalent). This approach is very pragmatic and one could describe as lean and has been used successfully until now.

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A *Program Committee* has been set up for each IRT Program, the composition of which reflects the various players involved in said Program. This committee is placed under the direction of the corresponding *Program Director(s)* and is responsible for defining the Work Program precisely, and for monitoring its execution and development, including the examination of the admission into the Program of Partners not initially members of the said Program and/or of new Partners of the consortium. It also decides on the relevance of launching in the program associated partnerships by verifying the consistency of these actions and the Program (providing skills not available, results dissemination ...).

The governance also includes a *Scientific Council* composed of French and/or foreign experts representative of the domain, outside of the Partners of the IRT. This Scientific Committee meets once per year. It is consulted regarding:

- Strategic orientations in the domain of nano electronics and related fields defined by the IRT's Steering Committee; The results of the research obtained by the Programs, taking account of the strategic orientations established by the Steering Committee and the means attributed for each Program.

1.2.2. Main IP rules

IRT Nanoelec is a consortium of 22 partners gathering non industry organizations partly funded through PIA subsidies as well as industrial actors, most of them part of a local pre-existing network.

CEA as holder of Nanoelec as a specific responsibility in managing and handling IP resulting from IRT's various programs. A common practice of the ecosystem is to follow a fundamental principle to govern the ownership of IP rights (especially patents and software files linked to collaborative projects) which translates in the devolution of property to the employer of the inventors and the co-ownership in proportion with the intellectual contributions of the inventors when results have been generated by employees from several entities. The owner or the co-owners share the cost induced by IP rights protection. IRT Nanoelec has adopted an IP policy consistent with this principle and adapted to comply with the framework established for all IRTs in the context of the Nanoelec consortium structure. The resulting policy is detailed as an appendix to the convention between ANR and CEA and in the consortium agreement signed by all partners of Nanoelec. As Holder of the IRT, CEA shall, as a rule, be appointed as sole agent for the commercialization of Foreground IP generated solely by non-industrial Partners in the framework of IRT Programs, owned or co-owned by CEA as Holder of the IRT, both vis-à-vis the IRT Partners and vis-à-vis third parties.

In ten years of activities the framework has enabled the transfer of technologies to large actors as well as SMEs and startups companies that are industrializing and commercializing products and services. These technology transfer have been negotiated through licensing agreements compliant with the European legal framework on state aids.

IRT Nanoelec brings to the LSQ program a strong background in the field of 3D stacking & packaging technologies as well as in the field of silicon photonics. This adds up to 60-or-so patent families that are part of Nanoelec IP portfolio as of December 2022.

In addition, CEA, CNRS, UGA and INRIA are bringing into the program a large background in the field of quantum technologies (control electronics, cryo electronics, error correction codes and algorithms, quantum physics ...) that will be used as a knowledge basis for the LSQ program. This knowledge will be accessible for R&D programs and accessible through license agreements to industrial partners if required for exploitation of results.

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1.2.3. Financial framework

The adaptation to the financial standard rules applicable to the IRT funding scheme has been included in the convention between the ANR and the CEA, holder of the IRT Nanoelec. PIA funding (subsidies granted to Nanoelec) received for the programs are only dedicated to academic organizations (CEA, CNRS, INRIA, UGA). The academic organizations are funded through PIA subsidies but also industrial cash contributions and European funds and/or funding from local authorities. The industrial cash contributions come from consortium industrial partners and also from R&D specific contracts.

Indeed, beyond its members, Nanoelec collaborates with other companies and private or public organizations in the framework of associated contracts. These actions are managed under specific contracts which involve the third party and the consortium partner(s) with a technical implication in the project. These actions are fully funded by the associated partner (no PIA subsidies), and allow either to make use of tangible and intangible assets (R&D services) or to bring very specific competencies that are not available in the consortium, for example with material suppliers or process equipment manufacturers. These actions are launched upon the validation by the program committee and the steering committee.

CEA is the holder of Nanoelec and acts in the name of the consortium as far as relations with the French public authorities are concerned (SGPI, ANR). Each partner of the consortium remains the employer of its staff involved in the IRT Nanoelec projects. As a result, the staff involved in the LSQ program will not be employees of Nanoelec. Each partner also remains responsible for the management of its own infrastructure and the financial consolidation of its contributions through its own specialized teams.

As a result, the budget of each Nanoelec program is established as an addition of all expenses incurred by each partner with a separation of OPEX and CAPEX. As far as research partners from Nanoelec are concerned, the activities are funded with resources of various origins: the PIA national scheme, state funding for the permanent staff of academic labs, cash contributions from industrial partners. Industrial partners, on the other hand fund their own resources in the project.

The overall financial control is managed by the Nanoelec management team and is ensured by an Auditor scrutinizing annually the expenses and revenues of the institute, which are the consolidations of the expenses and revenues of each partner-each certified by an independent auditor according to a common specification. For most partners of the consortium, the activity of the workers involved is traced in their analytical accounting files. It gives an accurate and reliable evaluation of the activity of each partner. Auditors – usually from one of the main actors in the field (KPMG, E&Y, PWC, Deloitte...) – are independent and certify the consistency between the declared resources and the analytical real data, following specifications that have been established by the auditors of Nanoelec. Consortium industrial in-kind contributions (silicon lots, human resources, HW/ equipment or SW platform ...) are a good indicator of their program effort and of the real multi-public/private partnership including cooperation through human capital.

Having introduced the existing governing rules and bodies that structure the framework of execution of the LSQ Challenge we will now focus on presenting the quantum computing context that calls for it.

1.3. Quantum computing context

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1.3.1. Disruptive technology: toward quantum computer

Thanks to ever-increasing computing power and cost reductions offered by Moore's law, electronic systems are now so pervasive that novel applications account for the biggest part of the value share of information technologies. Yet, an important range of applications remain unfeasible on modern classical computing due to their algorithmic complexity with respect to problem size. This is the case for a large category of optimization algorithms who fall in the NP-complexity¹ category for which there is no known polynomial time solution. Hence the practical execution of such algorithms on large inputs is intractable on existing high-performance computer, and will remain so no matter if Moore's law is able to keep its 20th century pace.

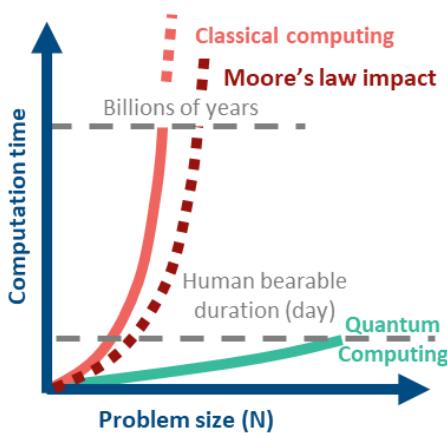


Figure 3 - Illustration of potential impact of quantum computing for complex problems

By carrying out operations on qubits with 2 superposed quantum states, quantum computers would be able to represent a large number of possible states on a limited number of qubits. It would thus be possible to simultaneously process several possible values and therefore significantly speed up certain processing operations as compared with a "classical" computer as depicted Figure 3. This is the property used by Shor's algorithm for polynomial time processing of numbers factorization whereas its complexity (sub-exponential) on a classical computer is one of the pillars of RSA type asymmetrical encryption approaches. Therefore, the ability of quantum computers to decrypt the ciphered data at the heart of modern information systems makes this a real challenge for State sovereignty, both technological and strategic. Over and above security issues, quantum acceleration could be of benefit for numerous areas of application, notably resolving widespread combinatorial optimization problems.

To achieve such a paradigm shift in computing, one would need quantum computers with a large number of entangled qubits and in which the computing error for each basic operation is low. The accumulation of errors during execution of an algorithm can bury the measured result in noise. For an error rate of about 10^{-3} , Quantum Error Correction (QEC) solutions exist, but imply a significant increase in the number of noisy gates used per ideal logic gate. For example, for this same error rate, Shor's algorithm applied to factorization of numbers of 2048 bits requires 4098 qubits for quasi-ideal gates, but requires 20 million once the error has been corrected².

¹ NP is the set of decision problems for which the problem instances are verifiable in polynomial time by a deterministic Turing machine

² <https://arxiv.org/abs/1905.09749v3>

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As such, only Noisy Intermediate Scale Quantum (NISQ) computing solutions exist to this date. These approaches exhibit fewer qubits and cope with their inherent errors by identifying quantum algorithm more robust to noise. Making the shift from NISQ to Large Scale Quantum Computing (LSQ) requires to address several challenges that the program supervised by IRT Nanoelec aims to tackle in close articulation to the research work conducted in other pillars of the French national strategy for quantum computing. In particular the proposed project will focus on the scalability of the solid-state qubit control chain and will rely on work conducted in the High-Priority research facility program (Programme d'Équipement Prioritaire de Recherche, PEPR) for the definition of high quality and reproducible qubits solutions.

Challenges for Large-Scale Quantum Computing

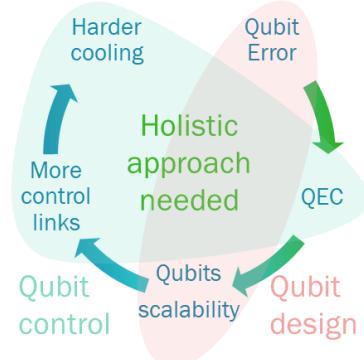


Figure 4 - Challenges for Large-Scale Quantum Computing

1.3.2. International overview

Due to its expected ability to render some complex computing problem feasible, the advent of Quantum Computing could disrupt the existing technological leaderships. This could grant a competitive edge to company embracing the technology ahead of their counterparts in several applications domains from biology and chemistry to transport, energy and finance. This is also an opportunity to reduce the dominion of the Silicon Valley on IT technologies in the future through the advent of novel players of the quantum computing domain, which nations aim to attract. One stronger area of Interest is the defense sector, as the processing power gain could significantly imbalance the technological advantages of some nations, especially in the cyphering domain.

As a direct consequence, nations that aim to play a first-rank role in the definition of tomorrow's world from its defense and economic standpoint, are all investing significant amount of funding to spur the emergence of universal quantum computers on their soil. As of 2022, international government investments in quantum computing research totaled to 30 Billion USD. The European countries are playing a significant part of this effort with 9 Billion USD, significantly ahead of USA 1.2 Billion USD National Quantum Initiative. France on its own is investing 2.2 Billion USD in its National Strategy for Quantum Computing. One must also notice the tremendous investments announced by The Popular Republic of China whose 15 Billion USD investments linked with the creation of Hefei's *National laboratory for quantum information sciences* account for 40% of worldwide investments³. Figure 5 summarizes global public investments in quantum research.

³ <https://english.ckgsb.edu.cn/knowledges/quantum-wars/>

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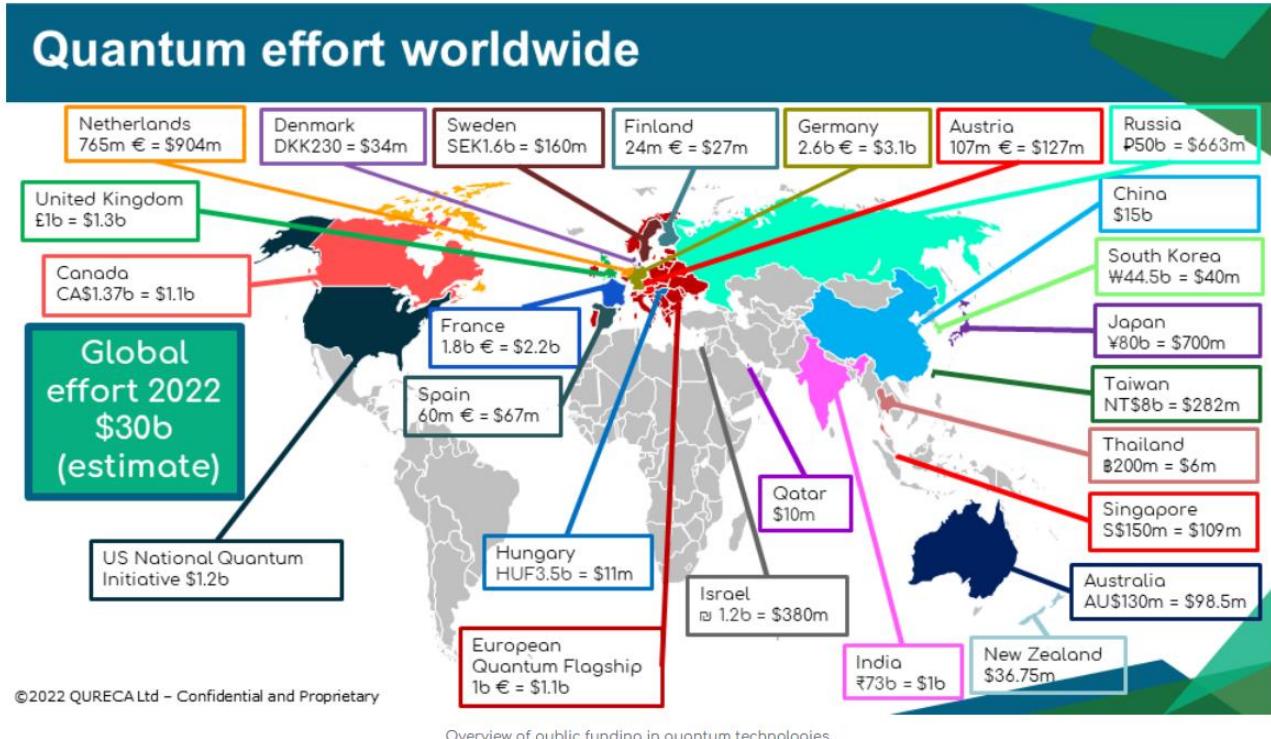


Figure 5- worldwide quantum research public funding
(source <https://quareca.com/overview-on-quantum-initiatives-worldwide-update-2022/>)

1.3.3. Promising qubit technologies (Tanguy et Corinne for review)

At the forefront of quantum computing technologies, lies qubits. Several technologies have emerged to implement superposed and entangled states on different elementary elements whether they are atoms, ions, photons or electrons as summarized in Figure 6. Photons technologies have shown a high potential as they can theoretically work at higher temperatures, however unique photon detectors usually require ~10K to perform correctly. Trapped Ions and cold atoms can also work at higher temperature, as local cooling is achieved by means of Doppler techniques. However the mass production of such particles is hard to achieve and often exhibit topological constraints limiting qubit interactions.

Both Photon qubits and Solid-state qubits, namely superconducting qubits and semiconducting spin qubits, differ from the previous solutions in that they use more classical microelectronic design processes. The potential use of 2D or even 3D meshes makes them good candidates for scaling up the number of qubits.

Historically, superconducting qubits have been the focus of fundamental research in physics. This lead to the emergence of first quantum computers based mainly on the usage of Josephson functions. Initial encouraging results triggered the emergence of more industrial roadmaps lead by big player in the computing ecosystem such as IBM and Google whose current quantum computers achieve respectively 433 and 72 qubits with plans to push forward their scaling. However quantity is not quality, and emerging startups also focus on improving the qubits quality to ease their usefulness at scale. Among French players, *Alice and Bob* targets significant error reduction thanks to the definition of *cat qubits* that can exhibit exponential reduction of bit flip errors.

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PHYSICAL QUBIT ROADMAP FOR QUANTUM COMPUTER – HISTORY AND FUTURE

Source: Quantum Technologies report, Yole Développement, 2021

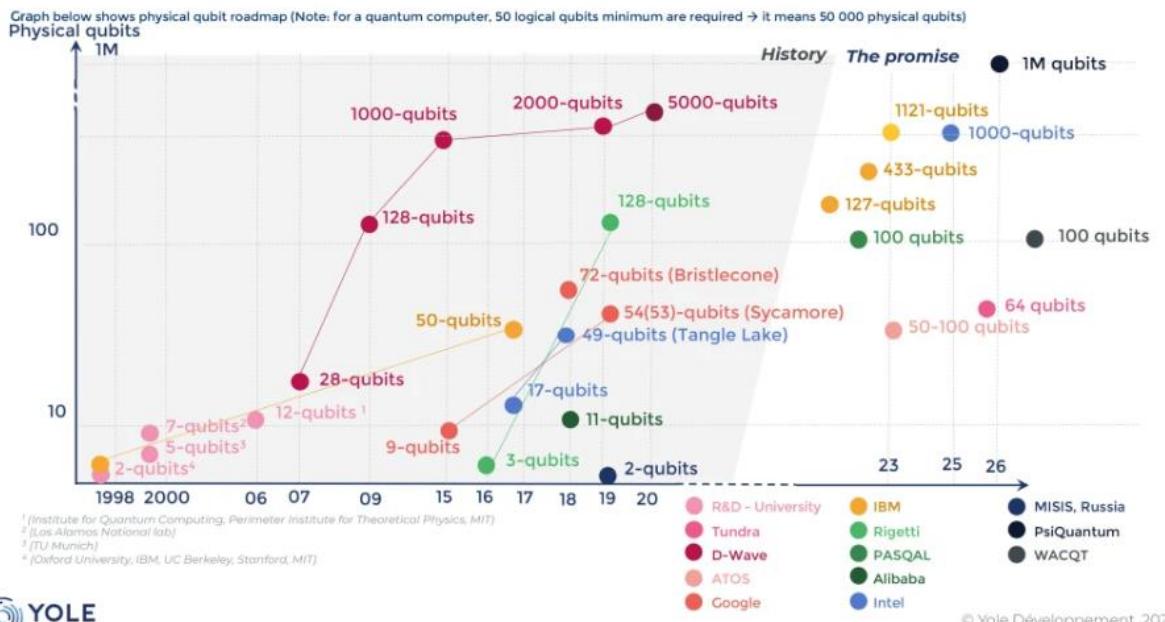


Figure 6 - qubit technologies, demonstrated scaling and roadmaps

Silicon spin qubits have a more recent track record and have therefore been demonstrated at a limited scale. However by relying on mature robust and scalable technology process that demonstrated its capacity to produce billions of high quality transistors, they have high qubit scalability perspectives. The quality of the process can also ease the control of so many qubits by enabling the sharing of the same exciting frequency among them. These qubits have been demonstrated on systems of a few qubits by various international research teams: 2 qubits by the University of New South Wales (UNSW)⁴ using silicon technologies, 3 qubits for SiGe technologies by the RIKEN⁵ (Princeton, QuTech) and QuTech recently demonstrated 4 qubits with a Ge channel⁶, and even more recently the control of a six-qubits quantum processor in silicon (SiGe/Si/SiGe)⁷. The QLSI European Quantum Flagship project is aiming for 16 qubits by 2025. Aiming for high-quality spin qubits, the French start-up C12 Quantum Electronics, proposes to exploit electron spin maintained in carbon nanotubes suspended over a wafer incorporating the qubit coupling control and read-out functions.

Both superconducting and spin qubit technologies face similar challenges to their scalability: multiplexing several qubit control signals into limited communication channels (to reduce coldsink) and ensuring real-time error correction. No matter the solid-state technology that emerges, the definition of generic control chain technologies that scale beyond

⁴ <https://www.nature.com/articles/nature15263>

⁵ <https://www.nature.com/articles/s41565-021-00925-0>

⁶ <https://www.nature.com/articles/s41586-021-03332-6>

⁷ <https://www.nature.com/articles/s41586-022-05117-x>

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today's NISQ solutions is doomed to become an essential part of tomorrow's universal quantum computing. Based on qubit maturity roadmaps, now is the time to create these enabling technologies to support the future quantum computing champions.

Closer to the qubit, specific control is needed in-line with the underlying physics, these specificities need to be taken into account as soon as information is available in the system analysis, and shall be specifically addressed in the maturation technology plan when qubit technologies mature.

1.3.4. Quantum national strategy

In order to support the excellence of French research towards the emergence of industrial champions, key to Europe's economic and strategic independence, France has adopted an ambitious 2-Billion-dollars *National Strategy for Quantum Technologies*⁷, coordinated with complementary European initiatives. This strategy is structured in several layers⁸ to best accompany the technologies at their various level of readiness.

The Priority Research Equipment Program (PEPR, Programme d'équipement prioritaire de recherche), started on January 1st 2022, targets the funding of academic research on all aspects of the quantum technologies. To give better traction to promising lines of research, targeted projects were defined, complemented by open calls to allow for the growth of less identified technologies. Covered subjects range from the different strategies for quantum error code correction (NISQ2LSQ) to quantum algorithm in the fields of optimization, machine learning, simulation of physical systems (EPIQ) and qubits technologies (e.g. RobustSuperQ and Presquile). Both superconducting and silicon spin qubits benefit from targeted projects, as well as research on QEC algorithms. Work conducted within the program supported by Nanoelec shall be conducted in close relationship with advances in these fields.

The NISQ Grand Challenge is a second layer of the strategy that covers the definition of Noisy Intermediate Scale Quantum Computing (NISQ) solutions. It targets more mature technologies able to be demonstrated in advanced research computing facilities. The challenge encompasses both NISQ machine investments and research program to define adapted algorithms and software stacks to better exploit them. GENCI (*Grand Équipement National De Calcul Intensif*) was appointed to integrate such NISQ solutions in its infrastructure. The resulting infrastructure, coined *HPC Quantum Initiative* (HQI) platform (formerly Plateforme Nationale de Calcul Quantique Hybride⁹ or PNCQH), will benefit to all academic and RTO actors. The funding schemes target successive investment plan to account for the maturation of promising qubit technologies and the expected emergence of industrial players. The project officially started retroactively in April 2022 but the official kick-off occurred in February 2023. First acquisitions of QPUs were conducted with the support of HPCQS European program that conducted European public tenders leading to the installation of Pasqal 100 qubit QPU by the end of 2023 at CEA's TGCC (Très Grand Centre de Calcul, Very Large Computing Centre).

⁷ Stratégie nationale pour les technologies quantiques, as part of several Stratégies nationales d'accélération or SNA- we will refer to this strategy as SNAQ in the remainder of this document

⁸ <https://www.enseignementsup-recherche.gouv.fr/fr/strategie-nationale-sur-les-technologies-quantiques-faire-de-la-france-un-acteur-majeur-de-ces-49233>

⁹ <https://www.gouvernement.fr/france-2030-strategie-quantique-lancement-d'une-plateforme-nationale-de-calcul-quantique>

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The [LSQ Grand Challenge](#), targets the innovations to be conducted to enable the advent of Large Scale universal Quantum computing (LSQ). The program addresses the challenge brought by the implementation, at scale, of the control chain and error correction of solid-state qubits. It will leverage work conducted on qubits and QEC within the PEPR, and will aim to provide a generic interface for LSQ control to ease the industrialization of emerging qubit solutions and their potential inclusion in HPC centers akin to the HQI infrastructure. This is the part of the National Quantic Strategy (SNAQ) that the letter of mission entrusts IRT Nanoelec to carry out.

The [Technology Maturation Plan](#) (PMT – Plan de Maturation Technologique), addresses the funding of emerging industrial actors in their first phase of developments. It targets direct participation in key companies by the means of public equity, as well as innovation partnership public tenders to sustain the emerging QPU market. This aspect of the strategy will ensure that competition is fierce between QPU vendors, while securing their cash flow and capacity to develop necessary technologies. The PMT and LSQ program are intended to work in a complementary fashion so as to separate common technologies, to be developed by the LSQ program so as to avoid double funding, and the vendor specific ones, that shall be supported by the PMT terms. In order to reach this goal, regular updates on LSQ progress shall be shared with the entity in charge of the PMT. In addition, it is expected that industrial QPU vendors, will seek to adapt the common technologies developed by the LSQ program to their specific needs in their strategies to meet the PMT tenders performance milestones. This will ensure the valorization of the technologies developed within the LSQ project, and increase global IRT industrial funding.

Due to their above-mentioned complementary nature, the LSQ and PMT projects are part of a broader vision to reach large-scale quantum computing named Proqsima.

The [Industrial development of enabling technology program](#) (Programme de développement Industriel relatif aux technologies capacitantes) targets the funding of technologies mature enough to hit market but with too high technology risk to be industrialized without accompanying public funding. Such technologies are analyzed with respect to strategic assets for the European independence in the quantum domain. One of such project of interest deals with the development of future cryogenic solutions, as its outcome can impact power consumption budget in next generation cryostat. Reversely, the LSQ program could help size requirements for future cryogenic system based on control electronics power dissipation needs. Several meetings with coordinators of this project took place in building this proposal, and it is intended to reinforce exchanges as the projects advance.

1.3.5. European strategy

The consortium will also build on the pre-existing works conducted in the framework of European projects.

CEA & CNRS are involved in the Coordination and Support Action (CSA) European project QUCATS started in 2022 to coordinate quantum initiatives in Europe with the European Quantum Flagchip. This will be useful to identify opportunities to leverage European Funding for some of the LSQ program tasks. CEA is also involved in the CSA InCoqFlag which aims at providing a roadmap toward international partnerships that are beneficial to the European ecosystem. For the LSQ program, this will serve as an input data for the launch of international cooperation initiatives as part of the third axis of the program.

CEA is also a key contributor to European projects addressing technology roadmaps: the projects QLSI, launched in 2020 and QuCube, initiated in 2019 are addressing the development of silicon spin qubits technologies that are

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integrating work on cryo-electronics and 3D assembly techniques. In this latter field, the project SEQUENCE, focusing cryogenic electronics, ended recently.

INRIA is involved in several projects as well. Q-FEEDBACK and DANCINGFOOL are addressing the control techniques for Superconducting Qubits. EQUALITY is a project launched in November 2022 that aims at developing cutting-edge quantum algorithmic primitives relevant for various industry-specific workflows.

Coordinating and participating to European projects is part of Nanoelec dissemination and program management strategy. Since 2012, Nanoelec has been involved in more than 30 European projects. In the case of the LSQ program, the partners will build proposals to leverage European funding on technology intensive hardware roadmaps such as cryo-electronics, silicon photonics, 3D packaging at cryogenic temperatures or other fabrication techniques. Other programs will target cooperation in the field of software and IP design and implementation.

The European framework will serve as a platform to build partnerships with key players outside France including the Netherlands and Germany to position the LSQ program as a key element of the QT Flagship.

1.4. Project positioning within Nanoelec IRT and its ecosystem

As a consortium dedicated to the microelectronic sector with a specific expertise in the field of heterogeneous integration technologies IRT Nanoelec brings a background essential to tackle efficiently the requirements of scaling quantum technologies both in terms of ecosystem and technologies. Seven of the current partners of Nanoelec have confirmed they will contribute to this new program bringing critical resources and expertise on collective manufacturing technologies, enabling tools, quantum expertise and software engineering. Two key elements will be (i) CAD tools necessary for modelling, simulating and designing circuits and architectures and (ii) the CMOS electronic technologies interfacing to qubits components. The developments performed since 2012 in the two main technology programs of Nanoelec (3D stacking, Silicon photonics) will accelerate the design and implementation of the control chain proofs of concept and demonstrations. In coordination with the national initiative on quantum technology training QuanTEdu led by UGA, a member of the consortium, a link will be established with Nanoelec's Training Design Program to build new training capsules, modules and programs when required. Finally, the potential involvement of Minalogic will help disseminate and build momentum in the regional and national ecosystem. Minalogic has already initiated the organization of workshops and seminars in the quantum computing field helping build a community of scientists, business professionals coming from laboratories, large companies as well as SMEs.

1.4.1. Proposed governance structure

IRT Nanoelec intends to address all three actions (system model and exploration, demonstration, IP strategy) entrusted by the SGPI into a single IRT-Nanoelec program. The objective of this approach is to keep an efficient interoperability of the actions and a single reporting view encompassing all aspects.

This structuring by program thus appeared more appropriate than a segmentation by projects which could have led to a dispersion of activity and a lesser synergy between actions carried out on a theme. This structure allows strong interactions between the three different actions, and a very versatile and efficient operation that allows to adapt to the inherent changes in a program with a disruptive technology. This structure has been proven to be effective and

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successful in previous programs conducted within Nanoelec. The evaluation conducted by the funding agency (ANR) highlighted the high level of impact of the Nanoelec programs.

This single program structure will also help keep the visibility of other key Nanoelec research programs. The proposed governing scheme, seamlessly integrated in Nanoelec's current governing structure (see Figure 2) is depicted in Figure 7. The scheme is built on three main bodies:

- A Deputy Director dedicated to the program and integrated in the IRT Direction team, bringing a broader vision with an internationally recognized background in processor architecture and HPC.
- A Program direction team with two co-directors bringing different backgrounds in technologies, system architecture and design,
- An advisory board specific to the LSQ program that will support the governing structure on scientific and strategic issues.

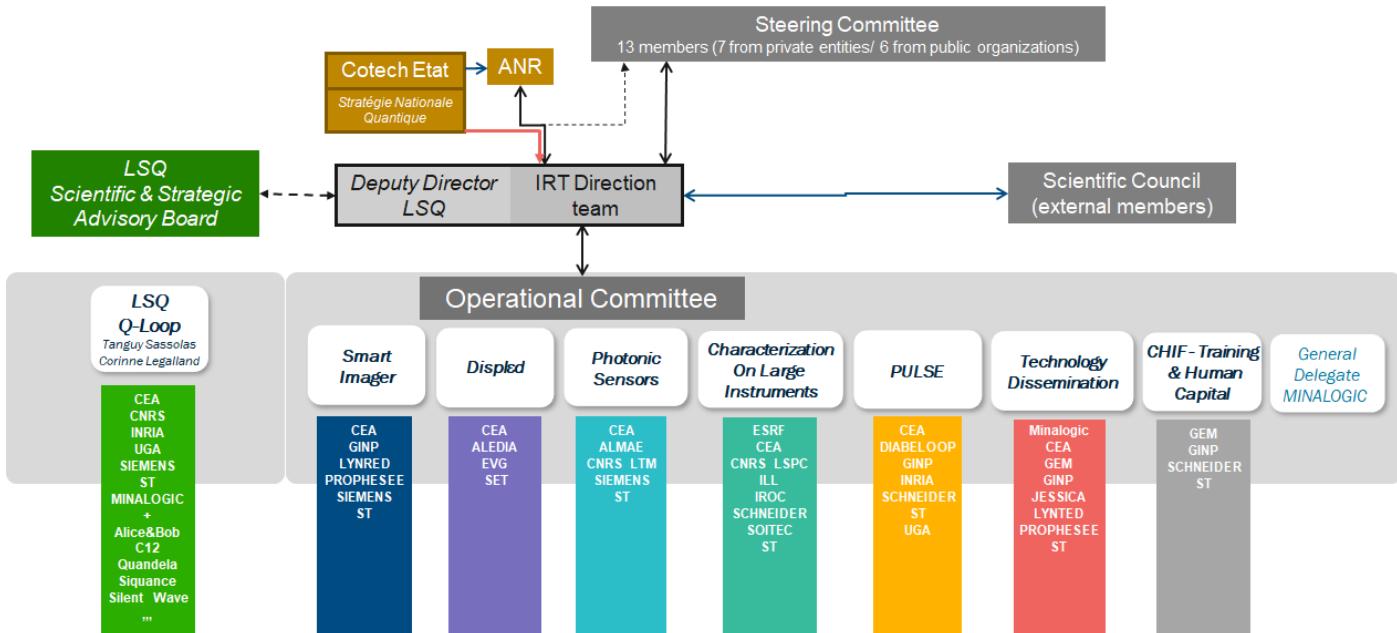


Figure 7 - Proposal of Quantum Computing Program's governing structure within Nanoelec

First of all, to better address this strategic challenge, and the significant increase of activities it represents for Nanoelec, we propose to strengthen the IRT direction team with a deputy director in charge of the quantum computing program, named *QC Deputy Director*.

The main objective of this QC deputy director is to keep a strategic view on the program in close interaction with the dedicated Program management structure that will be more dedicated to program execution. The QC deputy director thanks to its visibility would also seek international collaborations for the project and would suggest evolutions of the program to better align with a moving ecosystem. Specific survey of interactions with advances in HPC and Quantum communications will also be sought to integrate the work in a more global ecosystem.

The QC deputy director will also be in charge of animating and managing the *Scientific and Strategic Advisory Board* that will be set up during the first year of the program. This board will be led by a director chosen in the scientific quantum computing community and will have a twofold mission:

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- Advising Nanoelec program managers and IRT direction team on the key orientations of the project in terms of scientific and technological choices and helping analyze threats and opportunities arising from advances and innovation in the field. This mission will be filled in by building a team of 4 to 8 scientists whose expertise encompass the technical activities of the program
- Contributing to the interactions with the various initiatives of the National Strategy for Quantum Technologies, to position the LSQ program with regards to national and international HPC programs and ecosystems.

Finally, due to the diversity of the challenges on the road to reaching LSQ control, Nanoelec intends, in compliance with the program governing framework, to build a team based on two project leaders with complementary backgrounds to lead the project and conduct operating management : Corinne Legalland, stemming from CEA LETI¹⁰, experienced in CMOS and semiconductor technology, and Tanguy Sassolas, coming from CEA LIST¹¹, experienced in system architecture ; this will ensure correct execution of the program on a daily basis. The Nanoelec Quantum Computing Program itself will be structured in eight work packages to address the 3 ambitions stated in the mission letter. Each work package will be led by one or two leaders coming from the different partners of the program.

1.4.2. Proposed project structure

The work program structure which will be detailed later in the proposal is presented in Figure 8 and has been established in order to implement:

- A system approach with the development of a model of the full control chain in WP1 and the definition of control chain architecture specifications and their related demonstrations in WP2.
- The development and the demonstration of key technology blocks on each of the main challenges of the control chain: cryo-CMOS and cryo-electronics solutions (WP5), 3D integration and packaging techniques for the co-integration, with efficient thermal management, of the control layers with the qubits technologies implemented at large scale (WP6), Integrated photonics (WP3) to transfer data at high data rates and low latency to digital architectures that will implement the error codes developed (WP4).
- Specific setups and platforms to test components, subsystems and demonstrator in cryogenic conditions (WP7).
- Coordination and Management activities will be implemented in a specific work package, WP0, which will also host IP management issues and strategies as well as dissemination activities.

¹⁰ CEA-Leti, a technology research institute at CEA Tech, in micro and nanotechnologies

¹¹ CEA_LIST, a technology research institute at CEA Tech, and specializes on digital systems.

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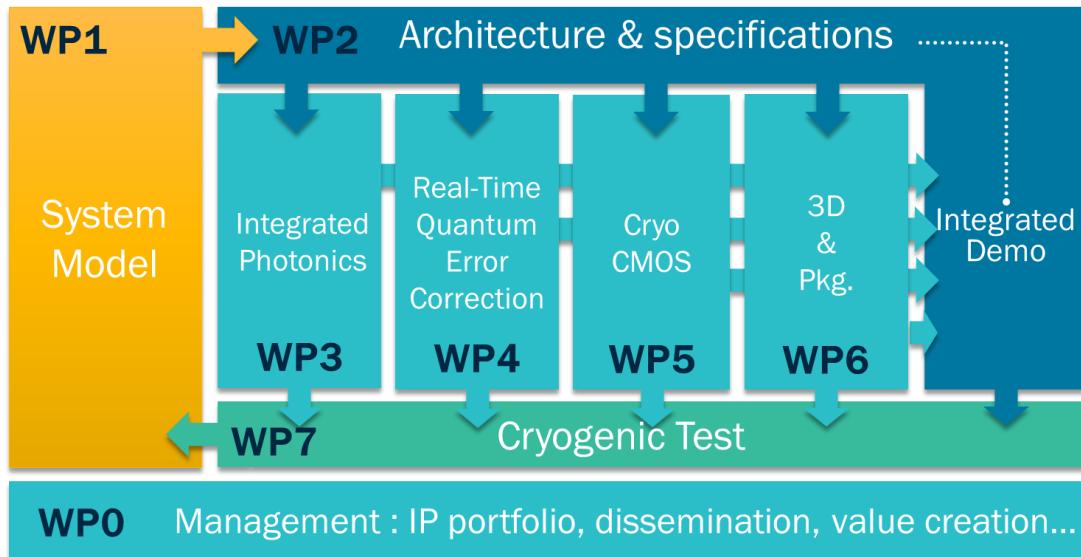


Figure 8 - LSQ Program WBS Structure

Second, using IRT Nanoelec's *associated projects* mechanism, the work conducted in the program in association with the emerging players that mature their qubits platforms will be further extended. Connecting the generic part of the control chain with their specific qubits, will necessitate definition of dedicated cryogenic control hardware closest to the qubits. Industrial actors will likely seek to leverage the IP developed by the Grand LSQ Challenge (cryo-electronic, 3D integration and packaging as well as system analysis) to accelerate their design. Consequently the emerging players are expected to fully fund IRT Nanoelec partners to perform these specific design actions. Such work, directly in line with the IRT program can be *de facto* considered as associated projects (cf. § 1.2.3) which will help balance the program industrial/institutional funding and grant access to the accumulated IPs to a greater community of national industrial players. This virtuous mechanism will ensure efficient valorization of the program spreads widely and accelerate the definition of sovereign universal quantum computers.

1.4.3. Considered partnership

The project will bring together current partners from Nanoelec together with new actors that are specialized in the field of quantum technologies. At the time of the proposal submission the program is expected to gather contribution from 12 members as described in the figure below.

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Current Members of Nanoelec involved in the program buildup:

STMicroelectronics will contribute to the development, characterization and industrialization of cryo electronics and cryoCMOS technologies. The objective is to establish a process flow and its related PDK (Design Kit) to build the control layers of the physical qubits in a range of temperatures that has not been explored today by such technologies essential to scaling. In addition, STMicroelectronics will bring a potential path towards industrialization for 3D integration and packaging solutions as well as silicon photonics devices.

Siemens EDA and Siemens ISS will provide CAD tools and software suites required for the design of key elements of the control chain with exploratory work to be performed on specific models and data collection with a particular focus on materials and devices behavior at Ultra Low Temperatures.

CNRS will contribute in several fields : Instrumentation and Tests at Cryogenic temperatures for both Silicon and Superconducting device (Neel Institute), tools and framework for system models (Neel Institute in partnership with Majulab), innovative photonic devices at low temperatures (C2N, IMP-LAHC), Cryoelectronics (UGA-IMEP-LAHC, and UGA-TIMA).

In addition to its contribution through UGA-IMEP-LAHC will contribute, together with INRIA on quantum error code correction. One ambition of the program is to establish a common team specialized on real time quantum error code algorithms and their implementation on digital or mix signal architectures.

CEA will be involved in system level and IC design as well as all technology developments (CryoCMOS design, Superconducting technologies for TWPs, photonic links, 3D stacking and packaging technologies) and will therefore be coordinating the final demonstration.

Minalogic¹² will help disseminate and build momentum in the regional and national ecosystem. Minalogic has already initiated the organization of workshops and seminars in the quantum computing field helping build a community of scientists, business professionals coming from laboratories, large companies as well as SMEs.

¹² Minalogic is the digital technology cluster for France's Auvergne-Rhône-Alpes region.

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Potential New members of the consortium:

The 4 startups, Alice & Bob, C12, Siquance and Quandela will bring some resources to support the development of generic elements of common interest. They have planned to dedicate resources for the design and tests of the functions of interest to them e.g. cryo-electronic building blocks, 3D assemblies, low temperature models, error code which can differ from one another depending on their roadmaps.

In coordination with their developments of prototypes in the framework of the Technology Maturation Plan, they will express to Nanoelec, the requirements for specific developments, designs and demonstrations that will be carried out as associated projects by Nanoelec teams when relevant. These projects will be fully funded by cash coming from the industrial partners.

Finally, another emerging player has expressed a strong interest in the program. Silent Waves develops and commercializes a TWPA technology which is a key component of the control chains of potential interest for many qubits platforms. Future generations of TWPs will require collective manufacturing technologies.

1.4.4. National and international ecosystem collaborations

Although Nanoelec is strongly embedded in its local ecosystem, the proposal has been built in coordination with some of the national key players and academic teams. Through the large organizations (CNRS / INRIA / CEA) and their network of common labs (Equipes Mixtes de recherche) connections to many of the main players in the academic field whether they belong to Universities or Engineering have been established during the preparation of this proposal. Collaborations will be possible through members of the consortium but R&D collaboration contracts can be set up when relevant. This is a practice that has already been implemented within Nanoelec with partnerships with CNRS/C2N in Saclay and Ampere Laboratory in Lyon.

The connection to ecosystems will be further reinforced by the choice of the members for the Scientific and Strategic Advisory Board whose members will be selected so that the program network is also expanded to non-members of Nanoelec. As far as international collaborations are concerned two main thrusts will be pursued:

- Assessment of opportunities through European Funding scheme. The consortium will benefit from an existing network of partnerships at the European level with Universities and other RTOs to build projects benefiting from European programs. This will allow to bring leverage to the national funding of the program but also build partnerships to access specific know-how or help develop access to pilot lines or industrialized platforms benefiting our industrial members. Opportunities within the KDT scheme are already under exploration for Cryo-CMOS developments.
- In parallel and in coordination with these European initiatives, opportunities for international partnerships will be assessed :
 - With universities that are already connected to the network of the program members,
 - New academic teams when unique expertise, know-how have been identified through scientific and technology watch,
 - Industrial players if the program members, and the governance of the LSQ program are considering that such a partnership will benefit the National Strategy. This can be easily done with specific players such as material providers or equipment manufacturers but may also be the case with other actors

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whose contributions might benefit our ecosystem (acceleration, cross-technologies development or licencing, ...)

Nanoelec has already been involved in such international collaborations with leading material suppliers (Nagase, JSR) and equipment manufacturers (AMAT, LAM Research, EVG, SPTS,...) and academic labs in Canada and the US for instance (Sherbrooke University, University of Minnesota).

1.5. Impact & dissemination plan

The French quantum industry is rich in state-of-the-art qubit technologies champions, but the advent of a universal quantum computer requires costly technological developments to define a control of these qubits that goes to scale. This ambition and commitment over time and volume is one of the key success factors for achieving breakthrough innovations in the field of disruptive technology as the quantum technology.

The LSQ program brings together partners engaged over a long period of time, which is an essential condition for success in implementing disruptive innovations. In this context where, as we pointed out, all the links in the value chain from technology up to architecture system have to move forward together. The LSQ program supported by the IRT Nanoelec, by its generic dimension, will allow to mutualize these costs for all the actors of the quantum field who will be able to focus on their core expertise, where other scalability challenges needed to be addressed. Setting up a reference LSQ control platform will reduce the cost of entry of national or European players in the race toward LSQ. This will compensate from tighter funding of European quantum ecosystem with respect to US one (fundraising for the start-ups¹³), and help them increase their success odds and therefore secure more significant equity raise.

The plan for dissemination of and value creation from the results of the program will be built around the three pillars that are currently used by Technology Research Organizations around a model described by some tech transfer communities as T-C-R:

- **Transfer** Position IRT partners in the best conditions to use the results of Nanoelec programs : partnerships for value creation –
- **R&D** Build on technology bricks developed in Nanoelec programs through new R&D projects fully funded by industrial partners –
- **Create** and support new companies and provide opportunities for new company creation). In the case of the LSQ program Figure 9 illustrates how this could be implemented:

¹³ <https://web-assets.bcg.com/36/c4/1a807b3648d5a9eac68105641bfd/can-europe-catch-up-with-the-us-and-china-in-quantum-computing.pdf>

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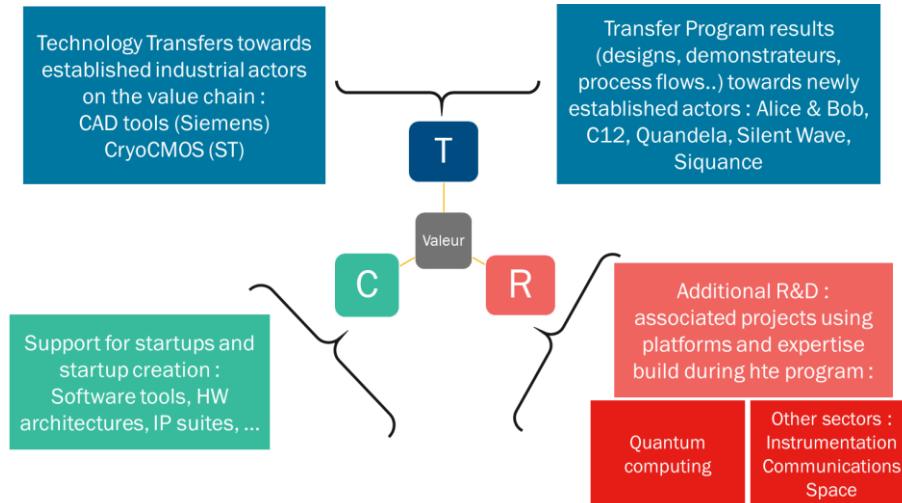


Figure 9 - TCR model applied to the IRT Nanoelec case for the LSQ program

Transfer: technologies developed in the program including results, patents, know-how and software IPs will be, if relevant, subject to:

- Technology transfer to industrial partners that are already established on the value chain such as STMicroelectronics as far as cryo-CMOS, 3D stacking and Silicon Photonics technologies are concerned but also Siemens EDA for CAD tools and software:
 - The benefits of the program will not be limited to the quantum IPs domain, but will encompass all technology domains it will rely on. In particular, the benefit of enabling holistic cryo design (from CMOS to SiPho and 3D integration to packaging), opens new strategic markets for the validated technologies. One can foresee the benefits of mastering extreme cold electronic designs for the space domain, which can bring significant systemic gains in reducing needs for temperature balancing between exposition phases, thus reducing overall system weight. In addition these extensions of validity domain would not require novel foundry process but would thrive on existing one, limiting the cost to access these markets.
 - Considering EDA, quantum computing constitutes a new market with emerging players that will need to devise their own design flows. Developing early relationships with emerging players is key to entering this market with its growth potential. Investing with the ecosystem in such a research project enables access to the all players and provides an efficient playground to define novel solutions fitting their specific needs. This framework also constitutes a relevant entry point to evaluate the advent of QC solutions and their benefit for EDA applications which often encompass several optimization phases that could be significantly accelerated. By this way, it will save time and money.
- Technology Transfer to the quantum technology companies that need these technologies for the development, industrialization and commercialization platforms. All 5 companies identified to date (A&B, C12, Quandela, Siquance, Silent Wave) are potential targets for exploitation of the program results.

R&D: The platform, expertise and IP generated in the program will also enable the Nanoelec Consortium to further engage in additional R&D projects aiming at bringing the technologies to higher levels of maturity and specialization;

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probably for the very same companies that are involved in the program but could also be used by future companies emerging in the national and European ecosystem thanks to disruptions in technologies. Besides, the very same set of results, IPs and equipment may also benefit other applications field especially in Space and Defense, Communications or Instrumentation. The economic impact of the results obtained by IRT Nanoelec is at the heart of its mission. In coherence with the consortium structure, this activity is managed by the IRT Direction team, and relies upon the deployment of resources brought by the partners and especially CEA. This is to benefit from a leverage effect from the business and marketing teams of partners and their background.

Create and Support Startups companies and emerging players: Specific CMOS IPs, whether soft or hard, will be generated by the project, in particular for readout signal amplification and in subsequent works on real-time error correction. Such IPs can be valorized on their own, and the go-to market strategy shall be assessed depending on the level of genericity reached and the projected volumes. If ASIC implementation is required to meet real-time QEC constraints, reaching significant volume needs will be paramount to the industrialization of the solution. It must be noted that depending on the maturity of qubits technologies available, the demand for QEC hardware may vary significantly. Alternatively, test chips may meet small volume demand before moving to more mature production as demand scales. Valorization of generated HW QEC solution will likely require specific PMT funding to build a QEC chip with all external IPs needed (IOs, control CPU...), partnership with design houses shall be sought to increase TRL of the solution. Valorization as an IP will also be investigated. The reuse potential of QEC accelerators by several chip vendor appears low compared to other more pervasive IPs (IOs, CPUs, DNN accelerators) and would likely deter IP licensing strategies. However, if FPGA implementations turns out to be relevant, soft IP licensing could benefit a larger ecosystem and bring faster return on investments to accompany further scale-up. This is an area where scenarios for company creation will be assessed on a regular basis. This will be done by evaluating the genericity of generated results and IPs, the confrontation with market opportunities and data and by interacting with the economic ecosystem.

Specific efforts to integrate the control chain in GENCI HPC Quantum infrastructure will also likely accelerate the go-to-market of the qubits solutions. The objective to bring-up a generic control platform will also help in the definition of common interfaces for the software stack, and will therefore help national actors in the quantum integration and compilation domain (such as Atos) extend their span to multiple qubit technologies while avoiding costly dispersion.

A link will be established with Nanoelec's Training Design Program to build new training capsules, modules and programs when required, in a complementary fashion with the QuanTEdu led by UGA. This sector requires an increasing number of human resources. Human capital will be a key factor. In this program, temporary resources recruitment aims at reinforcing the program work force but, also and mainly, at developing a broad quantum computing skills base in the ecosystem with the involvement and training of engineering students or young engineers, PhD Students, post-doctoral researchers.

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2. OBJECTIFS ET FEUILLE DE ROUTE DU PROGRAMME/PROJET

2.4. Ambition/Main Scientific and technical objectives

By using proven industrial technological processes – such as CMOS technologies for silicon spin qubit – solid-state qubit technologies aim to scale the number of qubits by reproducing them in large-sized matrices. A quantum dot for a spin qubit in silicon has a size of about 100 nm². Fabricating a matrix of 10⁸ qubits of this type would then require a silicon surface of 1 mm². However, utilizing such a large number of qubits must overcome several technological obstacles, which are described below.

The quantum effect of these technologies only appears in specific temperature conditions [10mK-1K], depending on the technologies, and over a short coherence time. Achieving such cryogenic temperatures (called Ultra-Low Temperature or ULT) is only possible with optimized management of the volume to be cooled and of heat insulation. The external communication interfaces between the quantum computer and its classical control system must thus be as compact as possible to avoid creating a thermal bridge and unreasonably increasing the volume to be cooled. In addition, a quantum calculation systematically involves (1) an initialization phase for all the qubits in a known state, (2) computation phases where several operations over the qubits are performed to apply quantum gates, (3) measure phases of the quantum states. Performing these steps in a scalable fashion that additionnaly supports QEC requires to define a multi-constrained control chain. The required components and associated constraints are summarized inFigure 10

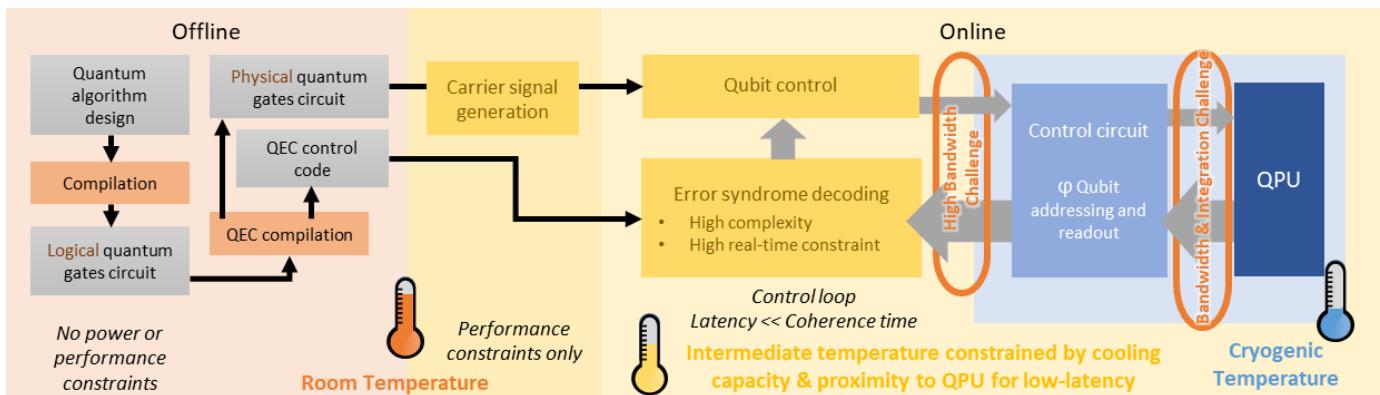


Figure 10 - schematic of a fault-tolerant control chain for solid-state qubit, and associated constraints

This results in a serious constraint on the design of the nearby control electronics for the quantum chip, which must on the one hand address large matrices of qubits and, on the other, communicate with the rest of the control system via a small number of links, while operating at ULT within a limited energy budget. This requires the design of CryoCMOS control circuits operating at temperatures below 4K and capable of communicating via high-speed links with the rest of the control chain.

The use of QEC solutions requires additional control as execution progresses. This involves the measurement of qubits called *ancillas* which collectively constitute a computing error syndrome the analysis of which allows feedback to

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correct the rest of the execution. This analysis must take place within a period constrained by the coherence time of the qubits (which varies according to the technologies). It therefore requires the design of dedicated real-time hardware solutions for which the energy budget also remains limited owing to the temperature. The consideration of error correction thus becomes a dimensioning factor for the control chip next to the qubit.

The challenge of defining a qubit control chain, taking QEC into consideration and communicating with the user at ambient temperature is thus common to all the solid-state qubit technologies. The strategies of the qubit designers are very similar in many ways, hence the need to have CryoCMOS control circuits (see architectures proposed by QuTech, Berkeley on superconducting SFQ, Google) and high-speed links (state-of-the art optical solutions being explored by Berkeley and NIST). The solutions designed by the Great LSQ Challenge could thus be applied to various promising qubit technologies.

Taking up this challenge implies defining design methodologies suitable for cryogenic temperatures. This entails controlling the behavior of standard transistors in these temperature ranges by characterizing and modelling them before performing combined analog-digital functions. The 3D design challenges are also considerable, with mechanical expansion stresses and differences in thermal behavior in these cryogenic and vacuum conditions (e.g. absence of convection, limited thermal diffusion outside the metal traces). The construction of dedicated models able to analyze these behaviors during the design phases would thus appear to be essential. The data rates involved between the cryogenic environment and the ambient temperature will for their part likely require fiber optic communications which demand expertise in silicon photonics technology and its packaging as well as the design of fibers dedicated to this type of thermal gradient. Finally, the design of processing control channels will be accelerated by the use of models such as digital twins to assess the target performance and energy consumption and allow architectural choices to be made in accordance with the QEC constraints.

These obstacles must be overcome in order to develop all the technological building blocks leading to control of an LSQ computer.

2.5. Positioning of the project in relation to the state of the art

Under Construction

Will be provided on March 3rd

2.6. Key Science and Technology Challenges and Technology Leads considered

To take up the challenges of scaling solid-state quantum machines, IRT Nanoelec will set up and manage an ambitious LSQ Program as part of the Great LSQ Challenge, which will aim to develop the technological value chain for control and programming of qubits in cryogenic conditions. The development of solid-state qubit solutions is not covered by the Program, but by other complementary actions within the national quantum strategy and in particular the Priority Research Equipment Program (PEPR).

Based on the expertise developed with previous IRT Nanoelec programs on 3D integration and silicon photonics, along with the expertise of the quantum technology research players (CNRS-Institut Néel, INRIA, CEA), the IRT proposes developing a unique program designed to overcome the 7 challenges to the arrival of LSQ for solid-state qubit technologies:

Challenge 1– Digital model of the quantum control chain: The first challenge aims to define a functional digital twin type model for the control chain, from the logical qubit up to the matrix of imperfect solid state qubits, taking account

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of the error correction code. This digital model will enable designers to explore architectural solutions for the complete control chain, taking account of needs in terms of computing, throughput and impacts in terms of dissipation budget consumption for the processing chains. It will be used to define the first technology demonstrators and to define the architecture of the future generation, with the aim of producing an integrated demonstrator. This model will allow the evaluation of different options to facilitate architecture design choice by taking account of multi-criteria constraints and thus selecting the best solutions in order to save time in the design/production processes. This digital model will take account of the control constraints of the various qubit technologies (subject to the availability of information from the project stakeholders). The experimental results obtained during the course of the program will feed the model with experimental data.

System architecture (Challenge 2):

The second challenge is tightly linked with the difficulty to build a system vision for the control architecture. Redefining control chain in a scalable fashion, requires to question all choices made at a smaller scale and making a decision on one component can directly impact the applicability of the remainder of the chain. Consequently, the first architectural challenge will consist in bringing together expertise from different fields, through the system modelling approach, and with direct involvement of the project stakeholders, to lay down the foundations for scalability. This will enable achieving high optimization of the overall system control for both performance and energy efficiency. As many quantum technology are being developed, the architecture work will target to encompass the external technological evolution on the scalability roadmaps. Another challenge that will need to be faced is the lack of full understanding of component behaviors in cryo conditions that can hinder the capacity to understand and debug experimental demonstrators. Therefore, a specific attention to find novel design for cryo-testing methodology will need to be sought out. Finally the most impacting challenge comes from the dual target of realizing a generic control chain for several qubit types while optimizing it at the same time. Arbitration towards performance or genericity will be required in the project.

Challenge 3 – Optical links: Faced with the considerable challenges of rate and latency needed for qubit control and d'error correction codes, the third research challenge will address the design of a fiber optic communication chain. The thermal stresses on such a chain and the design of special optical fibers in a thermal gradient ranging from ULT to ambient temperature will be investigated. According to the target technologies chosen, the project will investigate the issues of silicon photonics at ULT and its specific packaging problems. Signal conversion solutions in cryogenic conditions will also be studied.

Challenge 4 – Real-time QEC: In order to provide data required to overcome the above mentioned challenge, this research challenge will study the error mitigation and correction chain, as a dimensioning parameter of the control chain for known algorithms in the literature. This challenge will also aim to define the real-time hardware processing chain for analysis of surface code syndromes and feedback decision-making. To a certain extent, the technologies developed will be generic and modular, so as to address the various constraints of solid-state qubit technologies (coherence time, error rate). A solution optimized for a given qubit technology will be implemented in an FPGA demonstrator.

Challenge 5 – Cryo electronic: The fifth research challenge aims to develop CMOS design libraries and electronics components in cryogenic conditions suitable for the definition of AMS circuits. This will involve work to characterize

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and model transistor behavior at these temperatures. This work could lead to the definition and production of minimal subsets of characterized components leading to a design using a traditional design flow. It is here important to note the full potential of FDSOI technologies in cryogenic conditions thanks to the possibility of back-biasing the substrate to compensate for certain behavioral drifts. The scaling up challenge is to enabling a French/European robust industrial supply chain for cryo-electronic devices and superconducting quantum circuits.

Challenge 6 – 3D Integration and Packaging: Over and above the behavior of the transistors, the design of a control chain next to the qubit requires the use of advanced 3D integration technologies for which it is important to evaluate the applicability at low temperatures (mechanical stresses, differential expansion, behavior of materials). Thermal dissipation behavior also differs at these temperatures. The sixth research challenge will therefore aim to establish a 3D design and packaging stream compatible with very low temperatures, on the basis of the existing streams. Additional tools capable of assessing behaviors below a temperature of 4K could be defined for this purpose.

Challenge 7 - Cryogenic Tests: The technical challenges above, will need test capacities and capabilities à cryogenic temperatures to be addressed. But characterization protocols themselves need to be improved or developed: current means and methods are academic grade and not adapted to systematic and statistical tests, devices self-heating phenomena impact on large scale electronic have to be evaluated.

These 7 challenges, supported in the operational phase by as many WPs, will be articulated together toward a common goal of achieving an integrated control chain demonstrating the relevance of the building blocks created and validated by the project. One key aspect for this ultimate challenge will consist in defining adapted testing methodologies to validate correct functioning. Especially the fact that qubit resources may not be immediately available abundantly shall be considered while providing confidence in the overall chain. Smaller scale testing might prove necessary as well as the use of more mature qubit control technologies to provide high-quality measure of the achieved communication links. This work will also target integration into the software stack developed within HQI. This demonstrator will be the root for ever more integrated FTQC (Fault Tolerant Quantum Computation) demonstrations with potentially several types of qubits with the definition of complimentary *Associated Projects* to the core IRT one.

2.7. Technological Roadmap

To give an overall vision of the technical work envisioned in the project, Figure 11 summarizes the planning of key milestone of the project.

WP1 will address the challenge of spanning the expertise from several domains within a single simulation environment. First stages will therefore focus on laying the infrastructure for a first system model then populate it with control chain components and quantum application requirements data. Then the work will be focused on continuous evolution of the models with project and international state of art evolutions. A last line of work will be started in the last part of the project to provide a programmer's view of the QEC hardware interface for validation of its integration in hybrid HPC-quantum environments

WP2 that will supervise the architectural decision will first detail specification for the system modelling approach developed within WP1. Then based on its availability, will start projecting scalability routes leading to the definition of

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the demonstrator spec. The work package will thereafter supervise the demonstrator work up to its final testing since it will require developments from all technological WPs 3-6.

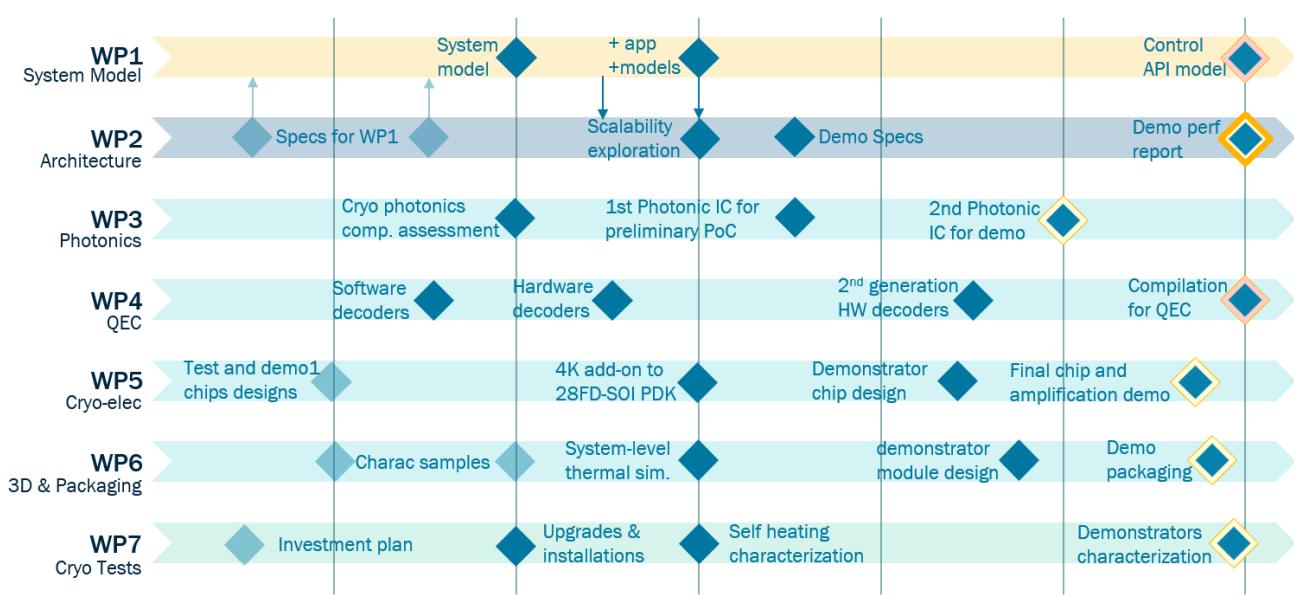


Figure 11 - Key milestones of the LSQ program technological roadmap (yellow contours highlight IC productions for the final demonstrator while red contour are for applicative QEC demonstrator),

WP3: The WP will start with the cryogenic evaluation of existing photonics components, so as to focus design efforts on key missing functions. Then two photonic integrated components designs will be done, one preliminary proof of concept and then the final demonstrator. Synchronously CMOS ICs for the photonic drivers will be designed, so as to build a complete communication photonic subsystem.

WP4 will initially be focused on existing QEC decoder software then hardware implementation, then will study in a second stage novel codes impact on performance. Last stage of the program will address compilation issues with QEC to better integrate QEC in the software stack.

WP5: First major milestone will be the design of the first test chips for CMOS FDSOI cryogenic evaluation. In the meantime, characterizations and model enrichment will lead to the second milestone: 4K add-on to 28FD-SOI technology. Then final chip design and fabrication for the demonstrator and pre-industrial amplification demonstration will be the two last milestones

WP6 will start by developing samples for material testing that will help populate datasets for thermal simulation and 3D interconnection in cryo-condition. Specific tests and software developments shall lead to the definition of a system level thermal simulation methodology accounting for the photonic transport of heat at small scale and low temperature. Based on this knowledge, the work will then focus on the definition of the thermally and electrically efficient 3D integration scheme for the final demonstrator, and will ensure its packaging.

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WP7: The WP will start with the definition (first milestone) and the execution (second milestone) of the investment plan needed to be able to characterize the program work packages evaluations and demonstrators. In the meantime, self-heating effect will be evaluated (third milestone), and the WP will end with the demonstrators characterization as the fourth milestone.

2.8. Link and coordination with other projects

The LSQ project will be tightly linked with other projects in the SNAQ as depicted in Figure 12. With its unique position on technological transfer, IRT Nanoelec is naturally leveraging technologies developed in lower TRL projects. Indeed, the LSQ project will directly leverage research performed within the PEPR program that started ahead of it. In particular results from directed projects developing qubits -- such as Presquile for quantum-dots based spin-qubits and RobustSuperQ for superconducting qubits – will be used to populate system models for qubits and help project scaling roadmaps for these technology. These projects also fund technological developments necessary for qubit designs that can have a broader impact on the control chain development, and require further investigation within the LSQ program. One can mention 3D integration at low temperature or superconducting fabrication process that are also used for TWPAs. Even more crucial, the error correction algorithms developed in NISQ2LSQ will be studied for hardware decoding implementation within the LSQ program's WP4, making it a valorization vector for these technologies.

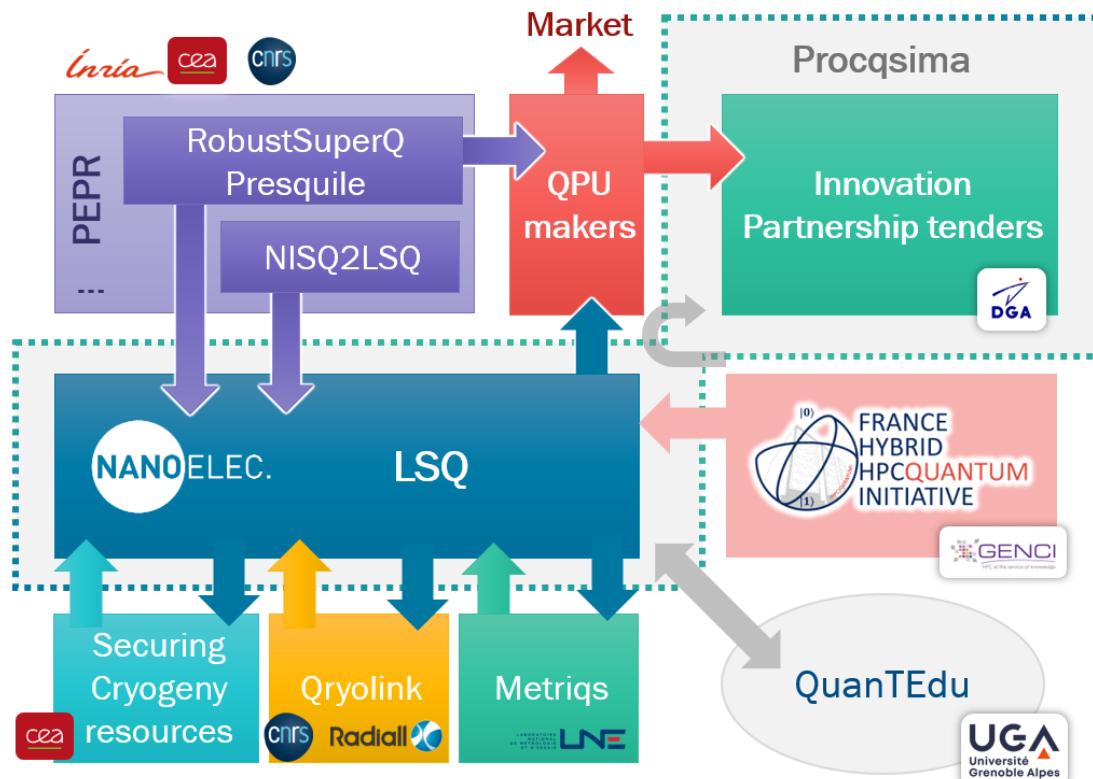


Figure 12 - Interdependence of the project with complementary projects in the SNAQ

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Another source of strong link with other projects in the SNAQ lie in the control chain system modelling approach sought in WP1. Indeed, the project will use reference data stemming from the Cryogeny project as constraints for the cooling capacities that can be expected when the scaling of the control chain will be required. Reciprocally, the LSQ program will provide requirements for future cryo-systems. Similarly, the Qryolink project, that develops novel generation of control chains for experimental and NISQ setups, will be a source of data for state-of-art components. The open cryogenic platforms that the project also aims to develop, could also be leveraged for the LSQ program test needs. Early discussion with Qryolink partners also stressed their interest for a system vision and projection of the market needs. They could therefore directly benefit from the system model set up in WP1. Last but not least, the Metriqs project supervised by the LNE (*Laboratoire National de métrologie et d'Essais* – National Laboratory of Metrology and Testing) will target the definition of reference figure of merits for a variety of quantum technologies. Defining the parameters of the system model components in agreement with the measured figure of merits would help populating the models in the long run. Reversibly, should a parameter be critical for system analysis, it shall be part of the assessed properties of a component in LNE's methodology. Therefore bridges will be built with the Metriqs project as both program make progress.

As previously mentioned future QPUs will likely be integrated within HPC centers similarly to the approach conducted with the HQI platform. Therefore quantum control chains need to interoperate with ease with such environment. In order to address this aspect, the LSQ program will rely on developments in the scope of the HQI program that will lead to the definition of standardized interfaces with QPUs. It was secured during the project build-up phase that such interfaces will be made public, and therefore exploitable by the LSQ program developments. In addition CEA teams involved on the QEC hardware definition – and therefore programming interfaces -- will also be involved in HQI for NISQ solution integration. This will ensure proper understanding and early access to this critical interface. This interface will also likely be part of the requirements of future provision of next generation QPU by the DGA's innovation partnership tenders, easing the way to valorization of the LSQ developments.

The LSQ program will also require the involvement of well-trained researchers that are becoming a scarce resource with the growing importance of industrial actors, and the steep acceleration of the research project in the past years. To cope with this issue, the program will seek to strengthen its links with the QuanTEdu France project to ensure its training needs are well covered by the courses set up and get a privileged access to first-rank students. This link will naturally grow with the involvement of QuanTEdu's pilot (UGA/Institut Néel) in the program.

Finally the last link with SNAQ projects is indirect and is in fact one aspect of the valorization strategy. Indeed the innovation achieved within the project will be exploited by quantum industrial partners in their route towards LSQ. One of their first commercial target is therefore likely to be the innovation partnership public tenders that are envisioned to be setup by the DGA. Consequently, in the State's vision, the LSQ program and this public tenders approach are part of a broader ensemble named Proqsima.

As the national quantum project landscape is evolving with changes in the international environment, one can foresee that other projects in the SNAQ will rise by the end of the program's execution. The program will therefore seek to continue developing links with these project to come, whenever it serves its objectives or valorization strategies.

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2.9. IP Development and IP strengthening strategy

As described in the work program, further in the document, a series of investments, in synergy with infrastructures brought by the various partners of the program, are envisioned to avoid delays on demonstration and test activities during the program:

- 2 cryostats and their instrumentation would be supplied and installed at CNRS/NEEL and CEA/IRIG. They are necessary to test the various technology blocks that will be developed and assembled over the duration of the program: cryo-electronics test vehicles and integrated circuits, key elements of the control chain such as TWPAS, Circulators, resonators, assembly and packaging of test chips as well as silicon photonic ICs designed for low temperature environments.
- 1 or 2 cryogenic probing systems with RF characterization capabilities
- The investment in a cryo-prober compatible with testing of devices at large scale (wafers) is also envisioned.
- QLM machines and high-end FPGA platforms will also be assessed as potential investments for the evaluation of error code correction algorithms and software blocks.

In addition, the main results generated by Nanoelec during the project are protected through the filing of patents and software. In the field of semiconductor technologies, the experience shows that, over the duration of a program, an average of one patent per million euro of funding is generated. As a result in the framework of the LSQ program we envision the filing of about 40 patents. These will add to the 60 patents brought by Nanoelec from its background in 3D and silicon photonics technologies.

Moreover, in order to address the requirement for reinforcing IP portfolios accessible to the partners of the program the approach proposed by the consortium is to set up during the full duration of the program a scientific, technological and economic watch. The aim is to identify, as soon as possible, potential threats stemming from scientific advances in the field or new patents that have been filed. The process will be based on a dual set-up:

- The construction and a constant update of search profiles on a diversity of databases to cover scientific publications, patents and economic news with a focus on emerging actors and key results of the main players in the field.
- The animation of a network of the scientists and engineers involved in the program to analyze the production and help the program management team identify the most relevant and impactful elements of information.

Based on these analyses, opportunities for collaborations will be identified. Contact will be established with the identified teams to explore opportunities for cooperation through research programs and agreements covering both technical and IP access rules. It is a practice that has been successfully experienced by CEA teams in the framework of various international cooperation agreements. A good example is the partnerships on NEMS technologies and applications, launched in 2006 between CEA LETI and CALTECH and that has resulted in a common startup specialized in gas sensing solutions, located in France, APIX ANALYTICS. The diagram below visualizes the process we propose to implement with the potential impact on the IP portfolio on which the partners will be able to build their industrialization and commercialization strategies. Such international partnerships will require additional funding.

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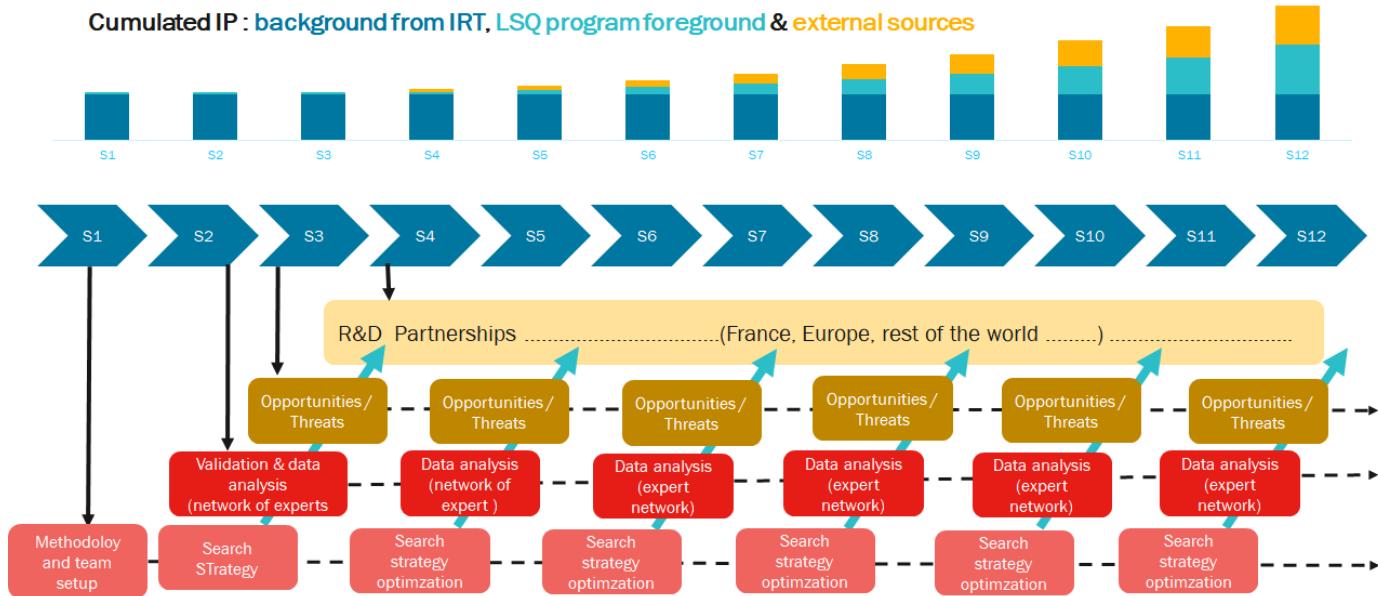


Figure 13 - IP development and IP strengthening strategy through scientific watch

The process will be led by CEA information management teams form the “Direction de la Valorisation” including the marketing department (SBEM). This department is a team of 30 professionals specialized in the analysis of data coming from data sources (patents publications). The team also provides market intelligence to help CEA teams position their projects with regards to industrialization opportunities and value creation. The team includes a group specialized in the field of information technologies, from microelectronics to software systems and has already been working in the field of quantum technologies for a few years. Thus, the team brings to the program a knowledge base on industrial ecosystems in the field, a follow-up of the main startups and industrial leaders in the field, as well as a market analysis of the high performance computing market. An analysis of technology dependence has also been performed for a variety of quantum technologies. The marketing team makes use of a series of information research tools such as **Orbit Intelligence**, **Scopus** and **Web Of Science**, **Cobaz**, **IPMetrix – Projets collaboratifs**, **Crunchbase**. The team has also access to **Orbit Intellixir** that allows to centralize data from patents and scientific publications in a common interface. The documents can then be segmented, commented, analyzed for quantitative statistical purposes or more qualitative evaluations. Finally, as far as articles in general and specialized media are concerned, the team uses the **Digimind** tool to configure data searches and then comment and share collected information. All profiles of information search and data collection are built and optimized in partnership with scientific and technical experts in a collaborative approach.

The teams involved in the LSQ program will also benefit from the experience of CNRS and CEA teams of managing the OMNT (Micro & Nano Technology Observatory). OMNT was a team of up to ten professionals that coordinated over a 10 year span a project gathering subgroups of national experts from different fields to collect scientific and technological information and share their analysis to identify innovation, evaluate their impact on the field. The methodology used by the teams (search profile, data sharing, bimensual meetings, yearly workshop) will be adapted to the specifics of the LSQ program expectations and implemented as a task of WPO.

A key success factor for the exploitation of these information will be the ability to launch action plans following the identification of relevant information:

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- Analyzing the best approaches for accessing the information of IOP of interest
- Establishing plans for setting up academic partnerships
- Having access to resources to fund such cooperation schemes.

The different organizations (CNRS, CEA, INRIA, UGA) involved in the program have a large experience in building international cooperation projects through common laboratories with universities abroad or through strategic partnerships. The management teams of IRT also benefit from such an experience.

It should be also noted that such international partnerships will probably require additional funds that have not been planned for in the current program.

The operating principles for the management of non-material assets is described in the consortium agreement and explained in § 1.2.2.

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3. PRELIMINARY DESCRIPTION OF PLANNED WORK

3.4. Scientific approach, method and work plan

Above all, the work conducted directly within the scope of the project shall target the definition of generic building blocks for the control chain. Genericity will be key to find applications for a variety of solid-state qubits and accelerate the maturation of most promising qubit technologies through the maturation plan. It is also a necessity to provide a fair development path for all the technologies. Thus the identification of common requirements from various qubit makers will be sought to refine the scope of the actions.

If the communication and error correction chains are inherently generic in terms of technological solutions, functioning point will likely differ. For instance, significant differences in qubit physics induce orders of magnitude of difference in the coherence time which dimensions both the communication bandwidth and QEC performance needs. Qubits errors as well as interconnection topologies will also likely differ impacting the whole control. To cope with this, the project will target generic hardware implementation of QEC methods that shall support various power/area/performance tradeoffs. Communication techniques investigated shall provide the necessary performance for the various qubit needs. To project system performance at scale, simulation of the complete control chain will be sought to help system decision for all qubit technologies which would likely yield to different setups based on the generic building blocks.

Part of the control chain are however very specific to some qubit technologies. This will likely be the case for the qubit control circuit which shall perform gate application through the emission of very specific RF signals as well as the readout of the qubits. Part of this cryo-electronics can be seen as generic. For instance parametric amplifier for the readout will be needed no matter the technology. However, they will likely need optimization to a given signal range to be exploited, and their operating conditions are expected to significantly differ. Other IPs, such as signal multiplexing, or encoding/decoding shall be more generic but may also need significant adaptation to cope with various qubit addressing strategies. Consequently, deeper analysis, with contributions from the qubit players, must be conducted as part of the project work plan to clarify the project boundaries closest to the qubits. The rationale that will guide decision during this phase will be to address all generic work in the Grand LSQ Challenge and keep all optimization for a given qubit for the maturation plan. Qubit control features not considered as generic will gracefully benefit from the cryo characterization work that will accelerate the design of qubit specific control circuits in the future.

Last but not least, the project will target the integration of the control chain in HPC infrastructure. Reaching this goal would permit various qubit technology to rapidly be exploited by infrastructures such as the one setup by GENCI in the HQI project. The programming interface of the control chain shall be kept unified no matter the qubit technology. Ideally this unified interface would be built on available standards developed at the national or European level or become one *de facto*. In doing so, work on the universal QPU API, the QEC compilation & mapping, and the transpilation for RT-QEC control will be required. This line of work will be very dependent on both the hardware QEC design (which depends on the QEC scheme itself), and the qubit technologies (which exhibit various error rates, and can handle some gates better than other). Consequently this line of work will start with limited activities to survey existing software stacks and evolutions of the HQI platform and will gain importance as the definition of the control hardware including QEC becomes mature enough.

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To validate the key control building blocks built in the project, significant efforts will be spent on setting up an adapted test plan. Due to dependency to the availability of qubits for complete control chain validation, the program will be built considering their lack, and will provide unit testing strategies. This will require to leverage all existing expertise in (non-scalable) qubit control to perform validation measures of the communication chain in cryogenic conditions. This approach of unit testing will therefore be conducted in each WP of the program, and will make use of common measure expertise and infrastructure shared by Nanoelec partners. Time sharing of these facilities will be needed among all quantum computing projects of the SNA. Tight supervision of the measure needs will be performed at the program level in close interaction with equipment's owners to ensure efficient usage of these resources.

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3.5. Décomposition du programmes

3.5.1. Liste des actions et lots

Premier niveau de découpage		Second niveau de découpage (optionnel)		Qualif. RGEC (1)	Rôle IRT (2)
Lot #	Description lot	Tâche #	Description tâche		
0	Management-& coordination	4	Coordination IRT/reporting/dissemination/Valorization/Development of the consortium	RI	S*
1	Digital models and EDA tools for quantum control chain system design exploration	3	Gap analysis for EDA tools evolutions for quantum computing/ System modelling/QPU functional models	RI	S*
2	Architecture specification towards integrated demonstrator	6	Expression of requirements for developed technologies/ Expression of requirements for system model analyses/Evaluation of scalability strategies for performance and energy efficiency/Specification for the control chain demonstrator/Control chain demonstrator supervision and integration/Specification for future generation of scalable control chain	RI	S*
3	Integrated photonX	4	Evaluation of existing components/Photonics for Cryo/CMOS driver/Integrated photonic sub-system for final demonstrator	RI	S*
4	Real-Time quantum error correction	6	Software implementation of topological codes decoders/Hardware implementation of topological codes decoders/Software implementation of decoders from PEPR NISQ2LSQ/Hardware implementation of decoders from PEPR NISQ2LSQ/ Exploration of error correction tradeoffs (correction rate, latency, power, complexity)/ Hardware aware compilation of universal set of logical gates/Final Demonstrator	RI	S*
5	Cryogenic electronic	5	Devices characterizations at 4K (and 77K sampling) for PDK Add-On/Compact model developments for FD-SOI transistors and diode at cryogenic temperatures/First 28FD-SOI PDK 4K (and 77K) add-on implementations/ Cryo CMOS design/ Electronics devices evaluations at cryogenic temperatures	RI	S*
6	3D integration and packaging	5	Test vehicle fabrication/Packaging of test vehicles and demonstrator/Experimental characterizations/Modelling and simulations/Control Chain Demonstrator	RI	S*
7	Cryogenic characterization	4	Equipment needs identification & equipment acquisition/Characterization methods development/Characterization PCB and systems design/Room temperature electronics for test and demonstration.	RI	S*

Indiquer tous les lots du projet, même lorsque l'IRT n'y participe pas.

(1) Qualification RGEC : RF : recherche fondamentale ; RI : recherche industrielle ; DE : développement expérimental ; EF : étude de faisabilité

(2) S* si l'IRT réalise le lot ou la tâche seul, Nanoelec est un consortium; le projet s'appuiera sur l'implication de plusieurs partenaires

R si l'IRT est responsable du lot ou de la tâche,

P si l'IRT est un partenaire non responsable du lot ou de la tâche,

N si l'IRT ne participe pas au lot ou à la tâche.

(3) Date relative par rapport au début du projet, en mois.

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3.5.2. Actions and Work packages organization

The Work Breakdown Structure is made of 7 technical Work Packages in addition to the WP Management as depicted in Figure 14:

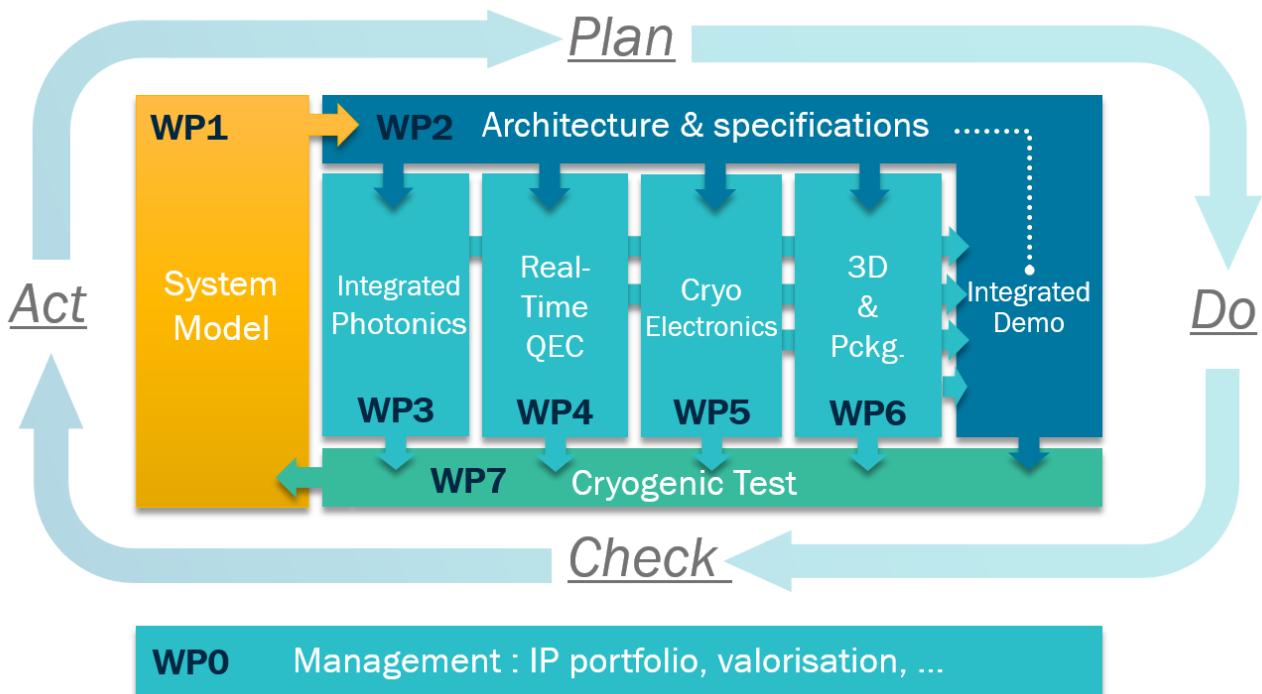


Figure 14 - LSQ program work package organization

- **WP0: Project management:** This WP is in charge of project management, ensuring reporting, dissemination, and IP management.

- **WP1- Digital models and EDA tools for quantum control chain system design exploration:** This work package consists in enabling the design of a scalable control chain by analyzing possible gaps of electronic design tools to comply with novel cryogenic constraints, and defining a novel system modelling solution for quantum control chains. Dedicated actions in WP1 will seek to provide applicative resource constraints, while technology WP3-6 will help populate the system model by providing hardware components constraints and performance figures.

- **WP2- Architecture specification towards integrated demonstrator:** This work package will centralize all design decisions regarding system design of an integrated control chain. It is in charge of gathering intelligence from the system modelling in WP1 to identify enabling technologies for the scalability of the control, and take design decisions for the project demonstrators.

- **WP3- Integrated photonics:** WP3 will study how integrated photonics can be leveraged to allow for increased scalability of the communication links between the cryo-stated qubits and the likely more power consuming error estimation hardware developed in WP4.

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- **WP4- Real-Time quantum error correction:** the ambition of WP4 is to design real-time QEC solutions that scale with the number of qubits. To reach this goal, software and hardware implementations of QEC decoders will be investigated, based either on existing decoding algorithms, or under development within the PEPR project NISQ2LSQ. Acquired knowledge will be fed back to the system modelling in WP1 for the complete control chain design.

- **WP5- Cryogenic electronic:** Solid-state circuits operating at cryogenic temperature requires classical electronic controllers operating at cryogenic temperatures. This work package aims at developing CMOS model & design-blocks in cryogenic conditions, at evaluating and maturing electronic devices technologies, and at developing a superconducting quantum circuit industrial sector to enable a French and European robust supply chain.

- **WP6 - 3D integration and packaging:** The aim of work package 6 is to validate the complete communication chain in terms of cryogenic electro-thermal behavior by developing 3D interconnection and packaging solutions which optimally manage heat flux and high-frequency signals that will propagate in the final demonstrator. Starting from WP2 recommendations, system architecture hypotheses will be investigated regarding interconnections key technologies, parasitics and power dissipation.

- **WP7- Cryogenic characterization:** This work package aims at addressing the cryogenic characterization needs of the other work packages. CEA-Leti, CEA-IRIG, CNRS-Neel, IMEP-Lahc already have cryogenic characterizations capabilities, but our first analysis highlights that the LSQ program will need additional testing resources since existing facilities workload is already high. In addition, the scaling naturally calls for statistical characterizations, which in turn requires tools and characterization methods industrialization.

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3.6. Envisioned thesis funding

We estimated that twenty to twenty-five Ph D. subjects will be launched during the program. The number and the subjects of the thesis may change during the project, in function of the results and the state of the art.

# Ph D	WP / Task	Etablissement	Directeur de thèse
7	T1.2.3 Applicative constraints T4.3 Software implementation of decoders from PEPR NISQ2LSQ T4.4 Hardware implementation of decoders from PEPR NISQ2LSQ T4.6 Hardware aware compilation of universal set of logical gates	INRIA	
4	T3.1&T3.2 Photonics for Cryo T5 CMOS Cryogenic characterization T5.2 Compact model developments for FD-SOI transistors and diode at cryogenic temperatures T7.2.3 Self-heating phenomena evaluation and impact simulation on cryogenic characterizations	UGA/IMEP UGA/IMEP	
5	T5.1.2 BEOL interconnect and RF passives models. T5.1.3 Reliability tests. T5.4 Cryo CMOS Design T7.2.3 Self-heating phenomena evaluation and impact simulation on cryogenic characterizations T7.3 Room temperature electronics for test and demonstration	CEA	
3	T3.2 Photonics for Cryo T5.5 Electronics devices evaluations at cryogenic temperatures	CNRS	
4	T5 Cryo CMOS	ST	

3.7. Identified risks and mitigation plan

Due to the very open research area this projects addresses, technological risk is high and was therefore addressed directly in the structure of the actions described before. Still some technological risks remain, whose fallback plan would require additional efforts, not covered by the current workplan. To apply the projected mitigation plan evolution of the work plan would be required, as shall be permitted by Nanoelec's convention with ANR to better adapt to experimental results. Other important risks (legal, financial, diplomatic) not covered in the work description are listed here **below**. To keep the current document tractable, full risk analysis is depicted in **appendix 03**

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4. WORK DESCRIPTION

4.4. WPO Operational management, intellectual property capitalization and valorization

4.4.1. Work package objectives

This work package aims at the global management and work-package coordination, intellectual properties management, dissemination and valorization of the work and communication. It will also provide scientific and technical watch, and generate possible synergies with other domains (as spatial...).

4.4.2. Partners Role

Entity	Role
IRT/DIR	Due to the importance of the program in IRT Nanoelec actions, IRT will dedicate resources to the program for financial, legal, communication and scientific actions.
<u>CEA</u>	As major provider of research works conducted in the project, CEA with its institutes CEA-list and CEA-leti will lead the project operational execution. CEA's marketing analysis office has developed key competences in market and patent survey for a wide range of technology. It will drive actions regarding access to IP rights and freedom to operate.
All partners	All partners in the project will be involved in the access IP strategy, by sharing on their own research and patent watch. They will also be in charge of the scientific dissemination of the works conducted in the program.

4.4.3. Detailed work description

T0.1 Operational Management		
Start: M1	End: M72	Lead: CEA
Contributors: CEA		
Description:		
<p>T0.1 will be in charge of the supervision of technical actions conducted in the WP1 to7 and will ensure correct flow of information in between work packages.</p> <p>The program directors will report to the IRT COPIL significant evolution of the program execution and will propose corrective actions whenever necessary. In order to achieve the necessary steering of actions the task will organize monthly WP leaders meetings, as well as regular Program Committee meetings.</p> <p>Task T0.1 will update risk assessment analysis, manage interactions with other French quantum strategy programs and European calls, and identify potential synergies with, for example, space domain applications. It will drive the interactions with the advisory board, consolidate annual ANR reports on achieved works and dedicated efforts.</p> <p>Task T0.1 will also monitor the worldwide publications to benchmark the program objectives and results.</p>		
Deliverables (due month/lead):		
D0.1 Annual report 1 (M12) D0.2 Annual report 1 (M24) D0.3 Annual report 1 (M36) D0.4 Annual report 1 (M48) D0.5 Annual report 1 (M60) D0.6 Annual report 1 (M72)		

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T0.2 Intellectual property management									
Start: M1		End: M72		Lead: CEA/SBEM					
Contributors: CEA/SBEM + All partners									
Description: <p>The main objective of T0.2 is to ensure the freedom to operate of developed IPs in the program. In order to achieve that, the task will focus on performing active watch of external IPs evolution. Specific search patterns will be setup for both OSINT analysis as well as closed publications and patent databases. Adapted filtering and data analysis will target to cluster retrieved information to assess IP generated by third parties. Then further analysis will be handed over to researchers with the correct background. The capacity to provide the good level of filtering will be critical to request analysis from researchers only when necessary.</p> <p>Complementary analysis will seek to identify ecosystem links for concurrent IP portfolio, to identify market opportunities.</p>									
Deliverables (due month/lead): Report on search request definitions (M24) Intermediate report on identified IP threats and opportunities (M36) Summary report on identified IP threats and opportunities (M72)									
T0.3 Dissemination, valorization, and communications									
Start: M0		End: M72		Lead: CEA					
Contributors: CEA/IRT									
Description: <p>The task will coordinate all communication and dissemination actions in the program. It will ensure scientific communications shed good light on the project by including proper references to the source of the research. To ease communications in all context, the task will prepare public communication documents for all supports whether digital (logo, slide decks, LinkedIn posts) and physical (kakemonos, posters, sustainable accessories).</p> <p>Both know-how and patents are an important production issued from the project and this is reported in this task. Publications, patents are all reported in each annual report.</p> <p>Additionally, economic and social valorization by industrial partners are also key success indicators of the project and will be highlighted in annual reports and specific reporting.</p> <p>Initial dissemination and valorization plan (cf 1.5) will be updated on regular bases taking into account technical results, IP portfolio evolutions, changes in the ecosystem landscape.</p>									
Deliverables (due month/lead): D0.4.1 Communication kit (M12) D0.4.2 Synthesis of communication actions (M72) D0.4.3 Valorisation plan update (M36) D0.4.4 Final valorisation plan (M72)									

4.5. WP1 Digital models and EDA tools for quantum control chain system design exploration

4.5.1. Work package objectives

The ambition of WP1 is to enable the design of a scalable control chain by analyzing possible gaps of electronic design tools to comply with novel cryogenic constraints, and defining a novel system modelling solution for quantum control

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chains. Gap analysis will support design works from WP3-6, while system modelling will be core to the architecture exploration and definition conducted in WP2-Architecture.

To provide relevant analysis the system model will be enriched from hardware and software data. Dedicated actions in WP1 will seek to provide applicative resource constraints, while technology WP3-6 will help populate the system model by providing hardware components constraints and performance figures. To ensure a holistic vision, the WP will develop strong interaction with other projects in the national strategy to encompass for instance RF links properties or cryogenic power.

At a later stage of the program, based on WP4-QEC developments, functional model of the programming interface of the control chain including error-correction will also be addressed to ease quantum software development and allow applicative performance evaluation.

4.5.2. Partners Role

Entity	Role
CNRS	With its expertise in quantum system modelling encompassing energetic issues, CNRS will provide the initial shared system modelling infrastructure and will extend knowledge databases with state of art review of technologies out of the scope of the program
CEA	Together with CNRS, CEA will bring the system model setup by CNRS for superconducting QPUs to a higher maturity level by defining a generic system modelling approach taking its roots from MBSE and ESL simulation. CEA will also enrich the applicative aspect by providing dimensioning application use cases, and will provide models build on acquired data in WP3-6. In later project stages, CEA will conceive programmer's view models for error-corrected quantum computers
Siemens	Work Package Leader As a major player in EDA and system simulation, Siemens will evaluate its tool applicability to cryo system design and support design work in WP3-6.
Inria	Inria/QUACS will provide dimensioning use-cases for numerical simulation such as HHL. The Quantic team at Inria will also provide hardware constraints and information flow structure for architectures based on stabilized bosonic qubits
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, industrial QPU makers would provide dimensioning data on qubits properties for system modelling (error model, connection topology)
Silent Waves	Upon joining the program, SilentWaves would provide data on TWPA

4.5.3. Detailed work description

T1.1 Gap analysis for EDA tools evolutions for quantum computing		
Start: M0	End: M12	Lead: Siemens
Contributors: Siemens, CEA		
Description: The target of this task is to identify for EDA tools involved in classical electronic design the specific evolutions needed to address the challenge of quantum computing. In particular, the impact of change of material behaviors at low/cryogenic temperature is expected to push the tools to their limits; this includes thermal phenomena at small scale and superconducting behavior. This task will gather feedback from CEA experts involved in WP3 to WP6 on existing tools and specific design needs. Siemens will identify to what extent their current offer can meet the project needs, or devise evolution plans in line with the project and market schedules.		

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Deliverables (due month/lead):

D1.1 Report on needed EDA tool evolutions (M12)

T1.2 System modelling

Description:

Bringing the gap between many expertise domains (application, QEC, 3D integration, integrated photonics, cryo-electronics, cryogenics...) is critical to the definition of innovative control chains for qubits that shall reach a global optimum rather than local ones. The following tasks together aim at defining a novel system approach for quantum control electronics.

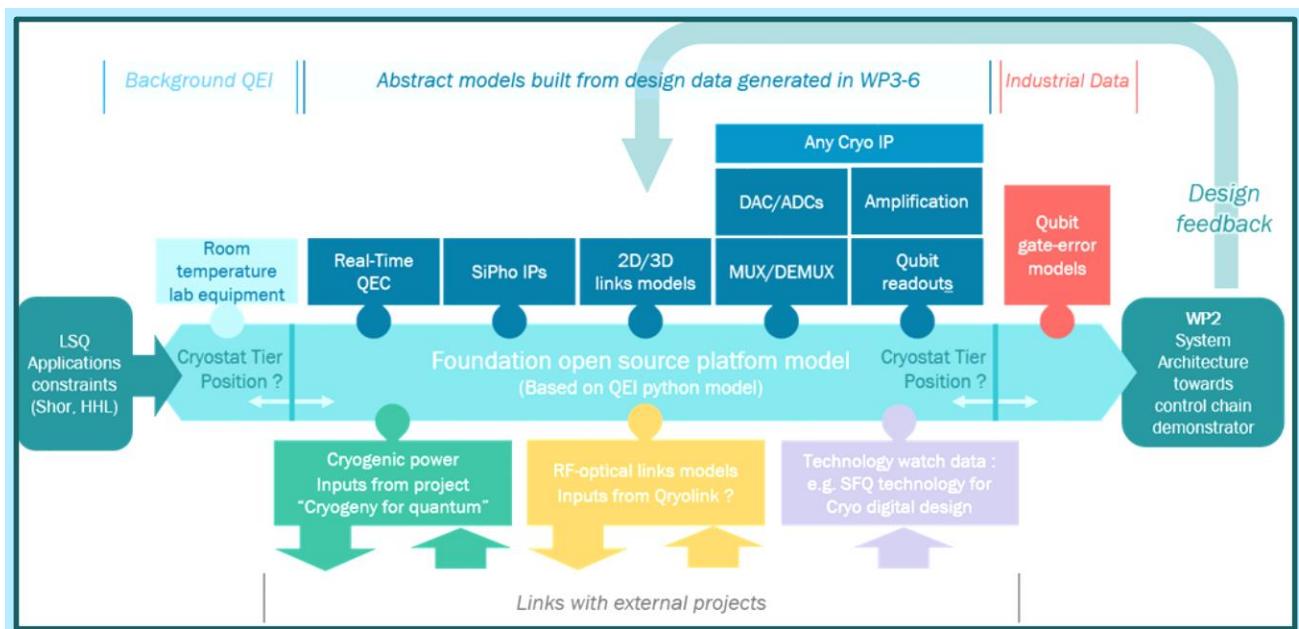


Figure 15 - System modelling approach

T1.2.1 Shared System Infrastructure

Start: M0 End: M72 Lead: CEA

Contributors: CNRS, CEA, Siemens

Description:

The goal of this task is to define an infrastructure for system modelling of the control chain that is able to encompass every IPs constraints and requirements and will therefore help system architect understand how each component can impact the system as a whole. To reach this objective, experts from different backgrounds will first be gathered to define the adapted data structure of the models. CNRS will bring its expertise in superconducting qubits control modelling, associated with a first python codebase used in <http://dx.doi.org/10.48550/arXiv.2209.05469>. CEA will bring its expertise in ESL simulation based on SystemC and FMI simulation as well as MBSE (Model-Based System Engineering). Siemens will bring its expertise in building holistic digital twins and tools like Veloce System Interconnect enabling multi-domain, multi-fidelity system simulation.

Involved personal will lead interviews from every stakeholder in the control chain to reach the definition of an infrastructure specification compatible with every element of the system and in capacity to assess their overall impact. Analytical performance models are envisioned whenever applicable, but simulation that is more complex may prove necessary for some components, or even co-simulation with existing domain specific tools.

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Then efforts will be spent in implementing the specified framework infrastructure, including components templates (to be populated by experts in T1.2.2). Open-source opportunities for the infrastructure will be investigated from day one to allow for adoption of a broader maintenance community. Additionally, automated analysis services will be added to help architecture decision in WP2-Architecture. After a strong initial development phase up to M42, the task will focus on evolving maintenance required by the project

Deliverables (due month/lead):

- D1.2.1.1 Specification of the system infrastructure and template components (M8)
- D1.2.1.2 Reference infrastructure implementation (M24)
- D1.2.1.3 Report on analysis services (M36)
- D1.2.1.4 Report on infrastructure maintenance updates (M72)

T1.2.2 Key Component models

Start: M12	End: M60	Lead: CNRS
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Contributors: CEA, CNRS

Description:

This goal of this task is to create models for each components of the control chain. IPs developed within the project in WP3-6 will be modelled by the teams, directly involved in their developments, and may be refined as the project progresses: CEA will provide CryoCMOS IP models; CNRS will provide TWPA models; INRIA together with CEA and CNRS will build QEC models; CEA and CRNS will provide optical links models; and CEA will provide 3D links models. CNRS, which is implicated in other SNAQ projects such as Qryolink will be in charge of building models from external data (HEMTs, RF links ..). Inria/Quantic will provide hardware constraints and descriptions of the informational flow extracted from stabilized bosonic qubits (noise-biased Schrödinger cat qubit and unbiased GKP qubits).

Additional qubits data is expected to be provided from industrial actors with in-kind contributions. Due to their critical intelligence value, qubit models may remain proprietary to their developers. To cope with this risk, approximate qubit models (representative of realistic performance bounds) may be used for architecture analysis in WP2-Architecture.

This task will seek to develop symmetric cooperation with the SNAQ Metriqs project that is expected to provide characterization of quantum components, so as to (1) share invaluable data for system architects that characterization shall address, and (2) gather additional components data for modelling.

Deliverables (due month/lead):

- D1.2.2.1 Report on initial component models (M36)
- D1.2.2.2 Report on refined component models (M60)

T1.2.3 Applicative constraints

Start: M0	End: M36	Lead: CEA
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Contributors: CEA, INRIA

Description:

As for classical architecture, to correctly size quantum systems, one needs to consider target applicative constraints. In order to achieve that, the task will consider application use-cases at different scales to pave the way to industrialization.

CEA will provide application constraints by means of cryptanalysis, including declinations of Shor's algorithms for hacking various classical cryptosystems. A co-design approach will be pursued aiming to find shortcuts in the implementation of cryptanalysis algorithms from hardware specificities, to identify resource efficient implementations of quantum computers but also to offer a guidance for the whole control chain

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Inria/QuaCS will provide application constraints in the field of numerical simulation with algorithms dedicated to resolution of systems of equations. A first candidate is the HHL algorithm and its refinements, but other algorithms for working with EDP will also be considered.

These various applicative constraints, together with QEC properties coming from WP4-QEC will be central to the overall control architecture scaling analyses performed in WP2-Architecture.

Deliverables (due month/lead):

D1.2.3.1 Report on resources, runtime and constraints for performing cryptanalysis with distributed quantum computations (M12)

D1.2.3.2 Report on the generic toolbox for cryptanalysis constraints at various scales (M36)

D1.2.3.3 Report on algorithms for numerical simulation at various scales (M36)

T1.3 QPU functional models (to be started in second project phase)

Start: M48	End:M72	Lead: CEA
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Contributors: CEA, INRIA (TBC)

Description:

In order to validate that the control chain architecture will be able to connect to existing HPC architecture, task T1.3 would build a functional view of the quantum system encompassing QEC hardware. The intent is to represent the programming interface offered by the QEC hardware and potential room temperature equipment.

This model will then be used to define additional software steps to convert operations from the “Quantum HW Specification Standard” defined by Atos in the HQI project and the interfaces made available by the QEC hardware(s). This shall allow to project performances for real-case full stack programming of error corrected QPUs

Deliverables (due month/lead):

D1.3.1 Programmer’s view model of the QEC hardware (M60)

D1.3.2 Report on software passes for QEC Hardware code generation (M72)

4.6. WP2 Architecture specification towards integrated demonstrator

4.6.1. Work package objectives

This work package will centralize all decisions regarding system design of an integrated control chain. It is in charge of gathering intelligence from the system modelling in WP1-System model to identify enabling technologies for the scalability of the control, and take design decisions for the final project demonstrator. To achieve this goal the work package will gather expertise from many entities, including the ones from industrial quantum players joining the program. The work package is expected to get a growing importance as the project moves forward, starting with a prescriptive role for enabling technologies, to initial system specification and finally to reach final demonstrator supervision.

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4.6.2. Partners Role

Entity	Role
CEA	Work Package Leader With its expertise and background in complex integrated architecture (e.g. EPI processor architecture) and system design (e.g. Renault FACE industrial project), CEA will lead the architecture specification work package, and contribute to it with its knowledge in WP3-6 technologies.
CNRS	At the root of the Quantum energy initiative, CNRS will focus its work on evaluating the energetic implication of the scaling of the control chain depending on used technologies and QEC schemes.
Inria	With a central program role on the definition of QEC schemes, Inria will mainly participate in WP2-Architecture to get better grips at how hardware constraints (topology, control multiplexing...) can affect applicability of proposed QEC schemes solutions.
Solid-state qubit vendors: A&B, C12, Quandela, Siquance	Upon joining the program, QPU vendors will leverage the system tools analysis from WP1-System model to devise their own scalability roadmap, and will help define needed system demonstrator needs to derisk their scalability roadmap.
SilentWaves	Upon joining the program, SilentWaves will contribute to specify co-integration strategy applicable to their amplification solutions

4.6.3. Detailed work description

T2.1 Expression of requirements for developed technologies		
Start: M1	End: M6	Lead: CEA
Contributors: CEA, CNRS, INRIA		
Description: Based on prior knowledge acquired on namely (1) the state-of-the art of quantum control electronics, (2) high-performance computing electronics such as high-speed IOs for data communications, (3) energetic issues stemming from quantum noise and cryogenic power and (4) quantum error correction, CEA and CNRS will define the target figure of merit for technologies investigated by the project in WP3-6.		
Deliverables (due month/lead): D2.1 Report on target technology figure of merit (M6)		
T2.2 Expression of requirements for system model analyses		
Start: M1	End: M18	Lead: CEA
Contributors: All partners		
Description: In order to ensure the system model will be in capacity to address questions raised in defining the system architecture, T2.2 will specify the expected exploration capacities required from the toolset developed in WP1-System model.		
Deliverables (due month/lead): D2.2.1 First Requirements for system modelling analysis (M6) D2.2.2 Requirements for system modelling analyses (M18)		
T2.3 Evaluation of scalability strategies for performance and energy efficiency		
Start: M25	End: M42	Lead: CEA

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Contributors: CEA, CNRS

Description:

Starting with the availability of first system models the task will evaluate different scalability strategies for the control chain of various qubits technologies from a pure performance driven perspective (CEA) and from an energetic one (CNRS). Leveraging the holistic system model build in WP1-System model, will enable system-scale optimizations for the control chain. A refined evaluation will be performed based on updated models available later in the project. Scalability scenario may encompass *what-if* analysis considering the advent of quantum technologies outside of the project scope, such as quantum communications or quantum memories.

Deliverables (due month/lead):

D2.3.1 Partial report on scalability strategies (M36)

D2.3.2 Final report on scalability strategies (M42)

T2.4 Specification for the control chain demonstrator

Start: M37

End: M42

Lead: CEA

Contributors: All partners

Description:

Based on partial scalability evaluations from T2.3, the task will focus on defining concrete specifications for a demonstrator in capacity to demonstrate the scaling potential of involved technologies. In particular, structuring choices such as I/O methods need to be made early enough in the project to allow for their development. As scalability routes may differ from one qubit technology to another, the demonstrator may require a certain level of versatility that will need to be put in adequacy with available design resources.

Deliverables (due month/lead):

D2.4 Specification report for the control chain demonstrator (M42)

T2.5 Control chain demonstrator supervision and integration

Start: M43

End: M72

Lead: CEA

Contributors: CEA

Description:

This task will be in charge of ensuring good cooperation between developments conducted in each WP3-6. A particular area of focus will lie in the definition of interfaces at all scales, be it 3D integration, packaging I/O, or board design, cryostat I/O, or QEC syndrome decoding accelerator I/Os and protocols. In order to achieve that, the task will centralize refined specifications of each subcomponent and keep a reference specification up to date with required adjustments for each subcomponent. In particular, to allow the demonstrator to be plugged with actual qubits that are not designed in the project, interfaces towards qubits will be defined with participating industrial players, to ensure the capacity to implement QPUs through associated projects.

Deliverables (due month/lead):

D2.5 Performance report on the demonstrator (M72)

T2.6 Specifications for future generation of scalable control chain

Start: M60

End: M72

Lead: CEA

Contributors: CEA, CNRS

Description:

The goal of this task is to prepare a second generation for the control chain demonstration based on results accumulated in the project. Having such specifications as starting point for a follow-up Nanoelec program would avoid work interruptions that could lead to loss of momentum. The second generation would prepare

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industrialization by demonstrating control at larger scale; it will also likely extend the scope of the program to scale-out strategies depending on results from PEPR actions.

Deliverables (due month/lead):

D2.6 Specifications for potential LSQ program phase 2 (M72)

4.7. WP3 Integrated Photonics

4.7.1. Work package objectives

WP3-Integrated Photonics will study how integrated photonics can be leveraged to allow increased scalability of the communication links between the cryostated qubits and the likely more power consuming error estimation hardware developed in WP4-QEC. Indeed, optical fibers offer higher bandwidth than RF cables and also provide good thermal isolation. The challenge for WP3-Integrated Photonics is thus to ensure proper functionality of integrated photonics in cryogenic conditions while keeping a constrained power dissipation budget and good Signal-Noise Ratio.

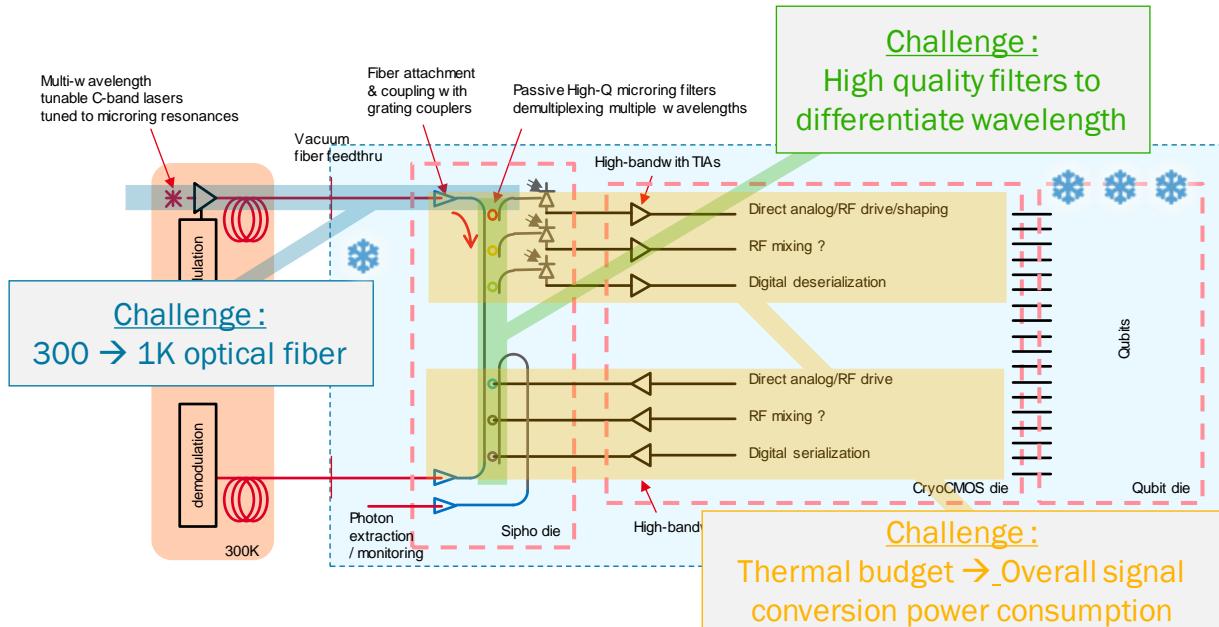


Figure 16 - Proposed solution for optical communication at cryo temperatures

WP3-Integrated Photonics will begin with an exploration phase to identify which existing integrated photonics do work in cryo-conditions, and which of them are the most promising to reach the expected performances. Then design of integrated photonics will start based on validated components, while design of advanced, high performances, key components will be investigated. As a starting point, integrated photonics use will be evaluated for both analog and digital output to provide data for system modelling in WP1-System model, while its use for ingress and the final subsystem design specification for egress (analog or digital) will be dependent on system architecture decision conducted in WP2-Architecture. Considered integrated photonics technologies may be based on either glass or SOI substrates or encompass both using 3D integration.

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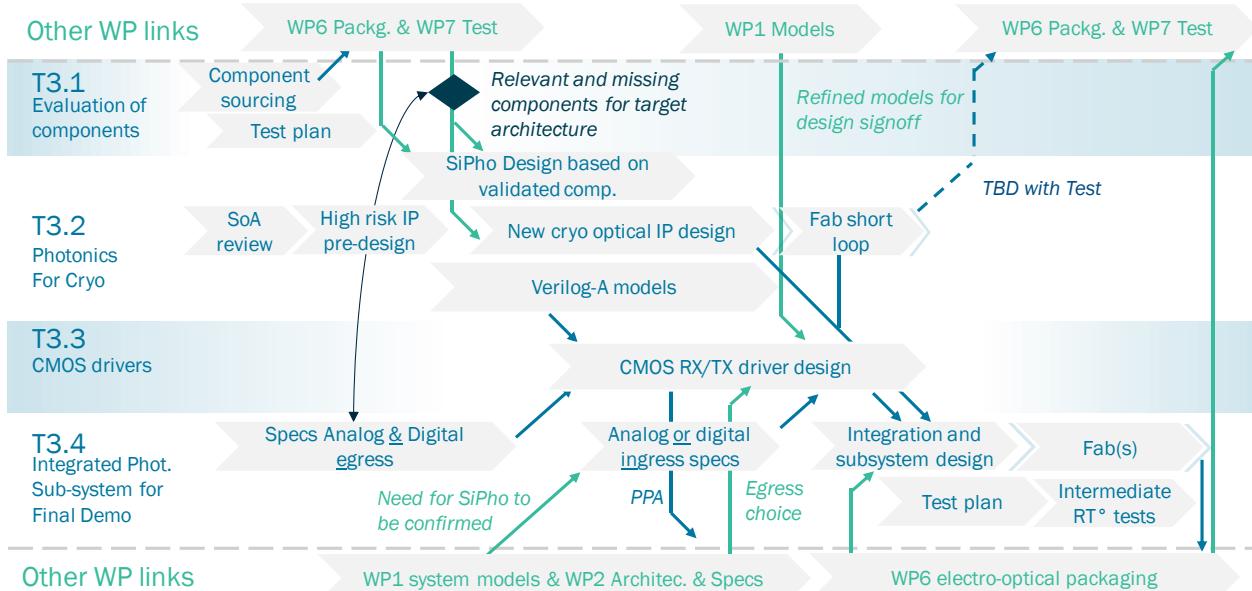
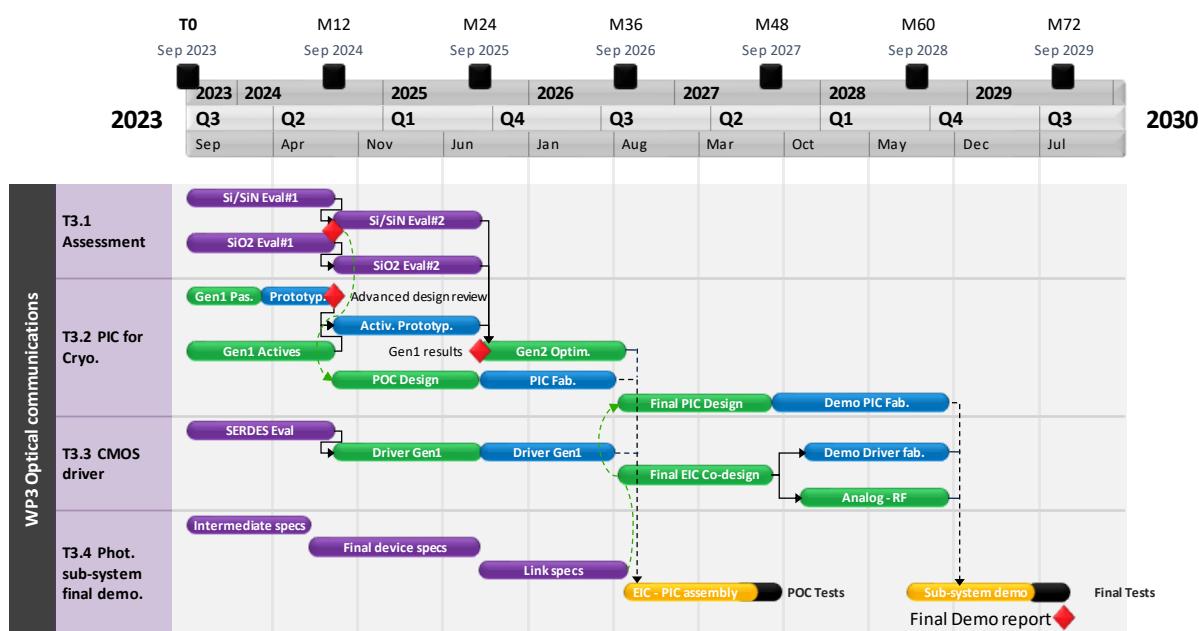


Figure 17 - WP3 PERT Chart showing intra & inter WP synergies

Another key aspect is the co-design and the assembly of the CMOS driver providing the appropriate bandwidth, voltage-swing and power supply at cryo conditions, and while keeping a limited heat dissipation. Thus, photonic and electronic IC packaging and 3D integration will be investigated, in relationship with WP6-3D&packaging. Discrete components will be evaluated at first in cryo conditions inside this WP and using the tools available/under development in WP7-Cryogenic tests. A proof-of-concept cryo-compatible transceiver will be designed after this assessment, while the final demonstrator is likely to require advanced photonics devices in order to reach the overall specifications (mostly regarding speed, heat dissipation, and compliance with drivers).



WP3 Gantt chart

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4.7.2. Partners Role

Entity	Role
CNRS	CNRS has a strong expertise in integrated photonics design. Contributions could encompass specific integrated photonics device design as well as provide characterization environments in cryo-conditions.
CEA	WP leader. As an RTO, CEA has developed a strong expertise in integrated photonics architecture design, more specifically using Silicon-Photonics processes. It will lead the architecture definition of the photonic integrated circuits necessary to provide a scalable communication between cryostat and room temperature
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design teams with its design tools and expertise (e.g. Lightsuite Photonic Compiler).
ST	ST would support actions by providing SiPho device samples to be tested in cryo conditions and will also evaluate applicability of newly developed SiPho designs to other application domains
UGA-IMEP-LAHC	UGA-IMEP-Lahc has a strong expertise in integrated photonics design, especially over glass. Contributions could encompass specific passive integrated photonics device design as well as provide characterization environments in cryo-conditions.

4.7.3. Detailed work description

T3.1 Evaluation of existing components		
Start: M1	End: M24	Lead: C2N
Contributors: CNRS-C2N, UGA-IMEP-LAHC, CEA		
<p>Description :</p> <p>This task is devoted to the assessment of existing photonics passive and active devices in cryogenic environment, in relationship with WP6-3D & Packaging and WP7-Cryogenic tests. CEA and CNRS will be mainly focused on Silicon-based and Silicon Nitride-based components, while UGA-IMEP-LAHC will be centered on Glass-based structures. For passive devices, insertion losses, spectral responses, and propagation losses will be evaluated, while for actives devices, speed, energy consumption, thermal dissipation, and compliance with Driver voltage limitation will be assessed, offering early inputs for T3.2.</p> <p>In this task, CNRS proposes to participate to the determination of the limit of Si and SiN photonics devices in Cryo environment. That includes (i) the determination of the limit of plasma dispersion (electro-optics effect currently used in Si) effect as a function of the temperature, (ii) the determination of the temperature limit of germanium waveguide detectors and avalanche photodetectors in terms of speed and responsivity and noise and the validation of passive photonic structures.</p> <p>UGA-IMEP-LaHC will contribute by providing its expertise and facilities in evaluating the performances of existing passive devices made on glass and pigtailed to optical fibers operated at cryogenic temperatures. It will provide with low-loss waveguides (<0.1 dB/cm at ambient temperature) connected with optical fibers (insertion losses < 2dB) and will evaluate the potential loss of transmission quality when the devices is brought to cryogenic temperatures (~4K). Cycled measurements to evaluate the aging of the fiber-waveguide connection could be carried-out if needed thanks to our new cryogenic bench test that is operating in a close-loop configuration. Once the connection between the waveguides and the fiber is validated, the behavior of wavelength multiplexing and de-multiplexing functions (typically AWG) will be performed in order to document the expected shift of their spectral response when cooled down from room temperature to cryogenic ones. During this assessment task, we could also perform measurements on photodiodes at the wafer layer (top illumination) thanks to the microwave</p>		

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and electric probes that complete the optical line of our cryogenic bench. Si-waveguides based functions like high-speed modulators or grating coupler-based devices could eventually be tested on our bench but it would require some developments.

In this task, CEA will provided passive and active devices based its 300mm SOI and 200mm SiN photonic platforms. Electro-Absorption modulator (SiGe, III-V/Silicon), or Polymer-based modulators might be added to the study, providing a first comparison with plasma dispersion-based modulators. For each device, room temperature characterization will be performed prior to the packaging and cryogenic tests. Cryo tests will be performed by other partners participating in this WP and WP7-Cryogenic tests, depending on the requirements (purely optical, electrical, DC, and RF measurements). It is worth noting that additional devices could be added in the test plan on the fly (phase change material, others...), relying on inputs from T3.2 and T3.4 that will precise further the system to circuits and devices specifications.

Deliverables (due month):

D3.1.1 Intermediate report on Si-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M12/CNRS-C2N)

D3.1.2 Intermediate report on Glass-based passive and active photonics devices assessment in Cryo conditions (M12/UGA-IMEP-LAHC)

D3.1.3 Final report on Si-based and SiN-based passive and active photonics devices assessment in Cryo conditions (M24/CNRS-CNRS-C2N)

D3.1.4 Final report on Glass-based passive and active photonics devices assessment in Cryo conditions (M24/UGA-IMEP-LAHC)

T3.2 Photonics for Cryo

Start: M1	End: M60	Lead: CEA-Leti
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Contributors: CEA, CNRS-C2N, UGA-IMEP-LAHC, Siemens EDA

Description:

This task is focalized on the design and fabrication of high-speed photonic integrated circuits operating at cryogenic temperature. While passive devices evaluated in T3.1 may require 'only' some adaptations/customizations, high performances active devices at cryo temperature appear to be more challenging, especially when considering other constraints such as energy efficiency, temperature dissipation, and low swing voltage. Thus, this task will anticipate the need for disruptive modulation and photo-detection solutions. After an in-depth state of the art review together with a device to system level analysis, high-risk designs will be proposed and evaluated. Short-loop of fabrication on small wafer format will be employed to accelerate the assessment of the new design, prior to circuit demonstrators to be manufactured on larger wafer scale (200/300mm). A relatively high level of synergy and coordination between the three other tasks of this WP will be required to ensure that the high-risk design will be validated within the appropriate timeline for the demonstrators. Two demonstrators will be planned, the first one being anticipated as a proof of concept (POC) that may not reach the full specifications, while the final demonstrator should aggregate the best developments available at the time.

The first goal is to be able to select the best candidates for high performance modulation and photo-detection, but not only taking into account the performances at cryo temperature but also the manufacturability on large wafer scale, thus minimizing the risks in term of integration when the fabrication of the demonstrators will start. CEA will participate to the state-of-the art review as well as the co-development of the PIC (Photonic Integrated Circuit) in regard with T3.3 and T3.4 related to the drivers and system integration. CEA will contribute also to prototyping of advanced devices emerging from either existing solutions assessed in T3.1 and/or disruptive approaches found during the review process (which take into account not only the performances but also manufacturing concerns as mentioned above). Depending on the technological solutions that will emerge from

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D3.2.4, CEA will lead the realization of the photonics chips for a 1st POC (simplified transceiver operating at cryo temperature) and next the photonics chips for the final demonstrator, both in direction to T3.4 (Photonics subsystem merging the PIC and its driver).

CNRS-C2N will design new silicon photonics devices adapted to cryo temperature. In particular, electro-optics effects at such a temperature require intrinsic electronic properties, e.g. Kerr and Pockels effect. CNRS-C2N, in collaboration with Leti and ST propose to study different photonic structures and exploit different effect. First DC Kerr will be considered and study in cryo environment. Such effect has already demonstrated promising results and requires a complete optimization and characterization. In parallel, CNRS-C2N propose to study Pockels based photonic devices by the hybridization of ferroelectric materials (Lithium Niobate and Barium Titanate) on silicon and silicon nitride photonics platforms. CNRS-C2N has also a strong expertise in the development of fiber couplers (grating and inverted tapers), efficient wavelength filters with high power rejection (>100dB) and passive photonic devices (waveguides, ring resonators, Mach-Zehnder interferometer....). CNRS-C2N has also all the necessary facilities to rapidly fabricate passive photonic devices using ebeam lithography to validate certain concepts before larger-scale fabrication at Leti and ST.

UGA-IMEP-LaHC contribution for this task will be to design and provide a glass-based solution for interfacing the PIC made on silicon with optical fibers. This solution could contain wavelength multiplexing and demultiplexing functions if required. UGA-IMEP-LaHC will collaborate with C2N and LETI to design and chose the most appropriate solution for this interfacing interposer, and will manufacture it before assembling it with the silicon PIC (TBC with LETI). UGA-IMEP-LaHC will rely on its state-of-the-art in-house simulation tools and its technology line dedicated to glass to perform these tasks. Depending on the determined test plan, our cryogenic bench will be part of the PIC qualification plan.

Siemens EDA will contribute to task 3.2 actions by providing access to its available industrial design tools (such as S-edit, L-edit, and LightSuite) and may allocate resources to support research and development work that would be performed when it is relevant.

Deliverables (due month/lead):

- D3.2.1 Design of passive photonics structures (fiber couplers and filters) (M9/UGA-IMEP);
- D3.2.2 Design of DC Kerr & hybrid Pockels-based active devices (M12/CNRS-C2N);
- D3.2.3 Review of high performance active devices solutions considering integration challenges and updated system specifications (M12/CEA);
- D3.2.4 Experimental results of the first run of photonic passive & active devices (M24/CNRS-C2N);
- D3.2.5 Optimized structures: electro-optics devices and passive devices) (M36/CNRS-C2N)
- D3.2.6 Delivery of 1st Photonic IC for preliminary POC (M42/CEA)
- D3.2.7 Delivery of 2nd Photonic IC for final Demo (M60/CEA)

T3.3 CMOS driver

Start: M1	End: M60	Lead: CEA-List
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Contributors: CEA-List, Siemens EDA

Description :

This task aims to design the appropriate CMOS drivers for the selected active photonic devices (modulation, demodulation). Considering a diversity of potential candidate physical phenomena used for these photonic devices, the task will be phased in steps from generic functions to co-designed electronics in interaction with the maturation of the photonic devices.

This task will have a high level of interactions with T3.2 and T3.4. It will start with device-independent functions, such as high-speed serializer and deserializer, to focus then on preliminary driver design with voltage or current modulation, with full-swing or low-swing signaling. Once the milestone for photonic device selection is reached, the next step is to specialize the drivers and to integrate all functions. Based on the milestone/deliverable D3.2.4

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regarding the evaluation of the first generation of the photonics components for Cryo, a first simplified CMOS driver may be designed in order to qualify the photonic and electronic IC together at cryogenic temperature with reduced specifications as a proof of concept. Alternatively, external driver will be used, prior to the final driver design work that will be conducted for the Co-design of the demonstrator expected to start M48. The fabrication of the drivers, mostly through foundry runs, and subsequent post-processing is included in this task.

In the longer perspective, analog/RF signaling over photonic links will be studied, and tentative drivers will be designed.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

Deliverables (due month/lead):

- D3.3.1 Generic Serdes characterization at cryogenic temperatures (M12)
- D3.3.2 Preliminary driver design with tentative device specs (current/voltage, swing amplitude & bandwidth) (M24)
- D3.3.3 Co-designed CMOS drivers for the selected photonic devices (M48)
- D3.3.4 Driver adaptation for analog/RF signaling (M60)

T3.4 Integrated photonic sub-system for final demonstrator

Start: M1	End: M72	Lead: CEA-list
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Contributors: CEA, Siemens EDA

Description :

This task covers the cryo-compatible transceivers sub-system specifications, from the architecture to the device. One of the main challenge will be adjust the sub-system specification with the inputs from T3.1 on the photonics device assessment, together with the inputs of the other WP that will provide insights on the total power dissipation acceptance, the number of I/Os, or other constraints on the system (density/footprint, packaging, materials...).

In this task, In the first years of the program, CEA LIST will provide system-level specification for ingress and egress needs through an optical cryo-photonic link, and iterate with T3.1/T3.2 to refine requirements in terms of bandwidth, integration, power consumption, interfaces between CMOS and photonics.

In a second phase of the program, CEA-List will coordinate the integration of the selected photonic devices and drivers in an electro-optical link architecture will be carried out , with potential integration on an optical interposer. This task will involve the interactions with WP6-3D&Packaging for the EIC – PIC assembly/packaging/3D integration and WP7-Cryogenic tests for the Cryogenic equipment for both the 1st POC and the Final demonstration.

Here, for the POC expected at M48 and for the Final demo expected at M72, the Photonic IC fabricated in T3.2 and the associated CMOS Drivers designed in T3.3 and fabricated in WP5-Cryo electronic must be assembled together through Packaging/3D integration in WP6-3D&Packaging (depending on the specs). Subsequently, the transceivers performances will be assessed by CEA-leti in this task at Cryo temperature by coupling the equipment from WP7-Cryogenic tests with high-speed communication setup corresponding to the specifications at both device and system levels.

Siemens EDA will contribute to task 3.3 actions by providing access to the same tools as described in T3.2, may allocate resources to support research and development work that would be performed when it is relevant.

Deliverables (due month/lead):

- D3.4.1 Intermediate report on device requirements and specifications for an optical cryo-photonic link (after preliminary reports and iterations with T3.1/T3.2 (M9)
- D3.4.2 Final report on device requirements and specifications for an optical cryo-photonic link (after preliminary reports and iterations with T3.1/T3.2) (M24)

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D3.4.3 Link architecture specifications (M36)

D3.4.4 Characterization report of integrated cryo-photonic link final demonstrator (M72)

4.8. WP4 Real-Time quantum error correction

4.8.1. Work package objectives

Quantum error correction (QEC) is key to the development of a large-scale, fault-tolerant quantum computer, achieving the full computational power of quantum computing. However, the efficacy of a QEC solution is heavily dependent on its decoder: a classical algorithm that processes the extracted error syndrome to determine appropriate corrections. Previous research essentially focused on the accuracy (i.e., error correction capability) of the decoder, mostly ignoring scalability and real-time implementation constraints (critically, the decoding must be faster than the syndrome generation rate, otherwise it will introduce an exponential time overhead – in the number of non-Clifford gates – which will hinder any quantum advantage). In this context, the ambition of WP4-QEC is to design real-time QEC solutions that scale with the number of qubits. To reach this goal, software and hardware implementations of QEC decoders will be investigated, based either on existing decoding algorithms, or under development within the PEPR project NISQ2LSQ. For each decoding algorithm, a design space exploration will be performed for parameters of interest, to identify best tradeoffs in terms of accuracy, latency, power, and scalability. Acquired knowledge will be fed back to the system modelling in WP1-System model for the complete control chain design. To ensure fast exploration, and increase the adaptability of the design to QEC evolutions, hardware implementation will leverage High-Level Synthesis tools.

4.8.2. Partners Role

Entity	Role
Inria	WP Co-leader Algorithmic Leader Expertise in QEC algorithms and compilation for quantum computing using logical gates
CEA	WP Co-leader Hardware design leader CEA will bring expertise from several teams, from QEC expertise (LETI) to hardware acceleration design (LIST) applied to error syndrome decoding and quantum circuit compilation and optimization (IPhT)
Siemens EDA	HLS tool supplier and expertise support to the hardware design teams

4.8.3. Detailed work description

T4.1 Software implementation of topological codes decoders

Start: M1 End: M18 Lead: CEA

Contributors: CEA

Description:

Topological codes (e.g., surface or color codes) are currently seen as the main and most promising approach to fault-tolerant quantum computing, for a wide range of quantum technologies. The prevalent decoding solution is based on the minimum-weight perfect matching (MWPM) algorithm, commonly used to assess the error correction thresholds of topological codes, due to its superior error correction capability (accuracy). However, its complexity scales cubically with the number of qubits, which may prevent its use in practical applications, especially for large

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scale systems. Thus, a number of alternative solutions have been proposed in the literature, including greedy or approximate versions of the MWPM decoder, renormalization group based decoding, machine learning techniques based on neural networks, or the so-called union-find decoder.

In this context, the goal of this task is to uncover bottlenecks and identify decoding solutions that lend themselves to low-complexity and high speed hardware. CEA-leti will contribute to the development and the software implementation of decoding algorithms for topological codes. Specific C/C++ coding style required for HLS will be used for the decoder implementation.

The proposed contribution will build upon existing decoding solutions, while proposing further adaptations and/or simplifications, in order to bridge the critical gap between the algorithmic solution and the latency-power-scalability constrained hardware design.

Deliverables (due month/lead):

D4.1.1 Software implementation of QEC decoders from the literature (M6)

D4.1.2 Software implementation of adapted QEC decoders with increased scalability potential (M18)

T4.2 Hardware implementation of topological codes decoders

Start: M7	End:M30	Lead: CEA
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Contributors: CEA, Siemens

Description:

CEA-list will design a hardware implementation of topological code decoders provided by T4.1. Typical hardware conception flows augmented with High Level Synthesis (HLS) brought by Siemens will be used to produce the Register Transfer Level (RTL) model implementing this algorithm. Then, exploration of the design space to find good tradeoffs between performance and complexity will be conducted by CEA-list with Siemens support. Physical synthesis for FPGA and advanced CMOS technologies will be performed to assess the interest of such an accelerator in a large scale QPU and assess power, performance and area.

Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant

Deliverables (due month/lead):

D4.2.1 Report on first naive hardware implementation of error estimator for generic topological code (M20)

D4.2.2 Report on refined hardware implementation of error estimator for generic topological code(M30)

T4.3 Software implementation of decoders from PEPR NISQ2LSQ

Start:M12	End: M36	Lead: INRIA
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Contributors: INRIA, CEA

Description:

Quantum low-density parity-check (QLDPC) codes are a generalization of topological codes. Similar to topological constructions, QLDPC codes are defined by low (constant) weight generators, which allows simple fault-tolerant syndrome extraction and logical state preparation. Moreover, the QLDPC family has been recently shown to yield good asymptotic codes, with linear minimum distance and constant rate, which augurs for practical constructions with increased error correction capacity or reduced qubit overhead. However, decoding QLDPC codes is in general a difficult problem, constituting a very active field of research, and a number of decoding solutions are currently being developed within the PEPR project NISQ2LSQ.

The goal of tasks T4.3 and T4.4 is to take the developed solutions from the algorithmic level to respectively the software and the hardware implementation stages. INRIA/QInfo will perform the implementation and benchmarking of the parallel decoders for QLDPC codes having large encoding rate and good error correction capacities, while Inria/Cosmiq will further investigate rapid decoding algorithms and provide support for their implementation. Inria/Quantic will investigate new LDPC codes designed for biased noise cat-qubits as the absence of one error

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component could significantly simplify the decoding requirements, and will also study cellular-automaton based decoders for topological codes designed for extremely biased noise qubits.

CEA-list will focus on message-passing decoding algorithms, for a class of QLDPC codes having the single-shot error correction property. Similarly to T4.1 coding style required for HLS will be used for the decoder implementation.

Deliverables (due month/lead):

D4.3 Software implementation of decoders for quantum LDPC codes and performance evaluation (M36)

T4.4 Hardware implementation of decoders from PEPR NISQ2LSQ

Start: M31	End: M54	Lead: CEA
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Contributors: CEA, INRIA Siemens

Description:

Similarly to the approach taken in T4.2, CEA-list will study in T4.4 hardware implementation of a selection of decoders from T4.3. Again, HLS will be used for early-stage exploration and then for the identification of performance-tradeoffs. Commonalities between the decoders of various codes will be studied to identify, where applicable, core IPs that could benefit from more optimization efforts. Finally physical synthesis for FPGA and advanced CMOS technologies will be performed.

Specific hardware implementation for cellular-automaton based decoders for topological codes may also be investigated by INRIA/Quantic as they may be integrated closer to the qubit using similar technologies. Siemens EDA will contribute by providing access to its available design tools, and may allocate resources to support research and development work that would be performed when it is relevant

Deliverables (due month/lead):

D4.4 RTL model of hardware implementation of specific estimator for specific codes (M60)

T4.5 Exploration of error correction tradeoffs (correction rate, latency, power, complexity)

Start: M37	End: M60	Lead: CEA
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Contributors: CEA, INRIA

Description:

Exploring the design space for efficient error correction requires to challenge its impact at all level, from the qubit topology constraints to the error decoding. Teams with complementary backgrounds will therefore conduct the exploration.

Having performed the hardware implementation of codes, CEA will focus is action on assessing the performance of decoding algorithms in terms of latency, power and resource usage (gates or mm²); as well as precision, since some codes, such as Edmond's MWPM algorithm, allow to trade latency for decoding accuracy by taking into account error locality.. As achieved precision shall be appreciated depending on the qubit properties, decoding procedure will be evaluated using Monte-Carlo simulations of error propagation for syndrome generation. Several aspects of the QPUs will be taken into account provided that input data is made available by partners developing qubit technologies (qubit connectivity, addressability and intrinsic parallelism, specific gate and qubit error models).

Inria/QInfo will study the limitations the geometry of the physical qubits imposes on the fault-tolerance memory and time overhead. In particular, the maximum encoding rate that can be obtained as well as the best error correction capacity will be determined. Additional work will focus on the efficiency of the standard algorithms for error correction: this includes runtime, latency, communication between the different parts of the processor and power consumption.

Generated data in T4.5 will be integrated in the system model in T1.2.2.

Deliverables (due month/lead):

D4.5 Report on QEC tradeoffs (M60)

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T4.6 Hardware aware compilation of universal set of logical gates

Start: M31 End: M72 Lead: INRIA

Contributors: CEA, INRIA

Description:

To exploit the benefits brought by the QEC, one must be able to perform quantum operations over logical gates composed of several physical qubits. Specific computation schemes must be sought out to do so. Task T4.6 will investigate several compilation approaches to provide efficient computing with error-corrected qubits :

(A) When using quantum error correcting block codes, encoding several logical qubits in one block, the set of fault-tolerant quantum gates accessible can be very different from standard gate sets. Indeed cases arise where one can have access to a few easy (transversal) gates acting on all logical qubits at once. For instance, in some situations, one can obtain a large circuit of CCZ or CZ on the logical level obtained from a transversal T gate on the physical level. While on the contrary being able to implement targeted single or two qubit gates within the code block is more difficult. Circumventing this often resort to using some tricks such as teleportation, code deformation or Pauli measurements all with additional auxiliary qubits needed making these gates more costly. Inria/Loria will develop compilers able to handle these constrained gate sets will allow to take advantage of the higher encoding rates of block codes without paying too much price in gate implementations.

(B) As the choice of error correcting scheme imposes strong constraints on the computational framework, possibly very distinct from the usual Clifford+T formalism, Inria/QuaCS will study various models of execution and the such as Measurement-based Computation (MBQC), Quantum Cellular Automata (QCA), and exotic gate-sets such as Clifford+Toffoli. The work conducted with the help of graphical languages such as ZX or ZH calculi could lead to the definition of transpilation or code optimization strategies.

(C) As magic state distillation is one of the most resource-consuming primitives in surface code-based quantum architectures, CEA will develop a hardware-agnostic tool that will translate a logical circuit for state distillation into a sequence of physical gates. Established techniques in quantum circuit optimization will be implemented. Then, a secondary goal will be to adapt this approach to specific architectures whose properties could be shared by industrial partners joining the program.

(B) To further reduce the overhead of error correction CEA/IPhT will develop a systematic numerical method to optimize low-depth circuits working on a limited set of qubits, and will seek to exploit it to optimize stabilizer measurements for different codes, and assess the impact on their correction thresholds.

Deliverables (due month/lead):

D4.6 Compilation flow for error correction (M72)

T4.7 Final Demonstrator

Start: M49 End: M72 Lead CEA

Contributors : CEA, INRIA

Description :

Concerning the final project demonstrator, options for the QEC contributions are very open at this stage. Indeed, it is yet to be confirmed that large enough qubit resources could be developed by industrial players to allow for their integration in complementary projects leveraging the final LSQ demonstrator. In addition, works conducted in T4.2 and T4.3 may conclude on the need for ASIC implementation of decoders, which is not in the scope of the project to date. Consequently, the practical validation of an error correction loop may be out of reach of the project.

Still, the final demonstrator shall seek to be able to prove correct interoperability between all elements of the control chain. Hence, in a pessimistic scenario, this task will focus on the definition, and implementation of interfaces to the remainder of the control chain for future QEC integration. In an optimistic scenario, the task will aim to provide inclusion of FPGA decoders and practical validation of QEC loop.

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Deliverables (due month/lead):

D4.7 Demonstration for quantum error correction (M72)

4.9. WP5 Cryogenic electronic

4.9.1. Work package objectives

Solid-state circuits operating at cryogenic temperature are more and more critical to address the challenges relating to quantum computing applications. Indeed, to perform operations on quantum bits (qubits) like control and read out, requires classical electronic controllers. As soon as quantum processors become more complex, classical electronic control approaches, requiring multiple RF and DC cables per qubit and each connected to room-temperature instruments, are no longer a sustainable way.

A promising approach consists in considering the integration of read-out and control circuitry in standard CMOS technologies operating at cryogenic temperatures. In such a way, significant form factor is reachable, enabling more qubit control complexity while limiting power consumption and being a cost-effective solution.

Beside the CMOS circuitry, solid-state qubits read-out and control need several superconducting electronic devices like specific very low power and very low noise amplifiers (for known as Traveling-Wave Parametric Amplifiers, TWPA).

This work package aims at developing CMOS model & design-blocks in cryogenic conditions, at evaluating and maturing electronic devices technologies, and at developing a superconducting quantum circuit industrial sector to enable a French and European robust supply chain.

CMOS circuits and electronic components developed in this WP will be integrated in the demonstrator.

4.9.2. Partners Role

Entity	Role
ST MICROELECTRONICS	Work Package Leader Will give access to the FD-SOI technology to update the 28FD PDK for 4K (and possibly 77K) applications.
CEA	Will characterize devices, develop models, and implement designs for cryogenic electronics. Will evaluate electronics devices.
UGA-IMEP-Lahp	Will characterize devices (noise and 77K), contribute to models development and to self-heating study.
Siemens EDA	As a major player in EDA and system simulation, Siemens will support design and modeling work in T5.2 and T5.4 tasks.
CNRS-Néel	Will contribute to TWPA developments
UGA-TIMA	Will contribute to design model evaluations

4.9.3. Detailed work description

T 5.1 Devices characterizations at 4K (and 77K sampling) for PDK Add-On

Description:

This task is very dependent of characterization means availabilities, capabilities and capacities (WP7-Cryogenic tests, T7.1 and T7.2.1). The tasks can start with manual and none statistical characterizations but the full task execution supposes strong amplification and industrialization of characterization means.

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T 5.1.1 FEOL devices characterization at 4K (and 77K sampling)

Start: M1 End: M36 Lead: CEA

Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP

Description:

To enable circuits 28nm FD-SOI circuits design at cryogenic temperatures especially at 4K, several FEOL devices such as NMOS and PMOS transistors, (if possible according to WP7-Cryogenic tests, resistors, decoupling capacitors, junction diodes) must be modeled. To do so, those devices must first be characterized in various domains, including DC, AC and noise (LFN for CEA / RTN for UGA-IMEP). Then, to address RF applications, extra HF characterization based on S-parameter and possibly Noise Figure (NF) measurements may be needed, coming with their own challenges in terms of calibration procedure (either on-wafer or based on external substrate standards) and linear (small-signal) device operation at cryogenic temperatures 4K (and 77K sampling).

According to the previous results and output of WP7-Cryogenic tests T7.2.1, it could be interesting to investigate the statistical approach and measurement strategies in the framework of the pre-industrialization of cryogenic PDK.

Perspective Y4 to Y6: next FD-SOI generation node characterizations at cryogenic temperature.

Perspective Y6: High frequency noise measurement at cryogenic temperature.

Deliverables (due month/lead):

- D5.1.1.1 Report on devices characterizations (M12)
- D5.1.1.2 Report on devices characterizations (M24)
- D5.1.1.3 Report on devices characterizations (M36)

T 5.1.2 BEOL interconnect and RF passives models

Start: M1 End: M36 Lead: CEA

Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP

Description:

Qubits control and read-out require the generation and acquisition of specific RF signals, leading to the need of several RF blocks that could be assimilated as wireless RF transceiver.

To enable electromagnetic RF passives modeling and dimensioning at cryogenic temperatures:

- The accurate extraction of BEOL physical values
- In addition to low frequency physical parameters, a validation of the above-calibrated stack will be mandatory versus frequency up to 30 GHz if possible according to WP7-Cryogenic tests T7.2.1.

The technology considered for BEOL interconnect model and RF passives devices enablement will be the 28nm FDSOI node from STMicroelectronics. Cryogenic temperature of interest will be 4°K (and 77°K by sampling).

Perspective Y4 to Y6: next FD-SOI generation node characterizations at cryogenic temperature.

Deliverables (due month/lead):

- D5.1.2.1 Report on BEOL and RF characterizations (M12)
- D5.1.2.2 Report on BEOL and RF characterizations (M24)
- D5.1.2.3 Report on BEOL and RF characterizations and passive RF model (M36)

T 5.1.3 Reliability tests

Start: M1 End: M36 Lead: CEA

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Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP

Description:

The specific simulation models for the Cryo modelling is planned to be available using a PDK Add On on the existing PDK release. This will require cryogenic environment reliability tests and collection of reliability data. The set-up of wafer level tests at cryogenic temperatures, should allow reliability testing to cover:

- (1) gate dielectric and inter-metal dielectric breakdown
- (2) NBTI/PBTI aging and
- (3) HCl aging in "on" and "off" state mode.

Measurements protocol will first have to be adapted and applied to cryogenic environment.

Based on experimental results, existing reliability models will then be extended down to 4K.

Deliverables (due month/lead):

- | | |
|----------|--|
| D5.1.3.1 | Report on measurement protocols (M12) |
| D5.1.3.2 | Report on aging characterization results (M36) |

T5.2 Compact model developments for FD-SOI transistors and diode at cryogenic temperatures

Start: M1	End: M72	Lead: CEA
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Contributors: CEA / ST MICROELECTRONICS / UGA-IMEP / SIEMENS EDA

Description:

The first year will be dedicated to the improvement of the core's model. Indeed, at cryogenic temperatures several effects appear such as the observed double kink effect on the drain current in inversion regime and a specific linear-saturation transition. In addition, a first model library containing NMOS and PMOS transistors models in typical case will be implemented in PDK environment. These models will reproduce DC and CV characteristics.

The low frequency noise (LFN) modeling and the substrate modeling will be done in the second year. An update of the model library will use the results of these last works. In parallel, a dedicated parameter extraction flow will be optimized for cryogenic temperatures.

During the third year, new MOSFET models for RF applications and models for diodes will be developed always for typical case. They will be implemented in the PDK. The MOSFET model will include the effect of multi-finger layout.

The variability modeling will be done during the fourth year, depending on data availability (WP7-Cryogenic tests industrialization). The goal will be to update the model library by introducing corners and Monté Carlo simulation capabilities.

The 2 last years will be focused on the implementation of reliability models in PDK and several updates of model library by introducing the best experimental data. Finally, during the last year of this project, high frequency noise (HFN) modeling will be covered to improve the RF MOSFET models.

Siemens EDA, will contribute to the actions by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre...) and needed support.

Deliverables (due month/lead):

- | | |
|--------|--|
| D5.2.1 | Report on MOSFET model developments at cryo temperature and validation using experimental data (based on DC-CV present silicon data) (M12) |
| D5.2.2 | Report on MOSFET modeling for RF applications at cryo temperature and validation using experimental data (M36) |
| D5.2.3 | Report on variability modeling at cryo temperature including RF aspect (M48) |
| D5.2.4 | Report on model libraries update and HFN modeling (M72) |

T5.3 First 28FD-SOI PDK 4K (and 77K) add-on implementations

Start: M1	End: M36	Lead: ST MICROELECTRONICS
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Contributors: ST MICROLELECTRONICS

Description:

The specific simulation models for the Cryo modelling is planned to be available using a PDK Add On to the existing 28FD-SOI PDK release. This will require the development of cryogenic models with the constraints of fitting to the PDK model interfaces. This will ease the development and ensure the alignment with the standard PDK for designer community. The Focus will be done on 4K model encapsulations (77K should be an extrapolation and option; not be consider as target for this study) compliant with the process and tools flow in industrial environment.

Perspective year 4 to year 6: new FD-SOI PDK add-on with variabilities.

Deliverables (due month/lead):

D5.3.1 Report on PDK add-on (M36)

T5.4 Cryo CMOS design

In this program, following the analysis performed in WP2-Architecture, CEA will specify and design generic integrated functions for scalability and dynamic control and read-out and exploring FD-SOI capabilities in cryogenic interface electronic for large scale quantum computing.

Because design at cryogenic temperature is not yet possible with appropriate process design kit, CEA will work the methodology to accomplish a valuable design process in the task T5.4.1. In the meantime, UGA-TIMA propose to work on design modeling.

Task T5.4.2 will aim at designing control, readout and digital communication functions with, if possible, 3 loops of learning.

On both tasks, Siemens EDA, will contribute by providing access to its available industrial design tools (such as Eldo, Symphony, Calibre...) and needed support.

T 5.4.1 Cryo CMOS design methodology and PDK evaluation 28nm

Start: M1

End: M72

Lead: CEA

Contributors: CEA, Siemens EDA, UGA-TIMA

Description:

Design oriented models allow simple but efficient analytical design method based on gm/ID or IC parameters. These models are based on charge modeling and use a very small set of parameters (between 3 to 7). Recent works show how such models are well suited to advanced nodes and to low and weak inversion regime, where region-based models are limited. In addition, these works show that non-linearities or bandwidth limitation can be captured. The model parameters can be extracted based on few DC measurements which are accessible in cryogenic frameworks.

In this context, UGA-TIMA propose three research lines:

- Using the models already developed, UGA-TIMA propose to investigate how these models are suited to cryogenic devices and which parameters are required to capture the MOS behavior in cryogenic environment.
- Based on a design-oriented model and a set of extracted parameters for MOS transistors in cryogenic environment, design methods will be investigated for readout devices.
- The issue of testing cryogenic devices can be investigated through the correlation that could exist between the model parameters at cryogenic temperature and room temperature. Testing methods could be investigate based on this approach allowing the screening out of devices at higher temperatures leaving only good candidates for cryogenic temperatures.

Design learning (CEA): because design at cryogenic temperature is not yet possible with appropriate process design kit, this task is focused on the methodology to accomplish a valuable design process. The objectives are to set up a properasic design and tests flow, based on partial cryogenic PDK

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to design cryogenic benchmark circuits, analog and digital (e.g. amplifier and integrated logic characterization circuits for flip-flop and combinational gates)

to benchmark and conclude on design rules and test practices thanks to characterizations results.

First year will be devoted on designing cryogenic test chip analog and digital: schematics design based on gm/id approach (tentative models), simulations at room temperature and approximate projection to cryogenic results, tape out preparation.

Depending on process cycle time, second year will deal with test chip characterizations, retrofit analysis, methodology refinement, and benchmarking of available cryogenic compact models based on circuit simulation vs circuit characterization. Optimized benchmark circuits could be proposed if necessary, depending on results and models development.

During the following years, CEA will continue the evaluations of the PDK add-on upgrades from WP5-Cryo electronic T5.3 through designs and characterizations loops.

Deliverables (due month/lead):

D.5.4.1.1 Report on benchmark test chip design (M12)

D.5.4.1.2 Report on benchmark test chip characterization (M30)

D.5.4.1.3 Report on retrofit analysis, methodology refinement, and benchmarking (M36)

D.5.4.1.4 Second report on retrofit analysis, methodology refinement, and benchmarking (M54)

D.5.4.1.5 Final report on retrofit analysis, methodology refinement, and benchmarking (M72)

T 5.4.2 Generic design for demonstrator: Qubit control and readout and digital control, processing and communication functions.

Start: M1 End: M72 Lead: CEA

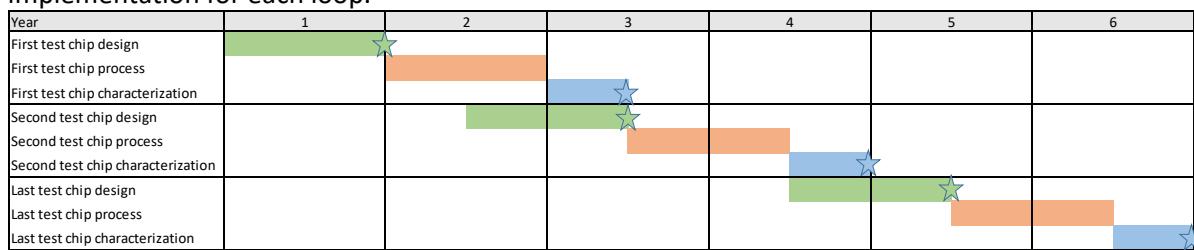
Contributors: CEA, Siemens EDA

Description:

This task aims at designing ultralow power consumption, Qubit control and readout functions (IP targeted could be: CMOS-based dynamic digital-to-analog converter, analog buffers, high-speed mux and demux, CMOS-based amplifiers and analog-to-digital converter for qubits readout, biasing circuits and oscillators) as well as digital functions for communication interfaces.

The task goes from blocks architecture study to design, and test and characterizations at cryogenic temperature. Different test chips are planned to be fabricated, and some will be designed to be embedded in 3D and supra demonstrators of WP3-Integrated Photonics.

During the 6 years of the program, CEA aims at performing 3 loops of design learning with new functions implementation for each loop.



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Deliverables (due month/lead):

- D5.4.2.1 Report on demo1 chip design (M12)
- D5.4.2.2 Report on demo1 chip characterization (M30)
- D5.4.2.3 Report on demo2 chip design with more functions (M30)
- D5.4.2.4 Report on demo2 chip characterization (M48)
- D5.4.2.5 Report on demo3 chip design with more functions (M54)
- D5.4.2.6 Report on demo3 chip characterization (M72)

T 5.5 Amplification devices evaluations at cryogenic temperatures

Start: M0 End: M72 Lead: CEA

Contributors: CEA, Silent Waves, STM, CNRS

Description:

The amplification chain requires parametric amplifiers (like TWPs) and LNA, specified and designed for cryogenic applications

TWPA:

High-fidelity qubit readout requires amplifiers with added noise near the quantum limit of noise. These amplifiers – called quantum-limited amplifiers – must be made of superconducting materials, either high kinetic inductance materials or Josephson junctions, to guaranty the lowest loss possible. One of the most promising architectures is the traveling-wave architecture, which either needs millimeter long high kinetic inductance strip lines or long arrays of Josephson junctions. The latter option, a Josephson-based traveling-wave amplifier (J-TWPA), allows to have near-quantum limited amplifiers with very low power consumption (less than a nanowatt). This option is going to be explored during the LSQ program.

Currently, J-TWPA are being manufactured in academic-grade clean room facilities and rely on fabrication processes that are not scalable nor reproducible enough for the anticipated volumes of TWPA necessary for the future solid-state quantum computing architectures. The development of a CMOS-like fabrication process for reliable and reproducible way to manufacture Josephson junctions is crucial for European Sovereignty. Such process can be developed in the CEA-leti. Furthermore, this development could not only benefit the TWPA manufacturing process, but also laboratories and companies related to quantum information with superconducting circuits.

This task goes from the design of the Josephson junctions (CEA) to their characterization (CNRS-Neel), both at room temperature and at sub-kelvin temperatures (10mK). It could include the design and the characterization of short Josephson junction arrays working as resonant parametric amplifiers as a proof of concept.

Low Noise Amplifiers: current available LNA power consumption is above 20mW. The quantum needs are to reduce from one decade (around 1 mW). This task aims at evaluating ST B55x technology, understanding the limitations, and through integrated design, improving the performance.

Circulators are "must-have" cryogenic components for the most advanced quantum experiments. They are necessary to avoid the noise from the front-end low noise amplifier (LNA) to radiate onto the sample. So far the only available cryogenic circulators which use a local static magnetic field are very bulky (typ. 2x2x1cm3) and they work only at high frequency (several GHz). Recent works using CMOS technology demonstrated that circulators based on transistors can be realized. This tasks aims first at evaluating and characterizing ST CMOS technology to realize circulators. CEA then propose to go beyond the state of the art by combining the best of both worlds thanks to the complementary aspect of BiCMOS technology: using the CMOS part for the circulator and the bipolar (HBT) transistor technology for the best LNA.

Components developed in this task will be implemented in the demonstrators.

Deliverables (due month/lead):

- D5.5.1 Report on the design of the first generation of test Josephson junctions for TWPA (M6)

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D5.5.2 Report on cryogenic and room-temperature characterization of the test Josephson junctions for TWPA (M24)

D5.5.3 Report on the design of the second generation of test Josephson junctions for TWPA (M24)

D5.5.4 Report on cryogenic and room-temperature characterization of the second generation of test Josephson junctions for TWPA (M42)

D5.5.5 Report on the design of the first generation of short array resonant amplifier (M48)

D5.5.6 Report on cryogenic and room-temperature characterization of short array resonant amplifier (M72)

D5.5.7 Report on LNA characterization and development (M36)

D5.5.8 Report on CMOS circulators characterization and development (M48)

D5.5.9 Report on circulators and LNA co integration (M72)

4.10. WP6: 3D integration and packaging

4.10.1. Work package objectives

The aim of work package 6 is to validate the complete communication chain in terms of cryogenic electro-thermal behavior. As illustrated in **Erreur ! Source du renvoi introuvable.**1, the scope of the study ranges from the qubits to the outside of the cryostat. Starting from WP2-Architecture recommendations, system architecture hypotheses will be investigated regarding interconnections key technologies, parasitics and power dissipation. To achieve this goal, low

temperature characterizations of raw materials and elementary integrated modules will feed simulation and modeling. A schematic view of the work package is introduced in Figure 2. Task T6.1 will be in charge of the fabrication of test vehicles that will be packaged within T6.2 (it will also include photonics packaging issues stemming from WP3-Integrated Photonics). Experimental characterizations of these packaged test vehicles will be performed in T6.3 and the output data will be used to feed

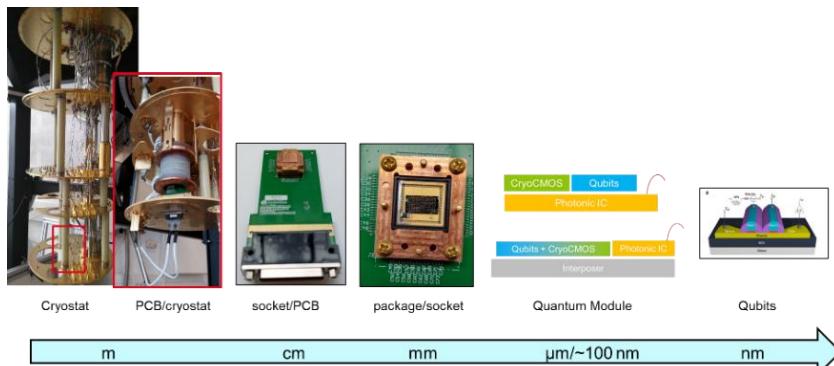


Figure 1 Scope and range of interconnections of a qubit control chain (Quantum Silicon Grenoble)

modeling and simulation task T6.4 that will also seek to define a thermal simulation methodology allowing to interoperate low-level simulations in cryogenic conditions with thermal simulation tools already qualified for standard temperature ranges. The methodology will be used to define specifications for the test vehicles of T6.1. Based on the acquired knowledge of T6.1, T6.2, T6.3 and T6.4 outputs, task T6.5 will develop 3D interconnection and packaging solutions to manage optimally heat fluxes and high-frequency signals that will propagate in the final demonstrator.

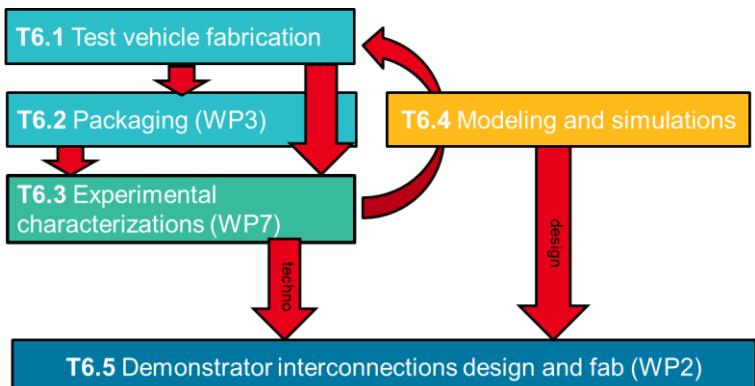


Figure 2 WP6: 3D & packaging - task chart

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4.10.2. Partners Role

Entity	Role
CEA	Work package leader With its expertise in 3D integration technology, demonstrator assembly (e.g. P. Coudrain <i>et al.</i> , ECTC (2019)) and superconductor integration (C. Thomas <i>et al.</i> , <i>Mater. Quantum. Technol.</i> , (2022)), CEA will lead the 3D and Packaging work package.
CNRS / Néel Institute	With its expertise in thermal characterization at low temperatures, CNRS will support the work of WP6 through the low temperature tests conducted in T6.3, and will therefore participate in the specification definition and design of the test vehicles in T6.1.
Siemens EDA	Siemens will provide the required support to assess their simulation tools applicability to cryogenic thermal conditions especially in T6.4.
STM	STM would support the work of WP6 by providing short loop BEOL samples for interconnection characterizations at low temperatures, as well as partial MPW wafers (with WP2-Architecture, WP3-Integrated Photonics and WP5-Cryo electronic) for specific CEA post-process for bumps and potential superconducting integration.

4.10.3. Detailed work description

T6.1 Test vehicle fabrication		
Start: M1	End: M48	Lead: CEA
Contributors: CEA, CNRS, STM		
Description: Test vehicles made from, first, raw materials deposited on blanket wafers and then, patterned materials, forming simple structures such as lines and bumps, will be fabricated to build a material and interconnection property database. During a second phase, elementary technological modules (daisy chain assemblies, superconducting multilayer stacks) will also be processed to complete the database and feed the model and simulations tools (T6.3). Process developments will involve superconducting material integration. Post-processing of Cryo electronic (WP5), Photonic IC (WP3) or Interposer wafers, will be envisioned with respect to developments conducted in the WP2-architecture.		
Deliverables (due month/lead): D6.1.1-2-3-4 Annual sample and module delivery report (M12-24-36-48/CEA)		
T6.2 Packaging of test vehicles and demonstrator		
Start: M1	End: M72	Lead: CEA
Contributors: CEA		
Description: While Printed Circuit Board (PCB) design & fabrication will be included in WP7-Cryogenic tests, the other packaging items and tasks will be addressed here. It includes the optical fiber attachment (Pig-tailing) in close collaboration with WP3-Integrated Photonics and qualification of the connectors and sockets (with PCB design inputs from WP7-Cryogenic tests). A dedicated study will be conducted on the behavior of co-packaged optics/electronics at low temperature and specifically on Ball Grid Array (BGA) or Quad Flat No lead (QFN) type of packages and their sockets, which will need engineering. Each of the investigated packaging solutions will be evaluated in terms of parasitic and thermal propagation properties.		
Deliverables (due month/lead): D6.2.1 Report on packaging strategy for test vehicles (M24/CEA) D6.2.2 Report on optical fiber attachment for low temperature operations (M36/CEA) D6.2.3 Report on demonstrator global packaging (M72/CEA)		

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T6.3 Experimental characterizations

Start: M1 End: M72 Lead: CEA

Contributors: CEA, CNRS Neel

Description:

The experimental characterizations will be divided in 3 main families as described below.

a) Mechanical and electrical characterizations. This will include the tests of different materials and technological bricks, such as 2D routing lines and 3D interconnects, to extract the following parameters: electrical resistance and capacitance @ 300K, electrical resistance at cryogenic temperatures, superconducting properties (T_c , J_c , B_c) when applicable, Coefficient of Thermal Expansion (CTE) between 300K and 77K (methods to be developed) and E (Young Modulus) @ 300K.

b) Thermal characterizations. This will comprise the experimental measurements in cryostat to extract the thermal conductivities of materials and technological bricks as well as fundamental thermal behavior characterizations for tool/model assessment of T6.4.

c) RF and photonic characterizations. The first objective will be to extract the RLCG parameters of simple structures at 7K using a dedicated VNA and cryo-prober set up. Concurrently, RF characterizations of the packaging environment will be carried out to evaluate signal bandwidth and losses through the packaging supports and sockets with WP7-Cryogenic tests. The second objective will be the elaboration and qualification of the optical test set up and measurement protocol at low temperatures to characterize photonic passive devices and then active ones.

Deliverables (due month/lead):

- D6.3.1 Report on raw material and simple interconnection database (M24/CEA)
- D6.3.2 Report on 1st optical test set up and simple photonic passive devices tests (M24/CEA)
- D6.3.3 Report on thermal measurements for fundamental thermal behavior (M36/CEA)
- D6.3.4 Report on RF & Thermal measurements of interconnections including package & socket (M48/CEA)
- D6.3.5 Report on opto-electrical tests of active devices (M48/CEA)

T6.4 Modelling and simulations

Start: M1 End: M60 Lead: Siemens

Contributors: Siemens, CEA, CNRS Neel

Description:

As thermal behavior, drastically changes at low temperatures and small scales, advanced thermal simulations will need to be carried out based on expected behavior of phonon transport. Thermal exchange at small length scale and below 4K, with specific attention to interfaces phenomenon will be explored thanks to dedicate experiments and samples design. Dedicated expert softwares such as Non-equilibrium Green's Function based FeNEGF will be exploited to this end. Adapted strategies for interoperations between low-level (FeNEGF) and system-level thermal simulation (Flotherm) tools will then be investigated in synergy between institutional and industrial actors. This shall enable the definition of a system-level thermal model methodology for cryogenic temperatures that will also be completed with a system-level RF modelling. Depending on software development and Task 6.3 test results , RF simulations will be carried out with the full control chain perspective

Deliverables (due month/lead):

- D6.4.1 Report on low level thermal simulation of individual interconnections (M24/CEA)
- D6.4.2 Report on system-level thermal model (including optical compound) (M36/Siemens)
- D6.4.3 Report on system-level RF and thermal models adapted to the architecture of control chain demonstrator (M60/CEA)

T6.5 Control Chain Demonstrator

Start: M37 End: M72 Lead: CEA

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Contributors: CEA

Description:

The first part of the task will concentrate on the delivery of an optimized design of the control chain interconnections based on thermal, RF and photonic data and models at all scales: integrated photonics, 3D integration, packaging I/O, PCB design, cryostat cables in close link with WP2-Architecture, WP3-Integrated Photonics and WP7-Cryogenic tests. The second part of the task will address the demonstrator module fabrication itself with incoming components such as photonic dies from WP3-Integrated Photonics, CryoCMOS dies or wafers from WP5-Cryo electronic and PCB from WP7-Cryogenic tests.

Deliverables (due month/lead):

D6.5.1 Report on interconnection specifications for control chain demonstrator (M46/CEA)

D6.5.2 Report on control chain demonstrator module design (M54/CEA)

D6.5.3 Report on control chain demonstrator module fabrication (M72/CEA)

4.11. WP7 Cryogenic characterization

4.11.1. Work package objectives

This work package aims at addressing the cryogenic characterization needs of the other work packages. CEA-leti, CEA-IRIG, CNRS-Neel, UGA-IMEP-Lahc already have cryogenic characterizations capabilities, but our first analysis highlights that the LSQ program will need additional testing resources since existing facilities workload is already high. In addition, the scaling naturally calls for statistical characterizations, which in turn require tools and characterization methods industrialization.

First actions in Task 7.1 will then aim at evaluating missing capabilities and capacities to address the program needs, defining the specifications, acquiring and installing needed tools and upgrades.

Besides the hardware needs, characterization methods, both at wafer level and at system level, need to be developed and improved. Task 7.2 will address these actions.

Task 7.3 will implement appropriate automation and systems to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

Finally, as required for nowadays qubit control, we expect that room temperature electronics will be needed using either RF signal sources as well as optical ones. Signal shaping solutions, adapted to the scaling, and able to interoperate with QEC may also be required for test and demonstration purposes and task 7.4 will address these points. As all work packages will need access to characterization tools, last task is the coordination and scheduling of these accesses.

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4.11.2. Partners Role

Entity	Role
CEA	Expertise and infrastructures for cryogenic test and room temperature electronic
CNRS Néel	Work Package Leader Expertise and infrastructures for cryogenic test
UGA-IMEP-Lahc	Expertise on Self-heating phenomena

4.11.3. Detailed work description

T7.1 Equipment needs identification & equipment acquisition		
Start:M1	End:M24	Lead: CEA
Contributors: CNRS-Neel, CEA, UGA-IMEP		

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Description:

Our first analysis highlights that the LSQ program will need statistical characterizations, which require tools and characterization methods industrialization.

Typically, WP5-Cryo electronic requires strong amplification and industrialization of characterization means for DC, RF and aging: 28FD PDK 4K add-on needs statistical wafer level characterization.

Statistical test required (wafer level)	Availability (CEA or CNRS-Neel or UGA-IMEP)
DC	Die only. Cryogenic prober available but strong need of industrialization.
RF	Die only. Cryogenic prober retrofit needed and probe card concept at cryogenic temperature to be evaluated: Instrumentation for MOS characterization (DC up to 1MHz) may be needed. Cabling for RF measurements up to few tenth of GHz
Aging	Die only. Cryogenic prober available but strong need of industrialization.

CEA manual cryogenic prober (Lakeshore CPX) are currently working with open loops cooling systems. To limit the project environmental footprint and reduce operation expenditures that would spur with test industrialization, we will plan the necessary upgrades. Some may also need an upgrade of RF probes for more reliable measurements.

UGA-IMEP's 6 arms prober is DC only and RF upgrades on 2 arms would add some capacity for RF characterizations.

Besides tools capabilities and industrialization needs, we suspect that scaling up will increase the need for statistical wafer level characterizations and therefore may require supplying a second cryogenic prober, and some manual probers.

For single transistors or devices characterizations (WP5-Cryo electronic), RF and photonic characterizations (WP3-Integrated photonics & WP6-3D&Packaging), new cryostat and control electronics capacities may be needed both at CEA-IRIG et CNRS-Neel.

This task aims at evaluating the exact needs of the program to define the investment plan for upgrades, or new tools supply, in coherence with 'Cryogenic Plan'. An in-depth analysis of characterization volumes, put in perspective with existing equipment workload and productivity ramp-up, will be conducted to assess the benefits of such investments.

Deliverables (due month/lead):

D7.1.1 Report on needs evaluation and investment plan (M3),

D7.1.2 Final report on tools upgrade and installations (M24)

T7.2 Characterization methods developments

Description:

Besides the hardware needs, characterization methods, at all levels (from transistor to system) and scales (from single device to wafer), need to be developed and improved. Task 2 will address these actions.

T7.2.1 DC, RF and Aging Cryogenic wafer level probing pre-industrialization

Start: M1

End: M72

Lead: CEA

Contributors: CEA

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Description:

Due to cryogenic conditions, the cryogenic wafer level prober needs specific designs on the last metal levels: pad pitches need to be relaxed compared to standard 28FD technologies and additional alignment structures are required in each die.

The first part of this task aims at specifying the last metal levels dimensions and structures required to speed up and improve the cryogenic characterization at wafer level. These specifications will apply to all wafers requesting cryogenic probing. Some wafers already available may need post processing (2 mask levels) to fit in the cryogenic probing specifications.

In the second and third part of this task, after the appropriate upgrades for RF measurement, RF probe cards will be evaluated to assess the RF characterization capability (frequency level) at wafer level at 4K. If some relevant conditions can be obtained, RF test protocols will be implemented.

In parallel those two phases, depending on tool workload, some DC and/or RF and/or Aging tests methodologies will be evaluated/optimized:

Example for DC: statistical measurement through addressable transistor arrays

Example for RF: impact mitigation of self-heating

Deliverables (due month/lead):

D7.2.1.1 Report on Cryo-prober industrialization for DC tests (M18)

D7.2.1.2 Report on Cryo-prober evaluations for RF tests (M48)

D7.2.1.3 Report on test protocols evaluations (M72)

T7.2.2 RF cryogenic characterization process development.

Start:M1

End:M72

Lead: CEA

Contributors: CEA

Description:

To evaluate RF performances and acquire data for a future RF cryogenic compact model, specific RF structures that can be measured on manual cryogenic prober with 2 RF pads (GSG) are needed, with various dimensions (W, L, number of finger gates...) oxide thicknesses (GO1, GO2),... New RF design with access to the back gate is required to fully take advantage of FDSOI capability at low T.

RF test protocol down to 4K need to be optimized as well.

M1-M24 : specification and evaluation of FDSOI test structures required to perform RF measurements at cryogenic temperature.

M1-M72 : all along the project, improvement of the test protocol, including optimization of the calibration and de-embedding procedure. Development of new characterization methods if needed

Deliverables (due month/lead):

D7.2.2.1 Report on RF measurements of dedicated FDSOI structures at cryogenic temperature (M24)

D7.2.2.2 Report on RF measurement protocol at cryogenic temperature (M72)

T7.2.3 Self-heating phenomena evaluation and impact simulation on cryogenic characterizations

Start:M1

End:M36

Lead: CEA

Contributors: CEA/UGA-IMEP

Description:

In FDSOI devices, the outflow of the heat generated at the drain side is impeded due to the low thermally conductive materials constituting the channel. Therefore, self-heating effects (SHEs) lead to a significant increase in the channel temperature when the device is tested. This temperature increase can severely affect the characterization results one intends to upload in the cryogenic models.

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This task aims at evaluating the self-heating impact on characterization results compared to real operating conditions to adapt the characterization protocols if needed (to be done in task 7.2.1 and/or 7.2.2).

Deliverables (due month/lead):

D7.2.3.1: Report on self-heating impact on characterization results (M24)

T7.3 Characterization PCB and systems design.

Start:M1

End:M72

Lead: CEA

Contributors: CEA, CNRS-Neel.

Description:

In relation to WP5-Cryo electronic tasks 5.4.1, 5.4.2, but also from WP3-Integrated Photonics, WP6-3D&Packaging and for program demonstrators, tests methodologies have to be developed to reduce test setup in cryostat environment, to implement appropriate automation and hardware equipment to be compatible with different cryostats, and to develop test boards adapted to cryostat cables and connectors.

First year will be devoted to a diagnostic on existing hardware and software equipment, and to the evaluation of the constraints of multi-site cryostats settlement. On this basis, a new test board architecture, as generic as possible to cover all WP needs will be proposed and designed.

Second year will be focused on fabrication, debug of the test bench (at room temperature and then cryogenic temperature), and application to the different WP samples.

The following years will be an iterative process to adapt test methodologies and design test boards and the task will be conclude by a proposal of system designs strategies for the scaling up.

Deliverables (due month/lead):

D7.3.1 Report on new board and system test architecture proposal (M12)

D7.3.2 Report on cryogenic test strategies for high speed and high scale integration (M72)

T7.4 Room temperature electronics for test and demonstration

Start:M1

End:M72

Lead: CEA

Contributors: CEA

Description:

Current Qubit control uses lab equipment leveraging FPGA for signal generation as it provides more flexibility for signal shaping feedback than traditional AWG. Industrial vendors such as Quantum Machines, Qblox or Zurich Instruments, market such devices, but they come with a consequent price and cannot be easily extended due to their closed source nature.

With the technologies envisioned for the scaling up of the control, such equipment's will face significant evolutions depending on the selected technology path. The use of optical channels, or the interactions with QEC decoders, may structurally modify their requirements.

Consequently, to provide the flexibility needed for the program tests and demonstrators, task 7.4 will initially seek to design signal generation solutions able to adapt to the project needs. Then, drastic evolutions may be required to cope with system design decisions for the demonstrator. This task would leverage existing competences both at CEA in target specific signal generation using commercial FPGA. Should these pieces of equipment be proven as a limit to the scaling, this task may also address their ASIC performance projection to provide necessary insight for system analysis.

Another development is envisioned on FPGAs: the high-speed link (whether copper or fiber) between cryo chips and room-temperature control electronics will require IPs for handling up and down-link communications. Presently a SerDes is developed as a primary brick in this scheme and the higher layers of protocol will have to follow.

Deliverables (due month/lead):

D7.4.1 Report on flexible room temperature signal generation (M36)

D7.4.2 report on room temperature equipment for final demonstrator (M72)

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T7.5 Characterization coordination and scheduling

Start:M1	End:M72	Lead: CEA
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Contributors: CEA, CNRS-Neel

Description:

Most of the work packages will need cryogenic characterizations: each work package will be in charge of its measurements in the cryostats or on the Lakeshores. This task aims at organizing the tools accesses, at CEA-IRIG, CEA-Leti and CNRS-Néel facilities.

Deliverables (due month/lead):

None

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5. FORECAST HUMAN RESOURCES AND MEANS

5.4. Human resources

From a legal point of view, Nanoelec is a consortium with 22 members. Each partner of the consortium remains the employer of the staff involved in the IRT Nanoelec projects. The staff involved in the LSQ program is not an employee of Nanoelec: each partner or potential partner proposes the allocation of permanent employees and the recruitment of temporary resources.

As permanent employees typical profiles of the human resources allocated to the program by the LSQ partners are, experienced engineers, doctors, research directors, all with strong expertise, not only in quantum and cryogenic technologies, but also in systems design and architecture, errors corrections algorithms, 3D & packaging, silicon photonics and CMOS technologies developments and characterizations.

Temporary resources recruitment aims at reinforcing the program work force but, also and mainly, at developing a broad quantum computing skills base in the ecosystem with the involvement and training of engineering students or young engineers, PhD Students, post-doctoral researchers.

5.5. Main used equipment

Equipment	Owner*	Unity **	Volume
CEA Clean Rooms in Grenoble	CEA	Cf below	
STMicroelectronics Cleanrooms in Crolles	STMicroelectronics	Cf below	
Cryostats	CNRS	Cf below	

* Propriétaire ou locataire de l'équipement dans le cadre du projet.

Indiquer également les équipements des partenaires ou sous-traitants éventuels si cette information est utile pour la compréhension des travaux du projet et pour la justification de coûts élevés. Préciser si l'accès à l'équipement est gratuit ou entre dans les coûts du partenaire.

** Unité utilisée pour l'indication de volume d'utilisation de l'équipement. Si les coûts ne sont pas dans le budget IRT du projet, il est inutile de donner des indications quantitatives

In its initial phases, Nanoelec invested in specific tools to process 200 and 300 mm wafers. These Nanoelec investments were dedicated to the projects carried out by the Institute. The tools have become a part of the much larger set of standard equipment available in the facilities of the project partners (STMicroelectronics, CEA). The past investments are now used to address challenges that have been identified on the current fabrication processes. CEA equipment expenses are computed proportionally to the time they are used by the project. Operations costs of the platform are computed every year through the real data. The rate is based on the ratio between all operations expenses and the total working time of all the staff that have been working on the platform. An independent auditor (KPMG) certifies every year the methodology used to compute this rate and the rate itself. This audit guarantees that the costs used for Nanoelec are different from the CEA general rates and indeed specific to Nanoelec. The resulting rate is an average figure applied to all the staff involved in the platform regardless of their position (engineers, technicians).

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Nanoelec specific clean room expenses at STMicroelectronics are not funded through the PIA subsidy. They are declared as process costs related to process steps called « Moves ». The expenditures on platform equipment (CNRS) associated with the project is made on a pro rata basis for the time the project takes. There are also the expenditures consumables used specifically for the project.

5.6. Background Intellectual property used by the project

IRT Nanoelec brings to the LSQ program a strong background in the field of 3D stacking & packaging technologies as well as in the field of silicon photonics. This adds up to 60 or so patent families that are part of Nanoelec IP portfolio as of December 2022.

In addition, CEA, CNRS, UGA and INRIA are bringing into the program a large background in the field of quantum technologies (control electronics, cryo electronics, error correction codes and algorithms, quantum physics that will be used as a knowledge basis for the LSQ program. These knowledge being accessible for R&D programs and accessible through license agreements to industrial partners if required for exploitation of results. The background IP concerning the Quantum activities will be identified at the beginning of the project.

Propriété intellectuelle antérieure produite par l'IRT mise en œuvre sur le projet

Description	Amortissement sur le projet
30 patents from 3D Integration program.	No
30 Patents from Photonic program	No

Propriété intellectuelle antérieure utilisée à titre gracieux par l'IRT

Description
The work performed within the Nanoelec projects can take advantage of background and side ground IP generated by CEA but also other partners. When the related IP is still available for licensing, it can be integrated to the Nanoelec IP portofolio under negotiation with Nanoelec partners willing to acquire exploitation rights.

5.7. Contributions of partners not funded by PIA

IRT Nanoelec is a consortium. Public funds (PIA subsidies granted to Nanoelec) received for the programs are only dedicated to academic organizations (CEA, CNRS, INRIA, UGA). Industrial partners do not receive any public funding for their activities in the project. The contribution of industrial partners is twofold: cash to fund the R&D effort of some of the public partners and In-kind. In-kind contributions are only accounted for the members of the consortium and auditors certify their amount. These in kind contributions are a very good indicator of each partner's involvement in the project and a clear marker of the collaborative nature of Nanoelec programs.

Contributions of industrial partners for the LSQ project are detailed in the financial exhibit accompanying this project submission file.

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6. ADMINISTRATIVE DATA

6.4. IRT Data

Dénomination et qualification de l'IRT

Raison sociale de l'IRT	IRT Nanoelec		
Représentant Légal	Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA)		
Etablissement principal pour le projet	CEA, 17 rue des martyrs, 38054 Grenoble cedex 9		
Equivalent Temps Plein	198	Total bilan €	NA
Budget Annuel	45M€	Filiale de groupe	Sans objet
Qualification de l'IRT			consortium

Chef de projet

Nom, Prénom	Fonction	Courriel	Téléphone
Co direction : Corinne Legalland coté Hardware CEA Leti, et Tanguy Sassolas Architecture CEA list	Codirectrice du Programme Codirecteur du programme	Corinne.legalland@cea.fr Tanguy.sassolas@cea.fr	

Responsable scientifique – si différent

Nom, Prénom	Fonction	Courriel	Téléphone
Marc Duranton	Responsable programme	Marc.duranton@cea.fr	+33169082910

Responsable administratif – si différent

Nom, Prénom	Fonction	Courriel	Téléphone
Maubert Sandrine	Directrice adjointe	sandrine.maubert@cea.fr	04 38 78 03 74

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6.5. Calendrier prévisionnel et lieu de réalisation

Calendrier prévisionnel

Date de commencement des travaux prévisionnelle	01/09/2023
Durée prévisionnelle (mois)	72
Date d'achèvement prévisionnelle	30/09/2029

Lieux de réalisation du projet

Site principal de l'IRT	CEA GRENOBLE, 17 rue des martyrs, 38054 Grenoble cedex 9
Autre site	CEA SACLAY, 91191 Gif-sur-Yvette cedex
Autre site	STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex
Autre Site	CNRS, 25 avenue des martyrs, 38000 Grenoble
Autre Site	INRIA, 655 Av. de l'Europe, 38330 Montbonnot-Saint-Martin
Autres sites	Laboratoires des partenaires académiques hors écosystème grenoblois

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6.6. Collaborative nature of project

Collaborative project within the meaning of the European Union Regulations	Yes
--	-----

Partner*				
Partner	consortium member (1)	Legal form (2)	Statut **	
CEA	YES	EPIC	AC	
STMicroelectronics	YES	SAS+SA (*)	LC	
Siemens EDA	YES	SARL	LC	
Inria	YES	EPST	AC	
Université Grenoble Alpes	YES	EPCSCP	AC	
CNRS	YES	EPST	AC	
Potential partners				
Alice & Bob	No ⁽⁴⁾	SAS	SME	
C12 Quantum Electronics	No ⁽⁴⁾	SAS	VSE	
Quandela	No ⁽⁴⁾	SAS	VSE	
Siquance	No ⁽⁴⁾	SAS	VSE	
Silent Waves	No ⁽⁴⁾	SAS	VSE	
Other industrial actors TBD***	No ⁽⁴⁾	-	-	

(1) Consortium member Yes/ No

(2) Legal Form. (*: several subsidiaries involved for STMicroelectronics)

(3) Statute from the European community perspective: ENT (enterprise) NEN (non enterprise).

(4) Considered/potential partners to join the program

*Partner whose contribution justifies the collaborative nature within the meaning of RGEC regulations

** VSE: Very small enterprise, SME: Small enterprise, Midcap: medium size enterprise, LE: Large Enterprise AC=Academic

*** Other partners will be considered (Radiall, ATOS, Thalès...)

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6.7. R&D sub-contractors for the project

Partenaire	Forme juridique	Statut **	% coûts

Only provide a list contractors that contribute to research activities under commercial agreements whose costs are included in the direct costs of the project.

** VSE: Very small enterprise, SME: Small enterprise, Midcap: medium size enterprise, LE: Large Enterprise AC=Academic

6.8. Public funding for IRT Nanoelec partners

6.8.1. Public funding allocated to the project for the IRT Partners

IRT Nanoelec is not a legal entity; the institute is a consortium of public and private actors. CEA is the holder of Nanoelec and acts in the name of the consortium as far as relations with the French public authorities are concerned (SGPI, ANR). This legal framework was suggested by CEA in 2011 to take into account the specificities of the project submitted to the French authorities. The IRT Nanoelec work plan was essentially built on pre-existing shared infrastructures (clean rooms, instruments) representing investments far beyond the financial capabilities of the project. Following an audit led by IGF and IGAENR, the CGI authorized this derogation. The audit concluded in 2011 that a consortium structure for IRT Nanoelec was consistent with the objectives of the IRT call for tenders. As a result, the adaptation to the standard rules was included in the convention between the *ANR and the CEA, holder of the IRT Nanoelec*.

The contribution of the different Nanoelec partners is not subject to any government funding beyond the PIA 4 allocated to this program. Public funds (PIA 4 funding to the Nanoelec LSQ) received for the R&D programs are exclusively allocated to CEA and other public laboratories (CNRS, INRIA, UGA for instance). The salaries and associated charges of academic organizations (such as CNRS, INRIA, UGA) statutory staff is funded by the French government. It amounts to 30% of the total expenses of these partners. Industrial partners do not receive any funds from the French government for this project.

6.8.2. Public funding for similar projects among IRT partners

In order to address long-term technical issues or to explore new application paths, European projects are built and submitted on a regular basis. They usually include the participation of one or several members of the LSQ Program and are associated to Nanoelec.

Upon signature of the consortium agreement, each partner of the IRT Nanoelec is bound to declare any financial aid received from a member state that fund the work performed for the project. The corresponding information is declared by the partner in its disclosure of annual expenses, which are certified by its auditor ("commissaire aux comptes") or its accounting officer. As far as CEA is concerned, the system that counts and allocates the work hours prevents any duplication of resources on more than one project. It prevents any overlap of public aids.

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7. FUNDING JUSTIFICATION BY PIA

7.4. Project context/ Market perspective/ Applications

Under construction

For 3th March

7.5. Collaborative dimension within the meaning of the regulation IRT DIR)

The R&D programs of IRT Nanoelec are intrinsically collaborative as they gather industrial actors and research organizations in order to address the challenges described in shared roadmaps and the subsequent Statements of Work. These roadmaps are validated by the steering committee of IRT Nanoelec and then by representatives from the French Public Authorities and integrated in the strategic plan of the “convention CEA ANR”. The partners of the project are also involved in various research collaborations with different actors of the local, national and international quantum communities. The industrial partners contribute to the works plan defined in the roadmap.

The partnership is built along the value chain in order to reinforce the collaborative momentum. As a whole, the role and the contribution of the partners have been defined with STMicroelectronics and CEA on the development of the Cryocmos platforms, CEA, CNRS and Siemens on the development of Electronic Design Automation and simulation tools, , and CEA, UGA and INRIA in the development of QEC implementation. The emerging players will contribute for the specifications of the system and of the architecture.



7.6. Large dissemination of results:

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[Large dissemination of results](#)

yes

The partners involved in one or several Nanoelec programs are bound by a consortium agreement. New partners sign this agreement when they enter a program and a related project. It addresses issues such as the management of communication and other dissemination initiatives and the management of IP rights. The operating principles of the immaterial assets are described in the consortium agreement. They guaranty the absence of any indirect aid to industrial partners by requiring fees at market conditions for the exploitation of IP rights.

Results that are not subject to any IP rights are largely shared through publications and talks at conferences.

IRT Nanoelec has been very active in terms of publications, more than 629 publications during the period 2015-2021, among which 205 referenced in Web of science. The impact is strong at the national as well as the international level with publications in the major journals (IEEE Design and test, Journal of solid State circuits, IEEE Electron Device Letter...) and the presence at key conferences and fairs (IEDM, DATE, VLSI, ISSCC, ECTC ...). Partners of the program intend to pursue this policy actively.

The partners of the program are highly connected to local, national, and international players from academics to start-ups, SMEs, and large companies. The objective of the consortium is to generate synergies and create added-value thanks to a close collaboration between industrial partners along the value added chain.

Additionally, collaborative projects are already running in the field of Quantum. The interaction with these initiatives are foreseen.

The results of those projects may benefit to the LSQ IRT project and the IRT project may also feed partly those programs.

In parallel of the technological development of LSQ, dissemination will be carried out through other projects. They are mainly supported by European collaborative projects and industrial associated projects.

Finally, during the project, some possible collaborations with others IRT in France and also with international research lab if relevant may be initiated and developed.

7.7. Compatibility of funding for IRT (within the meaning of the regulations RGEC)

By allowing industrial partners to access a set of technological tools and multi-disciplinary know-how and expertise at the interface of science and technology, Nanoelec generates a unique research infrastructure that even large industrial actors cannot create with their own resources. The involvement in the project of large companies such as STMicroelectronics and Siemens generates potentially for emerging actors opportunities that would have been otherwise out of reach. Nanoelec tools and expertise are systematically used to carry out projects with a strong technical risk, thus amplifying the leverage effect of the consortium.

The project requires the development of new know-how in terms of design, models and process that will create added value for the industrial partners in the mid-term. The PIA funding is of a real incentive value since the expected Return on Investment is of a long-term nature, which would prevent companies from fully supporting the required resources on their own. In addition, the collaborative nature of the work performed allows better expressions of the needs and reduces the risk that the knowledge created during the projects fails at generating economic value.

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Hence, Funds from the PIA are used to address technical challenges with a long-term perspective in terms of ROI. Further steps of development toward process maturity and industrialization are carried out with direct funding from the industrial partners in the framework that can be associated to IRT Nanoelec when relevant.

Concerning the IP generated during the projects, the rights are handled by rules agreed upon by all partners in the consortium agreement. By defining licensing conditions at market conditions, they guarantee the absence of indirect aids to the industrial partners exploiting the IP.

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8. ACRONYMS AND DEFINITIONS

Acronym	Meaning	Comment
ANR	Agence Nationale pour la Recherche National Research Agency	French National research agency
CSA	Coordination and Support Action	European project structuring academic and industrial ecosystems by funding training, conference and gatherings as well as technological roadmap definitions
EDA	Electronic Design Automation	Refers to the domain addressing the automation of electronic design. EDA tools are software used in this automation often using an EDA methodology to ensure several tools interoperation to achieve design goals
ESL	Electronic System Level	Electronic system level (ESL) design and verification is an electronic design methodology, focused on (higher) appropriate abstractions in order to increase comprehension about a system, and to enhance the probability of a successful implementation of functionality in a cost-effective manner.
FMI	Fonctional Mockup Interface	A standard for the cosimulation of numerical models https://fmi-standard.org/
FTQC	Fault-Tolerant quantum Computing	Refers to a universal quantum computer that can provide error correction mechanisms. One must bear in mind that FTQC will still exhibit a remaining quantum error. To the author's knowledge there is no formal definition of FTQC in terms of remaining error probability
HPC	High-Performance Computing	HPC uses supercomputers and computer clusters to solve advanced computation problems.
HQI	HPC Quantum Initiative	A research and investment project part of the SNAQ whose goal is to setup an HQI platform.
HQI Platform		National computing equipment shared between

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		research entities and piloted by GENCI, aiming to operate quantum computer accelerators within the HPC infrastructure in a NISQ then LSQ approach
IP	Intellectual Property	By extension in the electronic design domain, a functional block implemented by means of a hardware description language or its physical implementation on a given technology is referred as an IP, due to the fact that there use can be licensed to third parties that build system composed of several such IPs.
JJ	Josephson junction	
LNA	Low-noise amplifier	
LSQ	Large-Scale Quantum Computing	Refers to a universal quantum computer (gate based) who exhibits hundreds of error-corrected qubits, and therefore provides quantum supremacy
MBSE	Model-based system engineering	Model-based systems engineering (MBSE) is a formalized methodology that is used to support the requirements, design, analysis, verification, and validation associated with the development of complex systems. In contrast to document-centric engineering, MBSE puts models at the center of system design.
NISQ	Noisy Intermediate Scale Quantum	Quantum computers that exhibit few qubits with quantum error that limit the depth of computation that they can be used for.
QEC	Quantum Error Correction	Refers to solutions developed to reduce the quantum error of qubits by means of control feedback occurring during the processing
PIA	Programme d'Investissement d'Avenir <i>Investment program for the future</i>	Type of national funding that co-finances the IRT programs.
PNCQH	Plateforme Nationale de Calcul Quantique Hybride (France Hybrid Quantum HPC)	

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	Initiative)	
SNA	<i>Stratégie Nationale d'Accélération</i> National acceleration strategy	French Investment programs for several strategic technology domain
SNAQ or SNQ	<i>Stratégie Nationale (d'Accélération) pour les technologies quantiques</i> National Strategy for Quantum Technologies	The French investment program dedicated to quantum technologies as part of all SNA
TWPA	Traveling Waves Parametric Amplifier	High quality LNA based on JJ used as first stage of qubit readout for superconducting qubits. Due to their use of JJ they must be used in cryogenic conditions

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9. APPENDIX

9.4. APPENDIX 1 - BIBLIOGRAPHY

Under Construction

Will be provided on March 3rd

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9.5. APPENDIX 2 - RISK ANALYSIS

Under construction

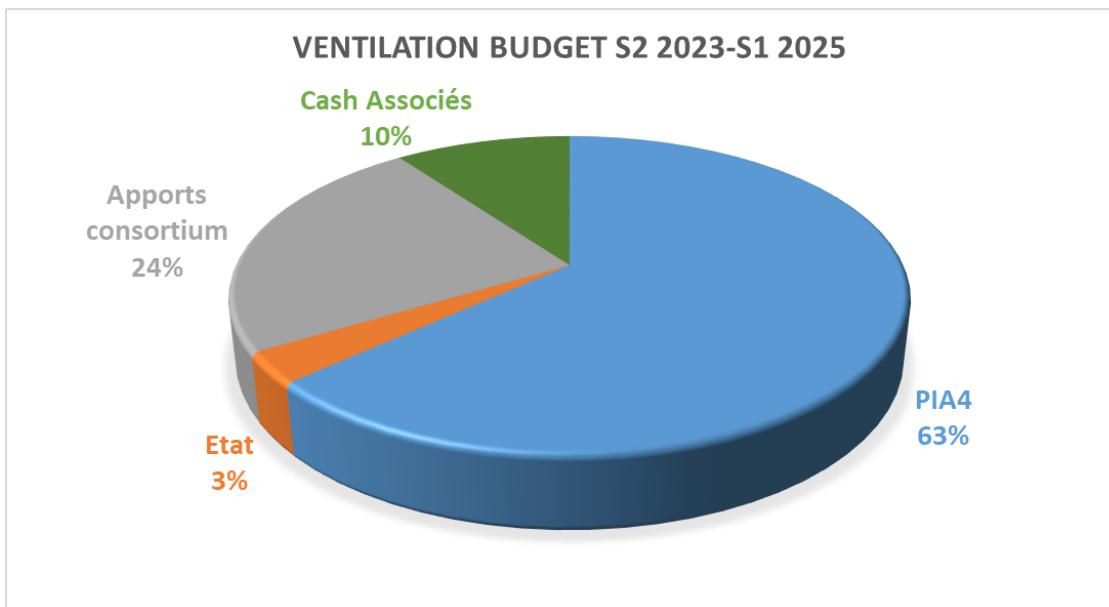
Will be provided on March 3rd

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9.6. : APPENDIX 3 - FINANCIAL DATA AND BUDGET

Budget for year one and two of the project

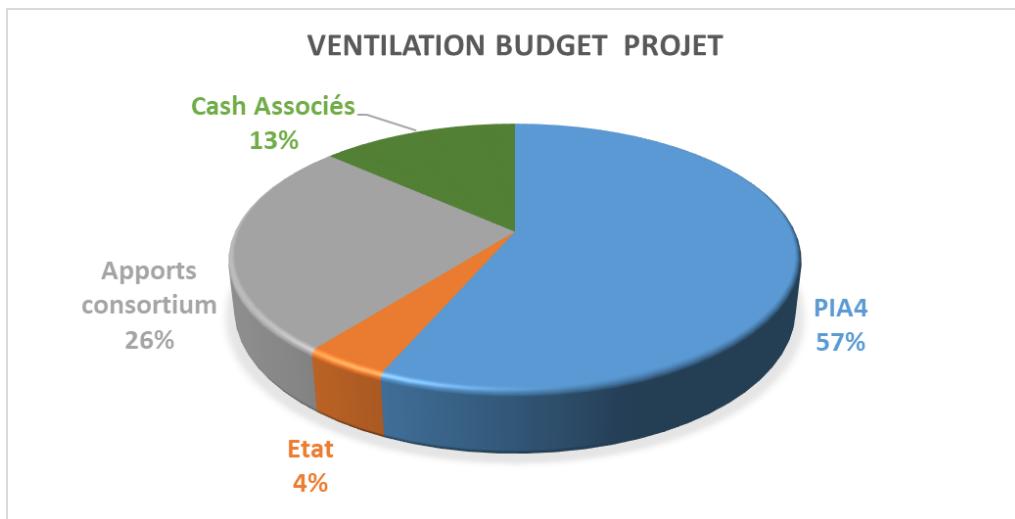
LSQ																	
LSQ	Partenaire	Fonctionnement (k€)					Investissement k€					Total					
		Dépenses	ANR (PIA dédié)	Etat (PIA4)	Etat	Industriels Membres	Autres apports privés	Dépenses	ANR (PIA dédié)	Etat (PIA4)	Industriels Membres	Autres apports privés	Dépenses	ANR	Etat (PIA4)	Etat	Privé
S2 2023	Académiques	2 614	0	2 096	118	150	250	750	0	0	750	0	3 364	0	2 096	118	1 150
	Industriels membres	420				420		0					420	0	0	0	420
	Total	3 034	0	2 096	118	570	250	750	0	0	750	0	3 784	0	2 096	118	1 570
S1 2024	Académiques	4 260	0	3 419	191	150	500	1 250	0	500	750	0	5 510	0	3 919	191	1 400
	Industriels membres	420				420		0					420	0	0	0	420
	Total	4 680	0	3 419	191	570	500	1 250	0	500	750	0	5 930	0	3 919	191	1 820
S2 2024	Académiques	4 510	0	3 419	191	151	750	1 750	0	1 000	750	0	6 260	0	4 419	191	1 651
	Industriels membres	420				420		0					420	0	0	0	420
	Total	4 930	0	3 419	191	571	750	1 750	0	1 000	750	0	6 680	0	4 419	191	2 071
S1 2025	Académiques	4 628	0	3 507	209	163	750	1 000	0	250	750	0	5 628	0	3 757	209	1 663
	Industriels membres	420				420		0					420	0	0	0	420
	Total	5 048	0	3 507	209	583	750	1 000	0	250	750	0	6 048	0	3 757	209	2 083
VENTILATION BUDGET S2 2023-S1 2025																	
Cash Associés																	
TOTAL S2 2023-S1 2025	Apports consortium	24%															
	Etat	3%															
	PIA4	63%															
10%																	



	IRT	IRT Nanoelec						
	Projet	Large Scale Quantum LSQ						
	Descriptif contractuel - document de référence							
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Budget global sur 6 ans – Années 1 & 2 – Années 3 à 6 – Total

Partenaire	Fonctionnement (k€)					Investissement k€				Total			
	Dépenses	Recettes				Dépenses	Recettes			Dépenses	Recettes		
	ANR (PIA dédié)	Etat (PIA4)	Etat	Industriels Membres	Autres apports privés	ANR (PIA dédié)	Etat (PIA4)	Industriels Membres	Autres apports privés	ANR	Etat (PIA4)	Etat	Privé
TOTAL S2 2023-S1 2025	Académiques	16 013	0	12 441	709	613	2 250	4 750	0	1 750	3 000	0	20 763
	Industriels membres	1 680	0	0	0	1 680	0	0	0	0	0	1 680	0
	Total	17 693	0	12 441	709	2 293	2 250	4 750	0	1 750	3 000	0	22 443
TOTAL S2 2025-S1 2029	Académiques	37 186	0	25 809	2 190	1 938	7 250	6 000	0	0	6 000	0	43 186
	Industriels membres	5 160	0	0	0	5 160	0	0	0	0	0	5 160	0
	Total	42 346	0	25 809	2 190	7 098	7 250	6 000	0	0	6 000	0	48 346
TOTAL PROJET	Académiques	53 199	0	38 250	2 898	2 551	9 500	10 750	0	1 750	9 000	0	63 949
	Industriels membres	6 840	0	0	0	6 840	0	0	0	0	0	6 840	0
	Total	60 039	0	38 250	2 898	9 391	9 500	10 750	0	1 750	9 000	0	70 789



	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
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9.7. APPENDIX 4: LETTERS OF INTENT

9.7.1. ALICE & BOB

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	Projet	Large Scale Quantum LSQ				
	Descriptif contractuel - document de référence					
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9.7.2. CNRS



Le Directeur Général Délégué à la Science

Mr Sébastien Dauvé
 Président du Comité de Pilotage
 IRT Nanoelec
 17 avenue des Martyrs
 38054 Grenoble Cedex 9

Réf. : DGDS/D-2022-26

Paris, le 17 novembre 2022

Lettre d'intérêt et de support du CNRS au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028

Le CNRS est membre de l'IRT Nanoelec depuis sa création en 2012. Ces 10 ans de participation et d'engagement conjoint avec les partenaires industriels et académiques associés ont démontré leurs bénéfices indéniables en termes de multidisciplinarité et d'agilité, constituant ainsi une source d'enrichissement de nos axes de recherche. L'IRT Nanoelec a su créer un cadre qui permet de nouer des relations de confiance entre les acteurs publics et privés tout en offrant la flexibilité nécessaire à la recherche et à l'innovation.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans et devrait débuter courant 2023. Le programme viendra s'insérer de manière complémentaire dans un environnement national riche au sein duquel de nombreux laboratoires du CNRS jouent un rôle pionnier et structurant dans le domaine des sciences et technologies quantiques.

De par notre expertise reconnue dans le domaine et en lien avec les initiatives déjà lancées au niveau national, notre contribution au programme pourra couvrir des champs variés telles que les technologies de conception de composants et systèmes innovants tels que ceux dédiés à l'électronique et à l'amplification bas bruit, de mesures et de tests en conditions cryogéniques, les chaînes et outils de modélisation de systèmes quantiques, la photonique intégrée, etc. Nous nous réjouissons de l'excellente complémentarité des compétences que l'IRT ambitionne de réunir pour répondre à cet enjeu critique vers l'ordinateur quantique universel. Notre contribution sera basée sur le modèle d'accord établi depuis 2012 entre le CEA porteur de l'IRT et le CNRS ainsi que sur la capacité de l'IRT Nanoelec à enrichir ses programmes de partenariats associés avec des laboratoires à l'échelle nationale. Notre participation sera conditionnée au financement du programme par l'Etat.


 Alain Schuhl
 Directeur Général Délégué à la Science

CNRS
 Campus Gérard Mégie
 3, rue Michel-Ange
 75794 Paris cedex 16
 T. 01 44 96 40 00
www.cnrs.fr

	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
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9.7.3. C12

	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
	Descriptif contractuel - document de référence					
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9.7.4. INRIA



Mr Sébastien Dauvé
 Président du Comité de Pilotage
 IRT Nanoelec
 17 avenue des Martyrs
 38054 Grenoble Cedex 9

Lettre d'intérêt et de support de Inria au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028.

Inria est membre de l'IRT Nanoelec depuis sa création en 2012. Ces 10 ans de participation et d'engagement conjoint avec d'autres partenaires industriels et académiques ont démontré leurs bénéfices indéniables en termes de multidisciplinarité, d'agilité et constitue donc une source d'enrichissement de nos axes de recherche. L'IRT Nanoelec a su créer un cadre qui permet de nouer des relations de confiance entre les acteurs publics et privés tout en offrant la flexibilité nécessaire à la recherche et l'innovation.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies numériques et électriques nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans et devrait débuter courant 2023. Le programme viendra s'insérer de manière complémentaire dans un environnement national riche au sein duquel de nombreux laboratoires d'Inria jouent un rôle structurant dans le domaine des sciences et technologies quantiques.

De par notre expertise reconnue dans le domaine de la théorie de l'information, et en lien avec les programmes PEPR déjà initiés, notre contribution au programme sera essentiellement focalisée sur le développement d'algorithmes de correction d'erreur en forte interaction avec les partenaires qui en évalueront l'implémentation matérielle. Un enjeu du programme sera l'exploration de nouveaux algorithmes prenant en compte les contraintes physiques apportées par les systèmes de commande et les technologies de qubits ciblées et réciproquement d'expliciter quels compromis ne sont pas envisageables afin d'aider à la spécification des technologies matérielles. Nous nous réjouissons de l'excellente complémentarité des compétences que l'IRT ambitionne de réunir pour répondre à cet enjeu critique vers l'ordinateur quantique universel. Notre contribution sera basée sur le modèle d'accord établi depuis 2012 entre le CEA porteur de l'IRT et Inria. Notre participation sera conditionnée au financement du programme par l'Etat.

Frédéric Desprez



Directeur du Centre Inria de l'Université Grenoble Alpes

Inria Centre at Université Grenoble Alpes
 Innovallée 655 avenue de l'Europe - CS 90051
 38334 Montbonnot Cedex - France
 Phone: +33 (0) 4 76 61 52 00

www.inria.fr/en

	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
	Descriptif contractuel - document de référence					
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9.7.5. QUANDELA

Quandela
7 rue Léonard de Vinci
91300 Massy

Mr Sébastien Dauvé
Président du Comité de Pilotage
IRT Nanoelec
17 avenue des Martyrs
38054 Grenoble Cedex 9

Lettre d'intérêt et de support de la société Quandela au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028.

La société Quandela, créée en 2017 a pour mission de développer un processeur quantique basé sur une technologie innovante de qubits photoniques susceptible d'un passage à grande échelle. Quandela joue un rôle important dans la structuration du domaine de l'informatique quantique en contribuant activement à la stratégie nationale sur les technologies quantiques : conception, validation et industrialisation de qubits et développement d'une nouvelle génération de processeur quantique.

Notre ambition nécessite le développement, le test et la validation d'un ensemble de technologies nécessaires au passage à l'échelle de notre concept de qubits. A ces fins, les technologies développées par la filière semi-conducteur sont d'un grand intérêt et l'écosystème de l'IRT Nanoelec offre un ensemble de compétences complémentaires de notre propre environnement.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans, qui devrait débuter courant 2023. Quandela confirme être en contact avec l'équipe chargée de la construction de ce programme au CEA et évaluer l'opportunité d'une participation au programme LSQ en cours de construction à l'IRT Nanoelec afin de contribuer à la construction de technologies génériques nécessaires à la chaîne de contrôle de qubits et de bénéficier de l'effet de levier apporté par la mise en commun des moyens et compétences dans les domaines de la simulation et de la modélisation, des technologies de fabrication collective, de la caractérisation de composants et systèmes à basse température, des technologies numériques et des technologies de correction d'erreur.

Les axes de développement du programme d'un intérêt potentiel plus particuliers pour Quandela concernent les technologies d'intégration 3D permettant d'hybrider les différents éléments d'un processeur, les solutions de gestion thermique ainsi que les techniques de correction d'erreur et leur implémentation sur architecture numérique.

Notre participation sera conditionnée au financement du programme par l'Etat.

A Massy, le 24 février 2023

Valérian Giesz

Valérian Giesz

Valérian Giesz
2023-02-25 LiveConsent ID DY4EUF

	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
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9.7.6. SIEMENS EDA

SIEMENS

Siemens Electronic Design Automation SARL
110 rue Blaise Pascal, Immeuble le Viséo, Bat B 38330
Montbonnot Saint Martin, France

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Mr Sébastien Dauvé
Président du Comité de Pilotage
IRT Nanoelec
17 avenue des Martyrs
38054 Grenoble Cedex 9

Letter of interest of Siemens EDA's involvement in the potential LSQ (Large Scale Quantum) program of IRT Nanoelec for the period 2023 – 2028

- Siemens EDA has been involved in IRT Nanoelec since its creation in 2012 in view of the challenges raised by the microelectronics industrial sector. Siemens notes, after almost 10 years of participation and investment within the IRT that a joint investment alongside other members, partners, industrial and academic shareholders is an indisputable source of agility, diversity, multidisciplinary and resourcing, and as a consequence of solidity in the face of numerous and rapid changes in economic, ecological and societal environments to come.

We hereby would like to express the interest of Siemens EDA to participate in the LSQ (Large Scale Quantum) program under construction within the consortium. Siemens EDA's pre-requisites to consider participating will be (i) the French government's approval to fund the program under the leadership of IRT Nanoelec and (ii) the extension of the consortium agreement signed on April 11th, 2012, whose terms shall be updated as per the last Siemens End-User agreement and EDA Software Supplemental Terms. We understood the program is built for a period of 6 years, tentatively from January 1st, 2023, to December 31st, 2028.

In view of the potential impact of such a program on the industry, we would like to express our interest in this new program by providing to CEA software licenses for non-production use only for the period defined above, under the terms of the CEA - Siemens Specific Agreement to be updated by the above-mentioned Siemens End-User License Agreement and EDA Software Supplemental Terms.

Provided we decide to participate, the resources we would potentially allocate would depend on the technical content of the program. Based on our present understanding of the scope of the program it may include additional licenses on tools addressing the field of transistor modelling, photonic devices simulation design and 3D packaging design, thermal simulation and modelling, high level synthesis tools. The supply of complementary tools for system level design and modelling would be explored according to the roadmaps of the program. Depending on the needs of the program, we may also allocate resources to support the research and the development work that would be performed in the program.

With kind regards,



Electronically signed by:
Dominique Thiriet
Date: Nov 9, 2022 16:01 GMT+1

Dominique Thiriet
Director
Date: Nov 9, 2022



Electronically signed by: JM
Saint-Paul
Date: Nov 9, 2022 15:51 GMT+1

Jean-Marie Saint-Paul
Director
Date: Nov 9, 2022

Siemens Electronic Design Automation SARL
Management: Jean-Marie Saint-Paul, Dominique Thiriet

110 rue Blaise Pascal, Immeuble
le Viséo, Bat B 38330
Montbonnot Saint Martin, France
Tel: +33 1 40 94 74 74
Fax: +33 1 46 01 91 75
siemens.com/eda

SARL au capital social de 10 398 000 € 328 751 276 RCS Nanterre – APE 4156Z
SIRET 328 751 276 00077 – N°TVA FR 35 328 751 276 Siège Social 13-15 rue Jeanne Braconnier, 92360 Meudon la Forêt, France

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9.7.7. SILENT WAVE

Silent Waves
25 Rue Ponsard
38100 Grenoble

Mr Sébastien Dauvé
Président du Comité de Pilotage
IRT Nanoelec
17 avenue des Martyrs
38054 Grenoble Cedex 9

Lettre d'intérêt et de support de la société Silent Waves au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028.

La société Silent Waves, créée début 2022 a pour mission de développer des solutions d'amplificateurs microondes à base de matériaux supraconducteurs pour améliorer les chaînes de lecture de qubits et d'étendre leur champ d'application au domaine des calculateurs quantiques à grande échelle. Silent Waves joue un rôle important dans la structuration du domaine de l'informatique quantique en contribuant activement à la stratégie nationale sur les technologies quantiques : conception, validation et industrialisation d'amplificateurs Josephson à ondes-progressives (TWPA) et intégration des fonctions passives associées.

Notre roadmap technologique nécessite une augmentation significative de nos rendements de fabrication afin de passer à l'échelle. Cela demande un saut technologique dans nos procédés de fabrication. Ce saut technologique sera favorisé par les moyens de fabrication collective développés au cours du programme.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans, qui devrait débuter courant 2023. Silent Waves confirme son intention de participer au programme LSQ en cours de construction à l'IRT Nanoelec afin de contribuer à la construction de technologies génériques nécessaire aux chaînes de contrôle et de lecture de qubits et de bénéficier de l'effet de levier apporté par la mise en commun des moyens et compétences dans les domaines de la simulation et de la modélisation, des technologies de fabrication collective, de la caractérisation de composants et systèmes à basse température, des technologies numériques et des technologies de correction d'erreur.

Nous sommes plus particulièrement intéressés par le développement au sein du consortium de solutions adaptées à la fabrication collective de nos technologies d'amplificateurs à base de supraconducteurs et au développement de la caractérisation de composants hyperfréquences à très basse température. Nous sommes également intéressés par l'exploration de solutions innovantes pour l'intégration de composants passifs nécessaire au filtrage des signaux microondes. Cela rendrait possible l'élimination de certains composants hyperfréquences volumineux, permettant la mise à l'échelle de l'architecture de l'ordinateur quantique.

Notre participation sera conditionnée au financement du programme par l'État.

A Grenoble, le 1^{er} novembre 2022

SILENT WAVES

 Luca Pavan
 25 RUE PONSARD
 38100 GRENOBLE
 TELEPHONE 06 19 89 69 49
 SAS AU CAPITAL DE 10 600 € - SIRET 9095122800010

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9.7.8. SSEQUANCE



Siquance
7 Parvis Louis NEEL
Bâtiment de Haute Technologie CS 20050
38040 Grenoble, France

Mr Sébastien Dauvé
Président du Comité de Pilotage
IRT Nanoelec
17 avenue des Martyrs
38054 Grenoble Cedex 9

Lettre d'intérêt et de support de la société Siquance au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028.

La société Siquance, créée en 2022 a pour mission de développer un processeur quantique basé sur une technologie innovante de qubits semi-conducteurs pour permettre le passage à grande échelle de l'ordinateur quantique. Siquance joue un rôle important dans la structuration du domaine de l'informatique quantique en contribuant activement à la stratégie nationale sur les technologies quantiques : conception, validation et industrialisation de qubits et développement d'une nouvelle génération de processeur quantique.

Notre ambition nécessite le développement, le test et la validation d'un ensemble de technologies nécessaires au passage à l'échelle de notre concept de qubits. A ces fins, les technologies développées par la filière semi-conducteur sont d'un grand intérêt et l'écosystème de l'IRT Nanoelec offre un ensemble de compétences très complémentaires de notre propre environnement.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans, qui devrait débuter courant 2023. Siquence confirme son intention de participer au programme LSQ en cours de construction à l'IRT Nanoelec afin de contribuer à la construction de technologies génériques nécessaire à la chaîne de contrôle de qubits et de bénéficier de l'effet de levier apporté par la mise en commun des moyens et compétences dans les domaines de la simulation et de la modélisation, des technologies de fabrication collective, de la caractérisation de composants et systèmes à basse température, des technologies numériques et des technologies de correction d'erreur.

Pour préparer, nos roadmaps, nous sommes plus particulièrement intéressés par le développement au sein du consortium de solutions génériques qui permettent de concevoir une architecture à plusieurs millions de qubits, c'est-à-dire de fonctions de base intégrées à basse température (amplification, génération signaux, périphérie d'adressage, multiplexage et démultiplexage de signaux), de technologies de transfert de données à fort flux entre la température ambiante et la basse température, de technologies d'assemblage intelligentes (gestion de la thermique, intégration d'éléments passifs,...), d'éléments de circuits pour les codes correcteurs d'erreur de surface de s'interfacer aux technologies de qubits dont nous poursuivons le développement....

Notre participation sera conditionnée au financement du programme par l'Etat.

A Grenoble, le 10 février 2023

Signature:

Maud Vinet

Aug

	IRT	IRT Nanoelec				
	Projet	Large Scale Quantum LSQ				
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9.7.9. STMICROELECTRONICS

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9.7.10. UGA-GINP



Saint-Martin-d'Hères, le 15 mars 2022

Vice-Présidence Recherche et Innovation
Université Grenoble Alpes

Chrono : 2022-115
vpcr@univ-grenoble-alpes.fr

M. Sébastien Dauvé
Président du Comité de Pilotage
IRT Nanoelec
17 avenue des Martyrs
38054 Grenoble Cedex 9

Lettre d'intérêt et de support de l'UGA et Grenoble INP au lancement d'un programme de recherche sur la thématique LSQ (Large Scale Quantum) au sein de l'IRT Nanoelec pour la période 2023 – 2028.

Madame, Monsieur,

L'UGA et Grenoble INP sont membres de l'IRT Nanoelec depuis sa création en 2012. Ces 10 ans de participation et d'engagement conjoint avec d'autres partenaires industriels et académiques ont démontré leurs bénéfices indéniables en termes de multidisciplinarité, d'agilité et constituent en conséquence une source d'enrichissement de nos axes de recherche. L'IRT Nanoelec a su créer un cadre qui permet de nouer des relations de confiance entre les acteurs publics et privés tout en offrant la flexibilité nécessaire à la recherche et l'innovation.

Nous attestons par la présente notre intérêt pour le lancement au sein de l'IRT Nanoelec d'un programme de développement de solutions de mise à l'échelle des technologies nécessaires au contrôle d'un calculateur quantique à base de qubits à l'état solide. Il est entendu que le programme est construit pour une période de 6 ans, qui devrait s'étendre, selon toute probabilité, du 1^{er} janvier 2023 au 31 décembre 2028. Le programme viendra s'insérer de manière complémentaire dans un environnement riche au sein duquel l'UGA et Grenoble INP jouent un rôle structurant dans les champs académiques et éducatifs à travers la fédération de recherche QuantAlps et le programme thématique Quantum de la Graduate School.

De par notre expertise reconnue dans le domaine de la théorie de l'information, et en lien avec les initiatives déjà lancées au niveau local et national, une de nos contributions au programme, en partenariat avec INRIA, sera focalisée sur le développement d'algorithmes de correction d'erreur en forte interaction avec les partenaires qui en évalueront l'implémentation matérielle. Un enjeu de ce projet, adressé en commun avec INRIA et le CEA, sera l'exploration de nouveaux algorithmes prenant en compte les contraintes physiques apportées par les systèmes de commande et les technologies de qubits ciblées et réciproquement l'aide à la spécification des technologies matérielles à partir des contraintes logicielles.

Université Grenoble Alpes
N° SIRET 130 026 081 00013
www.univ-grenoble-alpes.fr