Digital Pattern Generator memory map

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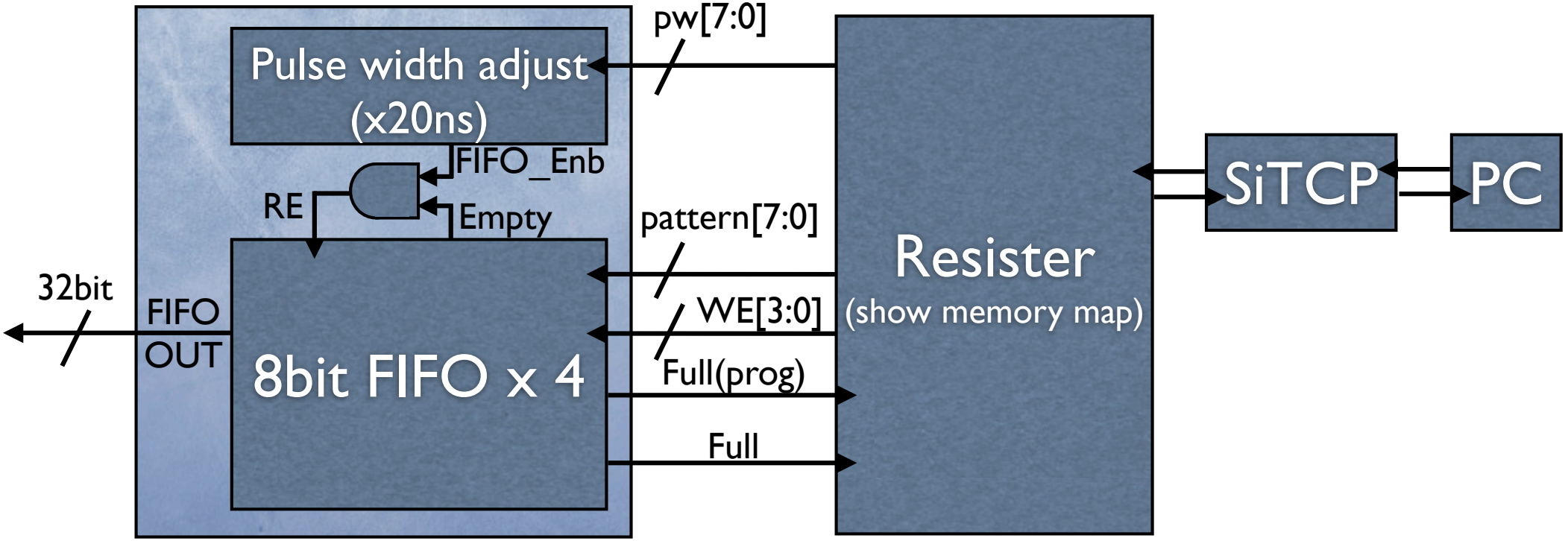
memory map

address	bit 7	6	5	4	3	2	1	0
0x08	FIFO FULL	Not used						RUN START (Active High)
0x0c	Pulse Width (x 20ns※) ※ Sysclk = 50MHz							
0x200	Pattern[31]	pattern [30]	pattern [29]	pattern [28]	pattern [27]	pattern [26]	pattern [25]	Pattern[24]
0x201	Pattern[23]	pattern [22]	pattern [21]	pattern [20]	pattern [19]	pattern [18]	pattern [17]	Pattern[16]
0x202	Pattern[15]	pattern [14]	pattern [13]	pattern [12]	pattern [11]	pattern [10]	pattern [9]	Pattern[8]
0x203	Pattern[7]	pattern [6]	pattern [5]	pattern [4]	pattern [3]	pattern [2]	pattern [1]	Pattern[0]
⋮	⋮				⋮			
0x2fc	Pattern[31:24]							
0x2fd	Pattern[23:16]							
0x2fe	Pattern[15:8]							
0x2ff	Pattern[7:0]							

FPGA回路


Pulse width adjust
(x20ns)
FIFO_Enb
RE
Empty
32bit
FIFO
OUT
8bit FIFO x 4
pw[7:0]
pattern[7:0]
WE[3:0]
Full(prog)
Full
Resister
(show memory map)
SiTCP
PC