COMP3211/9211 Computer Architecture 2019 Project

Multi-core Processor Design

This project is to be completed in teams of 3 people drawn from your Tute/Lab classes.

Deliverables for this project contribute to the group report due on Friday, April 26 (Week 10).

Project overview

Pattern searching is a typical problem in many application areas. In this project, you need to design a multi-core processor system to search a pattern in two input streams and dynamically (in real time) output the **total number** of occurrences of the pattern found so far. An example is shown in Figure 1, where two streams S_1 and S_2 are processed in parallel for pattern "*ab*". The real-time search results for each string, *N1* and *N2*, and the expected output *N* (total number of pattern matches), are illustrated in Figure 1(b). Note: the time that is required for finding a matched pattern is not shown in the illustration and the time is closely related to your design.

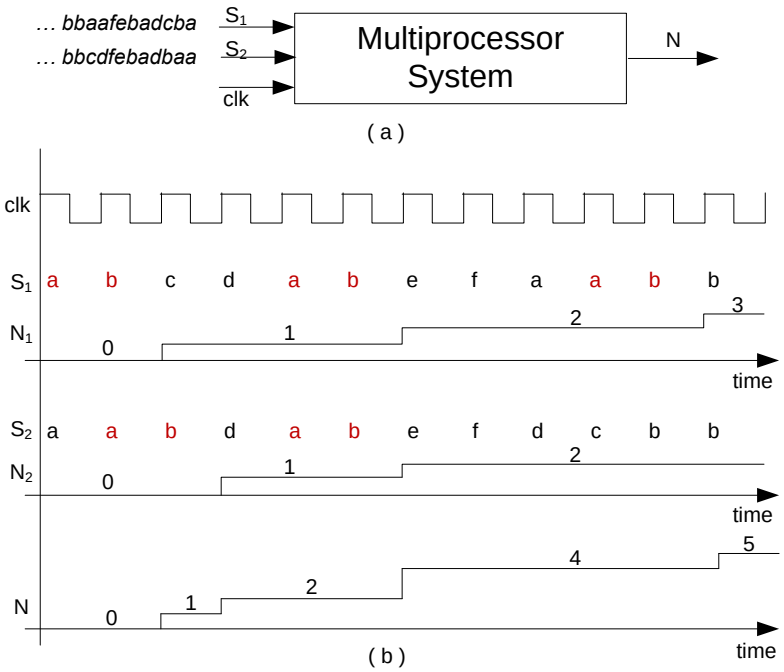

Figure 1

We assume the pattern size can be up to 64 characters. Both the input streams and the pattern are initially stored in separate files. To simulate the streamline behavior of the input, characters in the input file are dynamically fetched in sequence by the testbench and stored in a special small I/O register that can be accessed by the processor. You can also use the I/O register to load the string pattern into memory before execution.

The number of the pattern occurrences *N* is kept in the memory and should be updated in real time with the input. You are required to make the processing as real time as possible.

To make the design simple, you can assume each processor core has its own instruction memory, but the data memory should be shared.

Objectives

- To design an instruction set that is efficient, easy to implement, and allows the string search output as close to the real time as possible;
- To build a single core pipelined processor model for your instruction set;
- To build a multicore processor system based on the single core model;
- To simulate and verify your design; and
- To analyze the performance of your design.

Requirements

- Each project group is required to make a detailed project plan which includes:
    - tasks that need to be performed in order to complete this project,
    - schedule of the tasks,
    - role of each member for these tasks,
    - test method for each task, and
    - project management strategy to ensure that the project work is carried out smoothly and completed on time with a quality as good as possible.

The following serves as an example of some tasks (and suggestions) that you may consider for this project.

1. Developing a high-level program for the real-time string search function and running the program to generate results for a given input pattern.
2. Based on the high level program, developing an instruction set that provides the operations required by the program.
3. With the ISA designed in task 2, translating the high-level program into assembly code.
4. Building a single core processor (aiming to finish before Week 8)
    a. creating the hardware models for components to be used in the processor
    b. constructing datapath and control with these components
    c. determining the clock cycle time
    d. verifying the function of the pipeline
5. Building a two-core processor
    a. Identifying the potential issues with the multi-core processor for the string search problem.
    b. Developing a feasible solution
    c. Building the processor model
    d. Verifying the function of the model
6. Analysing the performance of the 2-core processor

Presentation

You and your group are required to present in Week 10 your group's design in three areas: a) ISA design, related assembly code, and the overall outcome of the project, b) the single core processor design and simulation result, and c) the multi-core processor design and simulation result. Each group is given 25 minutes. All members should work together for the presentation.

Presentations will be assessed by other groups and the lab tutor. The score sheets for the assessment will be available in Week 8.

Deliverables:

- Electronic copy of your HDL model
- Lab demonstration
- A report (about 8 pages, due in Week 10) that provides
    - Description of your design
    - Simulation results and discussion