數位電路設計 (Digital Circuit Design)

Lab2：組合電路之 HDL 模組撰寫與測試 (Writing and Testing the HDL Modules of Combinational Circuits)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉組合電路的設計原理，以 **gate-level modeling**、**dataflow modeling**、**behavioral modeling** 等不同方式撰寫其 HDL 電路模組，並撰寫測試模組。我們以減法器以及解碼器為設計實例，分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of Combinational Circuits. Please write their HDL circuit modules by gate-level modeling, dataflow modeling, and behavioral modeling, and write the testbench for these circuit modules. We take binary subtractor and line decoder for practice. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組（Design of the HDL Circuit Modules and Testbench)

A. 二元減法器之設計 (Design of Binary Subtractor)

(a) **半減器(Half Substractor)**：設計一個半減器(half subtractor, HS)，有兩個輸入變數及兩個輸出變數。輸入變數為被減數 x 與減數 y；輸出變數為差值 D 與借位輸出 B。

Design a half subtractor (HS) which has 2 input variables and 2 output variables. The input variables are the minuend (被減數) ***x*** and the subtrahend (減數) ***y***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請以 gate-level modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_gate_level(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_ gate_level.v。

Please write the Verilog circuit module in gate-level modeling. The

circuit module and port list should be named as Lab2_half_sub_gate_level(output D, B, input x, y), and its file should be named as Lab2_half_sub_gate_level.v .

ii. 請以 dataflow modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_dataflow(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_dataflow.v。
Please write the Verilog circuit module in dataflow modeling. The circuit module and port list should be named as Lab2_half_sub_dataflow(output D, B, input x, y), and its file should be named as Lab2_half_sub_dataflow.v .

iii. 請以 behavior modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_behavior(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_behavior.v。
Please write the Verilog circuit module in behavior modeling. The circuit module and port list should be named as Lab2_half_sub_behavior (output D, B, input x, y), and its file should be named as Lab2_half_sub_behavior.v .

iv. 請撰寫一測試模組來測試上述三個以不同方式撰寫之半減器電路模組，請將此測試模組命名為 t_Lab2_half_sub，檔案則命名為 t_Lab2_half_sub.v
Please write a testbench to test the half-substractor circuit module which is described in three different way above. The testbench module should be named as t_Lab2_half_sub, and its file should be named as t_Lab2_half_sub.v .

(b) 全減器(Full Substractor)：設計一個全減器(full subtractor, FS)，有三個輸入變數及兩個輸出變數。輸入變數為被減數 *x*、減數 *y*、及借位輸入 *z*；輸出變數為差值 *D* 與借位輸出 *B*。
Design a full subtractor (FS) which has 3 input variables and 2 output variables. The input variables are the minuend (被減數) ***x***, the subtrahend (減數) ***y***, and the borrow-in ***z***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請利用**(a)**中的 gate-level 半減器來建構全減器。請撰寫出全減器之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_full_sub(output D, B, input x, y, z)，檔案則命名為 Lab2_full_sub.v。

Please use the gate-level half-substractor designed in **(a)** to construct the full-substractor. Plase write the HDL circuit module of the full-substractor. The circuit module and port list should be named as Lab2_full_sub(output D, B, input x, y, z), and its file should be named as Lab2_full_sub.v.

ii. 請撰寫全減器之測試模組，命名為 t_Lab2_full_sub，檔案則命名為 t_Lab2_full_sub.v。
Please write the testbench of the full-substractor. The testbench module should be named as t_Lab2_full_sub, and its file should be named as t_Lab2_full_sub.v.

(c) **四位元漣波借位減法器(4-bit Ripple Borrow Subtractor, RBS)：**設計一個四位元漣波借位減法器，以產生兩個四位元二進位數字相減之結果。其輸入變數為四位元二進位被減數 ***X***、四位元二進位減數 ***Y***、及借位輸入 ***Bin***，輸出變數為四位元二進位差值 ***Diff*** 與借位輸出 ***Bout***。
Design a 4-bit binary subtractor which may produce the arithmetic difference of two 4-bit binary numbers. The input variables are the 4-bit binary minuend (被減數) ***X*** , the 4-bit subtrahend (減數) ***Y,*** and the borrow-in ***Bin***, and the output variables produce the 4-bit difference *Diff* and the borrow-out ***Bout***.

i. 利用**(b)**中之全減器來建構此 4-bit Ripple Borrow Subtractor (RBS)。請撰寫出此 RBS 之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_ripple_borrow_4_bit_sub (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案命名為 Lab2_ripple_borrow_4_bit_sub.v。
Please use the full substractor designed in **(b)** to construct the 4-bit Ripple Borrow Subtractor (RBS). Please write the HDL circuit module of the RBS. The circuit module and port list should be named as Lab2_ripple_borrow_4_bit_sub (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_ripple_borrow_4_bit_sub.v .

ii. 請撰寫此 RBS 之測試模組，至少以下述六組測資測試之。請將此測試模組命名為 t_Lab2_4_bit_sub，檔案則命名為 t_Lab2_ripple_borrow_4_bit_sub.v。
Please write the testbench of the RBS in which at least six test data showed in the following figure should be included. The testbench module should be named as t_Lab2_4_bit_sub, and its file should be named as t_Lab2_ ripple_borrow_4_bit_sub.v .

X	Y	Bin
1100	0101	1
1101	0110	0
0101	1101	0
0110	1101	1
1001	1001	0
0101	0101	1

B. 線解碼器之設計 (Design of Line Decoder)

(a) 具致能控制訊號之 2 至 4 線解碼器(2-to-4 line decoder with enable input)：設計一個 2×4 線解碼器，有兩個資料輸入、一個致能控制輸入、及四個輸出。資料輸入變數為二位元的 ***A***，致能控制輸入為一位元的 ***enable***，輸出變數為四位元的 ***Dout***。致能控制輸入及輸出均為 active-HIGH。此線解碼器之真值表如下所示：

Design a 2-to-4 line decoder which has two data inputs, one control input, and four outputs. The data inputs are a 2-bit variable ***A***, the control input is a 1-bit variable ***enable***, the outputs is a 4-bit variable ***Dout***. The enable line and the outputs are all active-HIGH. The truth table of this line decoder is given below:

enable	A[1]	A[0]	D[3]	D[2]	D[1]	D[0]
0	×	×	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

i. 請撰寫此 line decoder 之 Verilog 電路模組，模組名稱與 port list 請訂為 Lab2_decoder_2x4 (output [3:0] Dout, input [1:0] A, input enable)，檔案命名為 Lab2_decoder_2x4.v。

Please write the Verilog circuit module of this line decoder. The circuit module and port list should be named as Lab2_decoder_2x4 (output [3:0] Dout, input [1:0] A, input enable), and its file should be named as Lab2_decoder_2x4.v .

ii. 請撰寫一測試模組來完整測試上述之電路模組，並利用系統函式(Verilog system tasks)顯示出相對於輸入刺激(input stimuli)之輸出反應(output response)。請將此測試模組命名為 t_ Lab2_decoder_2x4，檔案則命名為 t_ Lab2_decoder_2x4.v。

Please write a testbench to test this line decoder circuit module. Display the output response with respect to the input stimuli by using Verilog system tasks, for examples, $display, $monitor, etc. The testbench module should be named as t_ Lab2_decoder_2x4, and its file should be named as t_ Lab2_decoder_2x4.v .

(b) 具致能控制訊號之 3 至 8 線解碼器(3-to-8 line decoder with enable input)：設計一個 3×8 線解碼器，有三個資料輸入、一個致能控制輸入、及八個輸出。資料輸入變數為三位元的 ***A***，致能控制輸入為一位元的 ***enable***，輸出變數為八位元的 ***Dout***。致能控制輸入及輸出均為 active-HIGH。

Design a 3-to-8 line decoder which has three data inputs, one control input, and eight outputs. The data inputs are a 3-bit variable ***A***, the control input is a 1-bit variable ***enable***, the outputs is a 8-bit variable ***Dout***. The enable line and the outputs are all active-HIGH.

i. 請撰寫此 line decoder 之 Verilog 電路模組，模組名稱與 port list 請訂為 Lab2_decoder_3x8 (output [7:0] Dout, input [2:0] A, input enable)，檔案命名為 Lab2_decoder_3x8.v。

Please write the Verilog circuit module of this line decoder. The circuit module and port list should be named as Lab2_decoder_3x8 (output [7:0] Dout, input [2:0] A, input enable), and its file should be named as Lab2_decoder_3x8.v .

i. 請撰寫一測試模組來完整測試上述之電路模組，並利用系統函式(Verilog system tasks)顯示出相對於輸入刺激(input stimuli)之輸出反應(output response)。請將此測試模組命名為 t_ Lab2_decoder_3x8，檔案則命名為 t_ Lab2_decoder_3x8.v。

Please write a testbench to test this line decoder circuit module. Display the output response with respect to the input stimuli by using Verilog system tasks, for examples, $display, $monitor, etc. The testbench module should be named as t_ Lab2_decoder_3x8, and its file should be named as t_ Lab2_decoder_3x8.v .

(c) 具致能控制訊號之 5 至 32 線解碼器(5-to-32 line decoder with enable input)：設計一個 5×32 線解碼器，有五個資料輸入、一個致能控制輸入、及三十二個輸出。資料輸入變數為五位元的 ***A***，致能控制輸入為一位元的 ***enable***，輸出變數為三十二位元的 ***Dout***。致能控制輸入及輸出均為 active-HIGH。

Design a 5-to-32 line decoder which has five data inputs, one control input, and thirty two outputs. The data inputs are a 5-bit variable ***A***, the control input is a 1-bit variable ***enable***, the outputs is a 32-bit variable ***Dout***. The enable line and the outputs are all active-HIGH.

i. 利用一個**(a)**中所設計的 2×4 線解碼器及四個**(b)**中所設計的 3×8 線解碼器來建構此 5×32 線解碼器。請撰寫出此 line decoder 之 Verilog 電路模組，模組名稱與 port list 請訂為 Lab2_decoder_5x32 (output [31:0] Dout, input [4:0] A, input enable)，檔案命名為 Lab2_ decoder_5x32.v。

Please use one 2-to-4 line decoder designed in **(a)** and four 3-to-8 line decoder designed in **(b)** to construct a 5-to-32 line decoder. Please write the Verilog circuit module of this line decoder. The circuit module and port list should be named as Lab2_decoder_5x32 (output [31:0] Dout, input [4:0] A, input enable), and its file should be named as Lab2_ decoder_5x32.v .

ii. 請撰寫一測試模組來完整測試上述之電路模組，並利用系統函式(Verilog system tasks)顯示出相對於輸入刺激(input stimuli)之輸出反應(output response)。請將此測試模組命名為 t_Lab2_ decoder_5x32，檔案則命名為 t_Lab2_ decoder_5x32.v。

Please write a testbench to test this line decoder circuit module. Display the output response with respect to the input stimuli by using Verilog system tasks, for examples, $display, $monitor, etc. The testbench module should be named as t_Lab2_ decoder_5x32, and its file should be named as t_Lab2_ decoder_5x32.v .

C. 注意事項：(Notes)

- 請用 ModelSim Student Edition 10.4a 做為開發環境。
  Develop your lab in ModelSim Student Edition 10.4.a.
- 請務必依照上述各項目之規定命名模組及檔案。
  Be sure to name the modules and files as described above.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar TestBench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：word 檔，命名為 Lab2_學號_姓名

包含下列項目：配分含隱藏測資之測試及 Demo 狀況

(1) 詳述半減器之電路設計流程，包括：真值表、布林代數式、邏輯電路圖。附上 2A(a)iv (半減器) 之模擬結果波形圖，並說明三個以不

同方式撰寫之半減器電路模組之波形圖是否有差異及是否正確。(20%)

(2) 詳述如何以半減器建構全減器，畫出電路方塊圖。附上 2A(b)ii (全減器) 之模擬結果波形圖，並說明是否正確。(15%)

(3) 詳述如何以全減器建構四位元漣波借位減法器，畫出電路方塊圖。附上 2A(c)ii (4-bit RBS) 之模擬結果波形圖，並說明是否正確。(15%)

(4) 詳述 2-to-4 線解碼器之電路設計，畫出電路方塊圖。附上 2B(a)ii (2-to-4 解碼器) 之模擬結果，並說明是否正確。(10%)

(5) 詳述 3-to-8 解碼器之電路設計，畫出電路方塊圖。附上 2B(b)ii (3-to-8 線解碼器) 之模擬結果，並說明是否正確。(15%)

(6) 詳述 5-to-32 線解碼器之電路設計，畫出電路方塊圖。附上 2B(c)ii (5-to-32 線解碼器) 之模擬結果，並說明是否正確。(15%)

(7) 心得與感想、及遭遇到的問題或困難 (10%)

Hand in a word file, named Lab2_StudentID_Name , including the following items: (Scores include answering problems in demo and the testing of extra data.)

(1) Describe the design process of the half substructor, including the truth table, the derived Boolean expressions, and the logic diagram. Attach the waveforms of the simulation results for the three modules of the half subtractor tested in 2A(a)iv, and determine whether the waveforms are correct or not and explain the difference of the waveforms, if any. (20%)

(2) Describe how do you construct the full substructor by using half subtractors as basic blocks and draw the block diagram of the circuit. Attach the waveform of the simulation results for the module of the full subtractor tested in 2A(b)ii, and explain whether it is correct or not. (15%)

(3) Describe how do you construct the 4-bit ripple-borrow subtractor by using full subtractors as basic blocks and draw the block diagram of the circuit. Attach the waveform of the simulation results for the module of the 4-bit RBS tested in 2A(c)ii, and explain whether it is correct or not. (15%)

(4) Describe the design process of the 2×4 line decoder in 2B(a) and draw the block diagram of the circuit. Attach the simulation results of the 2×4 decoder tested in 2B(a)ii, and explain whether it is correct or not. (10%)

(5) Describe the design process of the 3×8 line decoder in 2B(b) and draw the block diagram of the circuit. Attach the simulation results of the 3×8 decoder tested in 2B(b)ii, and explain whether it is correct or not. (15%)

(6) Describe the design process of the 5×32 decoder in 2B(c) and draw the block diagram of the circuit. Attach the simulation results of the 5×32 decoder tested in 2B(c)ii, and explain whether it is correct or

not. 15%)

(7) Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab. (10%)

B. Verilog modules 檔案繳交：14 files

Lab2_half_sub_gate_level.v、Lab2_half_sub_dataflow.v、
Lab2_half_sub_behavior.v、t_Lab2_half_sub.v、
Lab2_full_sub.v、t_Lab2_ full_sub.v、
Lab2_ripple_borrow_4_bit_sub.v、t_Lab2_ ripple_borrow_4_bit_sub.v、
Lab2_decoder_2x4.v、t_Lab2_decoder_2x4.v、
Lab2_decoder_3x8.v、 t_ Lab2_decoder_3x8.v、
Lab2_ decoder_5x32.v、t_Lab2_ decoder_5x32.v

Hand in the following Verilog modules: 14 files

Lab2_half_sub_gate_level.v, Lab2_half_sub_dataflow.v,
Lab2_half_sub_behavior.v, t_Lab2_half_sub.v,
Lab2_full_sub.v, t_Lab2_ full_sub.v,
Lab2_ripple_borrow_4_bit_sub.v, t_Lab2_ ripple_borrow_4_bit_sub.v,
Lab2_decoder_2x4.v, t_Lab2_decoder_2x4.v,
Lab2_decoder_3x8.v, t_ Lab2_decoder_3x8.v,
Lab2_ decoder_5x32.v, t_Lab2_ decoder_5x32.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (word file) and the corresponding HDL code (.v files) onto e-Campus platform.

- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab2_學號_姓名」的方式命名，如 ： 「Lab2_0416000_王大明」。
  Please compress the word file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file (rar file or other format is not accepted), and name the zip file as "Lab2_StudentID_Name" , for example, "Lab2_0416000_Kent Chang".

- 作業繳交截止日期為 **2017/5/14 (日) 23:59，不接受逾期繳交。**
  The deadline for handing in lab report and Verilog files is **May 14 (Sunday) 23:59. No late hand-in is allowed.**

- **Demo** 時間暫定為 **5/17 (三) 12:30pm~9:30pm**，之後會再發公告通知大家上網填寫 Demo 時間表。未繳交作業者，將無法參加 Demo；未 Demo 者，將不予計分。

  The **demo time** is arranged at **2017/5/17 (Wednesday) 12:30PM~9:30PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. Those who have not hand-in their lab reports and Verilog files will not be able to demo their work, and those who have not demo their lab units will get zero score.

- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。

  Any assignment work by fraud will get a zero point