數位電路設計 Digital Circuit Design

Lab0: ModelSim 之安裝與使用

(The Setup and Use of ModelSim)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉 ModelSim 的安裝與使用；我們將會提供一個電路模組檔案(*Simple_Circuit.v*)與一個測試檔案(*t_Simple_Circuit.v*)給同學，請同學按照實驗步驟執行，以便了解在 ModelSim 上的開發流程。

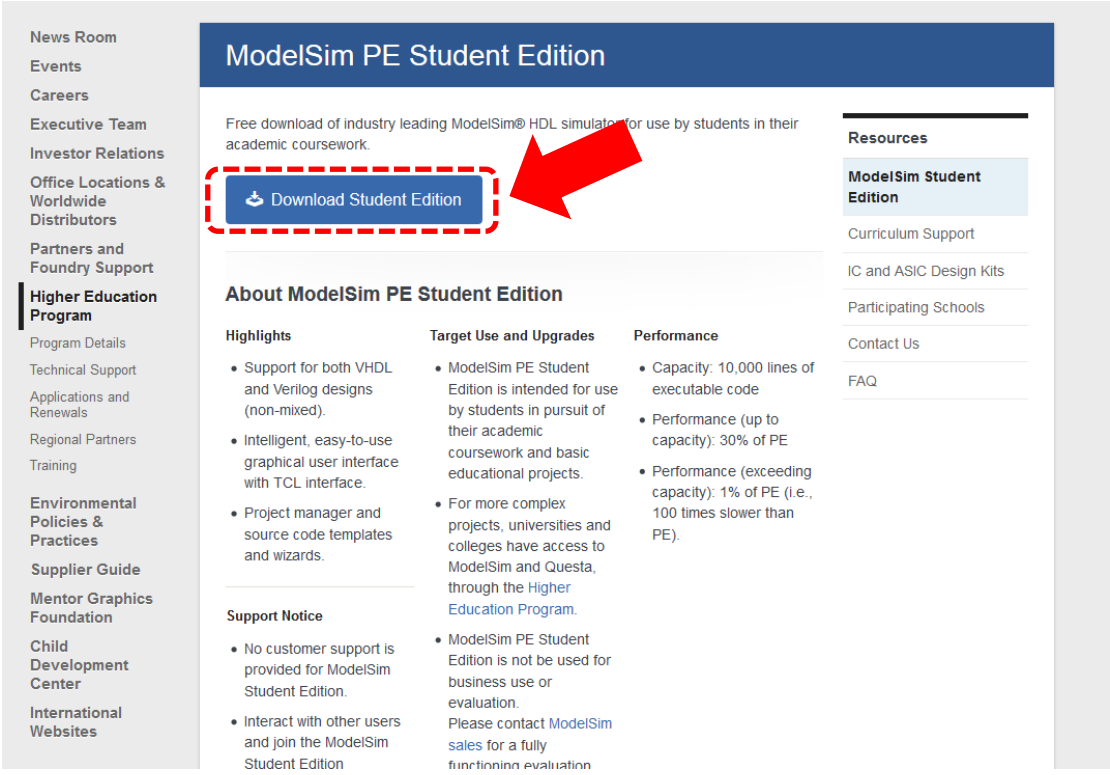
In this Lab, we hope that students could familiar with the installation and use of ModelSim. We will provide a circuit module file (*Simple_Circuit.v*) and a test file (*t_Simple_Circuit.v*) to students. Please the students to perform in accordance with the experimental procedure in order to understand the development process of ModelSim.

2. ModelSim 之下載、安裝及取得授權 (Download, Setup, and Authorization of ModelSim)

A. 下載 ModelSim (Download of ModelSim)

a. 連結至「http://www.mentor.com/company/higher_ed/modelsim-student-edition」頁面，如下圖所示：

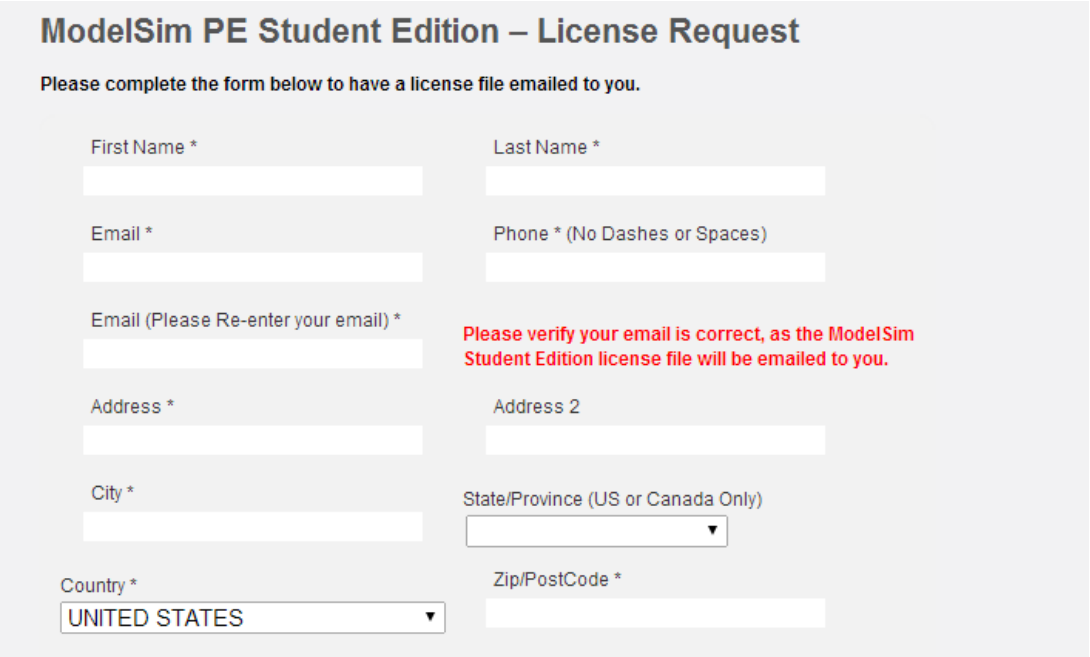
Connect to http://www.mentor.com/company/higher_ed/modelsim-student-edition, and the following page will be shown:



b. 點選頁面上的”Download”，下載並安裝 ModelSim PE Student Edition 10.4a。
Click the “Download” on the website to download and setup the ModelSim PE Student Edition 10.4a.

B. 取得授權 (Obtaining the Authorization)

a. 下載並安裝後，瀏覽器會跳出一個申請 license 的頁面，如下圖所示：
After Download and setup, the website will jump to the license application page, as shown in the following:



依照提示填好資料後，系統會將 license 寄至所填的 e-mail 信箱。請將其中的”student_license.dat”下載並複製到你的 ModelSim 資料夾(預設資料夾路徑是 C:\Modeltech_pe_edu_10.4a)。

After filling out the information in the page, the system will send the license to the e-mail address which you filled. Then, please download the “student_license.dat” and copy it to your ModelSim folder (the default path is “C:\Modeltech_pe_edu_10.4a”).

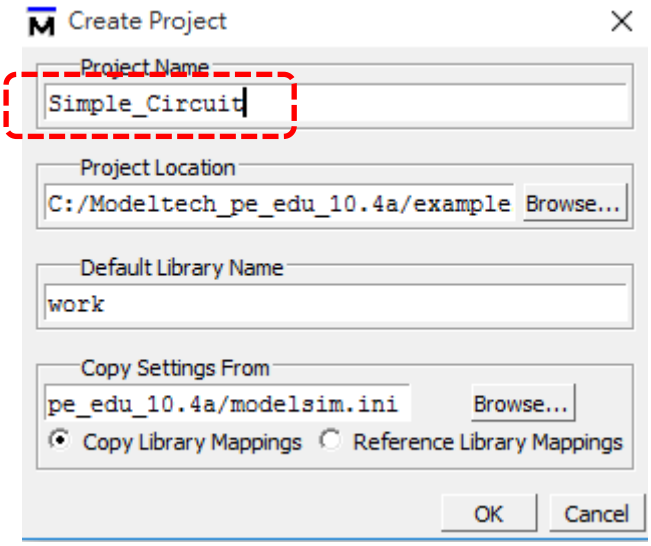
b. 點選桌面上的”ModelSim PE Student Edition 10.4a”即可開啟程式。
Click the “ModelSim PE Student Edition 10.4a” icon on your desktop to open it.

3. ModelSim 之專案建立、程式編譯及執行模擬 (Project Creation、Program Compilation and Simulation on ModelSim)

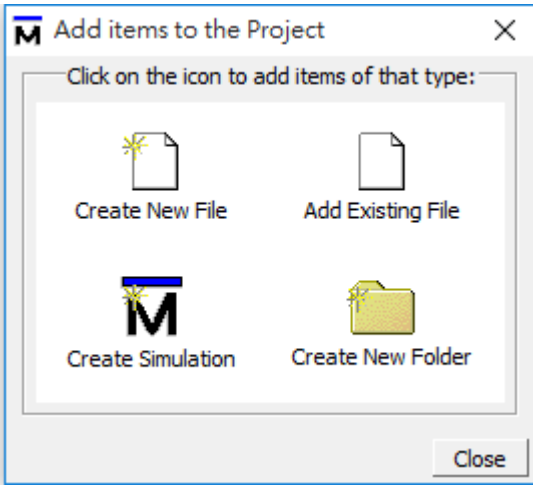
A. 建立專案&編譯程式 (Project Creation and Program Compilation)

a. 點選 ModelSim 工具列”File->new->project”，會出現以下視窗，填好 Project Name 後按 OK。
Click the toolbar of ModelSim ”File->new->project”, then the following

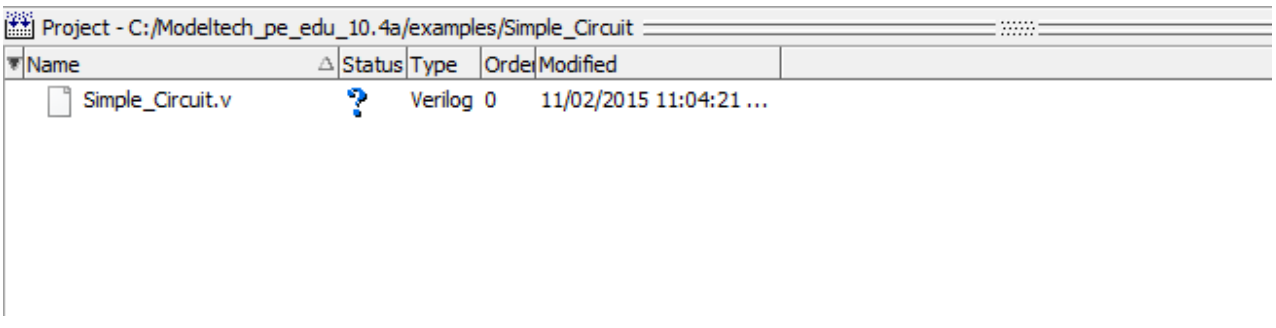
window will appear. Fill the Project Name, and then click “OK”.



b. 系統會詢問要加入專案的是 file 或 folder。在本次實驗中，請選擇「Add Existing File」，而後將所附的 *Simple_Circuit.v* 與 *t_Simple_Circuit.v* 加入專案。
System will ask you to add items (file or folder) to the project. In this lab, please choose ”Add Existing File”, and then add *Simple_Circuit.v* and *t_Simple_Circuit.v* to the project.

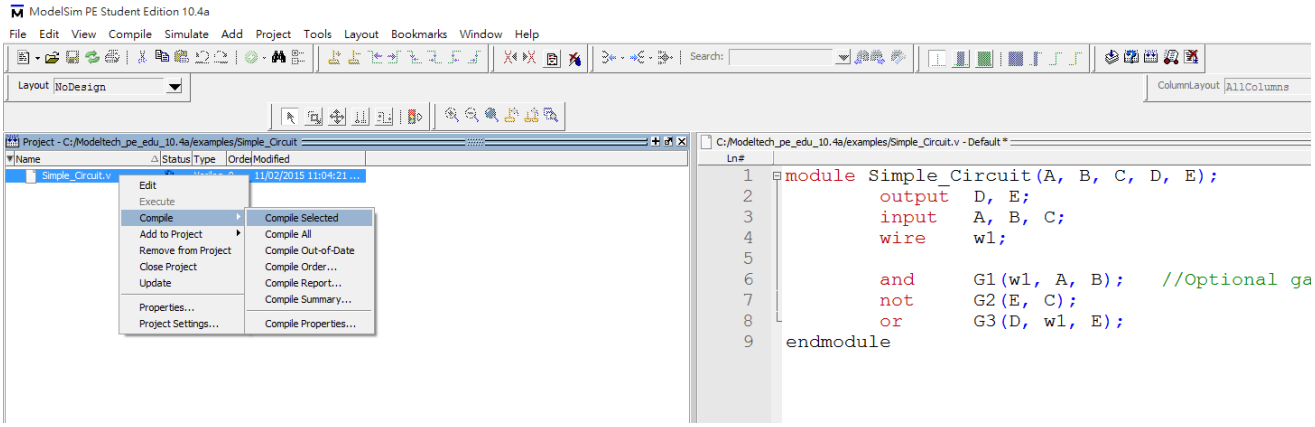


c. 首先，請加入 *Simple_Circuit.v*。之後即可在 Project 視窗中看到剛剛所開啟的 *Simple_Circuit.v* 檔，如下圖所示：
First, add *Simple_Circuit.v* to the project. After that, you can see the file on the project window as follows:



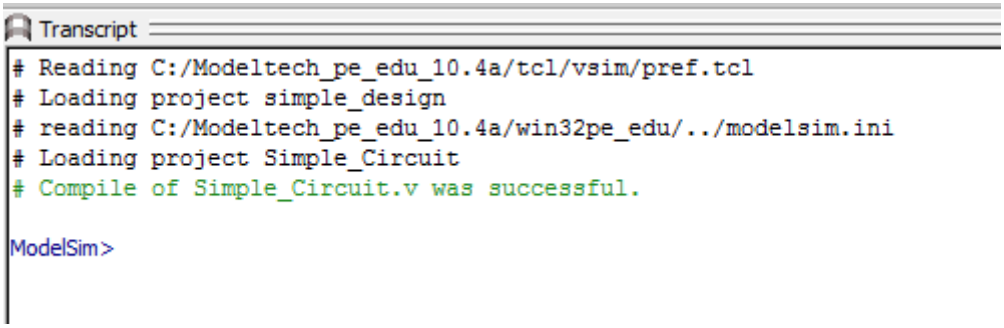
如需***編輯***此程式，請雙擊 Simple_Circuit.v 檔以顯示編輯視窗，如下圖右方所示。如需***編譯***此程式，請點擊後按右鍵選擇「Compile->Compile Selected」，如下圖左方所示；編譯後之模組預設的名稱為 *Simple_Circuit*。

If you need to edit the module, please double click the Simple_Circuit.v to display the edit window as shown in the right-hand side of the following figure. If you need to compile the module, please right-click to choose ”Compile->Compile Selected” as shown in the left-hand side of the following figure. After compilation, the default name of the compiled module will be *Simple_Circuit* .



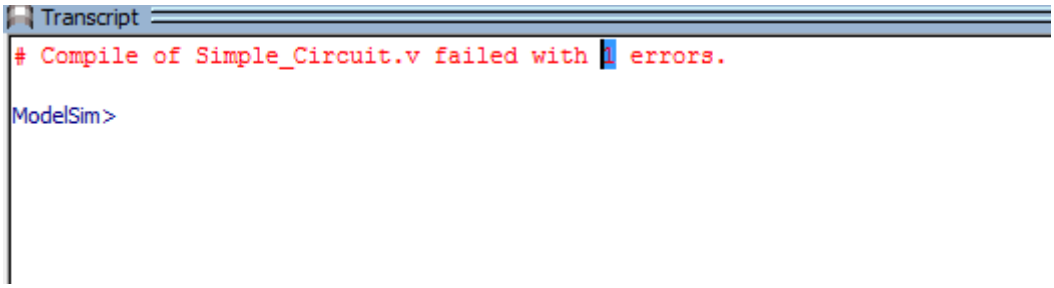
程式編譯後，左下角的 Transcript 視窗會顯示編譯結果；如果編譯成功，則會顯示如下圖所示。

After compiling the module, the lower left corner of the main screen, i.e., the Transcript window, will display the results of compilation. If the compilation succeeds, it will display the following information:



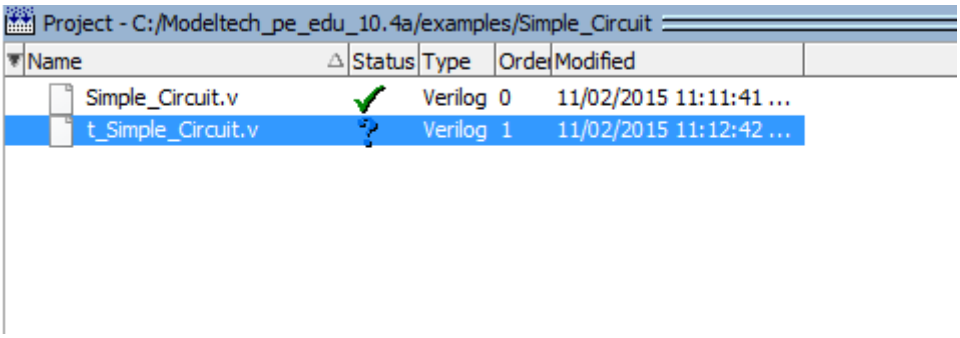
如果編譯失敗，則會顯示如下圖所示；雙擊紅字後，可查看編譯失敗之詳細訊息。繼續修改至編譯成功。

If the compilation fails, the following information will be displayed. Double-click the red words to see where the compilation fails, and then modify the module until the compilation succeeds.



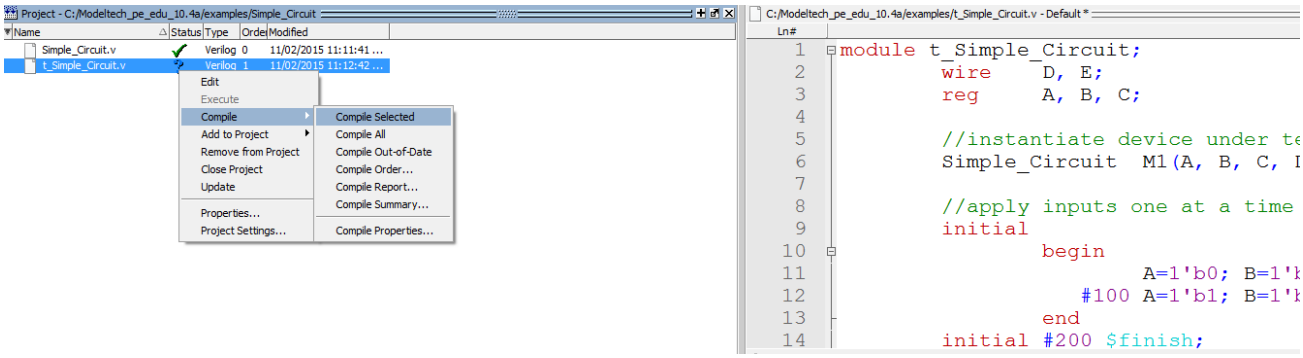
d. 接下來，請加入 *t_Simple_Circuit.v* 檔；在 Project 視窗中可看到新加入的檔案。

Then, add *t_Simple_Circuit.v* into the project and you will see the file on the Project window.



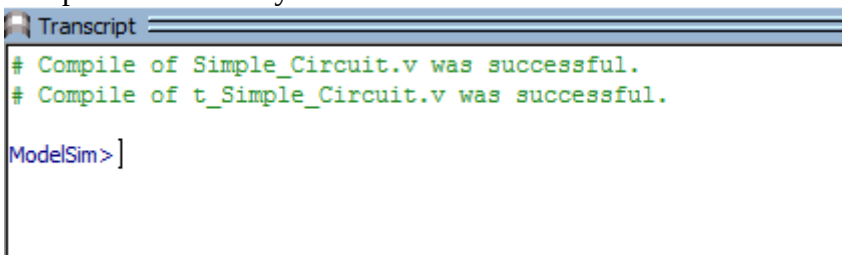
編譯 *t_Simple_Circuit.v* 檔，步驟同上(c)所述，顯示如下圖：

Compile the testbench *t_Simple_Circuit.v* by the same steps described in (c) and shown in the following figure:



修訂電路模組及測試模組，直到各個檔案都編譯成功。

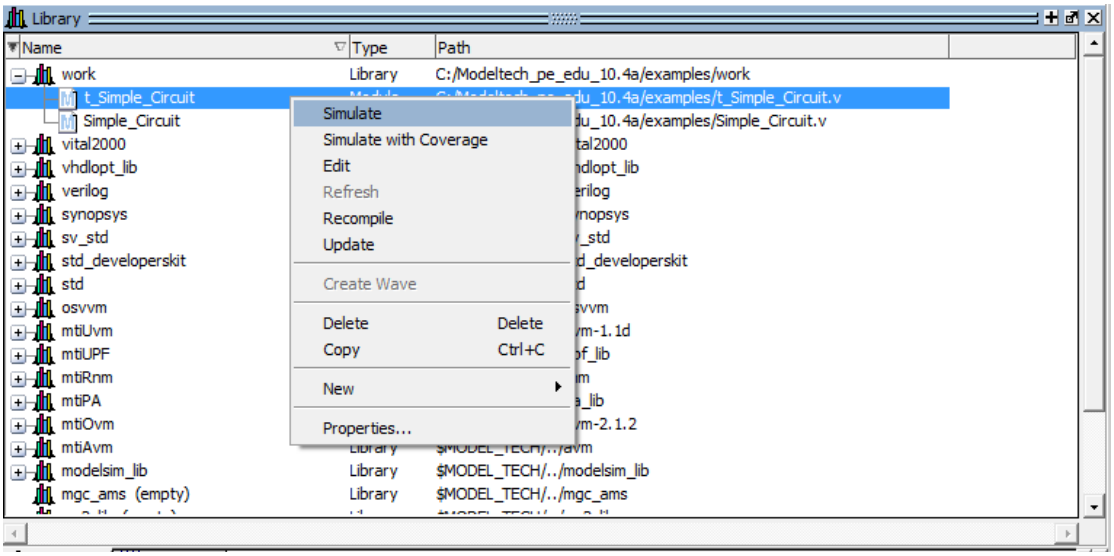
Modifying circuit modules and test modules until each of the modules is compiled successfully.



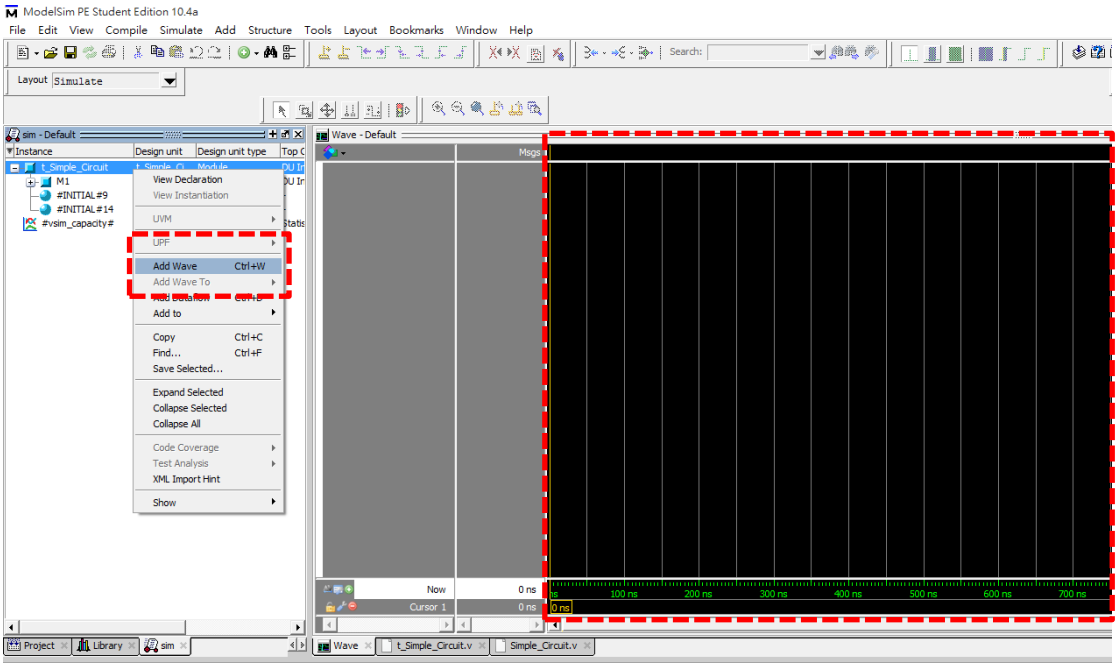
B. 執行模擬 (Simulation)

a. 將主視窗切到「Library」，展開「work」後可以看到剛剛編譯好的「*Simple_Circuit*」模組與「*t_Simple_Circuit*」。請直接執行測試模組「*t_Simple_Circuit*」進行測試。點選「***t_Simple_Circuit***」模組後按右鍵，可執行「Simulate」。

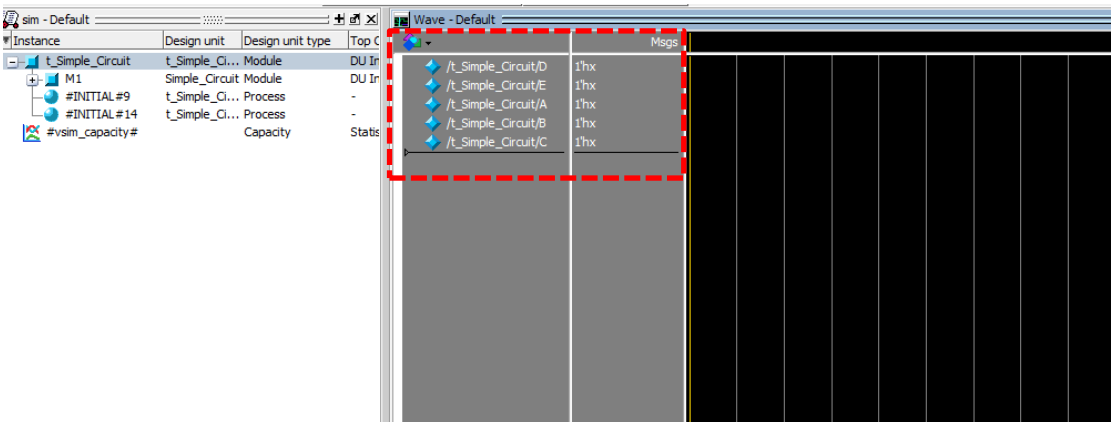
Switch the window to ”Library” . After expanding ”work” , you can see the “*Simple_Circuit*” and ”*t_Simple_Circuit*” modules which have been compiled successfully. Please simulate the compiled testbench ”*t_Simple_Circuit*” by right-clicking the **”*t_Simple_Circuit*”** and choose “Simulate” .



b. 執行後，如在測試模組點選右鍵「Add Wave」 (或是從上方工具列點選「Add→To Wave→All item in region」)，則可在下圖右方產生模擬波形圖：
After simulation, right-click the compiled testbench and choose “Add Wave” (or click the “Add→To Wave→All item in region” from the top toolbar). Then, the waveform of the simulation results will be shown on the right-hand side of the following window (the wave window):

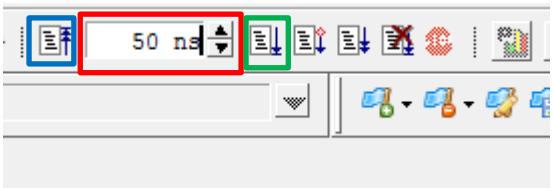


在 Wave 視窗中，可看到剛加入的 inputs 及 outputs，初始值皆為 1，如下圖紅框所示：
In the Wave window, the inputs and outputs simulated will be displayed with initial value to be 1 as shown in the following figure:



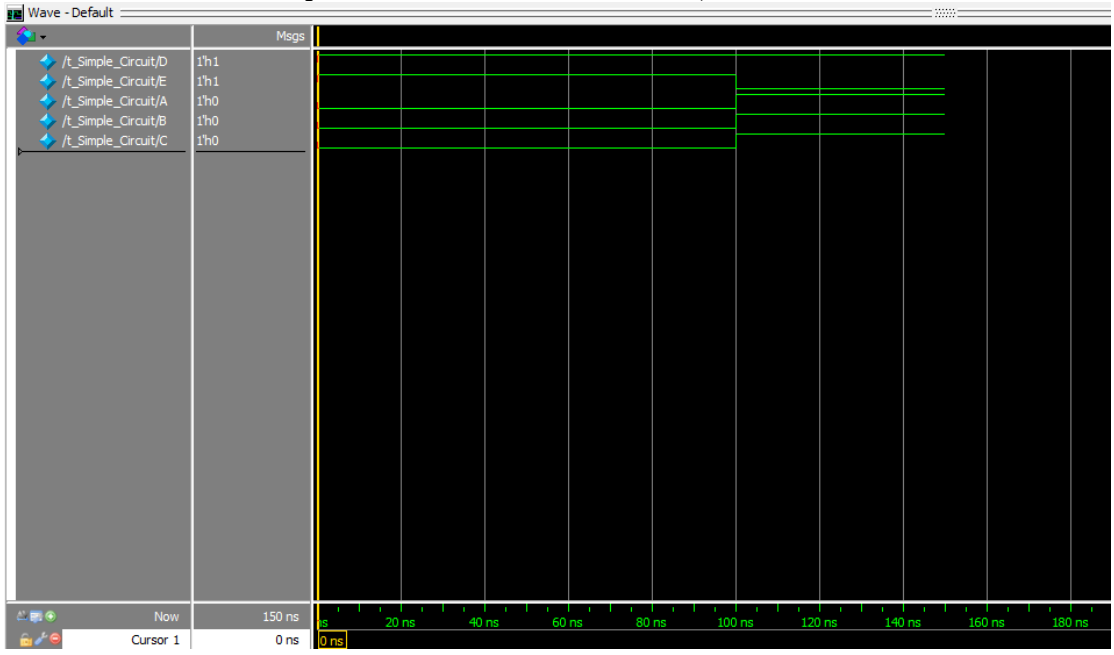
c. 設定每一次執行的時間間隔為 50ns(下圖紅色方框處)，之後每點擊一次「Run」(下圖綠色方框處)即可產生執行 50ns 後之模擬結果。如果想要重新執行，則可點擊「Restart」(下圖藍色方框處)來重設模擬結果。

Set the execution time interval to be 50ns, and then each click of the ”Run” (shown in green box of the following figure) will generate the result of the simulation for 50ns. If you want to restart the simulation, you can click the “Restart” (shown in blue box of following figure) to reset the simulation.



d. 最後可得到模擬出來的結果；下圖為「*t_Simple_Circuit*」模組執行 150ns 後的波形圖。(對波形圖按下 Ctrl+-可以放大或縮小範圍)

Finally, you can get the result of simulation. (In the following figure, it shows the simulation results of “*t_Simple_Circuit*” module for 150ns)



除了波形圖以外，在其下方的「Transcript」視窗可以看到執行的結果以及程式的輸出。如果沒有看到該視窗，則請至工具列點選「view→Transcript」即可顯示該視窗。

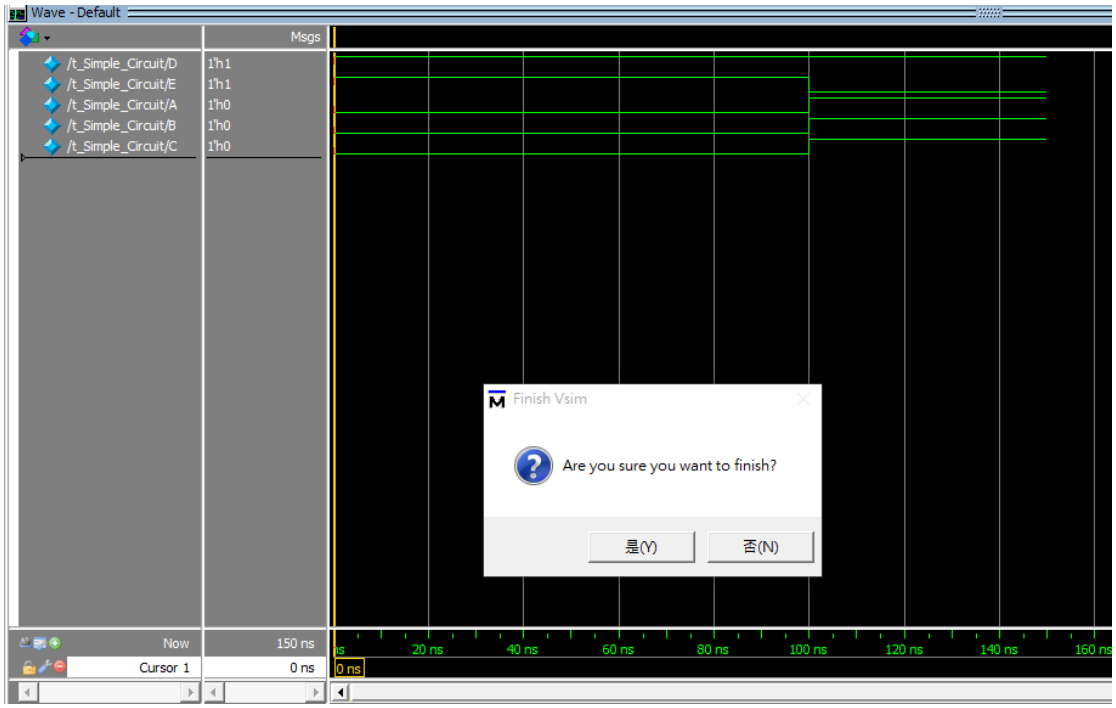
Besides the waveform, the ”Transcript” windows will display the result and the output of the program as shown in the following figure. If the Transcript window

does not appear, you can click “view→Transcript” on the toolbar.

```
Transcript
run
# ** Note: $finish    : C:/Modeltech_pe_edu_10.4a/examples/t_Simple_Circuit.v(14)
#    Time: 200 ns  Iteration: 0  Instance: /t_Simple_Circuit
# 1
# Break in Module t_Simple_Circuit at C:/Modeltech_pe_edu_10.4a/examples/t_Simple_Circuit.v line 14
run
run
VSIM 4> restart
VSIM 5> run
run
run
VSIM 6> run
# ** Note: $finish    : C:/Modeltech_pe_edu_10.4a/examples/t_Simple_Circuit.v(14)
#    Time: 200 ns  Iteration: 0  Instance: /t_Simple_Circuit
```

在所提供的測試模組 *t_Simple_Circuit.v* 中，已預設 200ns 時程式會結束($finish)。因此，執行至 200ns 時會跳出下圖視窗，若按下「是」，則會結束執行 ModelSim。若按下「否」，則可以繼續執行。完成後，請檢查波形圖是否正確。

In the testbench “*t_Simple_Circuit.v*” provided, it already have set 200ns for finishing the simulation ($finish). Therefore, when you perform to 200ns, the screen will appear the window which shown as follows. If press “yes”, the ModelSim will be terminated. If press “No”, you can continue the simulation. After finish your work, please check whether the result of waveform is correct or not.



4. 注意事項(Notes)

a. 本實驗單元為一人一組。

This lab unit is one student per group.

b. 本次作業無需繳交，但請於 **2017/3/24 (五)** 前完成上述實驗作業，以便進行後續的 Lab Units。

No hand-in is required for this lab, but please complete the experiment procedure describe above before **2017/3/24 (Friday)** for further Lab Units.