PCB Design Board Vesrsion_1

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1) Description the Board

- The board are used to human motion tracking system by used Inertial Measurement Unit (IMUs) are commonly used for movement classification intended as gait analysis. Where, IMUs measure and fuse the information obtained from the various kinds of sensors, such as accelerometers, gyroscopes, and magnetometers. the design of the related antenna capable of working properly despite the closeness to human skin, the optimization of the interface between sensors and radio front-end. Indeed, RFID guarantees adequate working distances of the order of a few meters and does not need the generation of a "power-hungry" radio carrier, thus allowing an extremely low-power data communication.

2) Create the Schematic

- The schematic has a many of block. First things first, we have a Battery charge block which contain that (TP4056) is a complete constant-current/constant-voltage linear charger for single cell lithium-ion batteries. Where, the charge voltage is fixed at 3.3V will give 3.3V for digital input the IMU and RF Module. This block other contains Step Up Converter (MT3608) will give 5V for all the digital parts.
- The next block is IMU 6050 block are commonly used for movement classification intended as gait analysis, due to its low cost and small size. We have the RF Module block a wireless sensing device Radio-Frequency IDentification (RFID) tag in the Ultra High-Frequency (UHF) band with IMU sensors could solve the problem.

❖The Schematic

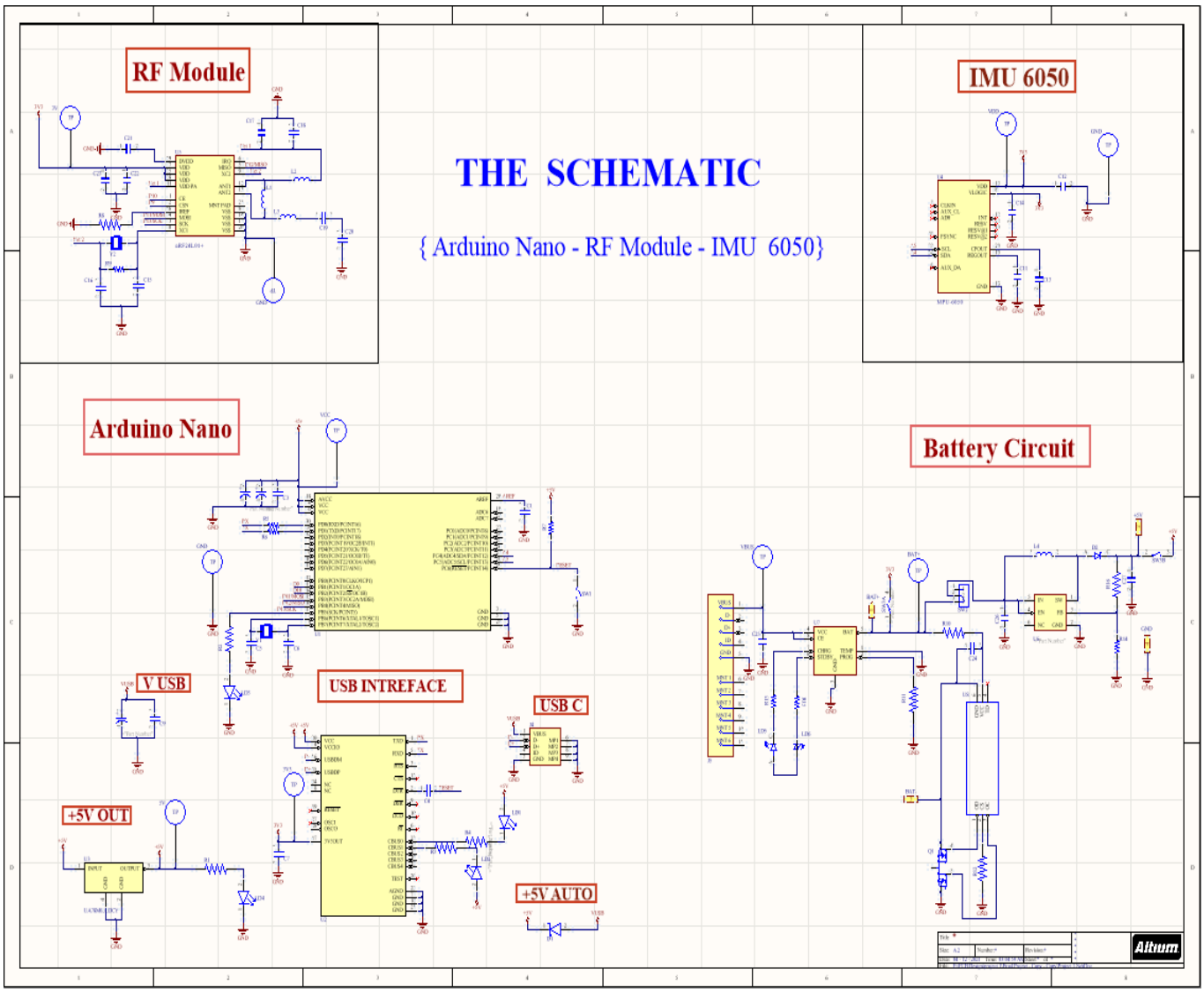


Fig 1. Schematic PCB Board.

3)Create the PCB

- **The PCB we've designed is 65 by 35 mm. The PCB thickness is 1.6mm, signal tracks are 0.15mm to conductor current (0.4862 Amps) and power tracks are 0.4mm to conductor current (0.8800 Amps).**

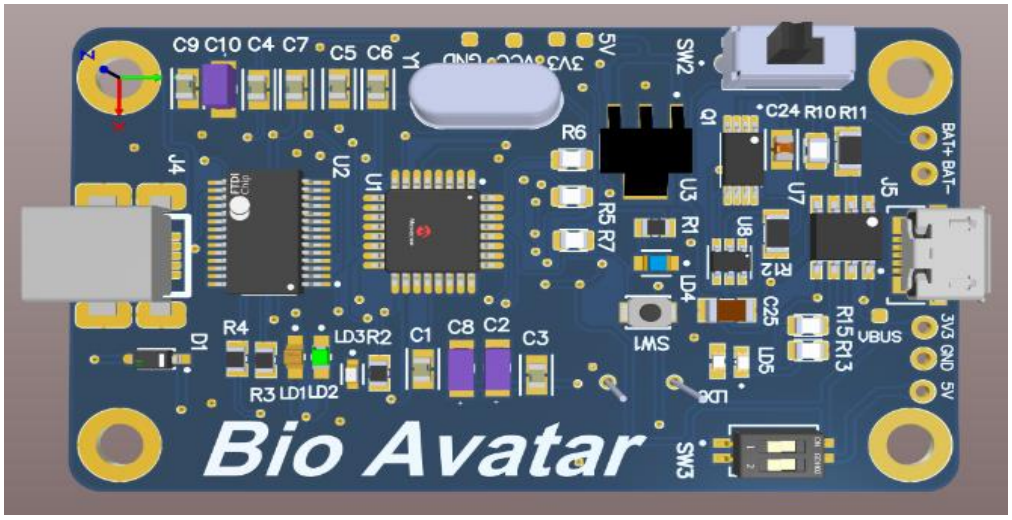


Fig 2. Top Layer Designed PCB Board.

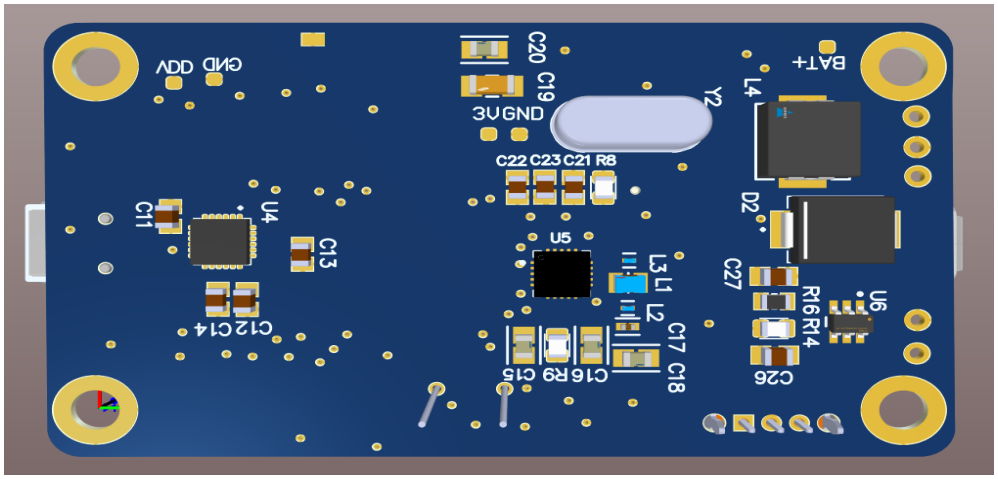


Fig 3. Bottom Layer Designed PCB Board.

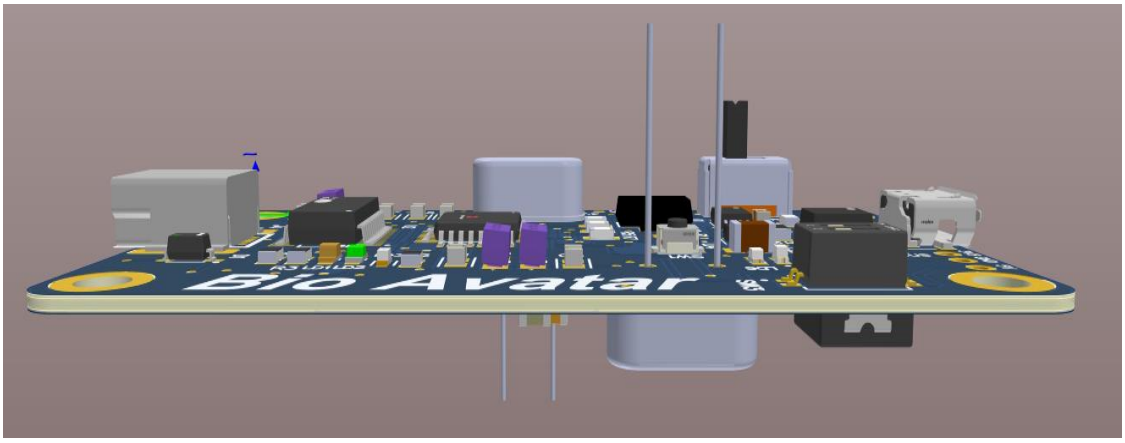


Fig 4. Side View of Designed PCB Board.

- **The Board consists of Multilayer PCB is more suitable for that face problems like noise, stray capacitance, crosstalk and the EMI shielding is easier and more flexible when power and ground layers are placed carefully.**
- **So that, the design consists of four layers is divide into Signals layers, Power and ground layers. {Signals /GND / Power /Signals}.**

- **Where:**

  - **A signal layer should always be close to a GND Plane to minimize electromagnetic radiation and crosstalk.**

  - **Power plane should also be adjacent close to Ground plane as this adds inter plane capacitance, which helps minimize power supply noise.**

- **Split Power Plane: the power (VCC) plane is split to 2 separate areas (3.3V – 5V), where the components are physically placed in different places on the board. Eliminating common return paths can be accomplished by splitting the power plane into separate areas.**

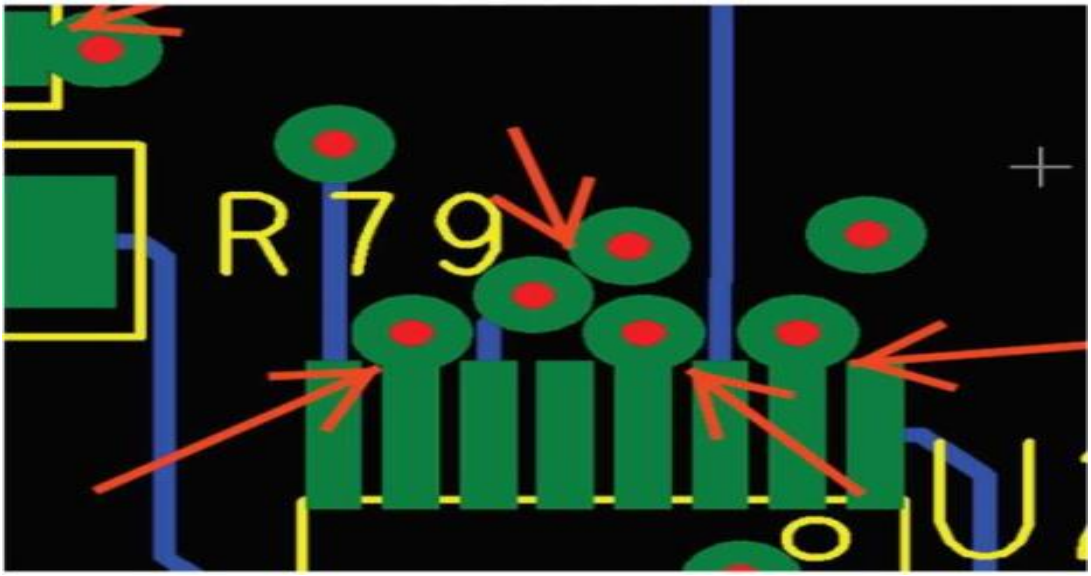
4) The Rules Usage for Design a PCB Board

The Rules Usage for Design a PCB Board				
Trace Data			**Via Properties**	
	Signal Trace	**Power Trace**		
Field	**Value**	**Value**	**Field**	**Value**
Required Trace Width (mm)	0.15	0.40	**Via Hole Diameter (mm)**	0.25
Conductor Current (Amps)	0.5	0.880	**Internal Pad Diameter (mm)**	0.51
Voltage Drop (Volts)	0.03	0.02	**Via Plating Thickness (mm)**	0.02
Power Dissipation (Watts)	0.017	0.019	**Power Dissipation (Watts)**	0.006
Resistance (Ohms)	0.06	0.02	**Via Current (Amps)**	2.01
Required Track Clearance (mm)	0.3			
Voltage Between Conductors (Volts)	3.3-5			
Plating Thickness (mm)	1			
Temperature Rise (C)	10			
Ambient Temperature (C)	25			
Conductor Length (mm)	25			
Layer Set	Multi-Layer (4)			

5) The Final Problems in PCB Design

❖ Problem (1): placing vias at the end of SMD pads

- **This is especially important if the vias are not masked-over. Placing vias too close to SMT pads will allow solder to migrate off the pad and through the via, resulting in a poor solder joint.**



- **Sol: Edge of via to edge of SMT pad should be (.025 mm \10 mil) or greater whenever possible, and masking over the via pad is recommended. So that, the distance between Edge of via to edge of SMT pad in this design 20 mil.**
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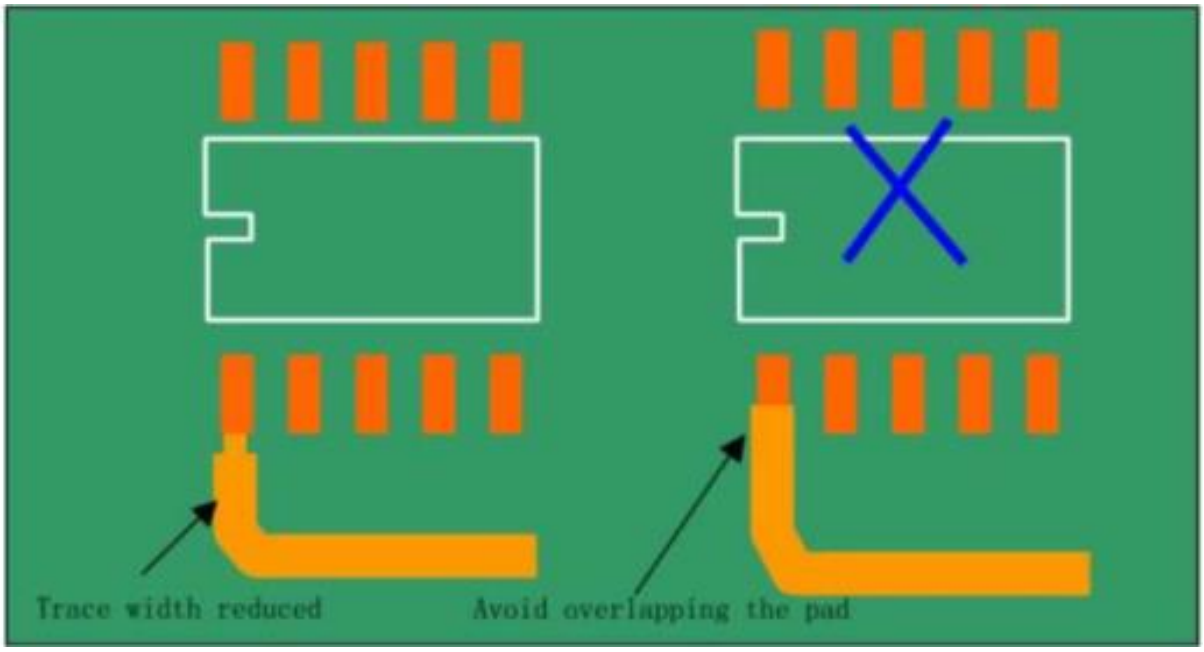
❖ Problem (2): Route Wide Traces into Narrow SMT Pads

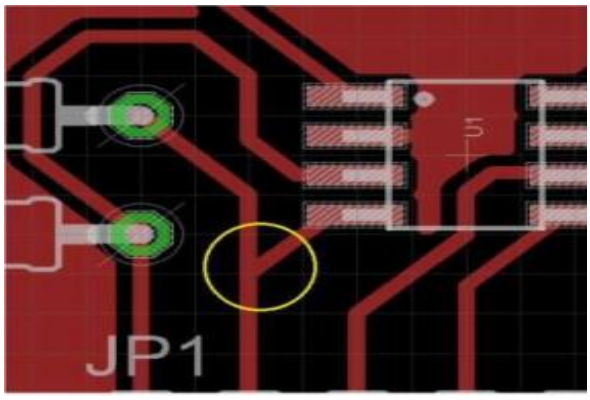
- **Traces which terminate at surface mount pads should be narrower than the pad itself. If the trace is wider, the soldermask aperture, rather than the pad area, will define the area to which surface finish will be applied to the PCB. The result will be insufficient paste coverage, because the stencil aperture size will match that of the pad only Using narrow traces also reduces the heat sink effect which can occur when wide traces are present.**

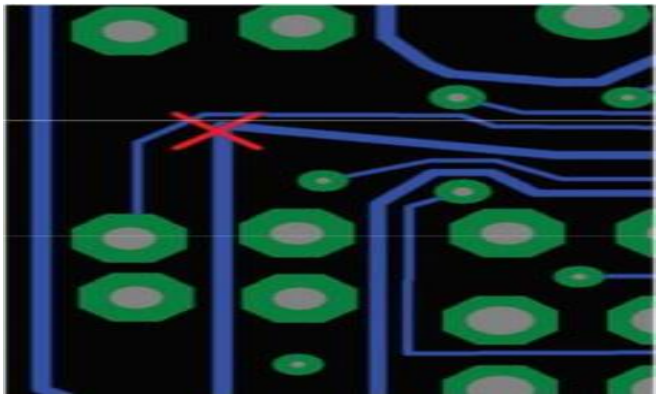


- **Sol:** **Traces which terminate at surface mount pads should be narrower than the pad itself. (Power Traces)**

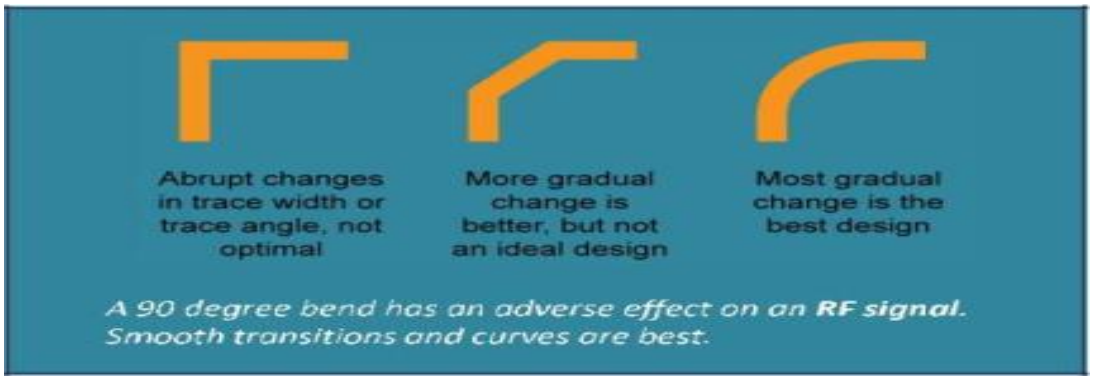
❖ Problem (3): Route Traces Along Sides of SMT Pads

- **Route traces into SMT pads mind way along one edge or the other. Some CAD systems will allow a small gap between the pad and the trace, with a short (0.005 or less) 90-degree connection to the pad. This can act as a tap for etchant, which will continue to eat away at the trace after the rinse cycle.**



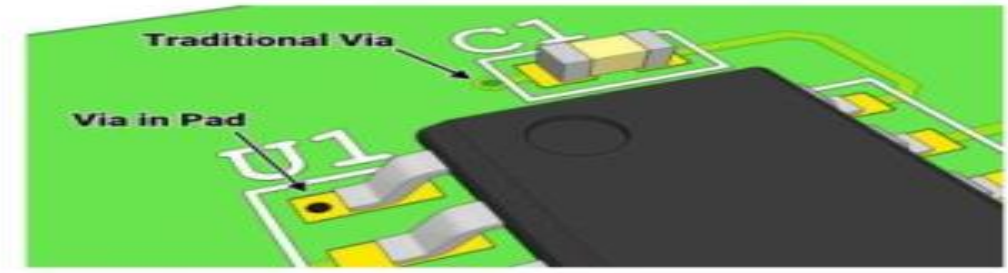


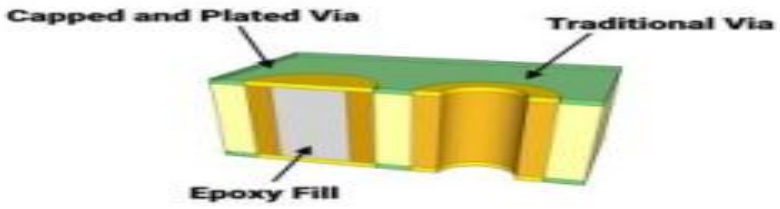
Sol: **Route All Traces at 90 Degree or Greater**



❖ Problem (4): Complex Processes Via In Pad

- **Vias in component pads will create a risk of leaking tin during the Solder process, which can cause shorts or corrupt pads.**

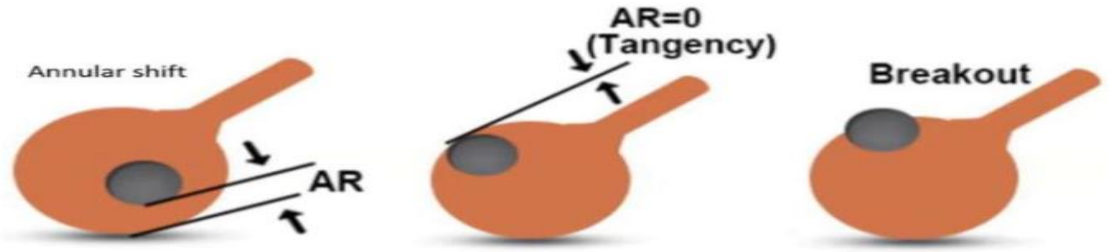




- **Sol: In order to stabilize the assembly process, vias in surface mount pads must be filled with epoxy, which requires additional cost and lead time. So that, the design avoiding this requirement complex process via in pad.**

❖ Problem (5): Annular Ring Size

- **Annular ring size is an important PCB design consideration since during PCB fabrication many conditions can cause holes to not be drilled perfectly centered. Therefore, it is necessary to design a sufficiently thick ring to allow for manufacturing tolerances and still produce a reliable electrical connection to the via. A small ring would put the via at risk of touching of the edge of the pad, which is called tangency or no longer being encircled by the pad at all. This is called an annular breakout.**



• Sol: Strong connection between a trace and hole

- **The general requirements for Lands with Holes, Lands shall be provided for each point of attachment of a part lead or other electrical connection to the printed board. Circular lands are most common, but it should be noted that other land shapes may be used to improve producibility. If breakout is allowed, modified land shapes shall be used. These may include, for example, filleting to create additional land area at the conductor junction, corner entry on rectangular land and Key Holing to create additional land area along the axis of the incoming lead.**

❖ Problem (6): Via Between Two SMD

- **It is generally a bad idea to place a via between two surface pads, this process increases a solder bridge process under the component. So that, the design avoiding this requirement complex process via between two SMD.**