Microprocessor and Interfacing
(MPI)
GTU # 3160712

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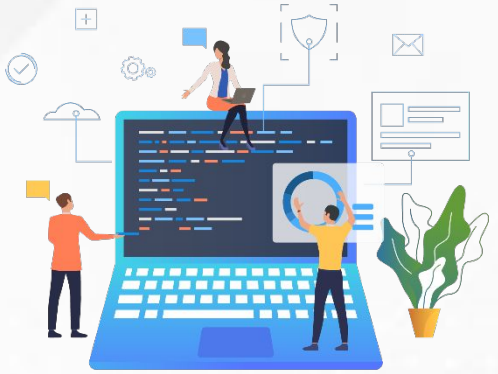
Unit-4: Assembly Language Programming Basics



PART-II: 8085 Assembly Program Basics

Prof. Swati R Sharma
Computer Engineering Department
Darshan Institute of Engineering & Technology, Rajkot

swati.sharma@darshan.ac.in
(O) 9727747317

Subject Overview

Sr. No.	Unit	% Weightage
1	Introduction to Microprocessor	8%
2	Microprocessor Architecture and Operations	7%
3	8085 Microprocessor	12%
4	**Assembly Language Programming Basics**	**13%**
5	8085 Assembly Language Programs	12%
6	Stack & Subroutines	13%
7	I/O Interfacing	20%
8	Advanced Microprocessors	15%

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Topics to be covered

- Addressing Modes in 8085
- 8085 Assembly Language Programs Basics
- 8085 Assembly Language Programs
  - ✔ Writing & Assembling the Programs
  - ✔ Executing the Programs
  - ✔ Debugging the Programs
- T-States & Machine Cycle of 8085 Instructions
- Timing Diagram

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Addressing Modes in 8085

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Addressing Modes in 8085

- Immediate Addressing Mode
- Direct Addressing Mode
- Register Addressing Mode
- Indirect Addressing Mode
- Implicit Addressing Mode

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Immediate Addressing Mode

- 8/16-bit **data** is specified in the instruction itself as one of its operand.
- **For example**:

```
MVI B,20H
LXI D,1034H
ADI 45H
SUI 30H
CPI 68H
```

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Direct Addressing Mode

- 8/16-bit memory address is directly provided with the instruction.
- **For example**:

```
LDA 1035H; here 1035 is 16-bit memory address
IN 02H   ; 02 is 8-bit I/O port address
OUT 03H     ; 03 is 8-bit I/O port address
```

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Register Addressing Mode

- It specifies register or register pair that contains data.
- **For example**:

```
MOV A,B   ; A ← B
ADD B ; A ← A+B
DAD H ; HL ← HL+RP
```

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Indirect Addressing Mode

- In this type of addressing mode, the 16-bit memory address is indirectly provided with the instruction using a register pair.
- **For example**:

```
LDAX D; A <- M[DE]
STAX B; A -> M[BC]
```

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Implicit/Implied Addressing Mode

- This mode doesn't require any operand; the data is specified by the Opcode itself.
- **For example**:

```
XTHL
SPHL
PCHL
```

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8085 Assembly Language Programs Basics

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Writing Assembly Language Programs

The steps to write Assembly Language Programs are as follows:

Step-1: Read the problem carefully.
Step-2: Break it down into small steps.
Step-3: Represent the sequence with flowchart.
Step-4: Translate flowchart into appropriate mnemonic instructions.
Step-5: Translate mnemonic into machine code.
Step-6: Enter machine code in memory and execute.
Step-7: Start troubleshooting-debugging a program

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Documentation

- Appropriate comments are critical for conveying the logic behind the program.
- The comment should explain what is intended; they should not explain mnemonics.
- Comment is optional.

Example:

```
MOV A,B    ; Move data from B to A                    X
MOV A,B    ; send data to accumulator for processing  ✓
```

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Program Execution

- Machine code can be loaded in R/W memory, with reference to starting memory location.
- Execution can be done in two ways:
  1. Execute entire code on click.
  2. Single step execution.
     - It will execute one instruction at a time.
     - We can observe the content of register and flag after execution of each instruction.

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Debugging Program

- Debug a program is similar to troubleshooting hardware.
- If the code doesn't work, it is essential to search carefully for errors in programming logic, machine codes and execution.

How to Debug machine code:

- Translating assembly to machine code is similar to building a circuit.
- Following errors are common:
  1. Writing a wrong code.
  2. Specifying the wrong jump location.
  3. Writing memory address in decimal, thus specifying wrong jump location.
  4. Writing lower order and higher order bits in wrong sequence.

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8085 Assembly Language Programs Basics

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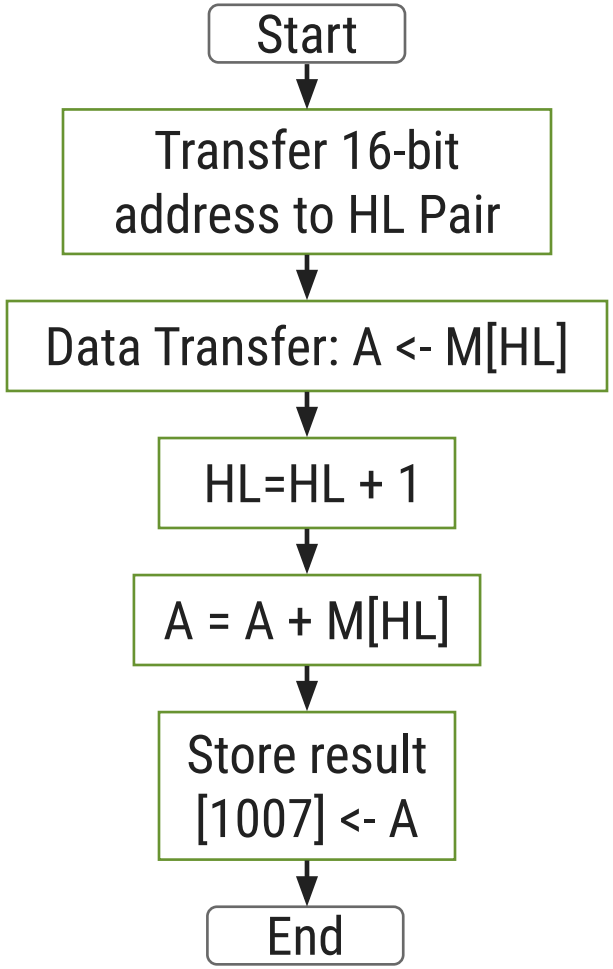
8085 Assembly Program: Add Two 8-bit Numbers

Write a program to add data at 1005H & 1006H memory location and store the result at 1007H memory location.

```
1. LXI H,1005   ; to retrive m/m addr
2. MOV A,M      ; retrieve m/m content
3. INX H        ; increment memeory to 1006H
4. ADD M        ; add accumulator with M[1006]
5. STA 1007     ; store result
6. HLT          ; HLT program
```



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8085 Assembly Program

Write a program to load register B with 37H and display number at the output Port 01

```
1.  MVI B,37    ; B <- 37H
2.  MOV A,B     ; A <- B for I/O processing
3.  OUT 01      ; PORT 01 <- A
4.  HLT
```

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T-States & Machine Cycle of 8085 Instructions

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Timing Cycle required by 8085 Instructions

Operation	T-States
Opcode Fetch	4-6T
Memory Read	3T
Memory Write	3T
I/O Read	3T
I/O Write	3T

- Instruction that require 5T-States for Opcode Fetch
  HLT
- Instructions that require 6T-States for Opcode Fetch
  1. CALL
  2. Conditional CALL
  3. DCX
  4. INX
  5. PCHL
  6. SPHL
  7. PUSH
  8. Conditional RET

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Machine Cycle required by 8085 Instruction

Operation	M/C
Fetch (F)	1
Memory Read (MEMR)	1
Memory Write (MEMW)	1
I/O Read (IOR)	1
I/O Write (IOW)	1
Read Immediate Data (R)	1

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Timing and Machine Cycle

1. **MOV B, D**

Machine Cycle:

1(F) = **1** Machine Cycle

Timing Cycle:

= **4T** (Fetch)

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Timing and Machine Cycle

2. MVI C ,17H

Machine Cycle: Fetch + R

1 + 1 = 2

Timing Cycle: Fetch + R

4T + 3T= 7T

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Timing and Machine Cycle

3. MVI M , 25H

Machine Cycle: Fetch + R+ Write data(MEMW)

1 + 1 + 1 = 3

Timing Cycle: Opcode Fetch + R + MEMW

4T + 3T + 3T = 10T

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Timing and Machine Cycle

4. MOV A,M

Machine Cycle: Fetch + Read Memory(MEMR)

1 + 1 = 2

Timing Cycle: Fetch + MEMR

4T + 3T = 7T

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Timing and Machine Cycle

4. MOV M, A

Machine Cycle: Fetch + Write Memory(MEMW)

1 + 1 = 2

Timing Cycle: Fetch + MEMW

4T + 3T = 7T

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Timing and Machine Cycle

5. NOP

Machine Cycle: Fetch

= 1 M/C Cycle

Timing Cycle: Fetch

= 4T

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Timing and Machine Cycle

6. HLT : Halt and enter wait state

Machine Cycle: Fetch + Wait

= 1 or more M/C Cycle

Timing Cycle: Fetch + Wait

= 5T or more T-States

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Timing and Machine Cycle

7. IN 18H

Machine Cycle: Fetch + R + IOR

= 1 + 1 + 1

= 3

Timing Cycle: Fetch + R + IOR

= 4T + 3T + 3T

= 10T

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Timing and Machine Cycle

8. OUT 19H

Machine Cycle: Fetch + R + IOW

= 1 + 1 + 1

= 3

Timing Cycle: Fetch + R + IOW

= 4T + 3T + 3T

= 10T

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Timing and Machine Cycle

9. ADD B

Machine Cycle: Fetch

= 1 Machine Cycle

Timing Cycle: Fetch

= 4T

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Timing and Machine Cycle

10. ADI 26H

Machine Cycle: Fetch + R

1 + 1 = 2

Timing Cycle: Fetch + MEMR

4T + 3T = 7T

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Timing and Machine Cycle

11. ADD M

Machine Cycle: Fetch + MEMR

1 + 1 = 2

Timing Cycle: Fetch + MEMR

4T + 3T = 7T

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Timing and Machine Cycle

12. SUB C

Machine Cycle: Fetch

= 1 Machine Cycle

Timing Cycle: Fetch

= 4T

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Timing and Machine Cycle

13. SUI 26H

Machine Cycle: Fetch + R

1 + 1 = 2

Timing Cycle: Fetch + MEMR

4T + 3T = 7T

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Timing and Machine Cycle

14. SUB M

Machine Cycle: Fetch + MEMR

1 + 1 = 2

Timing Cycle: Fetch + MEMR

4T + 3T = 7T

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Timing and Machine Cycle

15. LDA 2030H

Machine Cycle: Fetch + ReadL 8-bit + ReadH 8-bit +MEMR (content)

= 1 + 1 + 1 + 1

= 4

Timing Cycle: Fetch + MEMR + MEMR + MEMR

= 4T + 3T + 3T + 3T

= 13T

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Timing and Machine Cycle

16. POP R_P : POP B

Machine Cycle: Fetch + MEMR (SP) + MEMR (SP+1)

= 1 + 1 + 1

= 3

Timing Cycle: Fetch + MEMR + MEMR

= 4T + 3T + 3T

= 10T

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Timing and Machine Cycle

16. PUSH R_P : PUSH B

Machine Cycle: Fetch + MEMW (SP) + MEMW (SP-1)

= 1 + 1 + 1

= 3

Timing Cycle: Fetch + MEMW + MEMW

= 6T + 3T + 3T

= 12T

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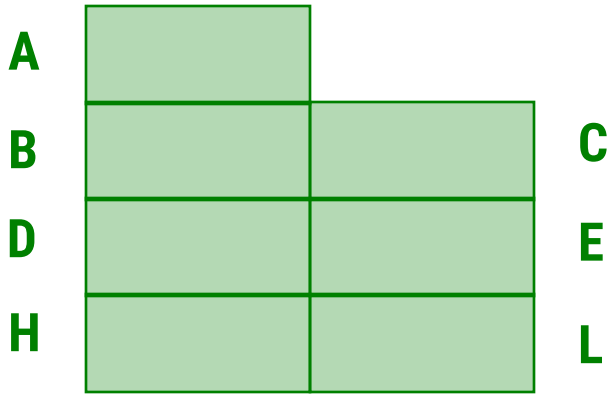
LHLD Instruction

Registers



LHLD **0006H**

Memory

02	0001
04	0002
0A	0003
06	0004
0F	0005
0D	0006 ←
05	0007 ←
03	0008

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Timing and Machine Cycle

17. LHLD 2034H

Machine Cycle: Fetch + MEMRL (20**34**) + MEMRH (**20**34)

+ MEMR_Content (**2034**)

+ MEMR_Content (**2035**)

= 1 + 1 + 1 + 1 + 1

= 5

Timing Cycle: Opcode Fetch+ MEMR + MEMR + MEMR + MEMR

= 4T + 3T + 3T + 3T + 3T

= 16T

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Timing and Machine Cycle

18. RAR

Machine Cycle: Fetch

= 1 Machine Cycle

Timing Cycle: Fetch

= 4T

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Timing and Machine Cycle

19. XTHL

Machine Cycle: Fetch + MEMR(SP)+MEMW(L)+ MEMR(SP+1)+MEMW(H)

= 1 + 1 + 1 + 1 + 1

= 5

Timing Cycle: Fetch+ MEMR + MEMW + MEMR + MEMW

= 4T + 3T + 3T + 3T + 3T

= 16T

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Timing and Machine Cycle

20. CALL 2030H

Machine Cycle: Fetch + MEMWL(**Store**) + MEMWH(**Store**)
+ MEMRL(**Call**) + MEMRH(**Call**)

= 1 + 1 + 1 + 1 + 1

= 5

Timing Cycle: Fetch+ MEMW + MEMW + MEMR + MEMR

= 6T + 3T + 3T + 3T + 3T

= 18T

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Timing and Machine Cycle

21. RET

Machine Cycle: Fetch + MEMR (SP) + MEMR (SP+1)

= 1 + 1 + 1

= 3

Timing Cycle: Fetch + MEMR + MEMR

= 4T + 3T + 3T

= 10T

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Exercise: Find Byte Size, Timing & Machine Cycle

1. LDAX B
2. SHLD 2470
3. SPHL
4. DAA
5. INR R/M
6. JMP
7. PCHL
8. CMP R/M
9. RRC
10. RIM
11. SIM
12. ORA R/M
13. XCHG
14. DI
15. EI

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Exercise Solution

Sr.	Instruction	Byte Size	Machine Cycle	T-States
1.	LDAX B	1	F+R=2	4T+3T=7T
2.	SHLD 2470	3	F+R+R+W+W=5	4T+3T+3T+3T+3T=16T
3.	SPHL	1	F=1	6T
4.	DAA	1	F=1	4T
5.	INR R INR M	1 1	F=1 F+R+W=3	4T 4T+3T+3T=10T
6.	JMP 2030	3	F+R+R=3	4T+3T+3T=10T
7.	PCHL	1	F=1	6T
8.	CMP R CMP M	1 1	F=1 F+R=2	4T 4T+3T=7T
9.	RRC	1	F=1	4T
10.	RIM	1	F=1	4T

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Exercise Solution

Sr.	Instruction	Byte Size	Machine Cycle	T-States
11.	SIM	1	F=1	4T
12.	ORA R ORA M	1 1	F=1 F+R=2	4T 4T+3T=7T
13.	XCHG	1	F=1	4T
14.	DI	1	F=1	4T
15.	EI	1	F=1	4T

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Timing Diagram

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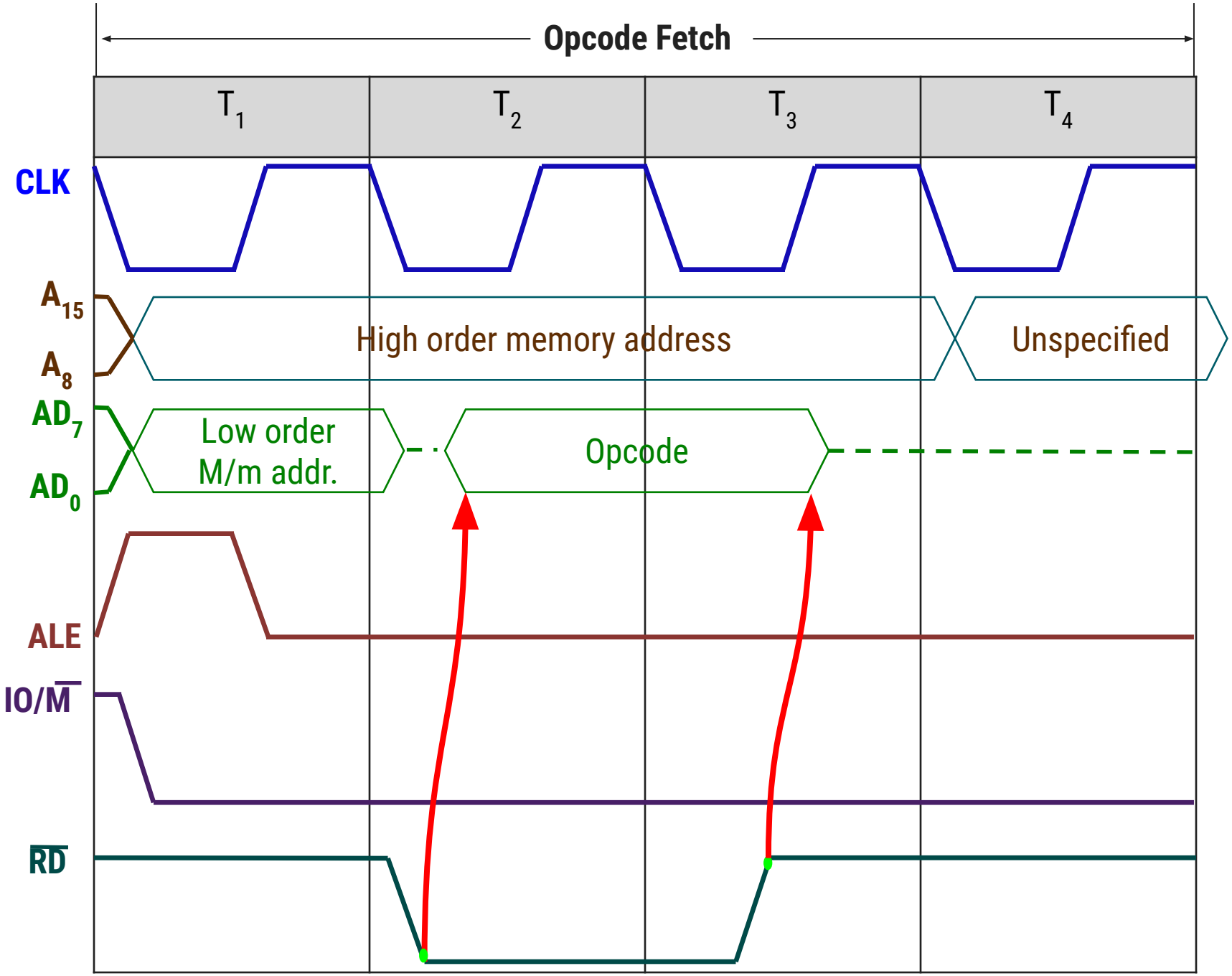
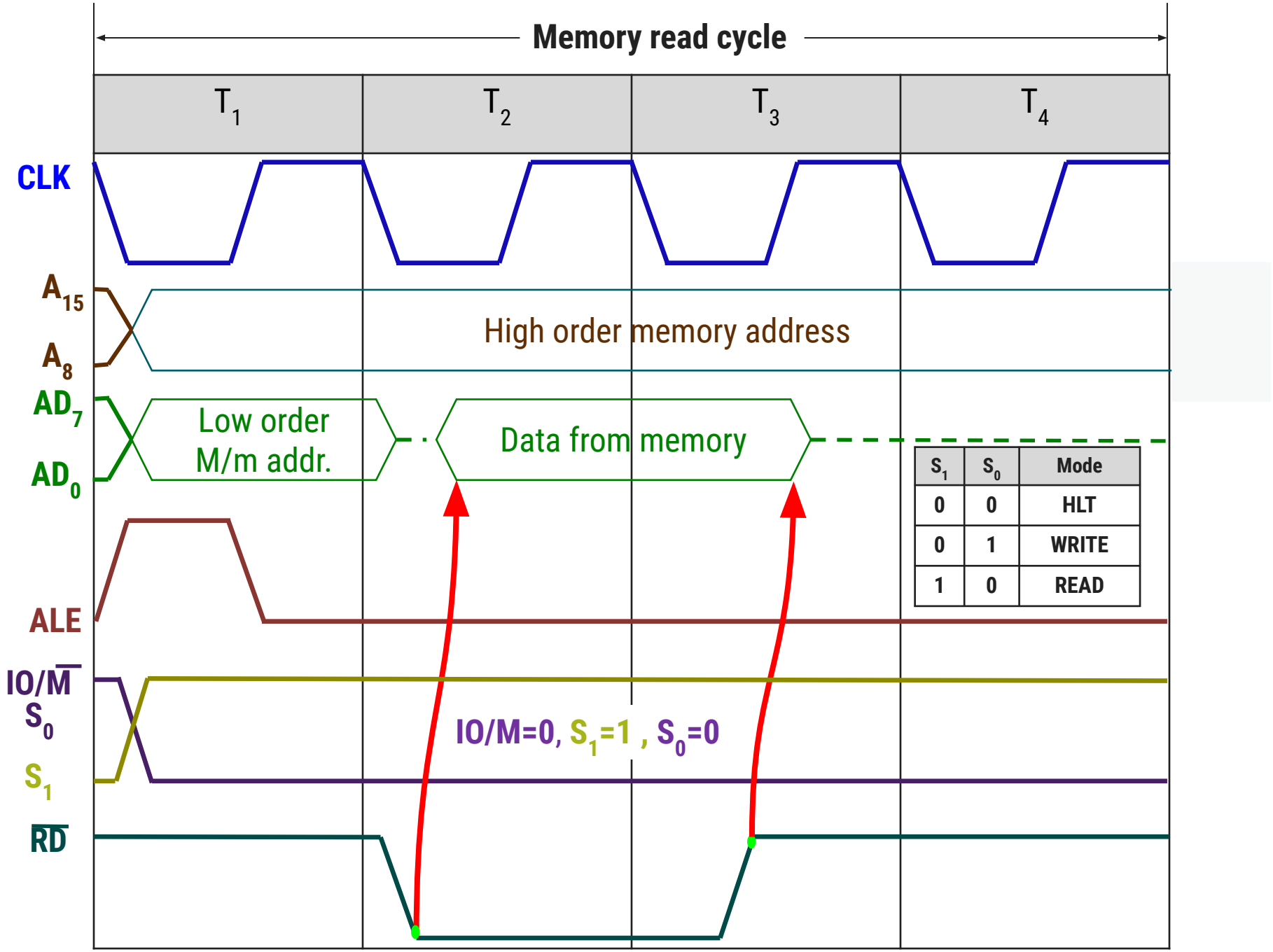
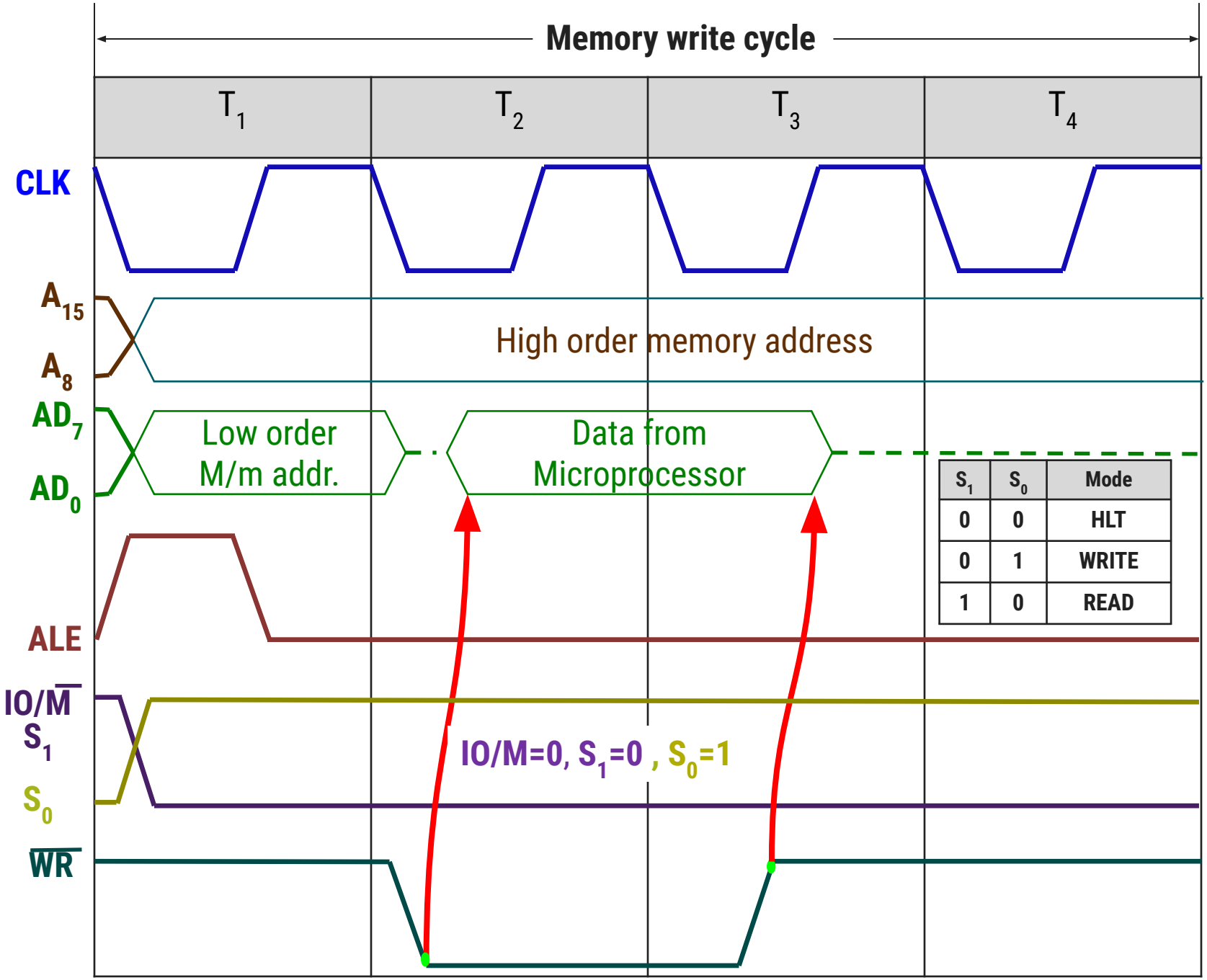
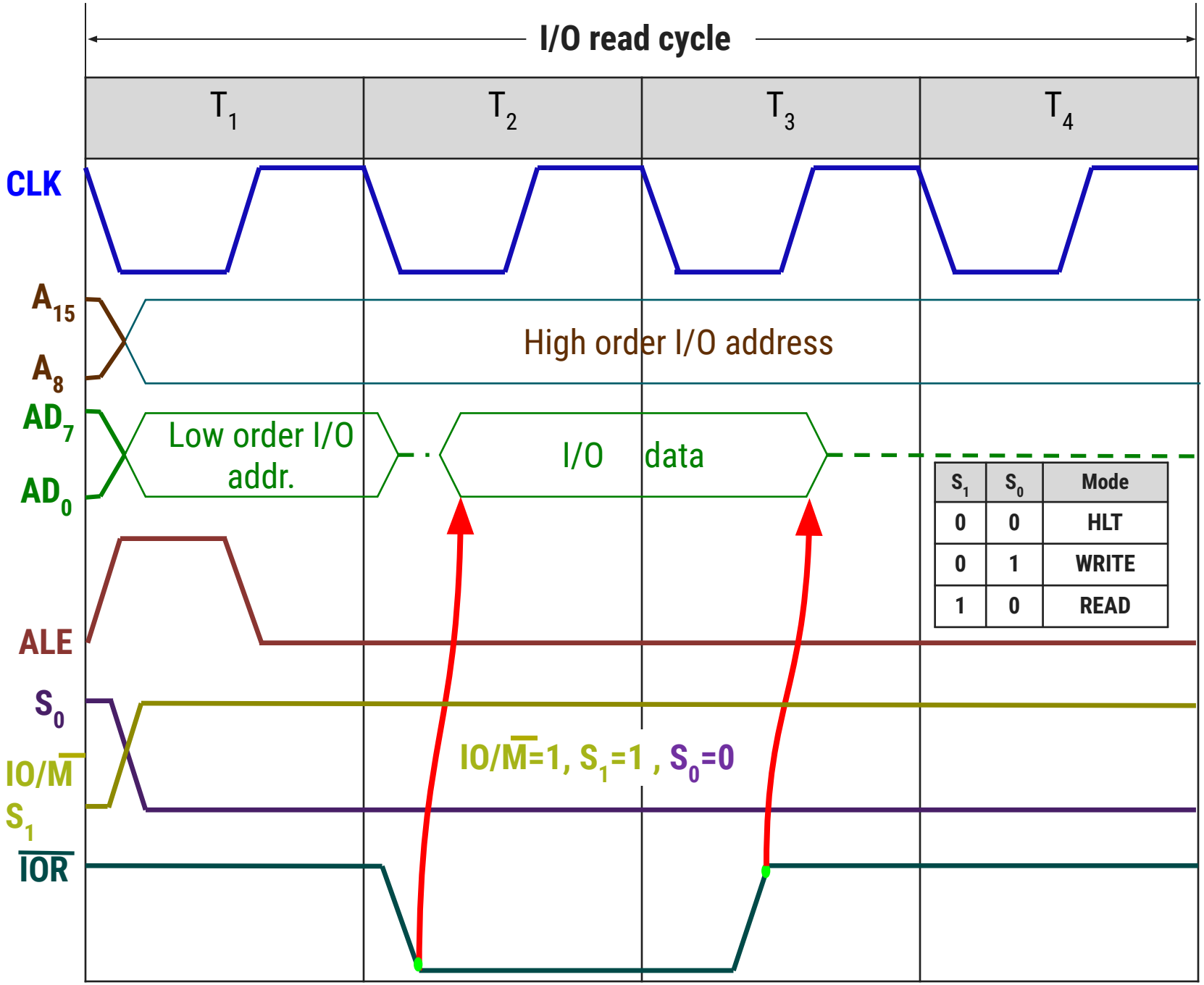
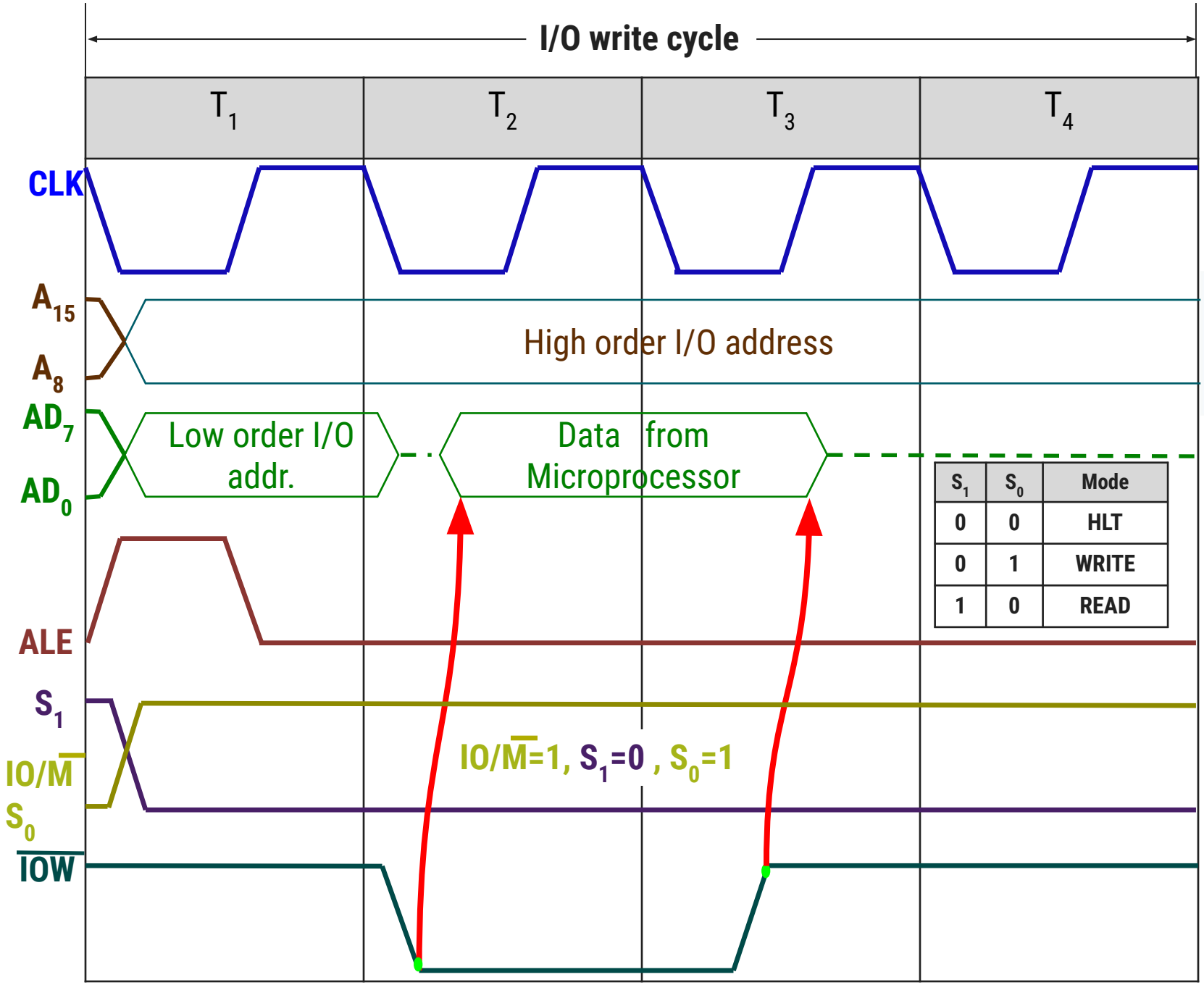

Opcode Fetch
T1
T2
T3
T4
CLK
A15
A8
High order memory address
Unspecified
AD7
AD0
Low order
M/m addr.
Opcode
ALE
IO/M
RD


Memory read cycle
T1
T2
T3
T4
CLK
A15
A8
High order memory address
AD7
AD0
Low order M/m addr.
Data from memory
ALE
IO/M
S0
S1
RD
IO/M=0, S1=1 , S0=0
S1 S0 Mode
0 0 HLT
0 1 WRITE
1 0 READ

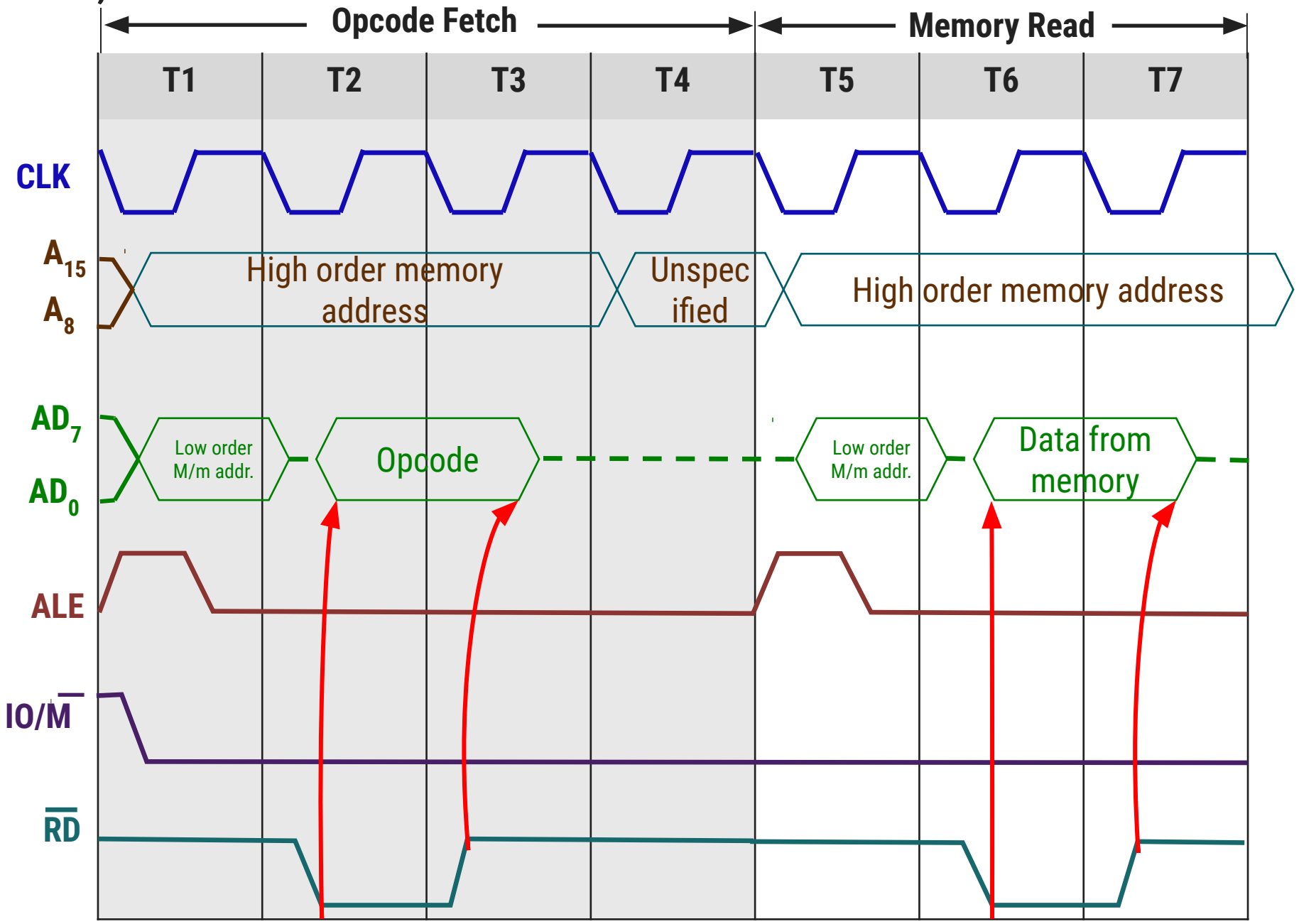

Memory write cycle
T1
T2
T3
T4
CLK
A15
A8
High order memory address
AD7
AD0
Low order M/m addr.
Data from Microprocessor
ALE
IO/M
S1
S0
IO/M=0, S1=0 , S0=1
WR
S1 S0 Mode
0 0 HLT
0 1 WRITE
1 0 READ


I/O read cycle
T1
T2
T3
T4
CLK
A15
A8
High order I/O address
AD7
AD0
Low order I/O addr.
I/O data
ALE
S0
IO/M
S1
IOR
IO/M=1, S1=1 , S0=0
S1 S0 Mode
0 0 HLT
0 1 WRITE
1 0 READ

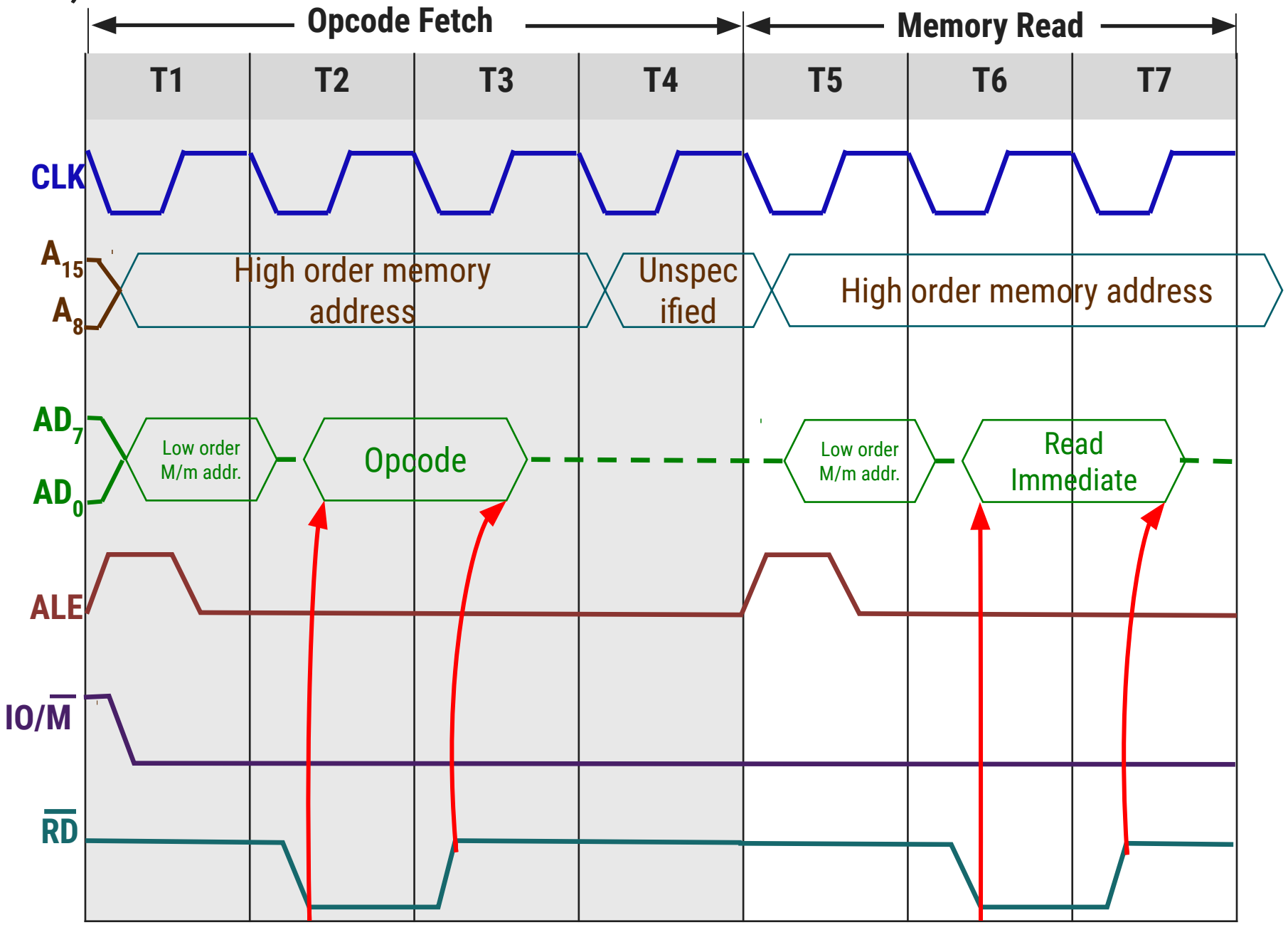


S_1	S_0	Mode
0	0	HLT
0	1	WRITE
1	0	READ

Timing Diagram : MOV B,M



Timing Diagram : MVI A, 32H



Calculate Execution time of MVI A,32H

Given: Clock Frequency (f) = 2 MHz

Calculation:

Step-1: T-state = clock period = $\frac{1}{f} = \frac{1}{2}$ = **0.5 μsec**

Step-2: Execution time for Opcode Fetch

= 4T x 0.5 = **2μsec**

Step-3: Execution time for Memory Read

= 3T x 0.5 = **1.5μsec**

Step-4: Execution time for Instruction

= (4T + 3T) x 0.5

= 7T x 0.5

= **3.5μsec**

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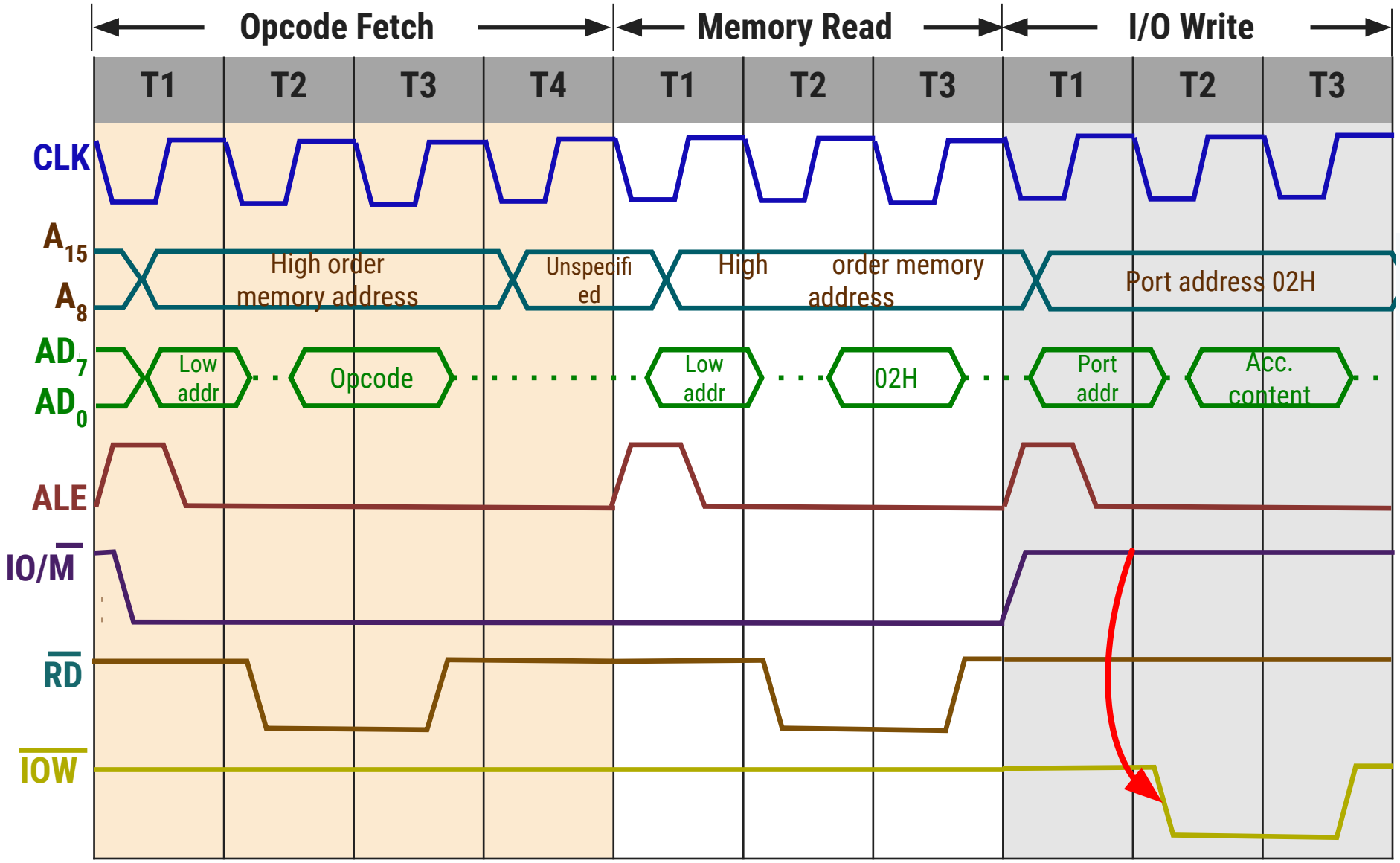
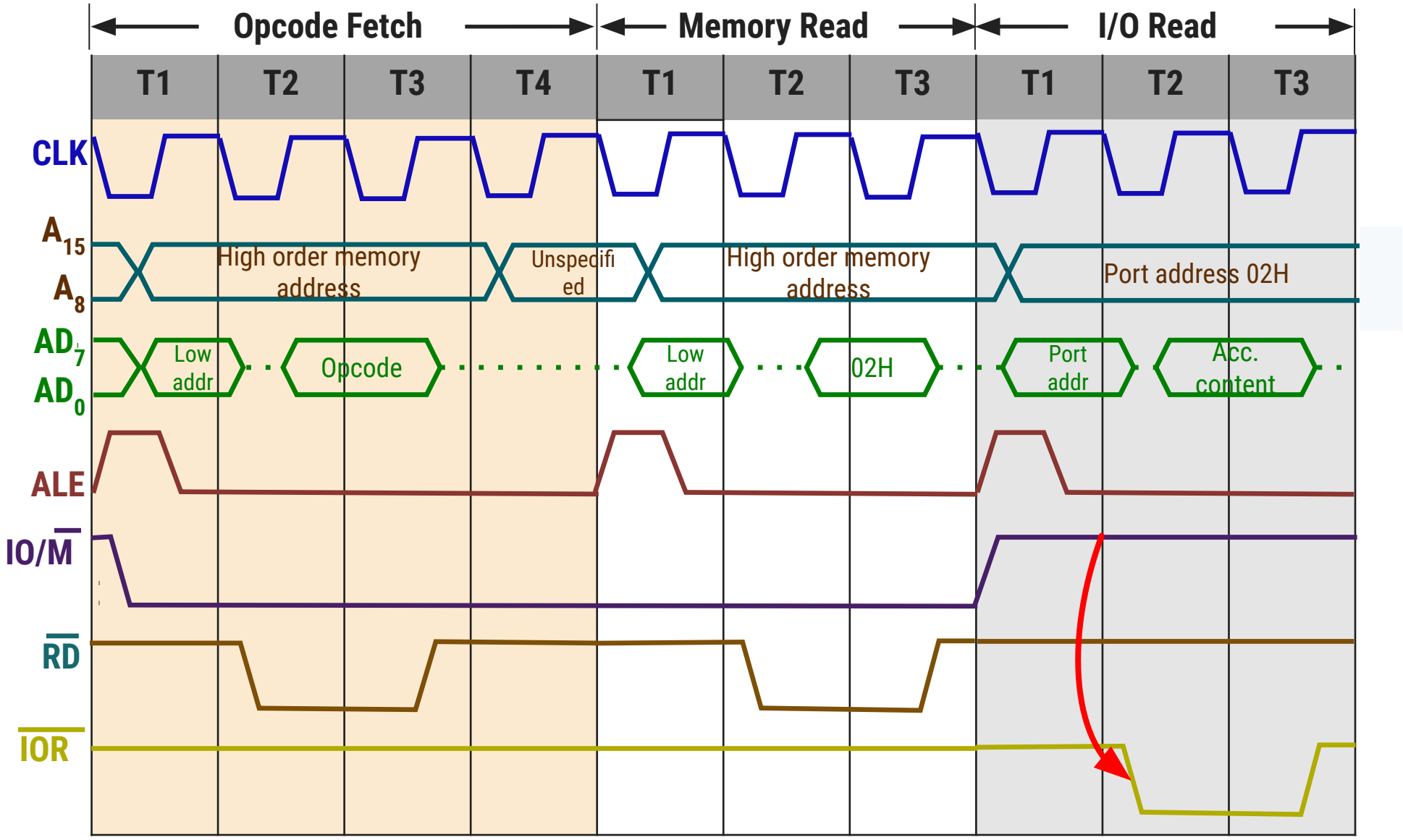
Timing Diagram : OUT 02H



Timing Diagram : IN 02H



GTU Exam Questions

Sr.	Questions	Marks	Year
1.	Draw the timing diagram of following instruction of the 8085 microprocessor. i. OUT 50h ii. MOV A, B iii. MVI A, 8bit	7	W'17 W'18 S'18 S'19
2.	How many machine cycles are executed by 8085 microprocessor? List down it.	1	S'18
3.	Explain various addressing modes of 8085 microprocessor.	7	S'18 W'18 W'19
4.	Identify the machine cycles in the following instructions 1. SUB B 2. ADI 47H 3. STA 2050H 4. PUSH B	7	W'18

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References

Book: Microprocessor Architecture, Programming, and Applications with the 8085, Ramesh S. Gaonkar Pub: Penram International

Mobile Application *8085 and 8086 Microprocessor Opcodes app from Play Store:* *http://tiny.cc/aopcodes*

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Thank You

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