Lab 2: Current Mirrors

Group No. ___ Group Members Name: Solution Guide
Name: Grading Guide

Lab Day: Monday Tuesday Wednesday Thursday Friday

Lab Time: Mornings Afternoons:

Introduction:

One of the most commonly used circuit structures in analog circuits is the current mirror. A current mirror has a relatively low input resistance and a high output resistance. Provided the output devices are operated in the saturation regime (MOSFETs) or the active regime (BJTs), the output current is a precisely controlled ratio of the input current. This feature makes current mirrors an attractive approach to the design of current sources. Current mirrors are widely used to bias transistors and to transport precise voltages around a chip. For further information, see Chapter 7, sections 8.2 and 8.6 in Microelectronic Circuits, 7$^{th.}$ Ed.

Key parameters for current sources are the output current (I_{OUT}), the output resistance (R_{OUT}) and the compliance range. I_{OUT} is self-evident, while R_{OUT} was defined in Lab 1. The **compliance range** is defined as the range of V_{OUT} over which the current source provides a reasonably constant current. The compliance range has a maximum (V_{OUT_MAX}) and minimum (V_{OUT_MIN}) value. Usually one of these two values is determined by the supply voltage.

Another useful term is Power Supply Rejection. In practical circuits, the supply voltage varies with time. These power supply variations often find their way into the circuit's output. Well designed circuits should reject, or not respond to, variations in the power supply. The ability of a circuit to reject power supply variations is expressed as the **Power Supply Rejection Ratio** or *PSRR*. Since the range of *PSRR*s can be quite large, the *PSRR* is commonly expressed as

$$PSRR = 20\log(v_s/v_{out}) \text{ dB} \quad (1)$$

where v_s is the ac component or "ripple" of the supply voltage while v_{out} is the ac component in the output due to the ripple in the supply voltage.

Preparation:

For this lab, the ALD1106 quad NMOS array and ALD1107 quad PMOS array will be used. As shown in Fig. 1a, the NMOS array contains four devices. The NMOS devices are specified to have V_{tn} = 0.7 V, $\mu_n C_{ox} W/L$ = 0.55 mA /V^2 and V_A = 60 V.

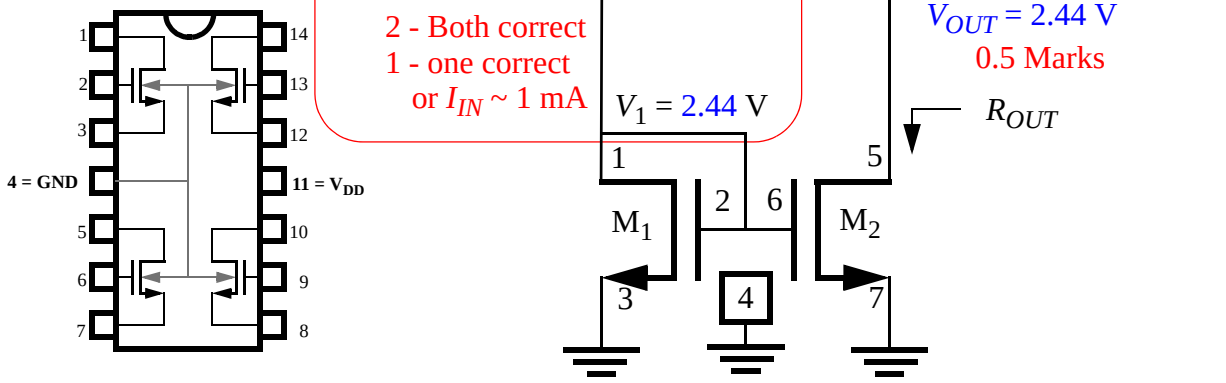
1. If the variable resistance, R_L, in Fig. 1b is set equal to R_1:

   a) Determine I_{IN}, I_{OUT}, V_1 and V_{OUT} and enter them on the schematic.

Knowing $I_{IN} = \dfrac{10\text{ V} - V_1}{9.1\text{ k}\Omega}$

and $I_{D1} = I_{IN} = \dfrac{\mu_n C_{ox}}{2}\dfrac{W}{L}(V_1 - V_{tn})^2$

we can solve for I_{IN} and V_1



a) b)

For dc analysis, we usually neglect second order effect like the finite output resistance. If we include it, we must solve a qubic equation. Doing so yields V_1 = 2.41 V and I_{IN} = 0.834

Figure 1) a) Pin diagram for the ALD1106. b) A simple current mirror.

b) Determine the minimum output voltage, V_{OUT_MIN} for which M_2 remains in saturation.

V_{OUT_MIN} = 1.74 V $(V_{DS2} \geq V_{GS2} - V_{tn})$ 0.5 Marks

c) Determine the mirror's output resistance, R_{OUT}.

R_{OUT} = 72.2 kΩ $(R_{OUT} = r_{o2} = V_A / I_{D2})$ 0.5 Marks

d) Pre-wire the circuit shown in Fig. 1b. Pin 4 must be connected to ground and pin 11 must be connected to +10 V. The variable resistor will be connected into your circuit in the lab.

Preparation Continued,

2. The circuit shown in Fig. 2, contains multiple current mirrors.

   a) Determine the voltage at each node, the indicated currents and the output resistance of the PMOS current mirror (R_{OUT}). The NMOS devices have the same parameters as before. For the PMOS devices, assume $|V_{tp}| = 0.7$ V, $\mu_p C_{ox} W/L = 0.18$ mA/V^2 and $|V_A| = 30$ V. Enter your voltage, current and resistance values on the diagram.
   b) Determine pin numbers for all NMOS and PMOS devices and enter them on the diagram.
   c) Pre-wire the indicated portion of the circuit to one side of the circuit board so that it can be added quickly in the lab.

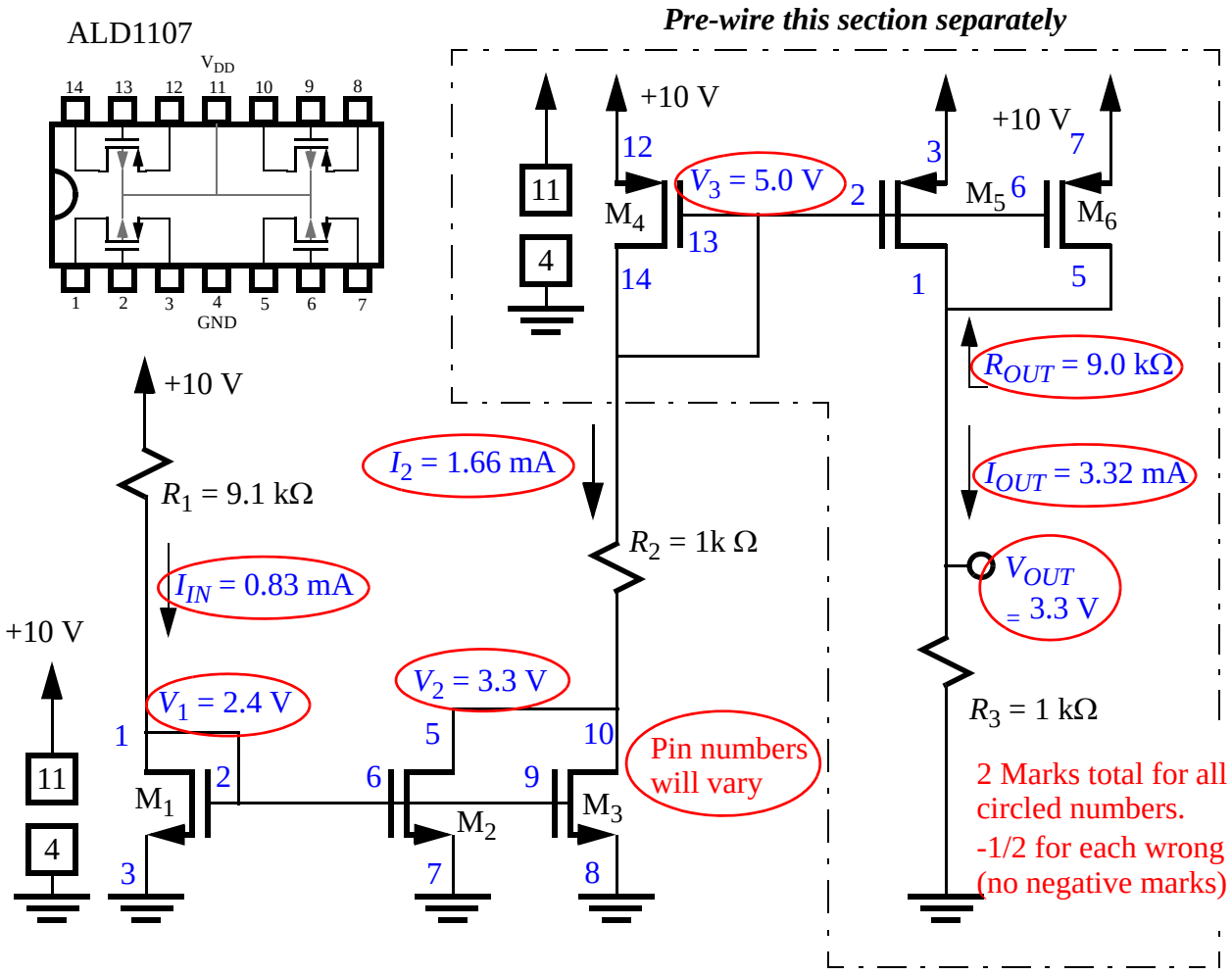


Figure 2) Multiple current mirrors.

- I_{IN} and V_1 are from figure 1.
- I_2 is mirrored by M_2 and M_3 or $2I_{IN}$, while I_{OUT} is mirrored by M_5 and M_6 or $2I_2$.
- $V_3 = 10$ V - $|V_{GS4}|$, where $|V_{GS4}|$ is set by I_2.
- $V_2 = V_3 - I_2 R_2$ while $V_{OUT} = I_{OUT} R_3$.
- $R_{OUT} = r_{o5} // r_{o6}$

Preparation Continued,

3. If R_L, in Fig. 3 equals R_1:

   a) Determine I_{IN}, I_{OUT}, V_1, V_2, V_3 and V_{OUT}. Then, enter them on the schematic. For these calculations, you can ignore the transistors' finite output resistances.

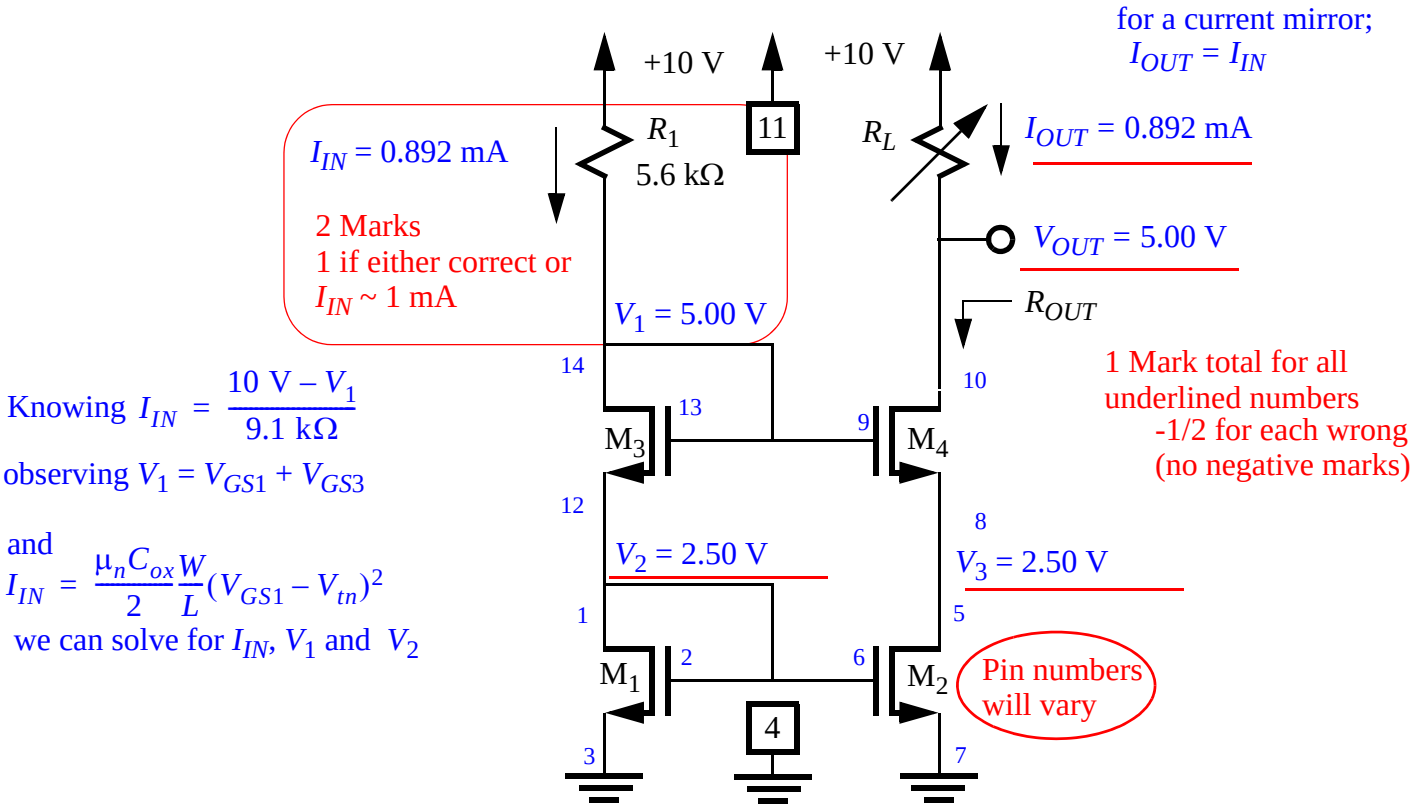


Figure 3) A cascode current mirror.

   b) Determine the current mirror's expected R_{OUT} and the minimum output voltage, V_{OUT_MIN}, for which the current mirror maintains a high output resistance.

   R_{OUT} = 4.62 MΩ (Cascode output resistance) V_{OUT_MIN} = 4.30 V ($V_{D4} > V_{G4} - V_{tn}$) 1/2 Mark each

   c) Determine pin numbers for the NMOS devices and enter them on the schematic of Fig. 3.

4. Download (from the class website) the workbook entitled *Lab 2.xlsx*. Then, review the laboratory instructions to determine which spreadsheets or tables would be helpful to have prepared in advance of the lab and prepare them. Be sure to submit them with your preparation.

Total Preparation Mark = 10. No marks for pre-wiring and pin numbering (lab performance may suffer)

Laboratory:

The Basic Current Mirror

1. Verify that your circuit analysis and the pre-wiring done in part 1 of the preparation are correct by applying 10 V and ground to your pre-wired circuit and measuring the node voltages. Record the measured voltages on Fig. 4 (lab version of Fig. 1).

   1 Mark -all should be close to the preparation

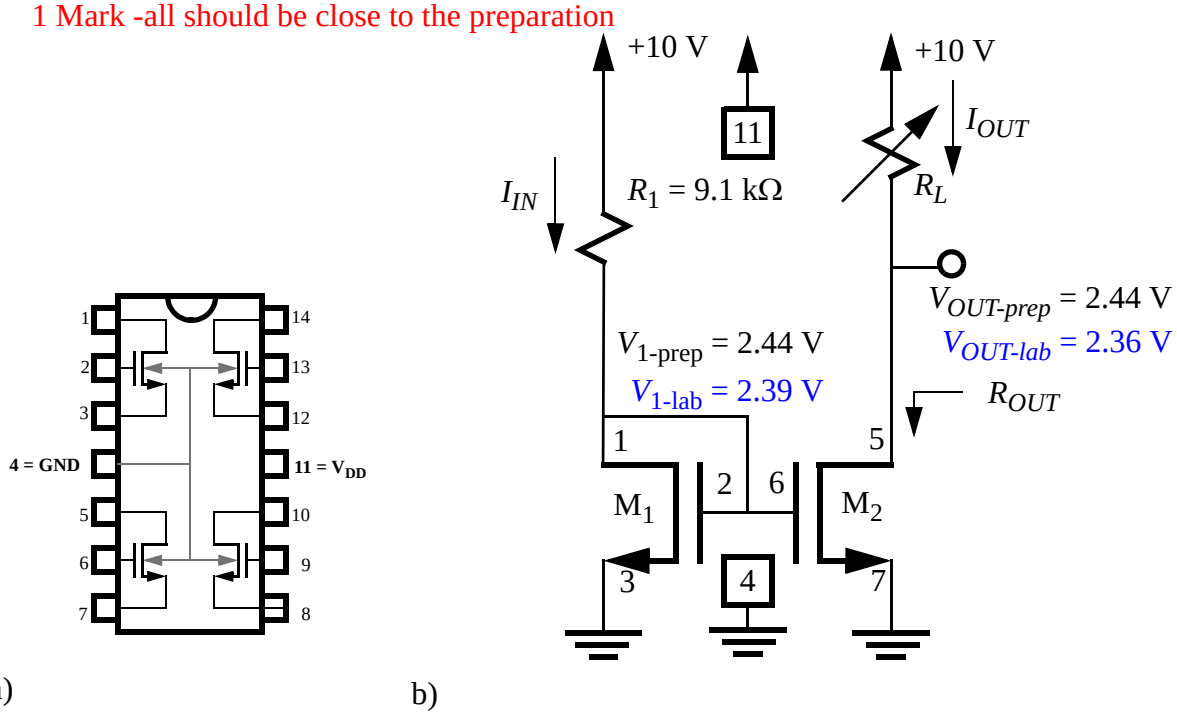


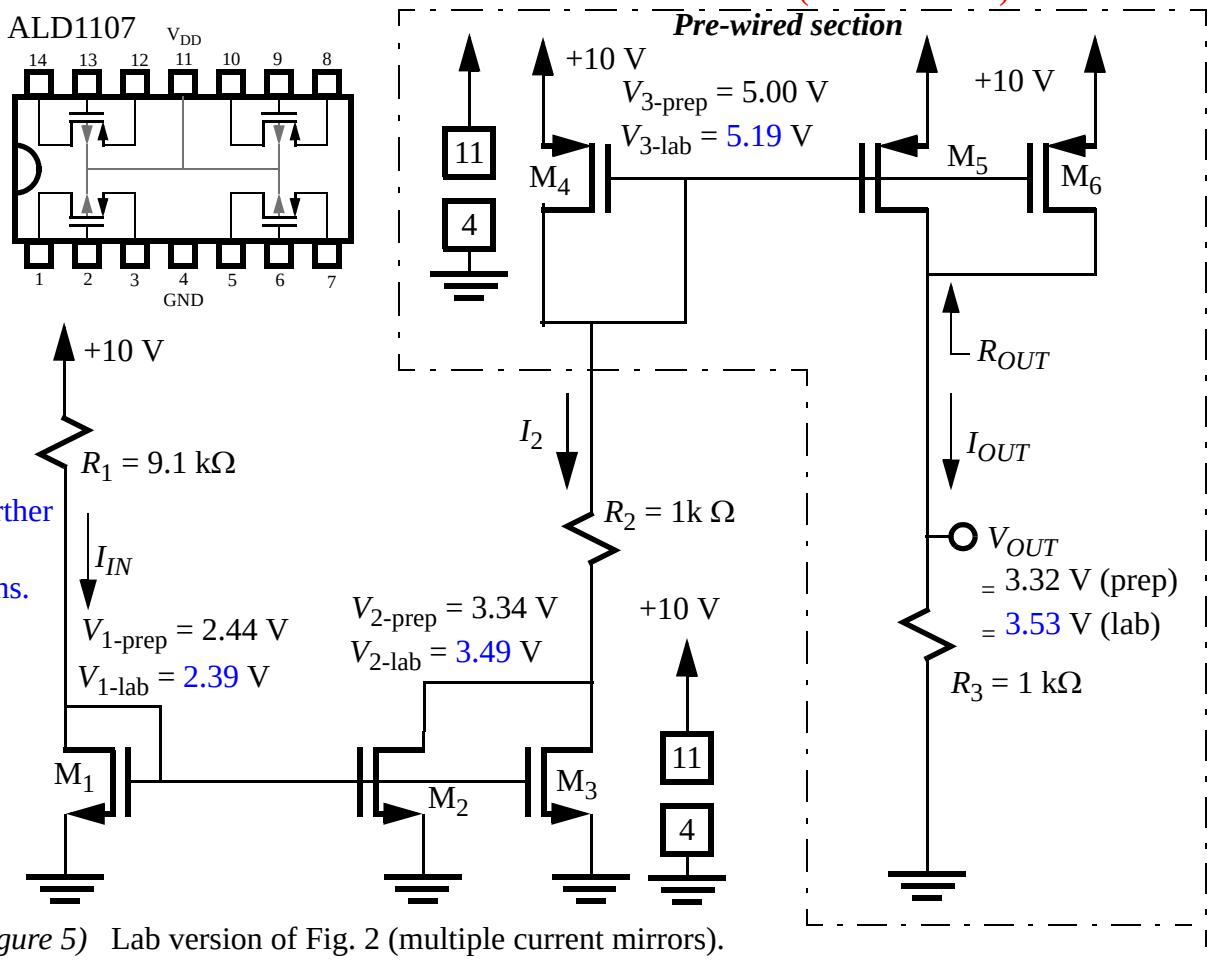
Figure 4) Lab version of Fig. 1, a) Pin diagram for the ALD1106. b) A simple current mirror.

2. Gather data to determine the mirror's output resistance. To do this, download (from the class website) the workbook entitled *Lab 2.xlsx*. On the sheet labeled "Basic Current Mirror", prepare a spreadsheet for finding output resistance, similar to those used in Lab 1. In this case, you will be finding the current through R_L ($i_O = (V_{DD} - V_{OUT})/R_L$). Consequently, you will need to measure and record $\boldsymbol{V_{DD} - V_{OUT}}$ for values of R_L similar to those used in Lab 1. Record at least three significant figures.

   1 Mark, should be similar to the attached table
   the quality of your measurements will greatly affect your results.

Multiple Current Mirrors

1. Construct a multiple current mirror circuit and verify its dc operating point. To do this, power down your circuit. Then, add an NMOS device (M_3) and the pre-wired PMOS mirror to your circuit, as shown in Fig. 5 (lab version of Fig. 2). Re-apply 10 V to the circuit. Verify that the circuit is operating properly by measuring its node voltages[1], recording them on Fig. 5 and comparing the voltages to the preparation values. 1 Mark - should correspond to your preparation (see note below)



Note: values farther from I_{IN} show greater variations.

Figure 5) Lab version of Fig. 2 (multiple current mirrors).

1 Mark each for being close to 2.0

2. Determine the current ratios of the NMOS and PMOS current mirrors from the currents through R_1, R_2 and R_3. $\frac{I_2}{I_{IN}} = 2.03$ $\frac{I_{OUT}}{I_2} = 2.08$

3. Gather data to determine the mirror's output resistance. To do this, replace R_3 with the decade resistor (R_L). Then, by using a procedure similar to that used in part 2 of *The Basic Mirror*, record, in *Lab 2.xlsx*, on the sheet labeled "Multiple Current Mirrors", sufficient data to determine the range over which the PMOS current mirror's output current is reasonably constant (*i.e.* the compliance range).

1. Note that V_{OUT} will only be close to the expected value if the MOSFETs are all perfectly matched.

4. Investigate power supply rejection. To do this, connect the sources of the PMOS mirror to a 1 V_p, 1 kHz sine wave in series with a 9 V_{DC} source, as shown in Fig. 6. Display v_s and v_{OUT} on the oscilloscope and record them using a scope capture in a file labeled PSRR.png (save the file as a portable network graphics file or ".png" file). Determine the amplitude of the 1 kHz sine wave on both v_s and v_{out}. These signals are known as the **supply ripple** and the **output ripple** respectively.

v_s = 0.99 V 1 Mark should be close to 1 V Note: we are looking for the amplitude. v_{out} = 0.172 V 1 Mark - should correspond to yourscope capture!

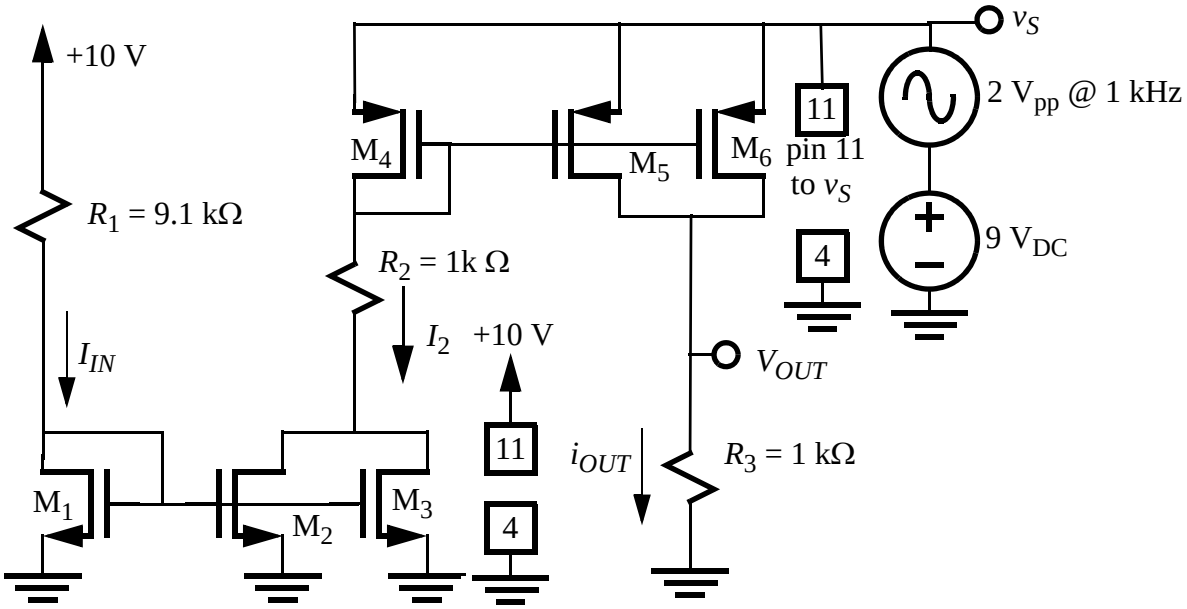


Figure 6) Power supply noise and current source behaviour.

- For the NMOS array, connect pin 11 to +10 V.
- For the PMOS array, connect pin 11 to v_s.
- For both arrays, connect pin 4 to ground.

The Cascode Current Mirror

1. Construct a cascode current mirror and verify its operating point. To do this, power down your circuit. Then, remove the PMOS current mirror. Create a cascode mirror by changing the position of M_3, adding M_4 to your circuit and changing the value of R_1, as shown in Fig. 7. Power up your circuit and verify that your circuit analysis is correct by measuring the node voltages and recording them on Fig. 7. 1 Mark - should correspond to your preparation (see note below)

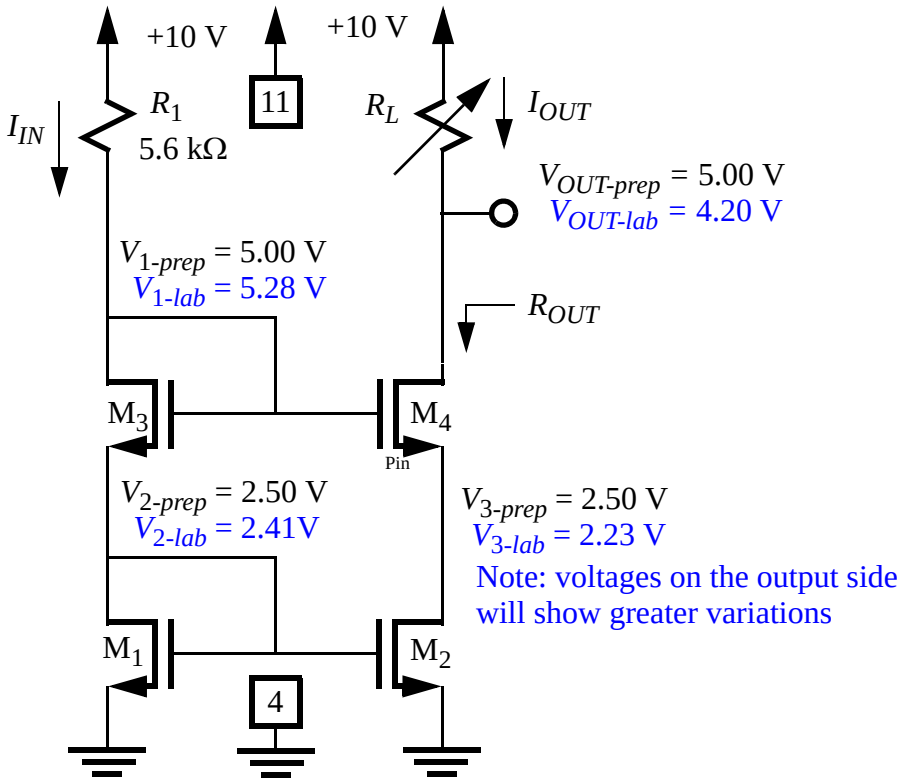


Figure 7) Lab version of Fig. 3 (a cascode current mirror).

2. Gather data to determine the mirror's output resistance. To do this, use the same resistor values and procedure as used in part 2 of *The Basic Current Mirror*. Record the data in *Lab 2.xlsx*, on the sheet labeled "Basic Current Mirror" by adding any necessary columns to the spreadsheet used in *The Basic Current Mirror*.

1 Mark - similar to attached table
1 Mark for a timely completion.

Total Lab Mark = 10

Report:

The Basic Current Mirror

1. Using the data recorded in your spreadsheet for the basic current mirror, plot I_{OUT} *versus* V_{OUT} on the sheet entitled "I versus V". See part 1 under *The Cascode Current Mirror* below, before preparing your plot. For the plot, see the notes. 2 Marks for the combined plot.

2. From the plot and your spreadsheet, determine the current mirror's R_{OUT} and the range of V_{OUT} over which the current mirror provides a reasonably constant current (*i.e.* the compliance range). Be sure to annotate the plot to unambiguously show the compliance range. Compare these values with parts 1b and 1c of the preparation.

R_{OUT} = 68 kΩ (see notes) 1 Mark (close to 70 kΩ)

V_{OUT_min} = 1.50 V 1 Mark (close to 1.5 V)

V_{OUT_max} = 9.00 V 1 Mark (close to 9 V)

3. Using the plot of part 1 above, determine the value of I_{OUT} when $V_{OUT} = V_1$ (see Fig. 1) and determine the value of I_{IN} based on your measured value of V_1. Then, based on these values of I_{OUT} and I_{IN} determine;

   a) The actual current mirror ratio (*i.e.*, I_{OUT}/I_{IN}) for the basic current mirror.

   $\frac{I_{OUT}}{I_{IN}} = 1.010$ — 1 Mark should be 1 +/- 5%

   b) If the only source of mismatch is due to W/L variations, what are the relative W/L ratios for M_1 and M_2?
   The current ratio is directly proportional to the W/L ratios.

   $\frac{W_2/L_2}{W_1/L_1} = 1.010$ — 1 Mark if identical to part a.

   c) If the only source of mismatch is due to variations in V_t, and M_1 has exactly the V_t given in the preparation, by how much does the V_t of M_2 differ from that of M_1?

   $V_{t2} - V_{t1} = -8.57$ mV (see notes) — 1 Mark if approximately $\pm 0.7\left(\frac{I_{OUT}}{I_{IN}} - 1\right)$

Multiple Current Mirrors

1. Based on your measured results, determine the PMOS current mirror's current ratio by comparing the currents through R_2 and R_3 (this should be the same value found in part 2 of the *Multiple Current Mirrors* section in the Lab.

   $\frac{I_{OUT}}{I_2} = 2.10$ — 1 Mark if identical to the lab result.

2. Based on your scope capture (from part 4 of the *Multiple Current Mirrors* section of the lab) labeled PSRR.png, determine the amplitude of the 1 kHz sine wave for both v_s and v_{out}. Annotate the PSRR.png to clearly indicate these two signals. These signals are known as the **supply ripple** and the **output ripple** respectively. Then determine the circuit's *PSRR*..[1]

   v_s = 0.99 V
   v_{out} = 0.17 V — 1 Mark if both identical to the lab result.

   $PSRR = 15$ dB — 1 Mark, calculation should be correct.

1. Obviously this is not the circuit's actual *PSRR* as the bias current (through R_1) is also affected by the supply. If interested in more details, do an internet search on "bandgap references".

3. Using the spreadsheet created in part 3 of *Multiple Current Mirrors* (in the lab), determine the PMOS current mirror's R_{OUT} and find the ratio R_{OUT}/R_3 (in dB).

   R_{OUT} = 15 kΩ
   1 Mark - should be close to 15 kΩ.

   R_{OUT}/R_3 = 23.5 dB
   1 Mark - should be 20log(R_{OUT})

4. Compare the *PSRR* found above, to the ratio R_{OUT}/R_3.

   The PSRR is worse (lower) than predicted by the simple ratio of the resistors.
   There must be other contributors!

   1 Mark for indicating the real result is worse than the simple prediction.

The Cascode Current Mirror

1. Using the data recorded in your spreadsheet for the cascode current mirror, plot I_{OUT} *versus* V_{OUT} on the same plot and scale as used in part 2 of *The Basic Current Mirror*. (See notes)

2. From the plot and your spreadsheet, determine the cascode current mirror's R_{OUT} and compliance range. Compare these values with part 3b of the preparation.

   R_{OUT} = 2.4 MΩ (see notes)
   2 Marks (4 MΩ +/– 50%)
   1 Mark (close to 300 kΩ)

   V_{OUT_min} = 3.50 V
   1 Mark (close to 3.5 V)

   V_{OUT_max} = 9.00 V
   1 Mark (close to 9 V)

3. Comment on the basic and cascode mirror's output resistances and compliance ranges.

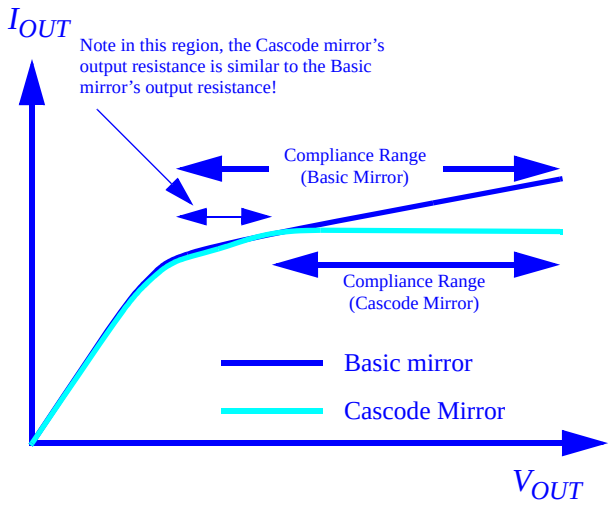
   • The cascode mirror provides a significantly higher output resistance. 1 Mark
   • The basic current mirror provides a wider compliance range. 1 Mark

Total Report Mark = 20, **Maximum Total Grade = 40**

Notes:

The Basic Current Mirror

1. A plot of I_{OUT} *versus* V_{OUT} for both the basic mirror and the cascode mirror.



When calculating the current using $i = V/R$, it is the voltage across the resistor you need. This implies your current calculations should look like: $i = (10\text{ V} - V_{OUT})/R$.

1 Mark for the basic mirror correct.
1 Mark for the cascode mirror correct.

2. Calculating R_{OUT}.
   - When calculating the current using $i = V/R$, it is the voltage across the resistor you need. This implies your current calculations should look like: $i = (10\text{ V} - V_{OUT})/R$.
3. Part c) If the only source of mismatch is due to variations in V_t, and M_1 has exactly the V_t given in the preparation, by how much does the V_t of M_2 differ from that of M_1?

$V_{tn2} - V_{tn1} = -8.4$ mV

Knowing both devices are in saturation, we can write:

$$\frac{I_{OUT}}{I_{IN}} = \frac{(K_{n1}/2)(V_{GS} - V_{t2})^2}{(K_{n2}/2)(V_{GS} - V_{t1})^2}$$

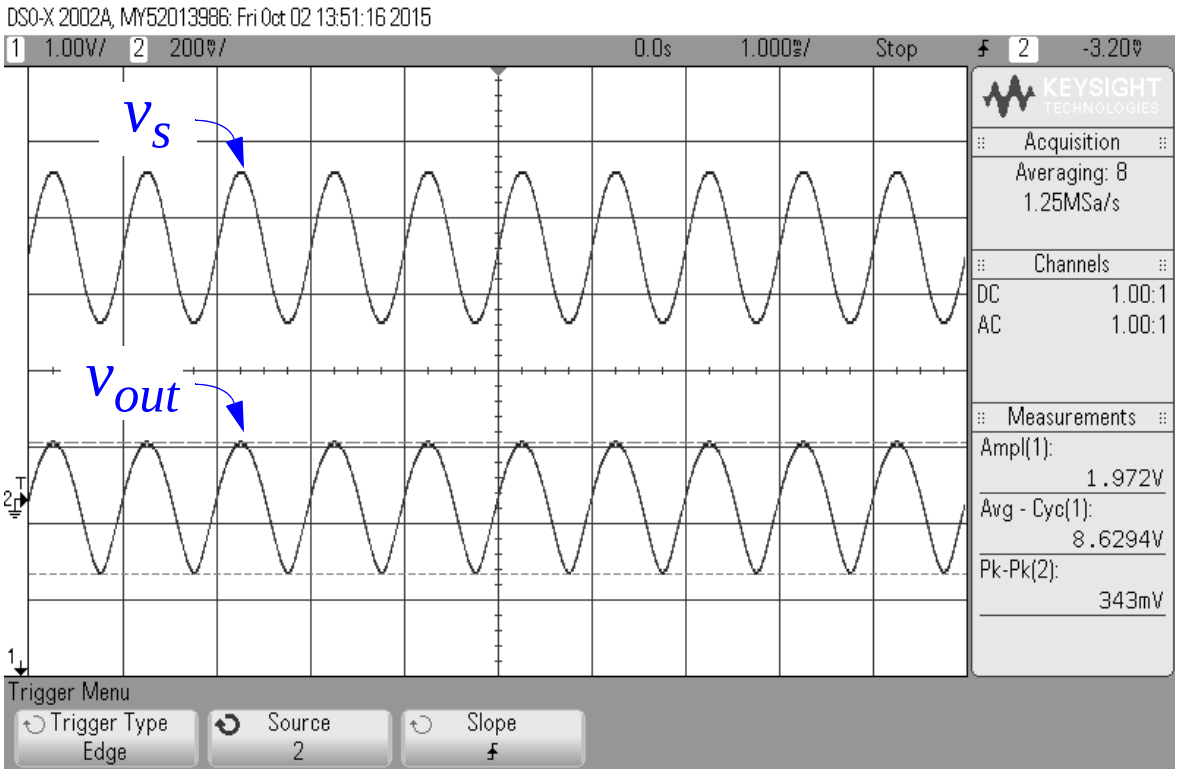
Assuming $K_{n1} = K_{n2}$ and $V_{tn1} = 0.7$ V
and using our measured values for V_{GS} (2.39) and I_{OUT}/I_{IN} (1.010) we get;

$$1.010 = \left(\frac{2.39 - V_{t2}}{2.39 - 0.7}\right)^2 \quad \text{or} \quad 1.005 = \frac{2.39 - V_{t2}}{1.69}$$

Solving for V_{tn2}, we find $V_{tn2} = 0.6916$ V
Or $V_{tn2} - V_{tn1} = -8.4$ mV
Answers will vary widely!

The cascode mirror, part 2

A sample scope capture is shown below.



If you did not take **extremely** careful measurements, your output resistance was likely to be much lower. Typical values for poor measurement technique yield R_{OUT} = 300 kΩ.

Sample Measured Data for Lab 2

The Basic Current Mirror

Basic Current Mirror Measurements			
R_L (Ω)	V_{OUT} (V)	I_{OUT} (mA)	R_{OUT} (kΩ)
999999	0.0080	0.00999	
100000	0.0803	0.09920	0.81028
70000	0.1161	0.14120	0.85187
50000	0.1654	0.19669	0.88784
35000	0.2415	0.27882	0.92654
20000	0.4573	0.47714	1.08818
14000	0.7371	0.66163	1.51694
10000	1.6818	0.83182	5.55071
9100	2.3126	0.84477	48.71332
7000	3.9380	0.86600	76.55870
5000	5.6000	0.88000	118.71429
3500	6.8975	0.88643	201.83333
2000	8.2305	0.88475	794.12766
1000	9.1444	0.85560	31.35163
700	9.4227	0.82471	9.01064
500	9.6114	0.77720	3.97144
350	9.7546	0.70114	1.88279
200	9.8988	0.50600	0.73895
140	9.9566	0.31000	0.29490
100	9.9953	0.04700	0.14715

Sample Measured Data for Lab 2

Multiple Current Mirrors

Multiple Current Mirror Measurements			
R_L (Ω)	V_{OUT} (V)	I_{OUT} (mA)	R_{OUT} (kΩ)
999999	10.08470	0.01008	
100000	10.02770	0.10028	0.63198
70000	10.00000	0.14286	0.65054
50000	9.96400	0.19928	0.63804
35000	9.91000	0.28314	0.64391
20000	9.77350	0.48868	0.66413
14000	9.63550	0.68825	0.69147
10000	9.45130	0.94513	0.71707
9100	9.38600	1.03143	0.75668
7000	9.16830	1.30976	0.78217
5000	8.78600	1.75720	0.85441
3500	8.19370	2.34106	1.01446
2000	6.49000	3.24500	1.88474
1000	3.56600	3.56600	9.10903
700	2.54260	3.63229	15.43922
500	1.83790	3.67580	16.19468
350	1.29600	3.70286	20.02798
200	0.74640	3.73200	18.85882
140	0.52510	3.75071	11.82519
100	0.37640	3.76400	11.19247

Sample Measured Data for Lab 2

The Cascode Current Mirror

Cascode Current Mirror Measurements			
R_L (Ω)	V_{OUT} (V)	I_{OUT} (mA)	R_{OUT} (kΩ)
50000	0.2330	0.19534	
35000	0.3378	0.27606	1.29853
20000	0.6265	0.46868	1.49876
14000	0.9730	0.64479	1.96751
10000	1.7250	0.82750	4.11572
9100	2.2741	0.84900	25.53953
7000	3.9856	0.85920	167.79412
5000	5.7285	0.85430	355.69388
3500	7.0347	0.84723	184.71515
2000	8.3441	0.82795	67.91997
1000	9.2186	0.78140	18.78625
700	9.4790	0.74429	7.01617
500	9.6543	0.69140	3.31469