Brukarmanual for plattformkortet NUCLEO-F103RB.
Denne utgåva inneheld det aller meste om mikrokontroller og plattformkort som ein vil trenga til øvingsarbeidet og eksamen i ELE210, samt i arbeid med denne plattformen elles også.
MT, 23/7-21.

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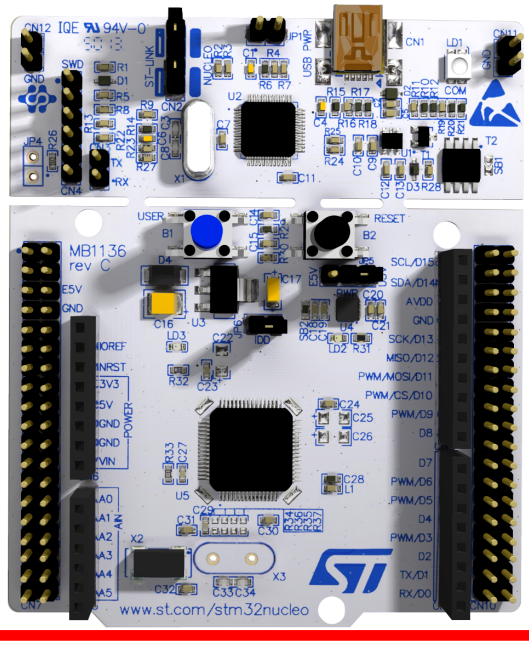
UM1724
User manual

STM32 Nucleo-64 boards (MB1136)

Introduction

The STM32 Nucleo-64 boards based on the MB1136 reference board (NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F103RB, NUCLEO-F302R8, NUCLEO-F303RE, NUCLEO-F334R8, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-L010RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L152RE, NUCLEO-L452RE, NUCLEO-L476RG) provide an affordable and flexible way for users to try out new concepts and build prototypes with the STM32 microcontrollers in the LQFP64 package, choosing from the various combinations of performance, power consumption, and features. The ARDUINO® Uno V3 connectivity support and the ST morpho headers provide an easy means of expanding the functionality of the Nucleo open development platform with a wide choice of specialized shields. The STM32 Nucleo boards do not require any separate probe as they integrate the ST-LINK/V2-1 debugger and programmer. The STM32 Nucleo boards come with the comprehensive free software libraries and examples available with the STM32Cube MCU Packages, as well as direct access to the Arm® Mbed™ online resources at http://mbed.org/.

Figure 1. STM32 Nucleo-64 board



Denne brukarmanualen er laga som ein kombinasjon av *UM1724 User manual*, databladet til mikrokontrolleren, *STM32F103x8 STM32F103xB datasheet* samt referansemanualen, *Reference manual .. STM32F103xx..* Irrelevante sider i UM1724 er tatt ut og så er det bakerst lagt til sentrale sider frå datablad og refmanual. Det er og lagt til kretsskjema frå UM1724, rev.13, som ikkje var med i rev.14. Det er i tillegg tilføyd kommentarar. Meir om alt dette kjem på s.3.
Merk: Når det er vist til sidetal, blir også sidetalet i originalskrivet vist i parentes.

Content

Frå brukarmanualen UM1724, rev.13, er det lagt til følgjande:
- Kretsskjema av plattformkortet, s.18-21.

Frå referansemanualen er det lagt til følgjande:
- Blokkskjema av systembussane inne i mikrokontrolleren, s.23.
- Litt spesifikasjon samt blokkskjema av ein GPIO-modul, s.32-33.

Frå databladet er det lagt til følgjande:
- Blokkskjema av klokkesignala og modulane som genererer desse, s.10.
- Blokkskjema av mikrokontrolleren (STM32F103RB), s.22.
- Minnekart for mikrokontrolleren, s.24.
- Pinnediagram for den brikketypen som blir brukt på plattformkortet, s.25.
- Tabellar som viser pinnenamn og -funksjonar for ulike brikketypar, s.26-31.
- Spesifikasjon av krav til spenningsområde for digitale inngangssignal mm., s.34.
- Spesifikasjon av spenningsområda for digitale utgangssignal mm., s.35.

Pensumlista viser kor du finn originaldokumenta som er brukte for å setja saman denne brukarmanualen.

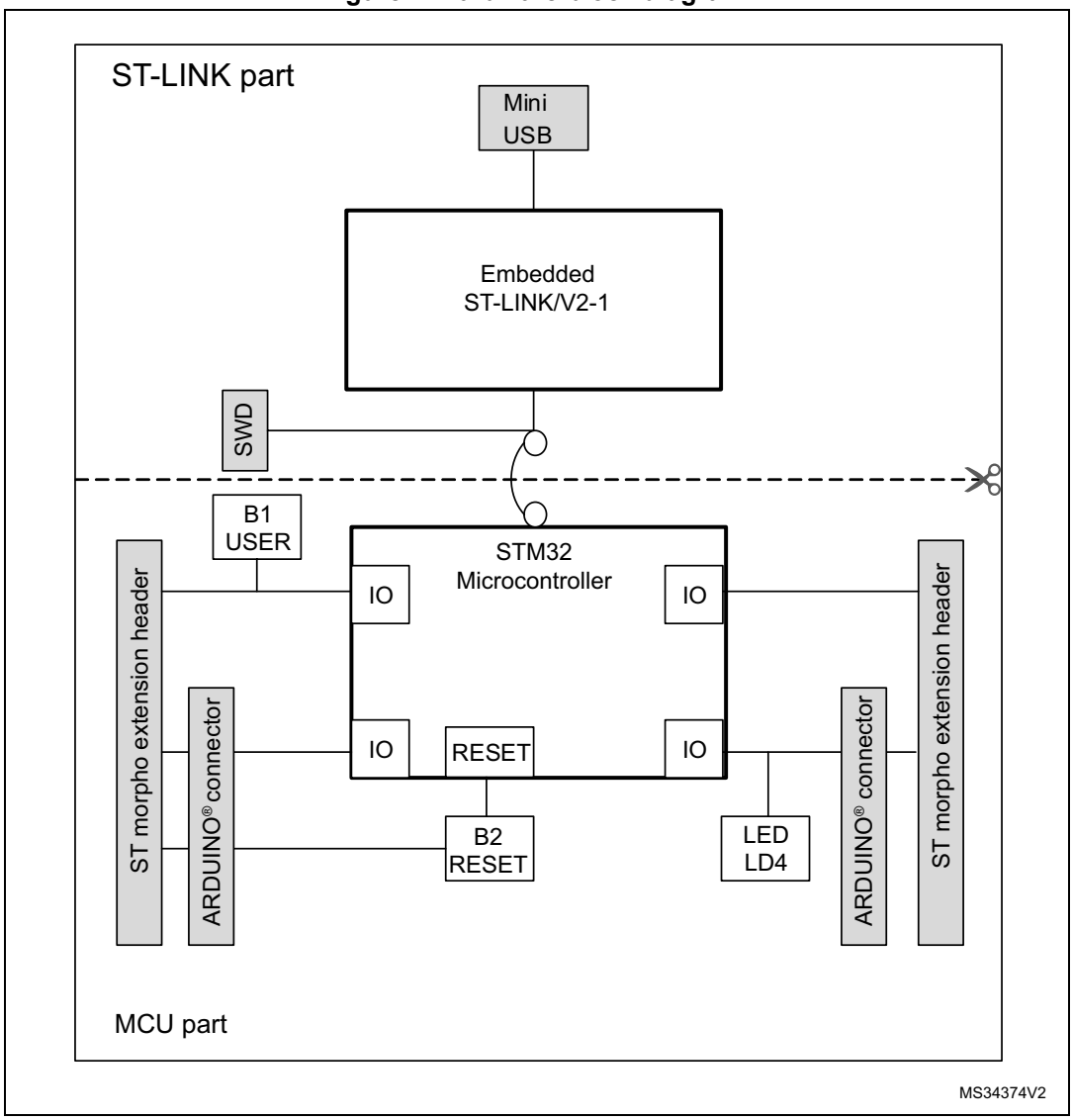
6 Hardware layout and configuration

The STM32 Nucleo board is designed around the STM32 microcontrollers in a 64-pin LQFP package.

Figure 2 shows the connections between the STM32 and its peripherals (ST-LINK/V2-1, push-button, LED, ARDUINO® connectors, and ST morpho connector).

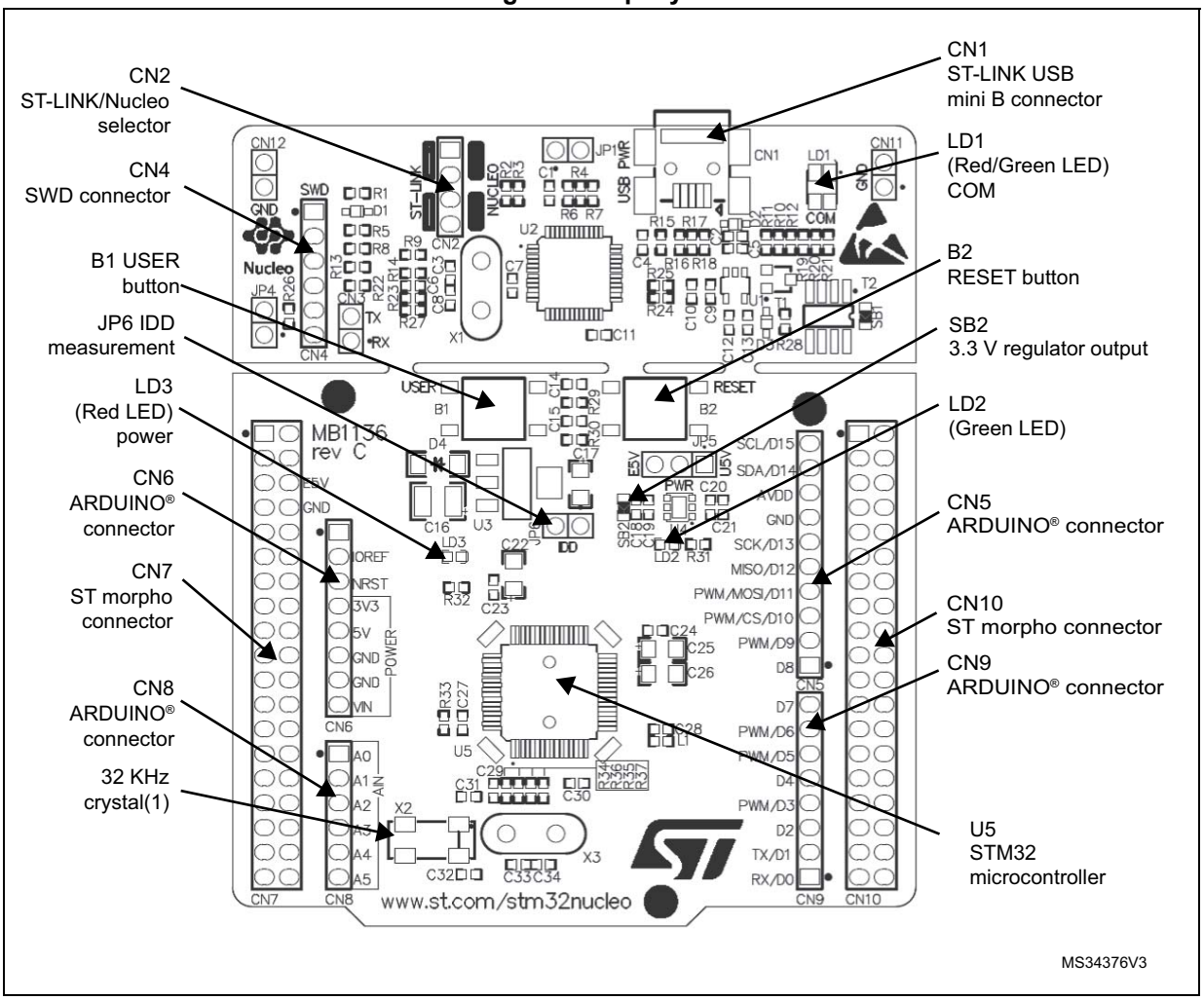
Figure 3 and *Figure 4* show the location of these features on the STM32 Nucleo board. *Figure 5* shows the mechanical dimension of the STM32 Nucleo board.

Figure 2. Hardware block diagram



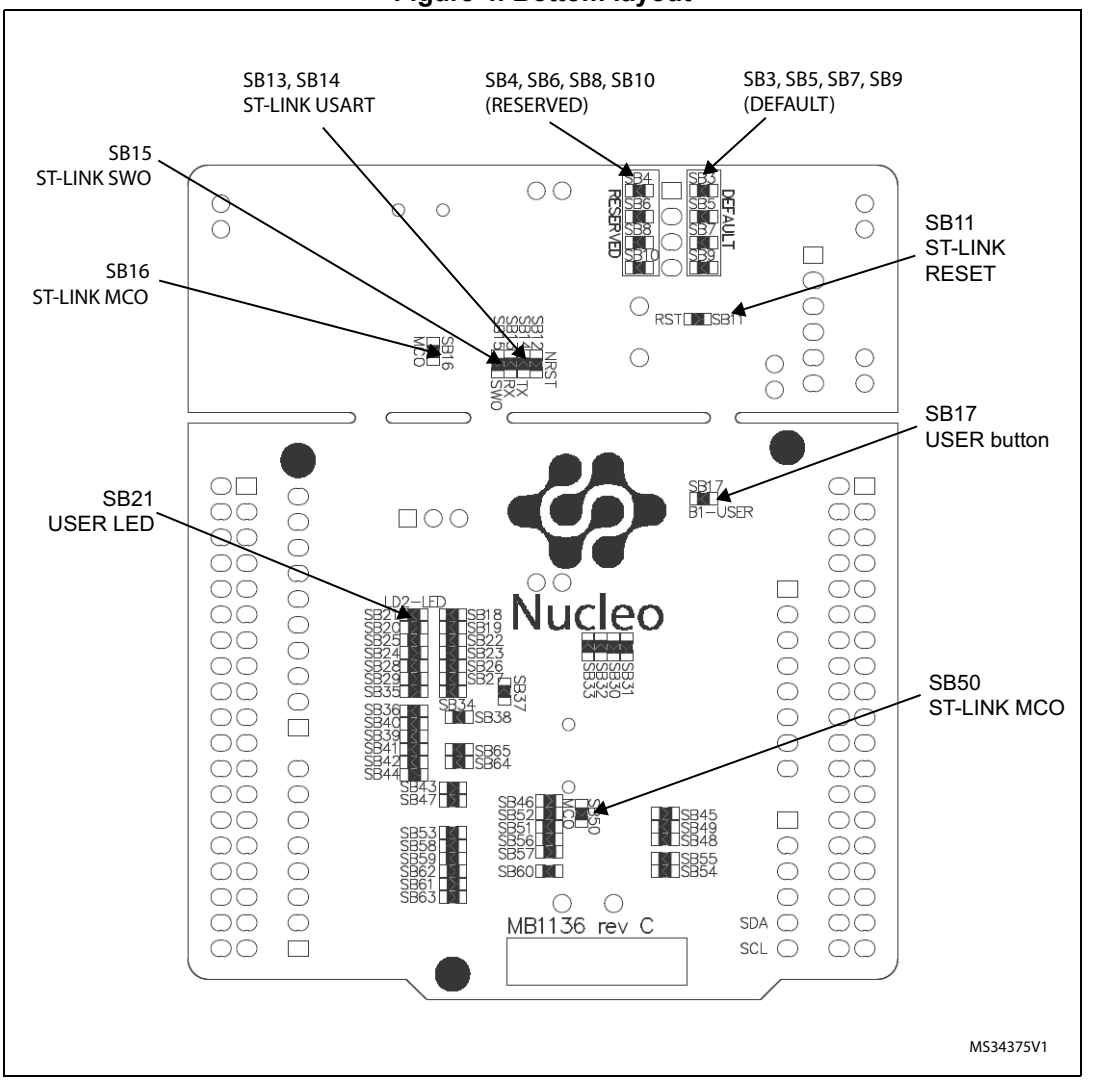
Merk: Eit blokkskjema av maskinvaren inne i mikrokontrolleren vår, STM32F103RB, er vist bakerst i denne brukarmanualen saman med andre viktige data som er henta frå databladet til mikrokontrolleren. Bl.a. er det lagt ved minnekart for mikrokontrolleren og nokre elektriske data. Kor du finn alt dette, er lista opp på s.3.

Figure 3. Top layout



1. Crystal may be present or not depending on board version, refer to *Section 6.7.2*.

Figure 4. Bottom layout



Merk: Du finn nokre kommentarar til desse koblingsbruene (*solder bridges*, SB) i samband med tabell 10, s. 11-12 (STM-side 26-27/68).

6.4 LEDs

The tricolor LED (green, orange, red) LD1 (COM) provides information about ST-LINK communication status. LD1 default color is red. LD1 turns to green to indicate that communication is in progress between the PC and the ST-LINK/V2-1, with the following setup:

- Slow blinking Red/Off: at power-on before USB initialization
- Fast blinking Red/Off: after the first correct communication between the PC and ST-LINK/V2-1 (enumeration)
- Red LED On: when the initialization between the PC and ST-LINK/V2-1 is complete
- Green LED On: after a successful target communication initialization
- Blinking Red/Green: during communication with the target
- Green On: communication finished and successful
- Orange On: Communication failure

User LD2: the green LED is a user LED connected to ARDUINO® signal D13 corresponding to STM32 I/O PA5 (pin 21) or PB13 (pin 34) depending on the STM32 target. Refer to *Table 11* to *Table 23* when:

- the I/O is HIGH value, the LED is on
- the I/O is LOW, the LED is off

LD3 PWR: the red LED indicates that the STM32 part is powered and +5V power is available.

6.5 Push-buttons

B1 USER: the user button is connected to the I/O PC13 (pin 2) of the STM32 microcontroller.

B2 RESET: this push-button is connected to NRST, and is used to RESET the STM32 microcontroller.

Note: The blue and black plastic hats that are placed on the push-buttons can be removed if necessary, for example when a shield or when an application board is plugged on top of the Nucleo board. This will avoid pressure on the buttons and consequently a possible permanent target STM32 RESET.

6.6 JP6 (IDD)

Jumper JP6, labeled IDD, is used to measure the STM32 microcontroller consumption by removing the jumper and by connecting an ammeter:

- Jumper ON: STM32 microcontroller is powered (default).
- Jumper OFF: an ammeter must be connected to measure the STM32 microcontroller current. If there is no ammeter, the STM32 microcontroller is not powered.

6.7 OSC clock

6.7.1 OSC clock supply

There are four ways to configure the pins corresponding to the external high-speed clock (HSE):

- **MCO from ST-LINK**: MCO output of ST-LINK MCU is used as an input clock. This frequency cannot be changed, it is fixed at 8 MHz and connected to PF0/PD0/PH0-OSC_IN of the STM32 microcontroller.

  The following configuration is needed:

  – SB55 OFF and SB54 ON
  – SB16 and SB50 ON
  – R35 and R37 removed
- **HSE oscillator on-board from X3 crystal (not provided):** for typical frequencies and its capacitors and resistors, refer to the STM32 microcontroller datasheet. Refer to the AN2867 Application note for oscillator design guide for STM32 microcontrollers.The X3 crystal has the following characteristics: 8 MHz, 16 pF, 20 ppm, and DIP footprint. It is recommended to use 9SL8000016AFXHF0 manufactured by Hong Kong X'tals Limited.

  The following configuration is needed:

  – SB54 and SB55 OFF
  – R35 and R37 soldered
  – C33 and C34 soldered with 20 pF capacitors
  – SB16 and SB50 OFF
- **Oscillator from external PF0/PD0/PH0**: from an external oscillator through pin 29 of the CN7 connector.

  The following configuration is needed:

  – SB55 ON
  – SB50 OFF
  – R35 and R37 removed
- **HSE not used**: PF0/PD0/PH0 and PF1/PD1/PH1 are used as GPIOs instead of clocks

  The following configuration is needed:

  – SB54 and SB55 ON
  – SB16 and SB50 (MCO) OFF
  – R35 and R37 removed

There are two possible default configurations of the HSE pins, depending on the version of the STM32 Nucleo board hardware.

The board version MB1136 C-01 or MB1136 C-02 is mentioned on the sticker, placed on the bottom side of the PCB.

The board marking MB1136 C-01 corresponds to a board, configured as HSE not used.

The board marking MB1136 C-02 (or higher) corresponds to a board, configured to use ST-LINK MCO as the clock input.

Note: For NUCLEO-L476RG and NUCLEO-L452RE the ST-LINK MCO output is not connected to OSCIN to reduce power consumption in low power mode. Consequently, NUCLEO-L476RG and NUCLEO-L452RE configurations correspond to HSE not used.

6.7.2 OSC 32 kHz clock supply

There are three ways to configure the pins corresponding to the low-speed clock (LSE):

- **On-board oscillator:** X2 crystal. Refer to the *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* application note *(*AN2867) for oscillator design guide for STM32 microcontrollers.It is recommended to use ABS25-32.768KHZ-6-T, manufactured by Abracon Corporation.
- **Oscillator from external PC14**: from external oscillator through the pin 25 of CN7 connector.

  The following configuration is needed:
  - SB48 and SB49 ON
  - R34 and R36 removed
- **LSE not used**: PC14 and PC15 are used as GPIOs instead of low-speed clocks.

  The following configuration is needed:
  - SB48 and SB49 ON
  - R34 and R36 removed

There are three possible default configurations of the LSE depending on the version of the STM32 Nucleo board hardware.

The board version MB1136 C-01 or MB1136 C-02 is mentioned on the sticker placed on the bottom side of the PCB.

The board marking MB1136 C-01 corresponds to a board configured as LSE not used.

The board marking MB1136 C-02 (or higher) corresponds to a board configured with on-board 32 kHz oscillator.

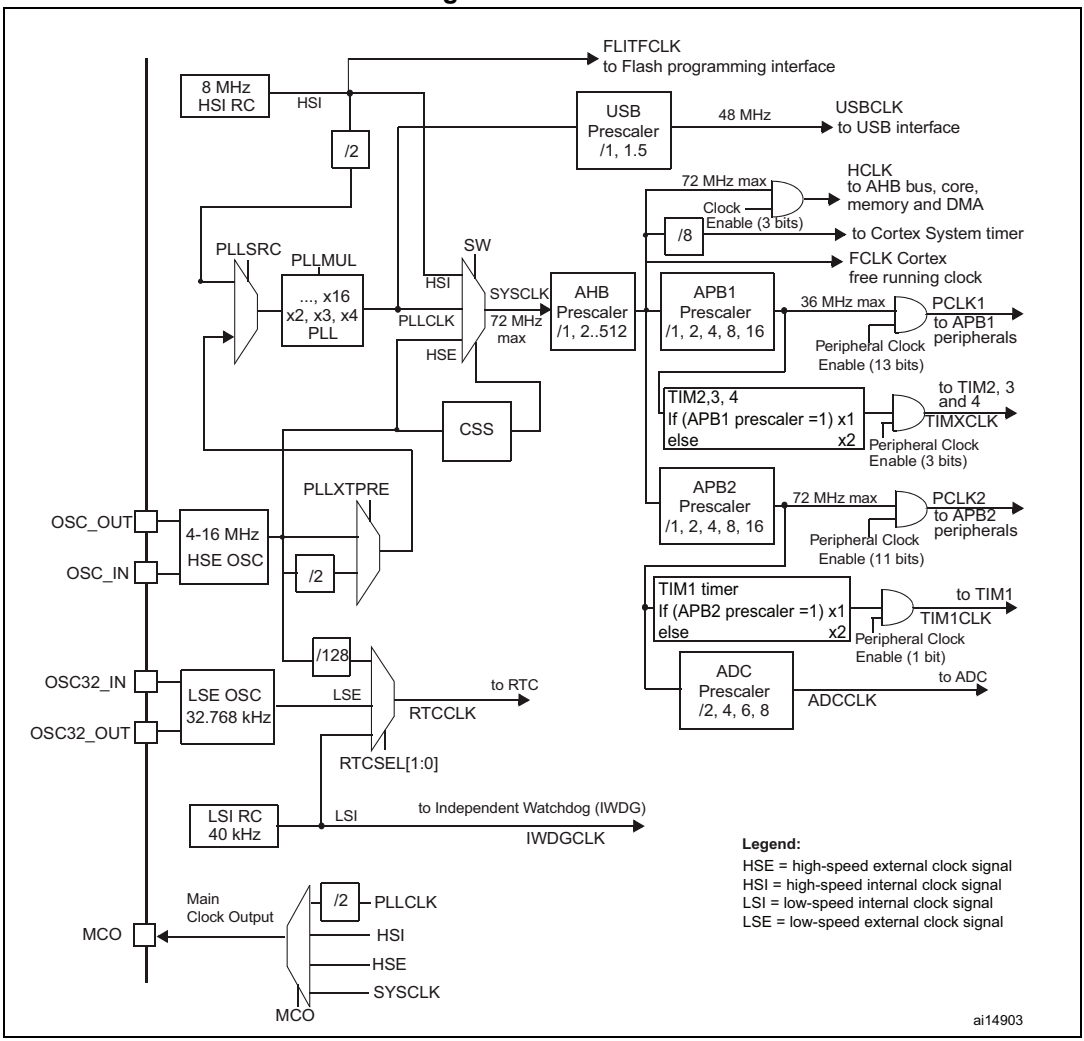
The board marking MB1136 C-03 (or higher) corresponds to a board using new LSE crystal (ABS25) and C26, C31, and C32 value update.

6.8 USART communication

The USART2 interface available on PA2 and PA3 of the STM32 microcontroller can be connected to ST-LINK MCU, ST morpho connector, or to ARDUINO® connector. The choice can be changed by setting the related solder bridges. By default, the USART2 communication between the target STM32 and ST-LINK MCU is enabled, in order to support virtual COM port for Mbed™ (SB13 and SB14 ON, SB62 and SB63 OFF). If the communication between the target STM32 PA2 (D1) or PA3 (D0) and shield or extension board is required, SB62 and SB63 must be ON, while SB13 and SB14 must be OFF. In such a case, it is possible to connect another USART to ST-LINK MCU using flying wires between the ST morpho connector and CN3. For instance, on NUCLEO-F103RB it is possible to use USART3 available on PC10 (TX) and PC11 (RX). Two flying wires need to be connected as follow:

- PC10 (USART3_TX) available on CN7 pin 1 to CN3 pin RX
- PC11 (USART3_RX) available on CN7 pin 2 to CN3 pin TX

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with USBCLK running at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

Frå s.12/117 i DocID13587 Rev 17 (databladet)

6.9 Solder bridges

Table 10. Solder bridges

Bridge	State(1)	Description
SB54, SB55 (X3 crystal)(2)	OFF	X3, C33, C34, R35, and R37 provide a clock as shown in electrical schematics PF0/PD0/PH0, PF1/PD1/PH1 are disconnected from CN7.
	ON	PF0/PD0/PH0 and PF1/PD1/PH1 are connected to CN7. (R35, R37, and SB50 must not be fitted).
SB3, SB5, SB7,SB9 (DEFAULT)	**ON**	Reserved, do not modify.
SB4,SB6, SB8,SB10 (RESERVED)	OFF	Reserved, do not modify.
SB48, SB49 (X2 crystal)(3)	OFF	X2, C31, C32, R34, and R36 deliver a 32 kHz clock. PC14, PC15 are not connected to CN7.
	ON	PC14 and PC15 are only connected to CN7. Remove only R34, R36.
* SB17 (B1-USER)	**ON**	B1 push button is connected to PC13.
	OFF	B1 push button is not connected to PC13.
SB12 (NRST)	ON	The NRST signal of the CN4 connector is connected to the NRST pin of the STM32.
	OFF	The NRST signal of the CN4 connector is not connected to the NRST pin of the STM32.
SB15 (SWO)	ON	The SWO signal of the CN4 connector is connected to PB3.
	OFF	The SWO signal is not connected.
SB11 (STM_RST)	**OFF**	No incidence on STM32F103CBT6 (ST-LINK MCU) NRST signal.
	ON	STM32F103CBT6 (ST-LINK MCU) NRST signal is connected to GND.
SB1 (USB-5V)	OFF	USB power management is functional.
	ON	USB power management is disabled.
SB2 (3.3 V)	ON	Output of voltage regulator LD39050PU33R is connected to 3.3V.
	OFF	Output of voltage regulator LD39050PU33R is not connected.
* SB21 (LD2-LED)	ON	Green user LED LD2 is connected to D13 of ARDUINO® signal.
	OFF	Green user LED LD2 is not connected.
SB56,SB51 (A4 and A5)	ON	PC1 and PC0 (ADC in) are connected to A4 and A5 (pin 5 and pin 6) on ARDUINO® connector CN8 and ST morpho connector CN7. Thus SB46 and SB52 must be OFF.
	OFF	PC1 and PC0 (ADC in) are disconnected to A4 and A5 (pin 5 and pin 6) on ARDUINO® connector CN8 and ST morpho connector CN7.
SB46,SB52 (I2C on A4 and A5)	OFF	PB9 and PB8 (I2C) are disconnected to A4 and A5 (pin 5 and pin 6) on ARDUINO® connector CN8 and ST morpho connector CN7.
	ON	PB9 and PB8 (I2C) are connected to A4 and A5 (pin 5 and pin 6) on ARDUINO® connector CN8 and ST morpho connector CN7 as I2C signals. Thus SB56 and SB51 must be OFF.

Table 10. Solder bridges (continued)

Bridge	State(1)	Description
SB45 (VBAT/VLCD)	ON	VBAT or VLCD on STM32 is connected to VDD.
	OFF	VBAT or VLCD on STM32 is not connected to VDD.
SB57 (VDDA/VREF+)	ON	VDDA/VREF+ on STM32 is connected to VDD.
	OFF	VDDA/VREF+ on STM32 is not connected to VDD and can be provided from pin 8 of CN5 (Used for external VREF+ provided by ARDUINO® shield)
* SB62, SB63 (USART)	**OFF**	PA2 and PA3 on STM32 are disconnected to D1 and D0 (pin 2 and pin 1) on ARDUINO® connector CN9 and ST morpho connector CN10.
	ON	PA2 and PA3 on STM32 are connected to D1 and D0 (pin 2 and pin 1) on ARDUINO® connector CN9 and ST morpho connector CN10 as USART signals. Thus SB13 and SB14 must be OFF.
SB13, SB14 (ST-LINK-USART)	**ON**	PA2 and PA3 on STM32F103CBT6 (ST-LINK MCU) are connected to PA3 and PA2 on STM32 to have USART communication between them. Thus SB61, SB62, and SB63 must be OFF.
	OFF	PA2 and PA3 on STM32F103CBT6 (ST-LINK MCU) are disconnected to PA3 and PA2 on STM32.
SB16,SB50(MCO)(2)	OFF	MCO on STM32F103CBT6 (ST-LINK MCU) are disconnected to PF0/PD0/PH0 on STM32.
	ON	MCO on STM32F103CBT6 (ST-LINK MCU) are connected to PF0/PD0/PH0 on STM32.

1. The default SBx state is shown in bold.
2. The default configuration depends on the board version. Refer to *Section 6.7.1: OSC clock supply* for details.
3. The default configuration depends on the board version. Refer to *Section 6.7.2: OSC 32 kHz clock supply* for details.

All the other solder bridges present on the STM32 Nucleo board are used to configure several I/Os and power supply pins for compatibility of features and pinout with STM32 supported.

All STM32 Nucleo boards are delivered with the solder-bridges configured according to the target supported STM32.

6.10 Extension connectors

Figure 10 to *Figure 26* show the signals connected by default to ARDUINO® Uno V3 connectors (CN5, CN6, CN8, CN9) and to ST morpho connector (CN7 and CN10), for each STM32 Nucleo board.

* Koblingsbruene (loddebruene/"solder brigdes") kan du sjå bak på plattformkortet. Når ei bru er PÅ/"ON", er det lodda på ein 0-ohmsmotstand som koblar dei to sidene saman.
Kretskjema på s. 18-21 (STM-side 63-66/69, UM1724, rev13) viser også desse koblingane.
Merk: Plattformkortet vårt har følgjande koblingar:
- Brytaren *B1-USER* er kobla til mikrokontrollerpinne PC13 via brua SB17. (Sjå og skjema s.19.)
- Lysdioden *LD2-LED* er kobla til pinne PA5 via bruene SB21 og SB42. (Sjå og skjema s.21.)
- Perifermodulen *USART2* inne i uC-en er kobla til pinnane PA2 (Tx) og PA3 (Rx).
Alle signal- og kraftlinjer frå uC-en er tilgjengelege på *Morpho*-kontaktane, sjå s.16-17.

Figure 14. NUCLEO-F103RB

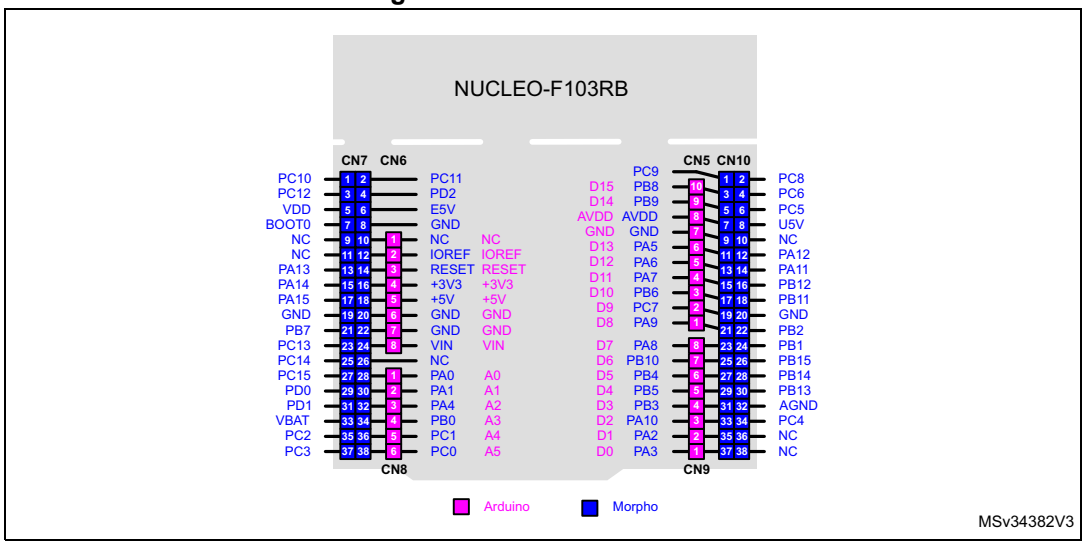
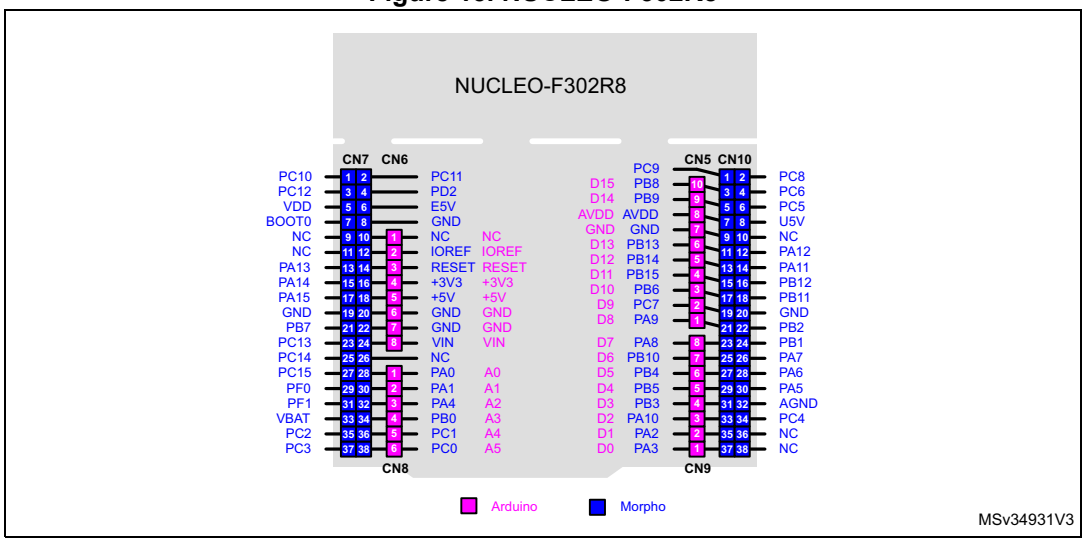


Figure 15. NUCLEO-F302R8



Figur 14 vist i større utgåve.Dette er ein veldig nyttig figur når du skal kobla plattformkortet til eksterne modular.

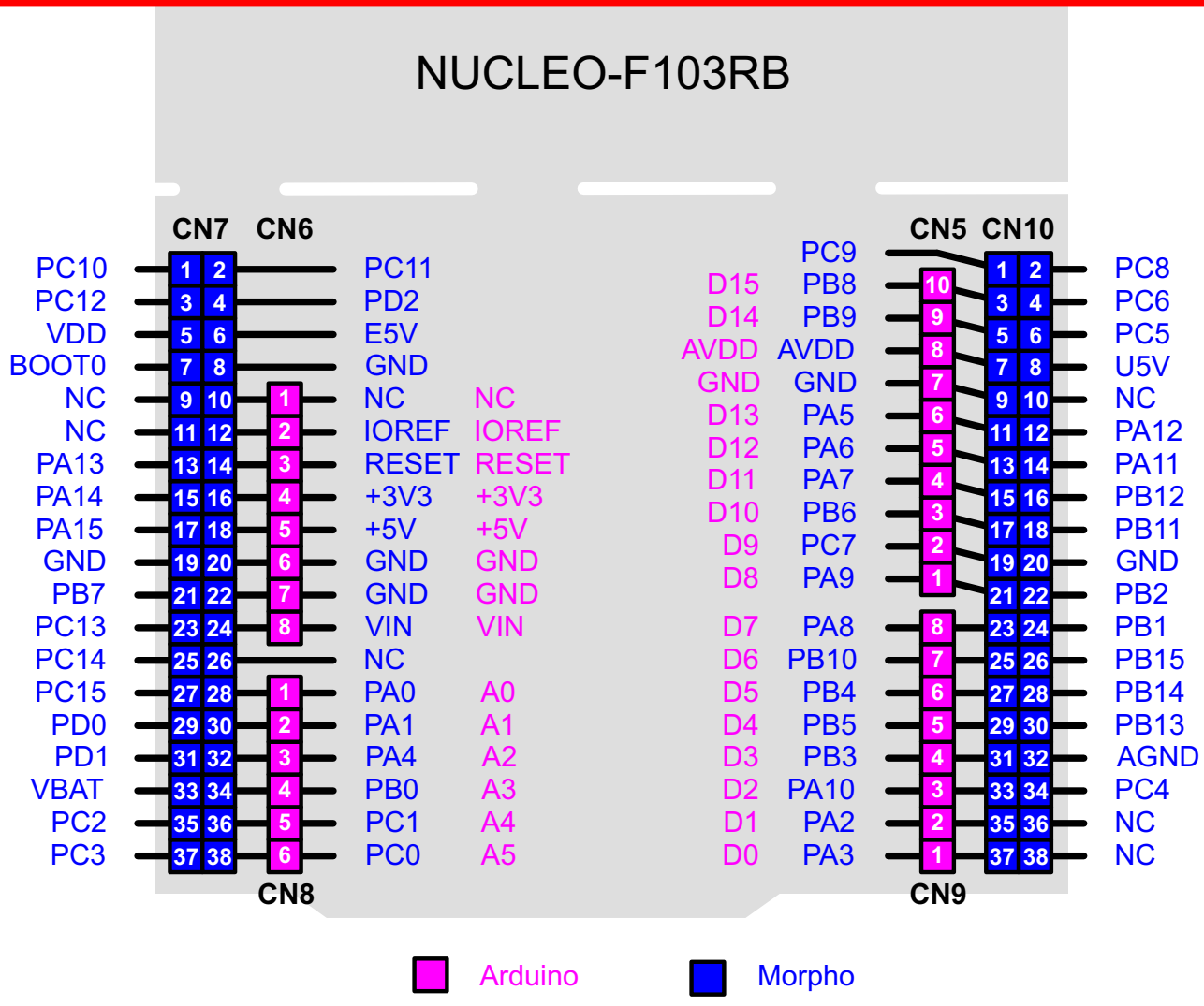


Table 23. ARDUINO® connectors on NUCLEO-L476RG (continued)

Connector	Pin	Pin name	STM32 pin	Function
CN5 digital	2	D9	PC7	TIM3_CH2
	1	D8	PA9	-
CN9 digital	8	D7	PA8	-
	7	D6	PB10	TIM2_CH3
	6	D5	PB4	TIM3_CH1
	5	D4	PB5	-
	4	D3	PB3	TIM2_CH2
	3	D2	PA10	-
	2	D1	PA2	USART2_TX
	1	D0	PA3	USART2_RX

1. Refer to *Table 10: Solder bridges* for details.

6.12 ST morpho connector

The ST morpho connector consists in male pin headers (CN7 and CN10) accessible on both sides of the board. They can be used to connect the STM32 Nucleo board to an extension board or a prototype/wrapping board placed on top or on bottom side of the STM32 Nucleo board. All signals and power pins of the STM32 are available on ST morpho connector. This connector can also be probed by an oscilloscope, logical analyzer or voltmeter.

Table 24 to *Table 33* show the pin assignments of each STM32 on ST morpho connector.

Table 24. ST morpho connector on NUCLEO-F030R8

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin	Name	Name	Pin	Pin	Name	Name	Pin
1	PC10	PC11	2	1	PC9	PC8	2
3	PC12	PD2	4	3	PB8	PC6	4
5	VDD	E5V	6	5	PB9	PC5	6
7	BOOT0(1)	GND	8	7	AVDD	U5V(2)	8
9	PF6	-	10	9	GND	-	10
11	PF7	IOREF	12	11	PA5	PA12	12
13	PA13	RESET	14	13	PA6	PA11	14
15	PA14	+3.3V	16	15	PA7	PB12	16
17	PA15	+5V	18	17	PB6	PB11	18
19	GND	GND	20	19	PC7	GND	20
21	PB7	GND	22	21	PA9	PB2	22
23	PC13(3)	VIN	24	23	PA8	PB1	24
25	PC14(3)	-	26	25	PB10	PB15	26

Table 26. ST morpho connector on NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F303RE, NUCLEO-F334R8

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin	Name	Name	Pin	Pin	Name	Name	Pin
1	PC10	PC11	2	1	PC9	PC8	2
3	PC12	PD2	4	3	PB8	PC6	4
5	VDD	E5V	6	5	PB9	PC5	6
7	BOOT0(1)(2)	GND	8	7	AVDD	U5V(3)	8
9	-	-	10	9	GND	-	10
11	-	IOREF	12	11	PA5	PA12	12
13	PA13(4)	RESET	14	13	PA6	PA11	14
15	PA14(4)	+3.3V	16	15	PA7	PB12	16
17	PA15	+5V	18	17	PB6	PB11	18
19	GND	GND	20	19	PC7	GND	20
21	PB7	GND	22	21	PA9	PB2	22
23	PC13	VIN	24	23	PA8	PB1	24
25	PC14	-	26	25	PB10	PB15	26
27	PC15	PA0	28	27	PB4	PB14	28
29	PF0	PA1	30	29	PB5	PB13	30
31	PF1	PA4	32	31	PB3	AGND	32
33	VBAT	PB0	34	33	PA10	PC4	34
35	PC2	PC1 or PB9(5)	36	35	PA2	-	36
37	PC3	PC0 or PB8(5)	38	37	PA3	-	38

1. The default state of BOOT0 is LOW. It can be set to HIGH when a jumper is on pin5-7 of CN7. Two unused jumpers are available on CN11 and CN12 (bottom side of the board).
2. CN7 pin 7 (BOOT0) can be configured by engineering byte as PF11 on NUCLEO-F091RC.
3. U5V is 5 V power from ST-LINK/V2-1 USB connector and it rises before +5V.
4. PA13 and PA14 share with SWD signals connected to ST-LINK/V2-1, it is not recommended to use them as IO pins if the ST-LINK part is not cut.
5. Refer to *Table 10: Solder bridges* for details.

Table 27. ST morpho connector on NUCLEO-F103RB

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin	Name	Name	Pin	Pin	Name	Name	Pin
1	PC10	PC11	2	1	PC9	PC8	2
3	PC12	PD2	4	3	PB8	PC6	4
5	VDD	E5V	6	5	PB9	PC5	6

Table 27. ST morpho connector on NUCLEO-F103RB (continued)

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin	Name	Name	Pin	Pin	Name	Name	Pin
7	BOOT0(1)	GND	8	7	AVDD	U5V(2)	8
9	-	-	10	9	GND	-	10
11	-	IOREF	12	11	PA5	PA12	12
13	PA13(3)	RESET	14	13	PA6	PA11	14
15	PA14(3)	+3.3V	16	15	PA7	PB12	16
17	PA15	+5V	18	17	PB6	PB11	18
19	GND	GND	20	19	PC7	GND	20
21	PB7	GND	22	21	PA9	PB2	22
23	PC13	VIN	24	23	PA8	PB1	24
25	PC14	-	26	25	PB10	PB15	26
27	PC15	PA0	28	27	PB4	PB14	28
29	PD0	PA1	30	29	PB5	PB13	30
31	PD1	PA4	32	31	PB3	AGND	32
33	VBAT	PB0	34	33	PA10	PC4	34
35	PC2	PC1 or PB9(4)	36	35	PA2	-	36
37	PC3	PC0 or PB8(4)	38	37	PA3	-	38

1. The default state of BOOT0 is LOW. It can be set to HIGH when a jumper is on pin5-7 of CN7. Two unused jumpers are available on CN11 and CN12 (bottom side of the board).
2. U5V is 5 V power from ST-LINK/V2-1 USB connector and it rises before +5 V.
3. PA13 and PA14 share with SWD signals connected to ST-LINK/V2-1, it is not recommended to use them as IO pins if the ST-LINK part is not cut.
4. Refer to *Table 10: Solder bridges* for details.

Merk: Eit fullstendig oversyn over pinnar og funksjonar kan finnast
på s.26-31 (s. 28-33/117 i databladet.)
Tabellane der samt uC-blokkskjemaet på s. 22 her (s.11/117) er sentrale når ein skal planleggja maskinvaren i eit innebygd system (IBS), som ofte er eit mikrokontrollerbasert system.
Ein må då ut frå spesifikasjonen til IBS-et
- finna ut kor mange signallinjer og kva type det er behov for,
- finna ut kva perifermodular inne i uC-en ein då skal bruka,
- og så ut frå dette setja opp kva konkrete pinnar som skal brukast.

Etter denne analysen kan ein laga eit detaljert blokkskjema av maskinvaren for IBS-et.

Appendix A Electrical schematics

Frå brukarmanualen UM1724, rev.13, s.63-66/69.

Figure 27 to *Figure 30* show the electrical schematics of the STM32 Nucleo-64 board.

Figure 27. Top and Power

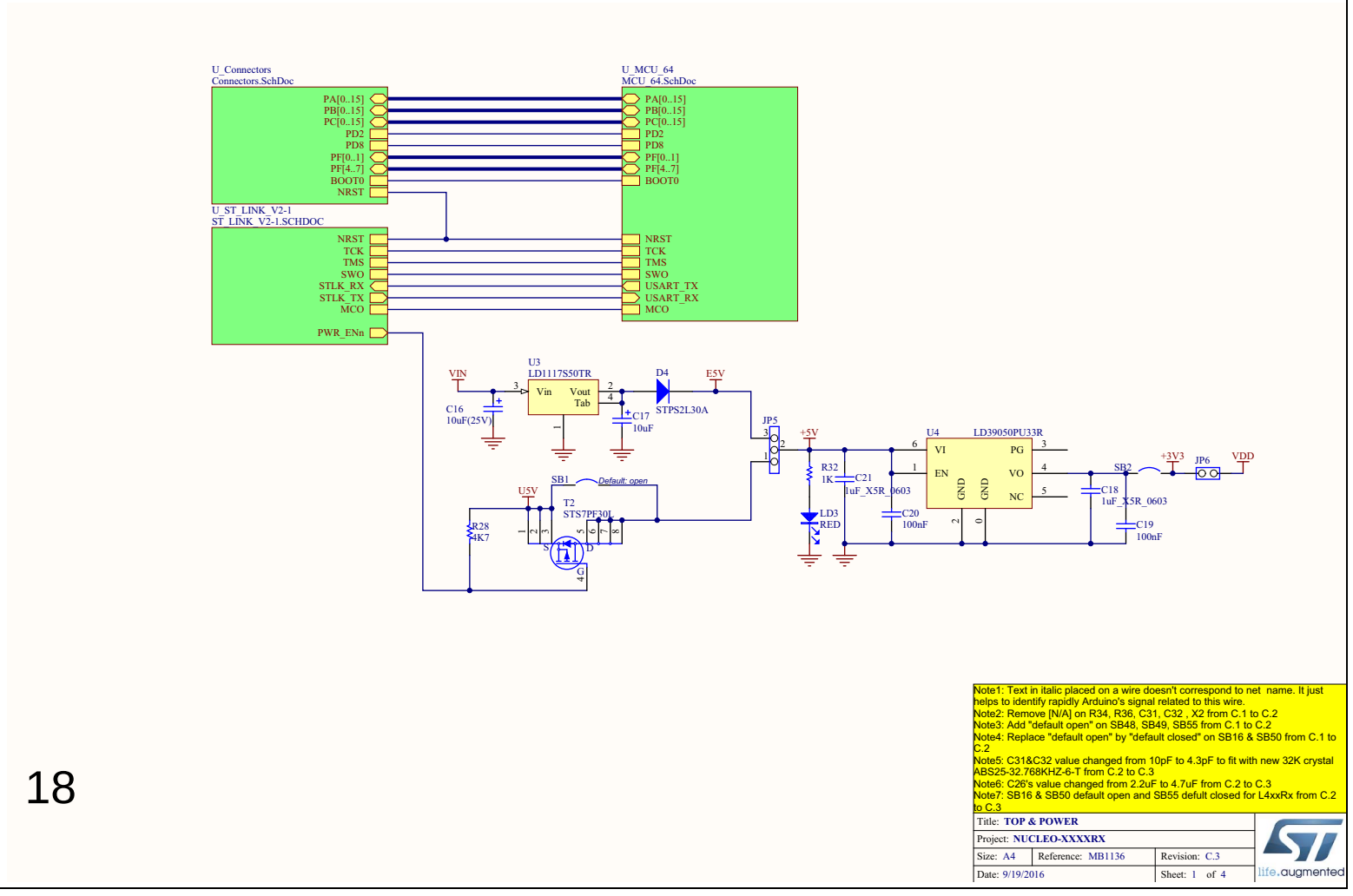


Figure 28. STM32 MCU

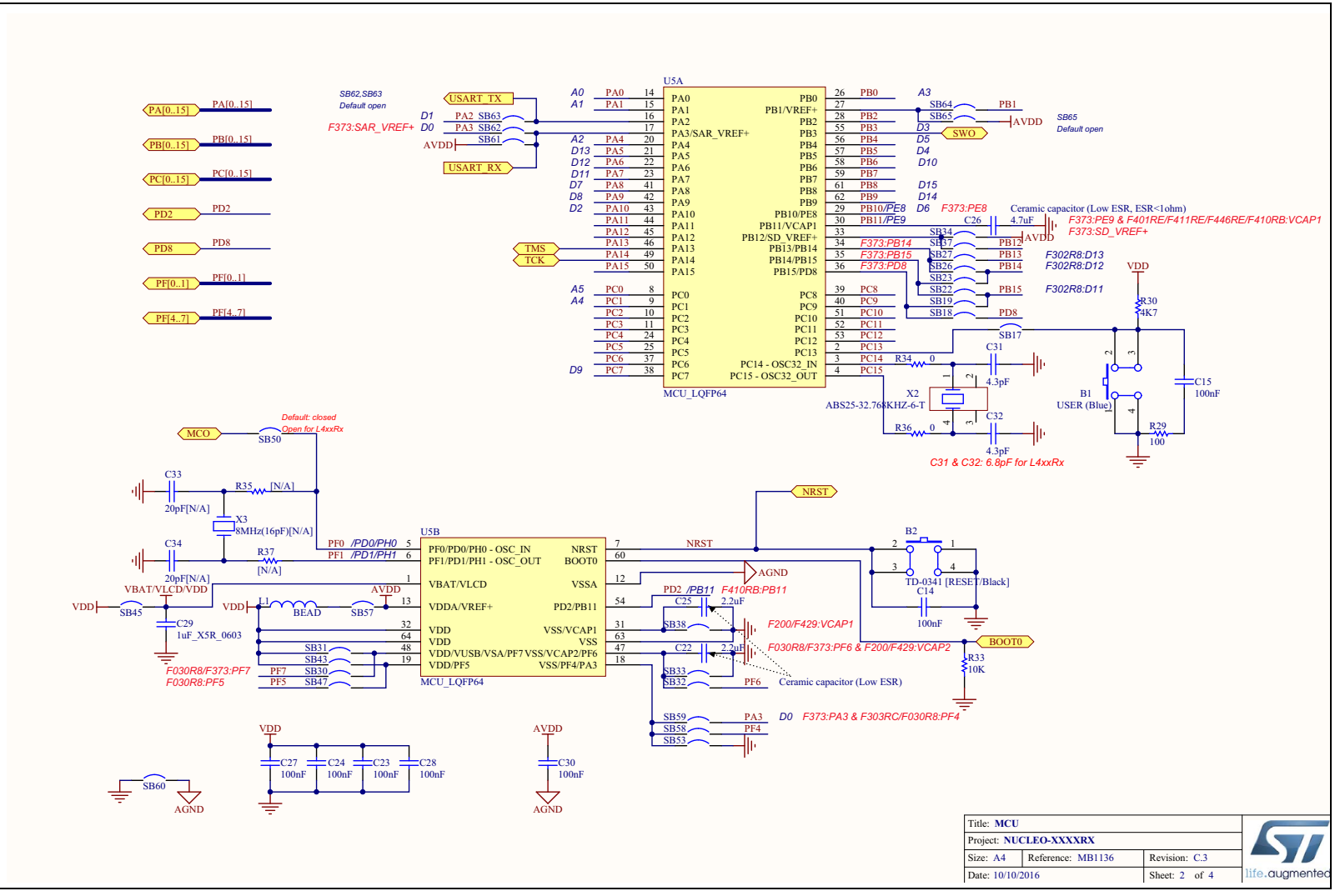


Figure 29. ST-LINK/V2-1

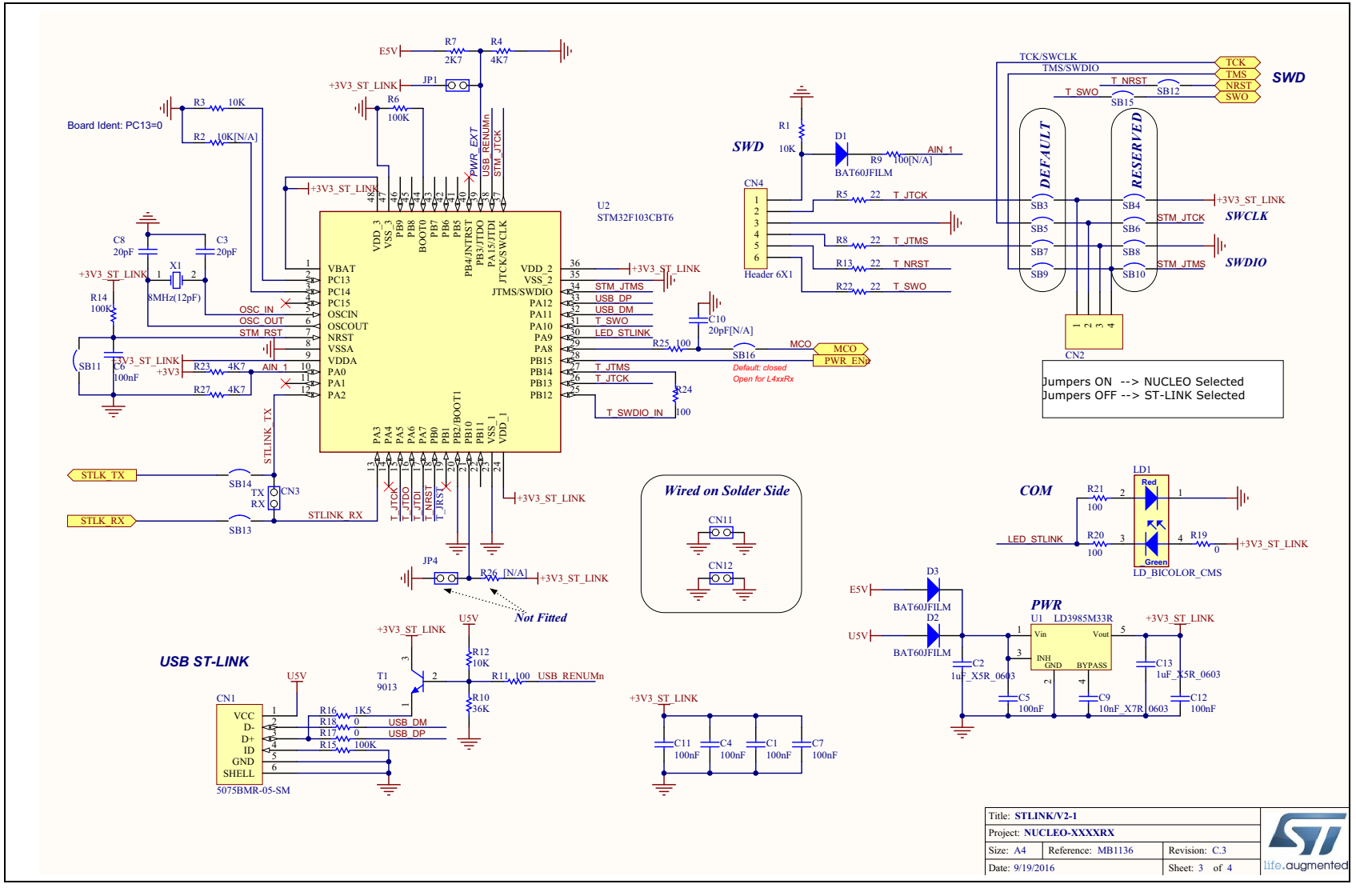


Figure 30. Extension connectors

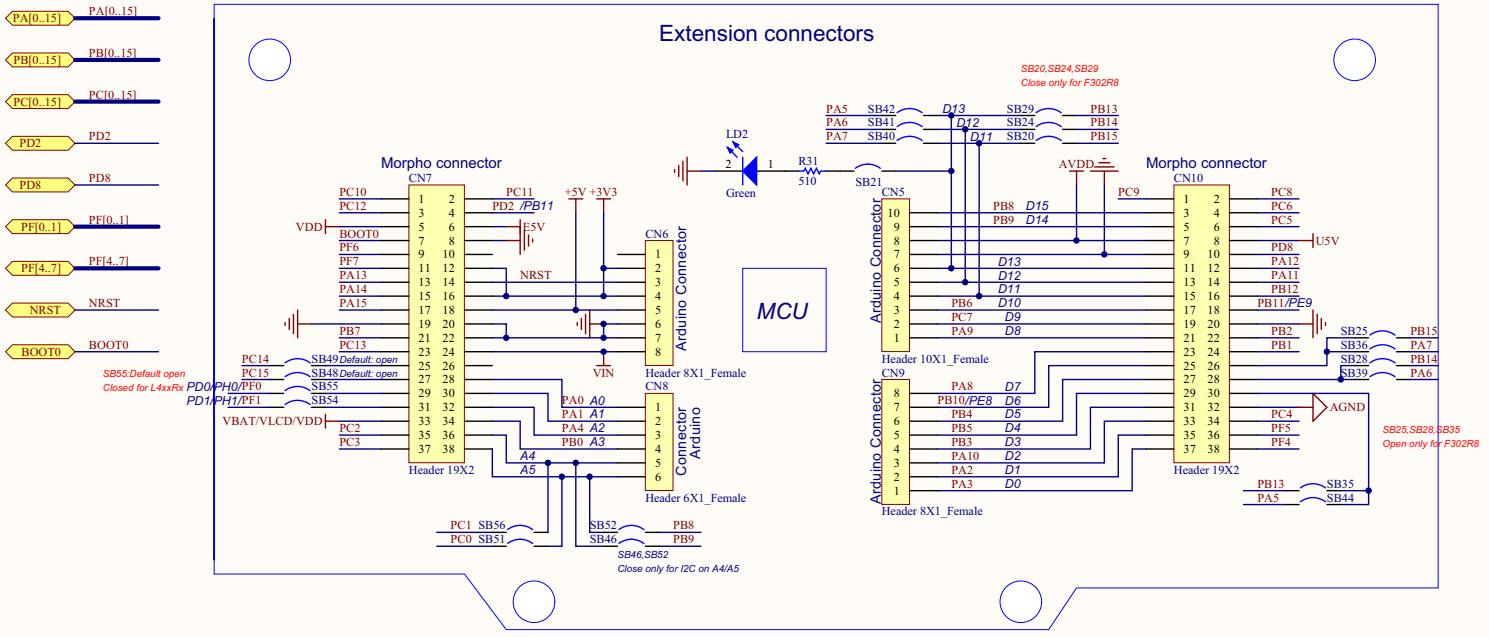
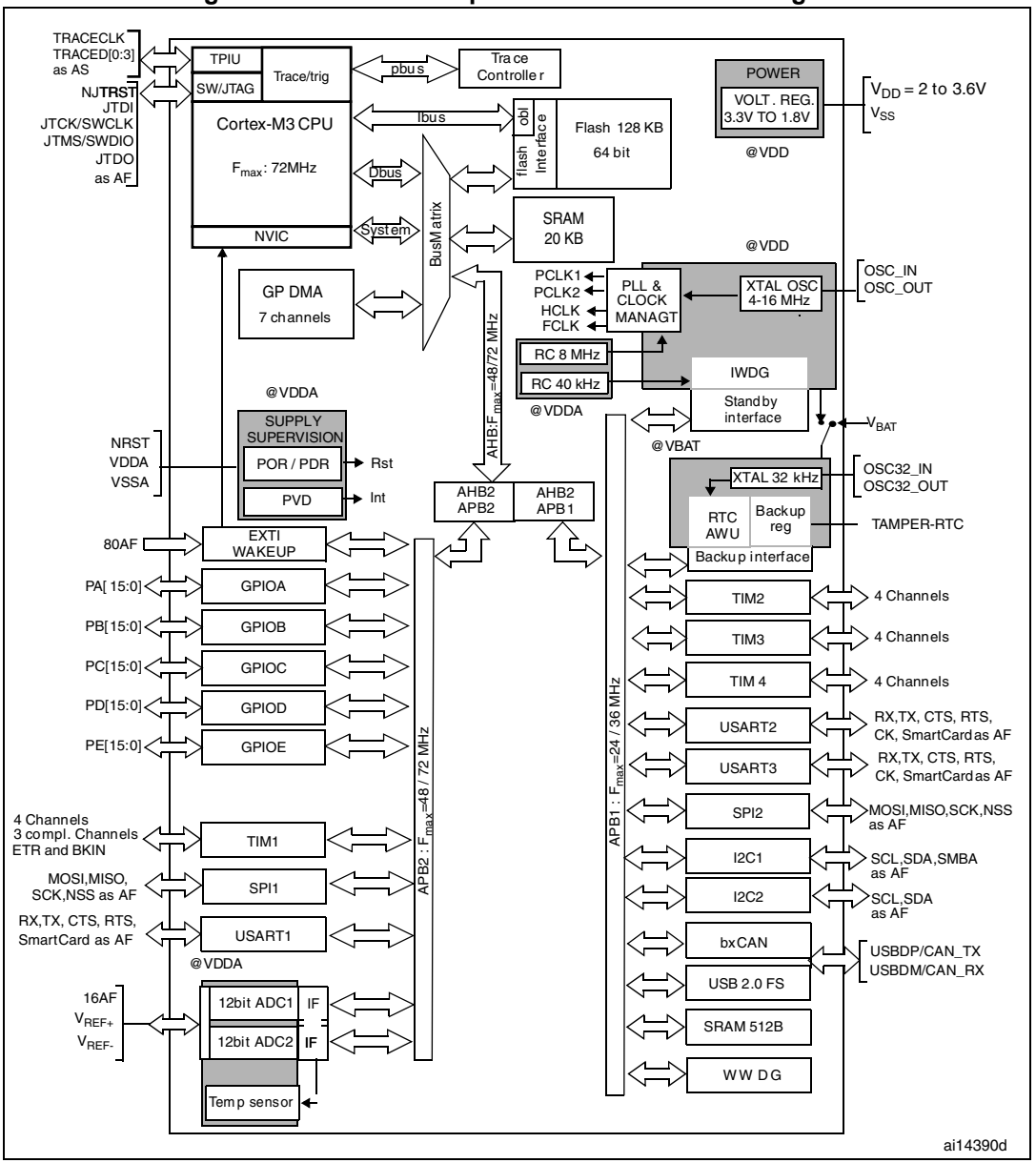


Figure 1. STM32F103xx performance line block diagram



1. T_A = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

Frå s.11/117 i DocID13587 Rev 17 (databladet)

3 Memory and bus architecture

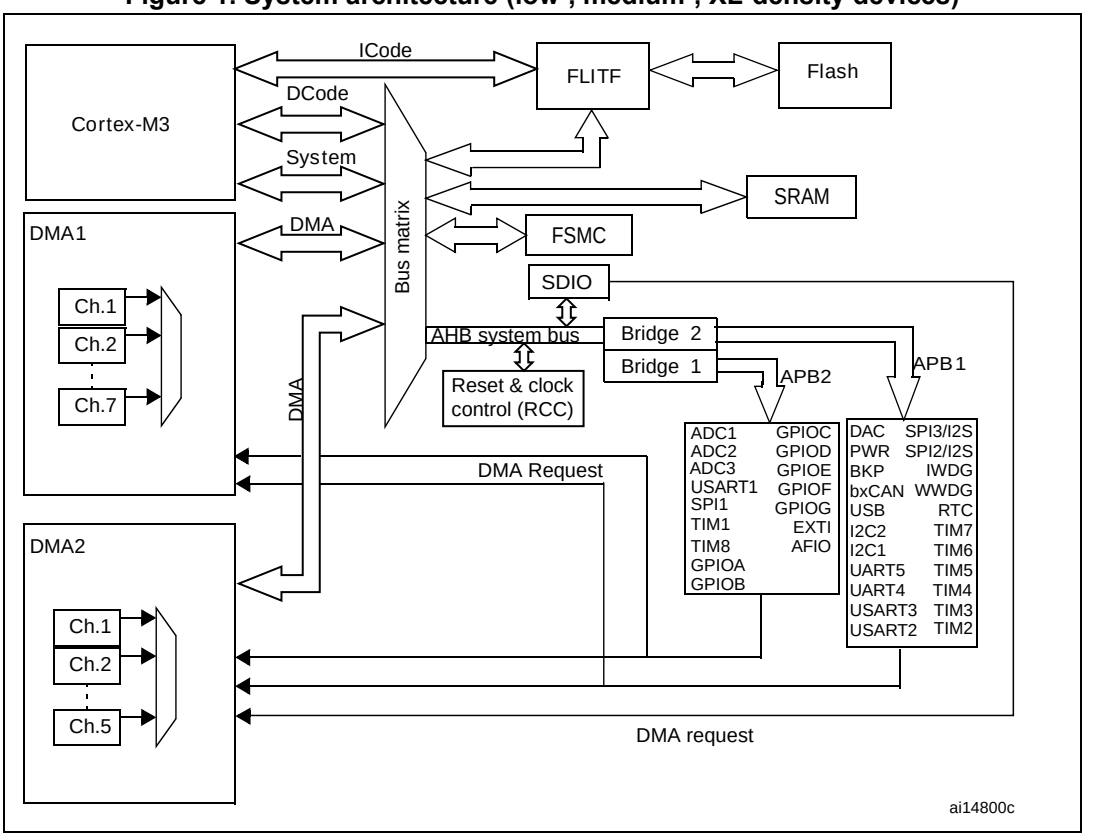
3.1 System architecture

In low-, medium-, high- and XL-density devices, the main system consists of:

- Four masters:
  - Cortex®-M3 core DCode bus (D-bus) and System bus (S-bus)
  - GP-DMA1 & 2 (general-purpose DMA)
- Four slaves:
  - Internal SRAM
  - Internal Flash memory
  - FSMC
  - AHB to APBx (APB1 or APB2), which connect all the APB peripherals

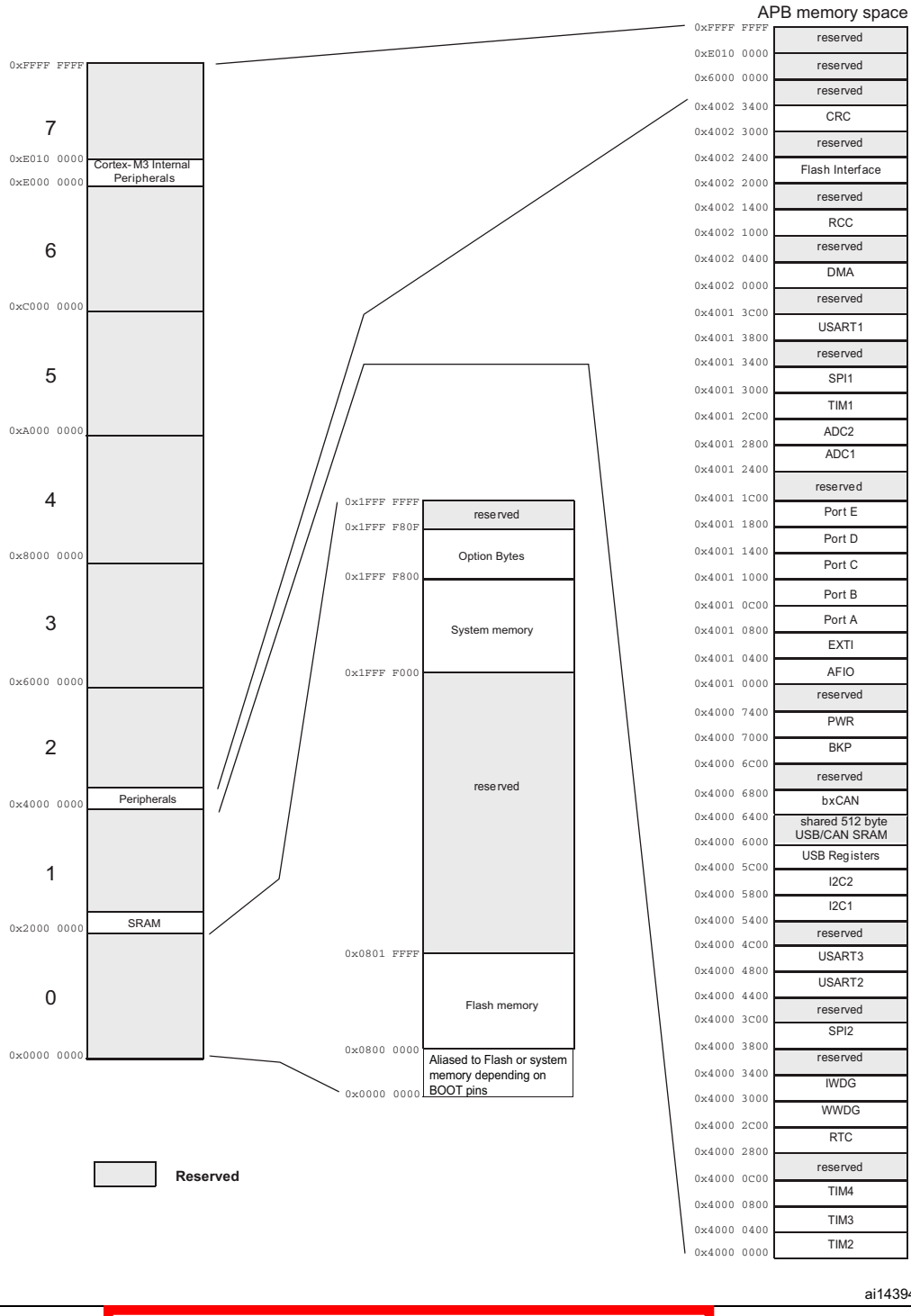
These are interconnected using a multilayer AHB bus architecture as shown in *Figure 1*:

Figure 1. System architecture (low-, medium-, XL-density devices)



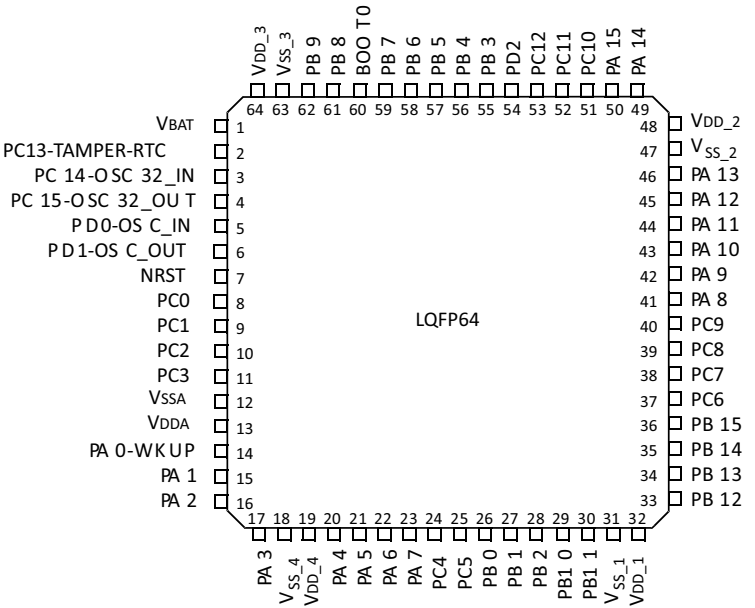
Frå s.47/1136 i RM0008 Rev 21 (Referansemanualen)

Figure 11. Memory map



ai14394f

Figure 6. STM32F103xx performance line LQFP64 pinout



Frå s.24/117 i DocID13587 Rev 17 (databladet)

Table 5. Medium-density STM32F103xx pin definitions

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	B2	-	-	-	1	-	PE2	I/O	FT	PE2	TRACECK	-
B3	A1	-	-	-	2	-	PE3	I/O	FT	PE3	TRACED0	-
C3	B1	-	-	-	3	-	PE4	I/O	FT	PE4	TRACED1	-
D3	C2	-	-	-	4	-	PE5	I/O	FT	PE5	TRACED2	-
E3	D2	-	-	-	5	-	PE6	I/O	FT	PE6	TRACED3	-
B2	E2	1	B2	1	6	-	V_{BAT}	S	-	V_{BAT}	-	-
A2	C1	2	A2	2	7	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
A1	D1	3	A1	3	8	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
B1	E1	4	B1	4	9	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
C2	F2	-	-	-	10	-	V_{SS_5}	S	-	V_{SS_5}	-	-
D2	G2	-	-	-	11	-	V_{DD_5}	S	-	V_{DD_5}	-	
C1	F1	5	C1	5	12	2	OSC_IN	I	-	OSC_IN	-	PD0(7)
D1	G1	6	D1	6	13	3	OSC_OUT	O	-	OSC_OUT		PD1(7)
E1	H2	7	E1	7	14	4	NRST	I/O	-	NRST	-	-
F1	H1	-	E3	8	15	-	PC0	I/O	-	PC0	ADC12_IN10	-
F2	J2	-	E2	9	16	-	PC1	I/O	-	PC1	ADC12_IN11	-
E2	J3	-	F2	10	17	-	PC2	I/O	-	PC2	ADC12_IN12	-
F3	K2	-	-(8)	11	18	-	PC3	I/O	-	PC3	ADC12_IN13	-
G1	J1	8	F1	12	19	5	V_{SSA}	S	-	V_{SSA}	-	-
H1	K1	-	-	-	20	-	V_{REF-}	S	-	V_{REF-}	-	-
J1	L1	-	G1(8)	-	21	-	V_{REF+}	S	-	V_{REF+}	-	-
K1	M1	9	H1	13	22	6	V_{DDA}	S	-	V_{DDA}	-	-

Desse tabellane gir eit fullstendig oversyn over pinnar og funksjonar og er frå s. 28-33/117 i databladet. Tilgjengelege signal for IC-kretstypen vår er markert med raudt.
Tabellane samt uC-blokkskjemaet på s. 22 (s.11/117) er altså sentrale når ein skal planleggja maskinvaren i eit innebygd system (IBS), som ofte er eit mikrokontrollerbasert system.
Ein må då ut frå spesifikasjonen til IBS-et
- finna ut kor mange signallinjer og kva type det er behov for,
- finna ut kva perifermodular inne i uC-en ein då skal bruka,
- og så ut frå dette setja opp kva konkrete pinnar som skal brukast.

Etter denne analysen kan ein laga eit detaljert blokkskjema av maskinvaren for IBS-et.

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
G2	L2	10	G2	14	23	7	PA0-WKUP	I/O	-	PA0	WKUP/ USART2_CTS[9]/ ADC12_IN0/ TIM2_CH1_ ETR[9]	-
H2	M2	11	H2	15	24	8	PA1	I/O	-	PA1	USART2_RTS[9]/ ADC12_IN1/ TIM2_CH2[9]	-
J2	K3	12	F3	16	25	9	PA2	I/O	-	PA2	USART2_TX[9]/ ADC12_IN2/ TIM2_CH3[9]	-
K2	L3	13	G3	17	26	10	PA3	I/O	-	PA3	USART2_RX[9]/ ADC12_IN3/ TIM2_CH4[9]	-
E4	E3	-	C2	18	27	-	V_{SS_4}	S	-	V_{SS_4}	-	-
F4	H3	-	D2	19	28	-	V_{DD_4}	S	-	V_{DD_4}	-	-
G3	M3	14	H3	20	29	11	PA4	I/O	-	PA4	SPI1_NSS[9]/ USART2_CK[9]/ ADC12_IN4	-
H3	K4	15	F4	21	30	12	PA5	I/O	-	PA5	SPI1_SCK[9]/ ADC12_IN5	-
J3	L4	16	G4	22	31	13	PA6	I/O	-	PA6	SPI1_MISO[9]/ ADC12_IN6/ TIM3_CH1[9]	TIM1_BKIN
K3	M4	17	H4	23	32	14	PA7	I/O	-	PA7	SPI1_MOSI[9]/ ADC12_IN7/ TIM3_CH2[9]	TIM1_CH1N
G4	K5	-	H5	24	33		PC4	I/O	-	PC4	ADC12_IN14	-
H4	L5	-	H6	25	34		PC5	I/O	-	PC5	ADC12_IN15	-
J4	M5	18	F5	26	35	15	PB0	I/O	-	PB0	ADC12_IN8/ TIM3_CH3[9]	TIM1_CH2N
K4	M6	19	G5	27	36	16	PB1	I/O	-	PB1	ADC12_IN9/ TIM3_CH4[9]	TIM1_CH3N

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
G5	L6	20	G6	28	37	17	PB2	I/O	FT	PB2/BOOT1	-	-
H5	M7	-	-	-	38	-	PE7	I/O	FT	PE7	-	TIM1_ETR
J5	L7	-	-	-	39	-	PE8	I/O	FT	PE8	-	TIM1_CH1N
K5	M8	-	-	-	40	-	PE9	I/O	FT	PE9	-	TIM1_CH1
G6	L8	-	-	-	41	-	PE10	I/O	FT	PE10	-	TIM1_CH2N
H6	M9	-	-	-	42	-	PE11	I/O	FT	PE11	-	TIM1_CH2
J6	L9	-	-	-	43	-	PE12	I/O	FT	PE12	-	TIM1_CH3N
K6	M10	-	-	-	44	-	PE13	I/O	FT	PE13	-	TIM1_CH3
G7	M11	-	-	-	45	-	PE14	I/O	FT	PE14	-	TIM1_CH4
H7	M12	-	-	-	46	-	PE15	I/O	FT	PE15	-	TIM1_BKIN
J7	L10	21	G7	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(9)	TIM2_CH3
K7	L11	22	H7	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(9)	TIM2_CH4
E7	F12	23	D6	31	49	18	V_{SS_1}	S	-	V_{SS_1}	-	-
F7	G12	24	E6	32	50	19	V_{DD_1}	S	-	V_{DD_1}	-	-
K8	L12	25	H8	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(9)/ TIM1_BKIN(9)	-
J8	K12	26	G8	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(9)/ TIM1_CH1N (9)	-
H8	K11	27	F8	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(9) TIM1_CH2N (9)	-
G8	K10	28	F7	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(9)	-
K9	K9	-	-	-	55	-	PD8	I/O	FT	PD8	-	USART3_TX
J9	K8	-	-	-	56	-	PD9	I/O	FT	PD9	-	USART3_RX

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
H9	J12	-	-	-	57	-	PD10	I/O	FT	PD10	-	USART3_CK
G9	J11	-	-	-	58	-	PD11	I/O	FT	PD11	-	USART3_CTS
K10	J10	-	-	-	59	-	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
J10	H12	-	-	-	60	-	PD13	I/O	FT	PD13	-	TIM4_CH2
H10	H11	-	-	-	61	-	PD14	I/O	FT	PD14	-	TIM4_CH3
G10	H10	-	-	-	62	-	PD15	I/O	FT	PD15	-	TIM4_CH4
F10	E12	-	F6	37	63	-	PC6	I/O	FT	PC6	-	TIM3_CH1
E10	E11		E7	38	64	-	PC7	I/O	FT	PC7	-	TIM3_CH2
F9	E10		E8	39	65	-	PC8	I/O	FT	PC8	-	TIM3_CH3
E9	D12	-	D8	40	66	-	PC9	I/O	FT	PC9	-	TIM3_CH4
D9	D11	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(9)/ MCO	-
C9	D10	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX(9)/ TIM1_CH2(9)	-
D10	C12	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX(9)/ TIM1_CH3(9)	-
C10	B12	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(9)/ USBDM/ TIM1_CH4(9)	-
B10	A12	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX(9) /USBDP TIM1_ETR(9)	-
A10	A11	34	A8	46	72	25	PA13	I/O	FT	JTMS/SWDIO	-	PA13
F8	C11	-	-	-	73	-	Not connected					-
E6	F11	35	D5	47	74	26	V_{SS_2}	S	-	V_{SS_2}	-	-
F6	G11	36	E5	48	75	27	V_{DD_2}	S	-	V_{DD_2}	-	-

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A9	A10	37	A7	49	76	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
A8	A9	38	A6	50	77	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ ETR/ PA15 /SPI1_NSS
B9	B11	-	B7	51	78		PC10	I/O	FT	PC10	-	USART3_TX
B8	C10	-	B6	52	79		PC11	I/O	FT	PC11	-	USART3_RX
C8	B10	-	C5	53	80		PC12	I/O	FT	PC12	-	USART3_CK
-	C9	-	C1	-	81	2	PD0	I/O	FT	PD0	-	CANRX
-	B9	-	D1	-	82	3	PD1	I/O	FT	PD1	-	CANTX
B7	C8		B5	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	-
C7	B8	-	-	-	84	-	PD3	I/O	FT	PD3	-	USART2_CTS
D7	B7	-	-	-	85	-	PD4	I/O	FT	PD4	-	USART2_RTS
B6	A6	-	-	-	86	-	PD5	I/O	FT	PD5	-	USART2_TX
C6	B6	-	-	-	87	-	PD6	I/O	FT	PD6	-	USART2_RX
D6	A5	-	-	-	88	-	PD7	I/O	FT	PD7	-	USART2_CK
A7	A8	39	A5	55	89	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI1_SCK
A6	A7	40	A4	56	90	31	PB4	I/O	FT	JNTRST	-	TIM3_CH1/ PB4/ SPI1_MISO
C5	C5	41	C4	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
B5	B5	42	D3	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL(9)/ TIM4_CH1(9)	USART1_TX
A5	B4	43	C3	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA(9)/ TIM4_CH2(9)	USART1_RX
D5	A4	44	B4	60	94	35	BOOT0	I		BOOT0	-	-

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
B4	A3	45	B3	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3(9)	I2C1_SCL / CANRX
A4	B3	46	A3	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4(9)	I2C1_SDA/ CANTX
D4	C3	-	-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	-
C4	A2	-	-	-	98	-	PE1	I/O	FT	PE1	-	-
E5	D3	47	D4	63	99	36	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	C4	48	E4	64	100	1	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48, UFQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
   The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.

9 General-purpose and alternate-function I/Os (GPIOs and AFIOs)

Low-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbytes.

Medium-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbytes.

High-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 256 and 512 Kbytes.

XL-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbytes and 1 Mbyte.

Connectivity line devices are STM32F105xx and STM32F107xx microcontrollers.

This section applies to the whole STM32F10xxx family, unless otherwise specified.

9.1 GPIO functional description

Each of the general-purpose I/O ports has two 32-bit configuration registers (GPIOx_CRL, GPIOx_CRH), two 32-bit data registers (GPIOx_IDR, GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 16-bit reset register (GPIOx_BRR) and a 32-bit locking register (GPIOx_LCKR).

Subject to the specific hardware characteristics of each I/O port listed in the *datasheet*, each port bit of the General Purpose IO (GPIO) Ports, can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain
- Output push-pull
- Alternate function push-pull
- Alternate function open-drain

Each I/O port bit is freely programmable, however the I/O port registers have to be accessed as 32-bit words (half-word or byte accesses are not allowed). The purpose of the GPIOx_BSRR and GPIOx_BRR registers is to allow atomic read/modify accesses to any of the GPIO registers. This way, there is no risk that an IRQ occurs between the read and the modify access.

Figure 13 shows the basic structure of an I/O Port bit.

Frå s.159-160/1136 i RM0008 Rev 21 (Referansemanualen)

Figure 13. Basic structure of a standard I/O port bit

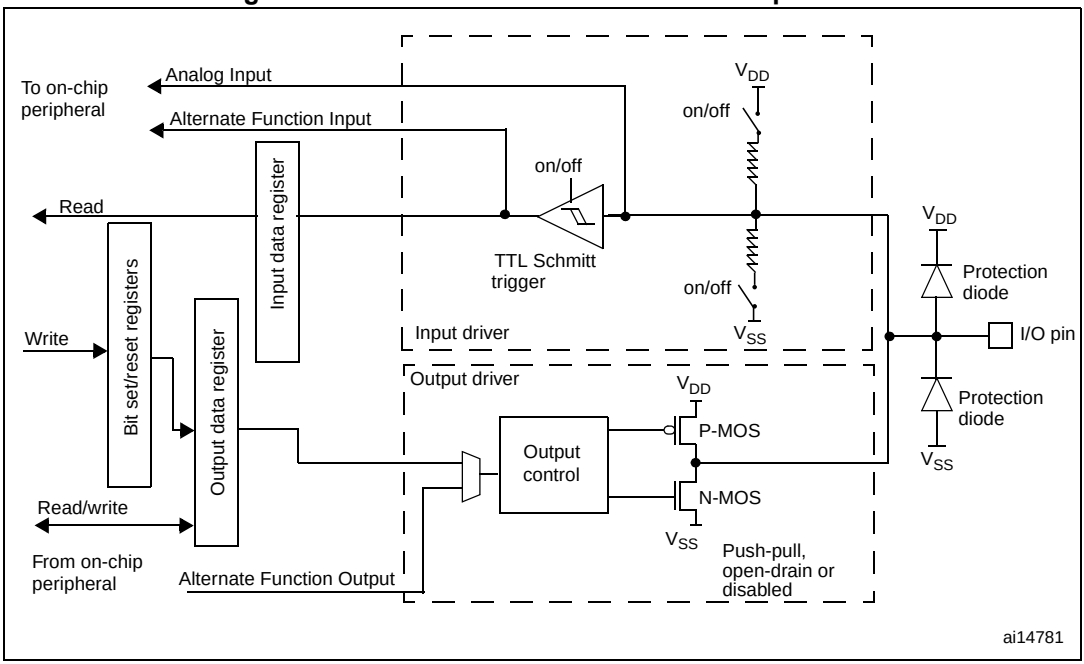
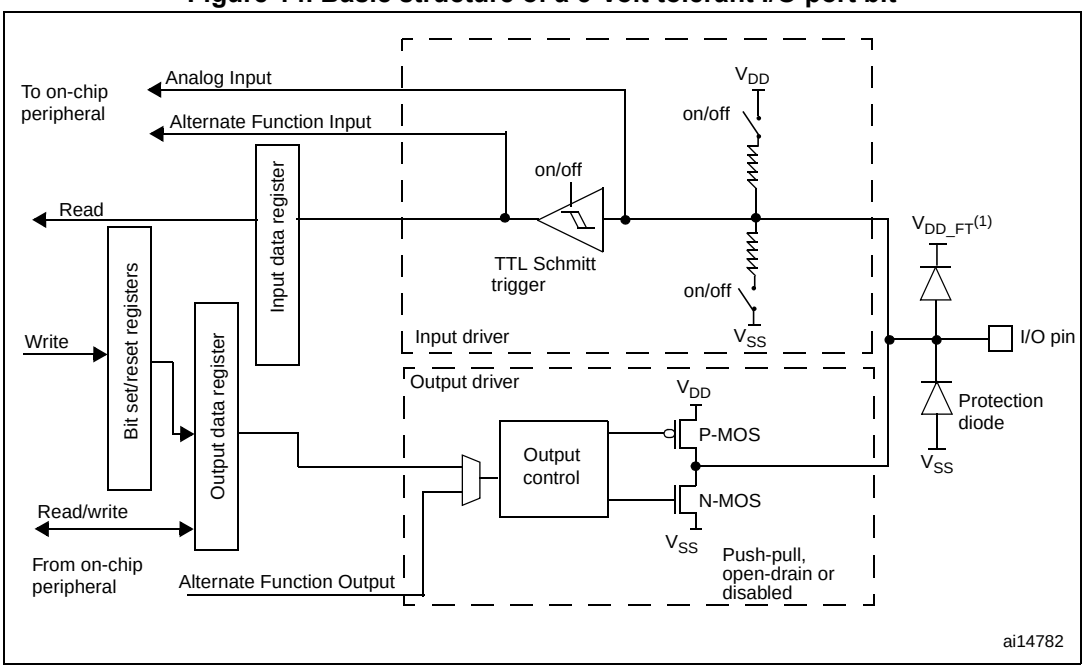


Figure 14. Basic structure of a 5-Volt tolerant I/O port bit



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

Kolonna "I/O-Level" i tabellane s.26-31, viser om ein pinne er laga for å tola å bli tilkobla ei spenning på opptil 5V, dvs. er 5V-tolerant (FT) eller ikkje. F.eks. ser ein på s.30 at pinne PB5 ikkje er FT, mens PB6 er FT.

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
		IO FT(3) input low level voltage	-	-	0.32*(V_{DD}-2V)+0.75 V(1)	
		All I/Os except BOOT0	-	-	0.35V_{DD}(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	0.41*(V_{DD}-2 V)+1.3 V(1)	-	-	
		IO FT(3) input high level voltage	0.42*(V_{DD}-2 V)+1 V(1)	-	-	
		All I/Os except BOOT0	0.65V_{DD}(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed based on test during characterization.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.

Frå s.62/117 i DocID13587 Rev 17 (databladet)

Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2), I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed based on test during characterization.

Frå s.65/117 i DocID13587 Rev 17 (databladet)