**VLSI Laboratory Report - Lab 4**

**Course:** ENCE 3501 - VLSI Design
**Date:** October 16, 2025
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## 1. Objective

The purpose of this lab is to design, simulate, and analyze two CMOS inverters with different transistor dimensions using Electric VLSI and SPICE. The first inverter uses transistor sizes of **PMOS 12µm / 6µm** and **NMOS 6µm / 6µm**, while the second inverter uses **PMOS 48µm / 6µm** and **NMOS 24µm / 6µm** with a multiplier of **M = 4**. The experiment includes schematic design, layout implementation, and simulation under varying capacitive loads to examine switching behavior and propagation delays.

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## 2. Schematic Design

Both inverters were designed using standard CMOS topology. The PMOS and NMOS transistors are connected in a complementary configuration, where the PMOS source is tied to VDD and the NMOS source to GND, with their drains connected to the common output node.

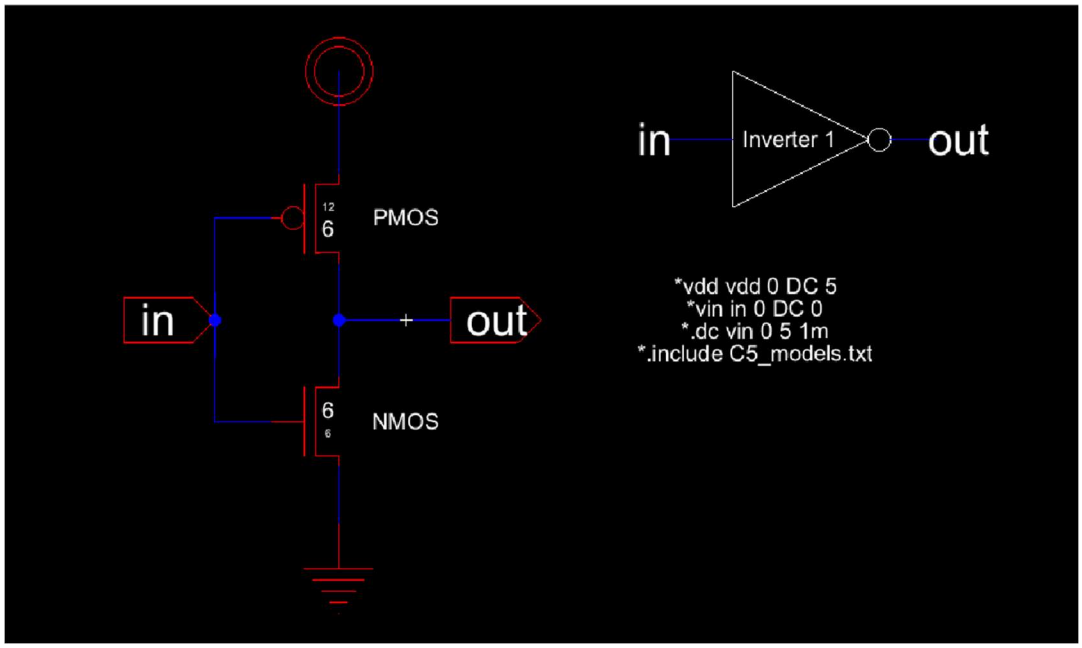


*Figure 1. Schematic of First Inverter (12/6 µm PMOS, 6/6 µm NMOS)*

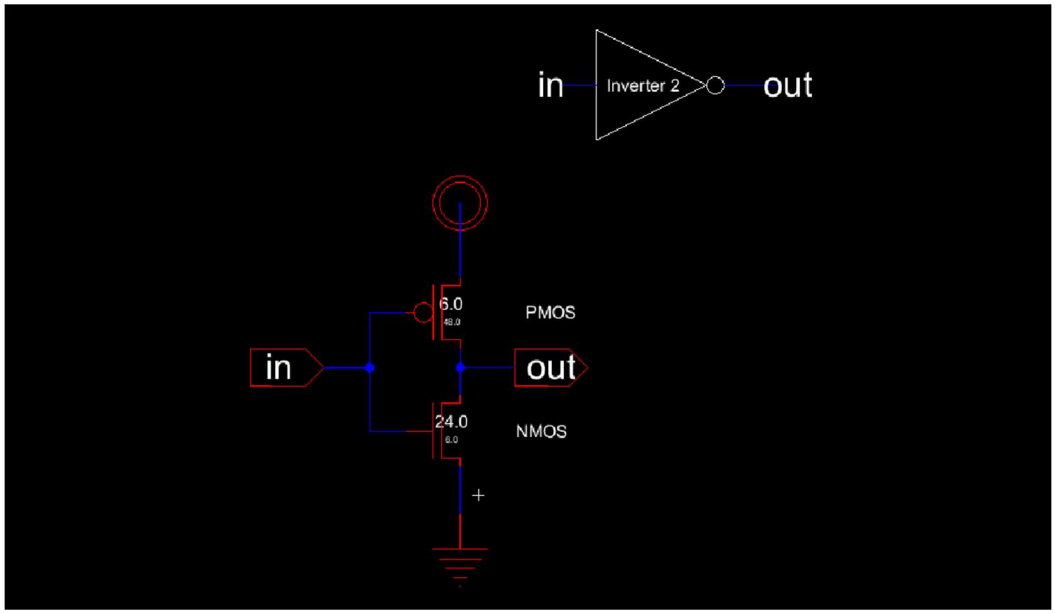


*Figure 2. Schematic of Second Inverter (48/6 µm PMOS, 24/6 µm NMOS)*

The SPICE code snippet for simulation is shown below:

```
*vdd vdd 0 DC 5
*vin in 0 DC 0
*.dc vin 0 5 1m
.include C5_models.txt
```

This code biases the inverter with a 5V supply and performs a DC sweep of the input voltage from 0V to 5V to capture the voltage transfer characteristic (VTC).

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## 3. Layout Design

Each inverter layout was drawn to meet MOSIS design rules. The **VDD rail** runs along the **top** using Metal1, and the **GND rail** runs along the **bottom**, also in Metal1. The input and output are routed using Poly and Metal1 interconnects.

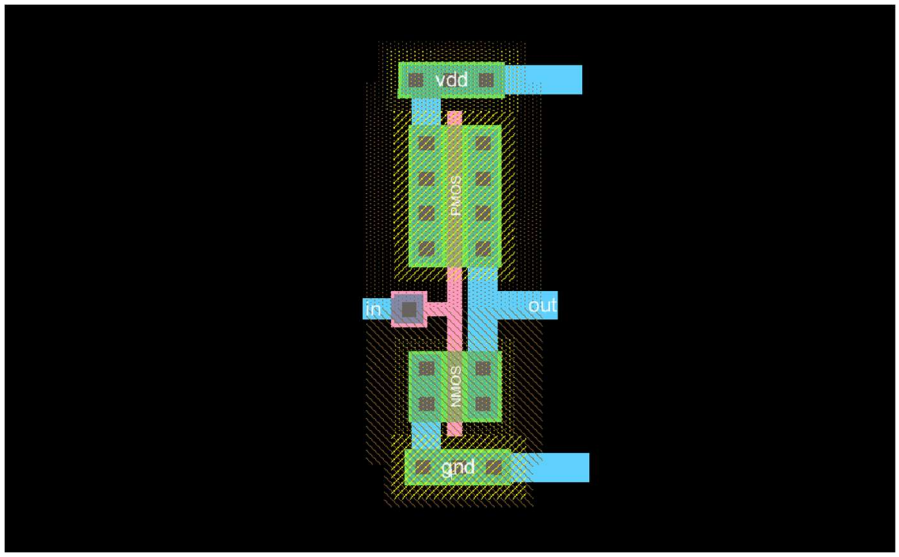


*Figure 3. Layout of Inverter 1 (12/6 and 6/6)*

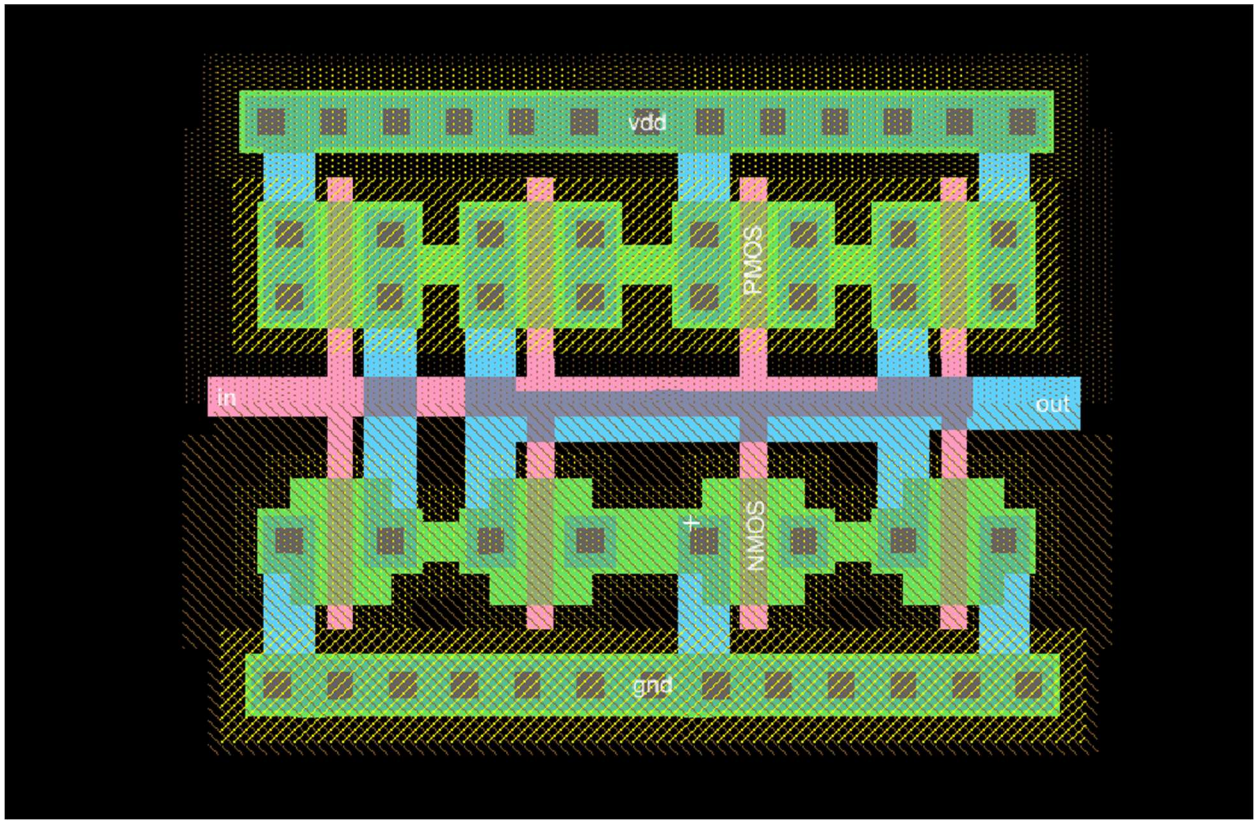


*Figure 4. Layout of Inverter 2 (48/6 and 24/6)*

All design rules were verified (DRC check passed), and node connections were confirmed through **LVS** comparison to match the schematic netlist.

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## 4. Simulation Results

### *A. DC Simulation (VTC Analysis)*

The voltage transfer characteristics were obtained for both inverters, as shown below.

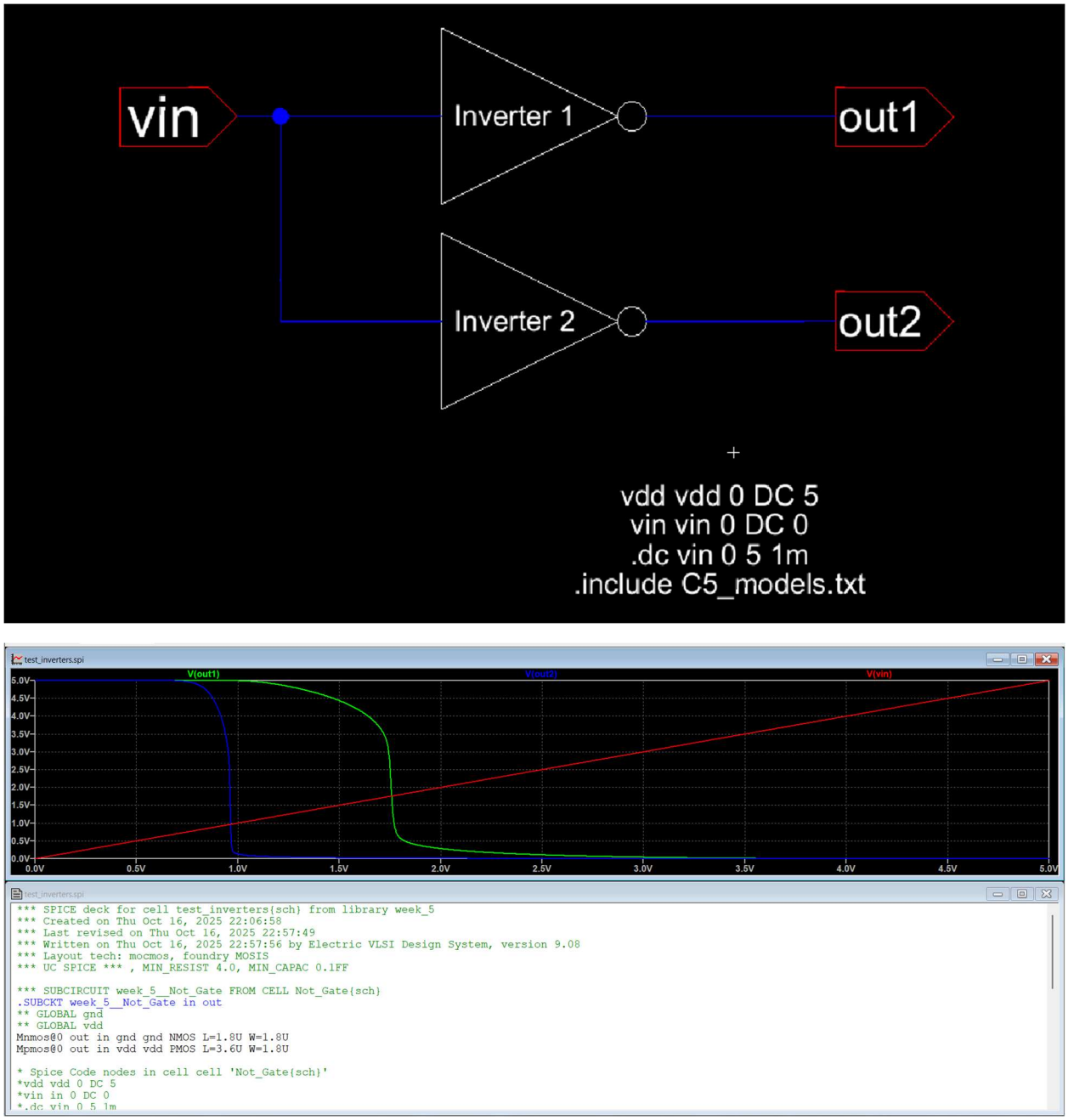


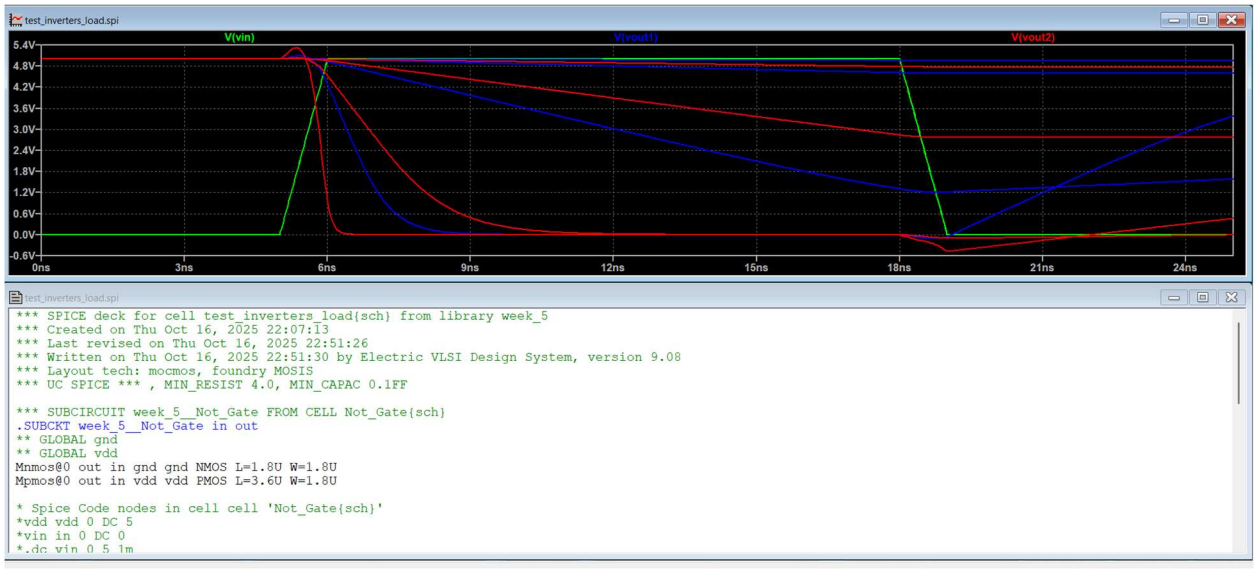

***Figure 5. DC Transfer Characteristic (VTC)***

The switching threshold (V_M) occurs near **VDD/2 ≈ 2.5V**, confirming symmetrical operation and correct transistor sizing. The wider PMOS ensures balanced rise and fall times.

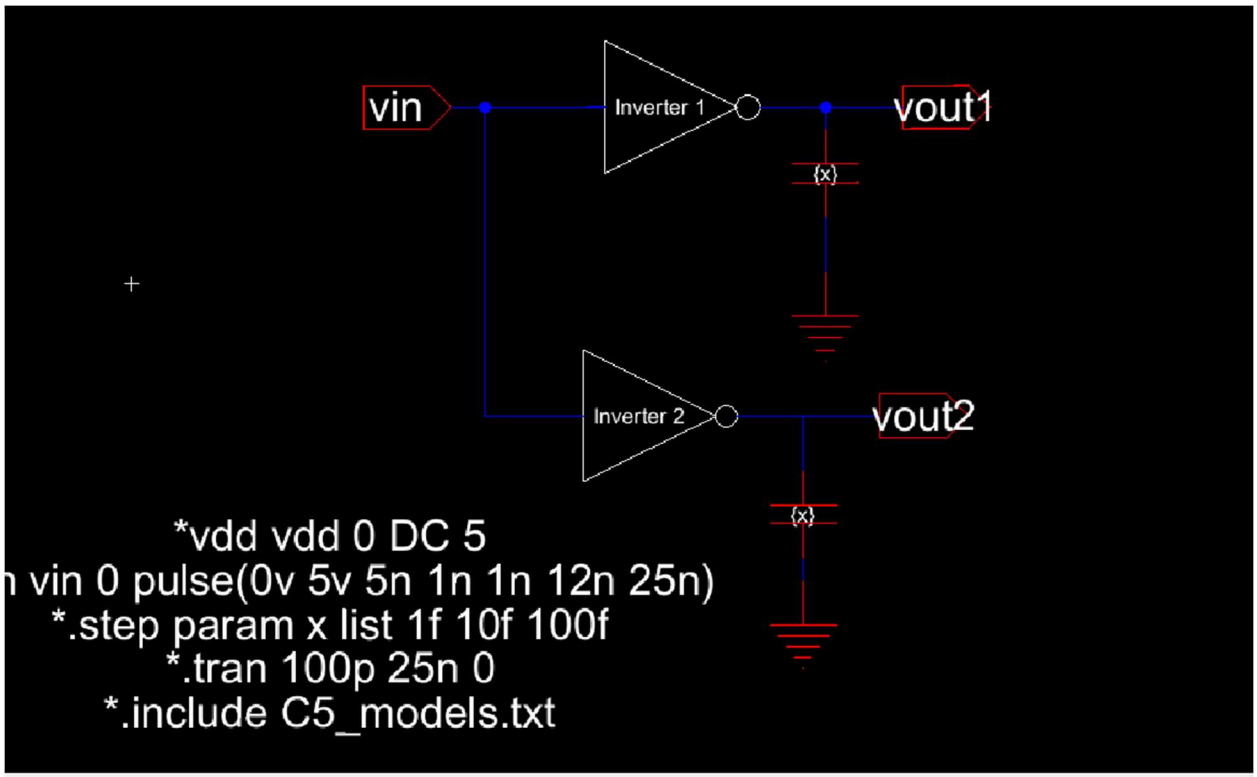
### *B. Transient Analysis with Capacitive Load*

Transient simulations were run by applying a pulse waveform to the inverter input, while varying the capacitive load at the output (1fF, 10fF, 100fF). The pulse was defined as:

```
Vin vin pulse(0v 5v 5n 1n 1n 12n 25n)
```




```
Vin vin 0 pulse(0V 5V 5ns 1ns 1ns 12ns 25ns)
```



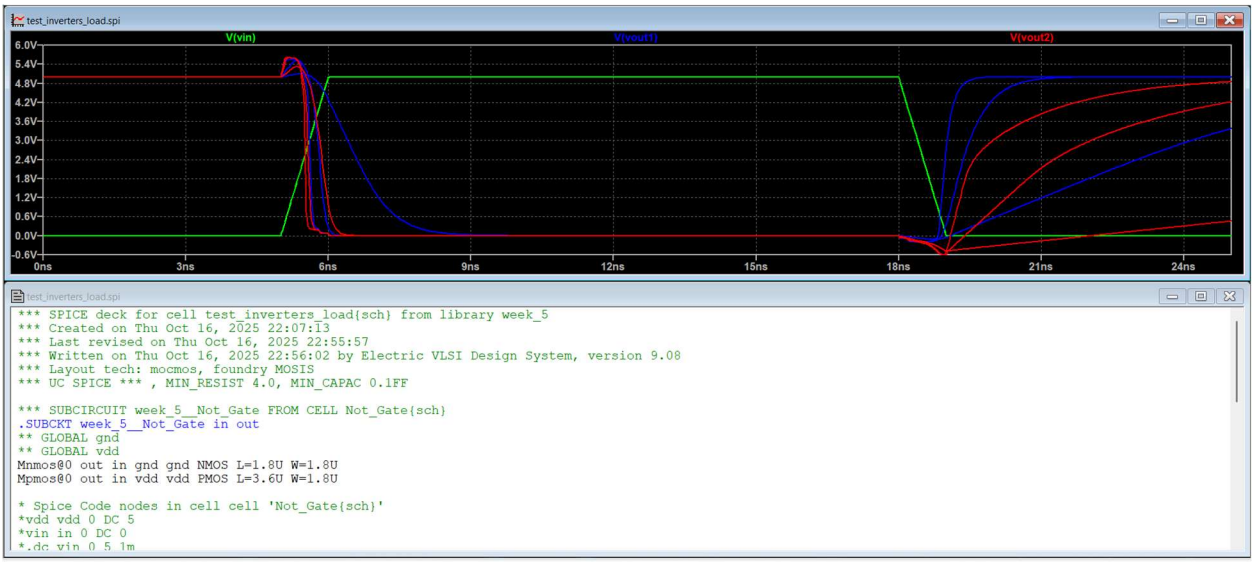



***Figure 6. Transient Response with Load Variation***

Transient Response 1 Transient Response 2 Transient Response 3

As seen from the waveforms: - Smaller capacitive loads (1fF, 10fF) result in faster output transitions (shorter rise and fall times). - Larger loads (100fF, 1pF) cause longer propagation delays and slower transitions. - The stronger (larger W/L) inverter can drive larger capacitive loads with less delay, confirming correct scaling.

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## 5. Results and Discussion

1. **Switching Point:** Both inverters exhibit a switching voltage near 2.5V. The inverter with larger transistor widths (48/6 and 24/6) demonstrates faster response due to higher drive strength.
2. **Load Dependence:** As the capacitive load increases, the rise and fall times increase proportionally, indicating slower charging/discharging through the transistor channels.
3. **Symmetry:** The PMOS width is approximately twice that of the NMOS, which helps equalize the rise and fall delays, optimizing the switching threshold.
4. **Design Decisions:** The choice of W/L ratios ensures adequate current drive capability for each stage. Metal1 was used for VDD and GND routing to minimize resistance and ensure good current distribution.

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## 6. Conclusion

This lab successfully demonstrated the design, layout, and simulation of CMOS inverters with varying transistor sizes. The simulation results confirm the theoretical expectations of inverter switching behavior and capacitive loading effects. The larger transistor inverter

exhibited improved performance for driving higher capacitive loads, while maintaining proper voltage transfer characteristics.

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## 7. References


- MOSIS Design Rules for CMOS Process
- Electric VLSI System User Manual (v9.08)
- C5 Model SPICE Parameters