ENCE 3501 – Lab 3: Padframe with ESD Protection and NMOS Integration

Date: October 10, 2025

Name: Ali Alalwia

1. Objective

The objective of this laboratory was to design and implement a die layout that connects an NMOS transistor to the outside world through a padframe that includes basic electrostatic-discharge (ESD) protection. The assignment involved creating and verifying both schematic and layout representations for individual diodes, the ESD-protected pad cell, and the final padframe integrating the NMOS transistor.

2. Introduction

In integrated-circuit (IC) design, the padframe provides the electrical interface between on-chip circuitry and external packaging or test probes. Each pad must protect internal devices from potentially destructive ESD events. To achieve this, ESD diodes are connected between the pad node and the power rails (VDD and GND).

The protection network typically uses complementary diodes:
- pWell–nActive diode clamps negative ESD pulses by conducting current to ground.
- pActive–nWell diode clamps positive ESD pulses by conducting current to VDD.

This lab demonstrates the design and layout of these ESD elements, their combination into a pad cell, and the integration of a padframe around an NMOS transistor.

3. Methodology

This section presents the schematics and layouts for each component, illustrating the ESD protection and padframe integration process.

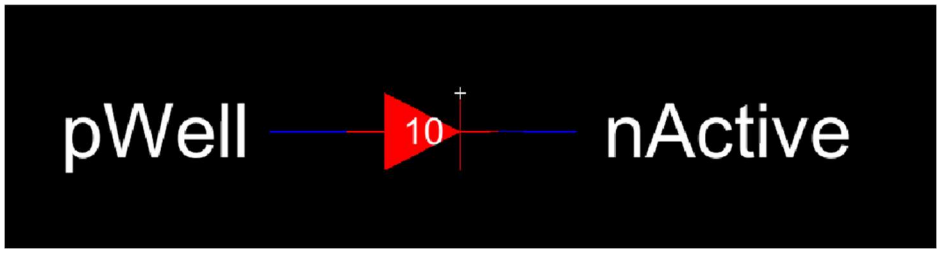

Figure 1. Schematic of pWell–nActive diode.

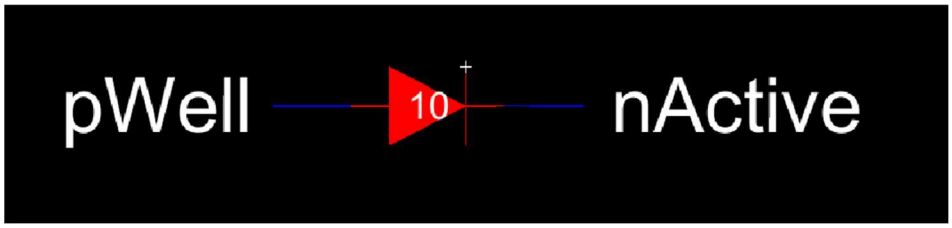

Figure 2. Schematic of pActive–nWell diode.

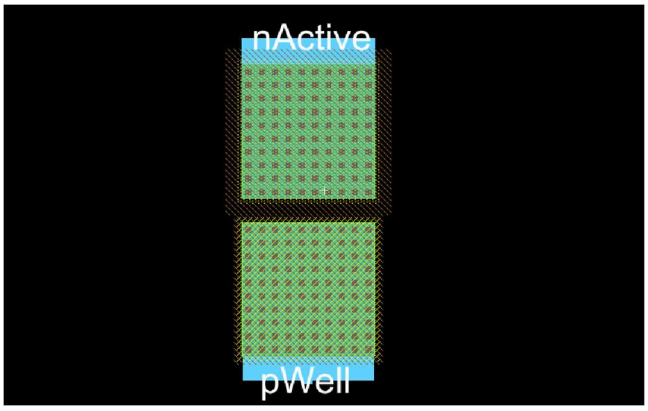

Figure 3. Layout of pWell–nActive diode.

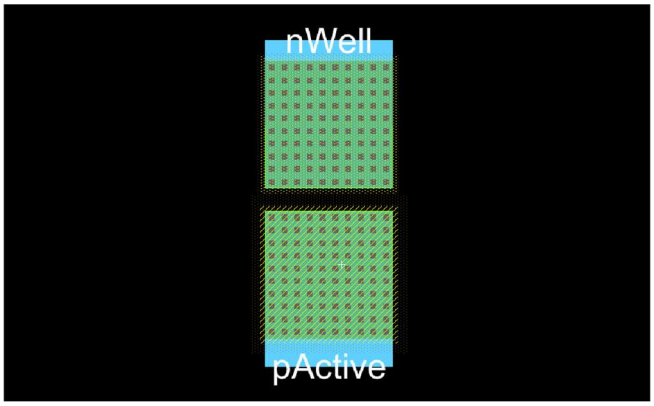

Figure 4. Layout of pActive–nWell diode.

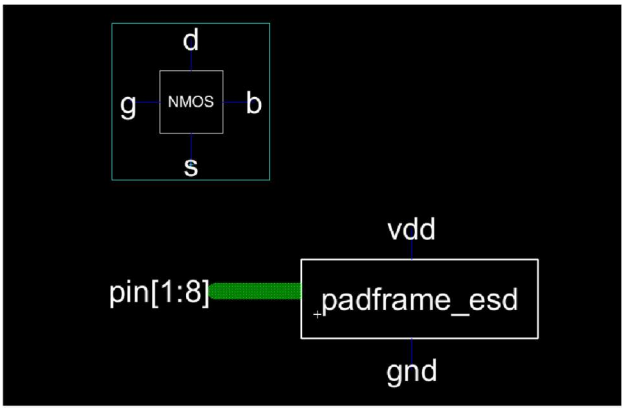

Figure 5. Schematic of pad cell with ESD protection.

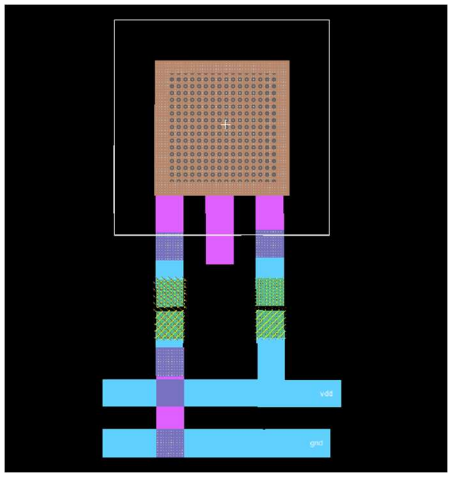

Figure 6. Layout of pad cell with ESD protection.

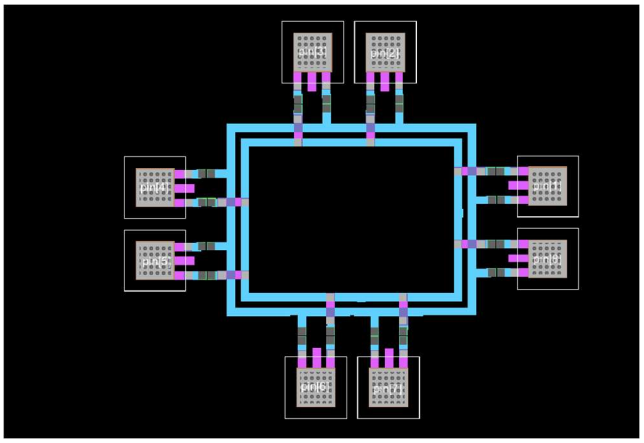

Figure 7. Layout of padframe with connected VDD and GND buses.

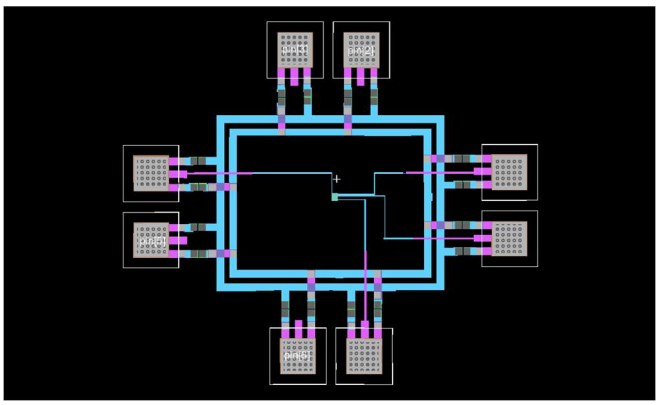

Figure 8. Layout of padframe including the NMOS device.

4. Results

The complete design successfully integrates complementary ESD diodes, a functional pad cell, and a padframe providing external connectivity to an NMOS transistor. DRC and LVS checks were satisfied, confirming layout-to-schematic matching.

5. Discussion

The pWell–nActive and pActive–nWell diodes act as clamping elements, ensuring protection from both positive and negative ESD pulses. The padframe layout was designed with symmetry and minimal parasitic effects. Routing and metal layering minimized resistance and ensured robust power distribution.

6. Conclusion

This lab demonstrated the design and implementation of an ESD-protected padframe integrating an NMOS transistor. The process reinforced CMOS layout design principles, emphasizing ESD safety and padframe organization.