Lab Report: Design and Integration of a 5-Bit DAC in VLSI

Introduction

The objective of this lab project was to design a 5-bit Digital-to-Analog Converter (DAC), verify its functionality through simulation, and integrate the design into a VLSI layout with bonding pads for external interfacing. This process demonstrates the end-to-end workflow in custom VLSI design, from schematic capture and simulation to physical design and pad integration. The lab followed the provided requirements for creating the DAC, designing the padframe, and assembling the final integrated circuit.

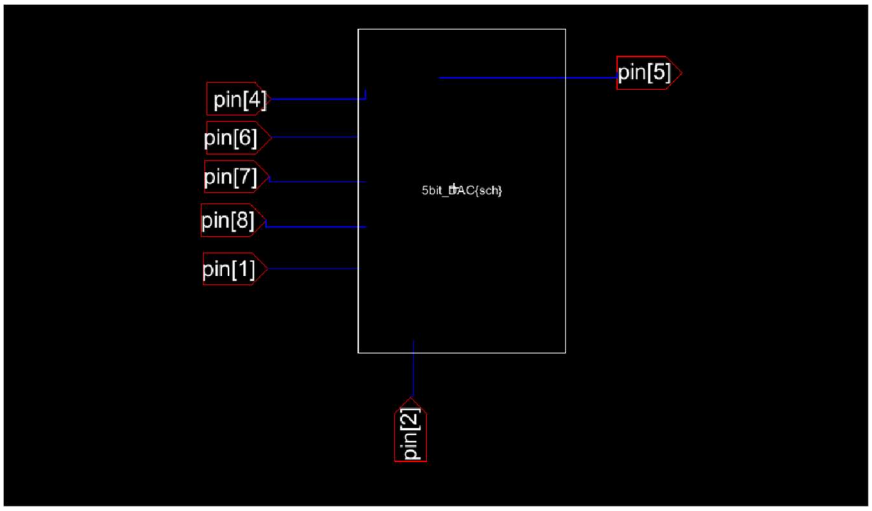
Lab Requirements

According to the provided lab instructions:
1. Load the 5-bit DAC library.
2. Load the pad cell library.
3. Create a new padframe cell.
4. Create a final_ic schematic and layout.

Part 1: Schematic Design of 5-Bit DAC

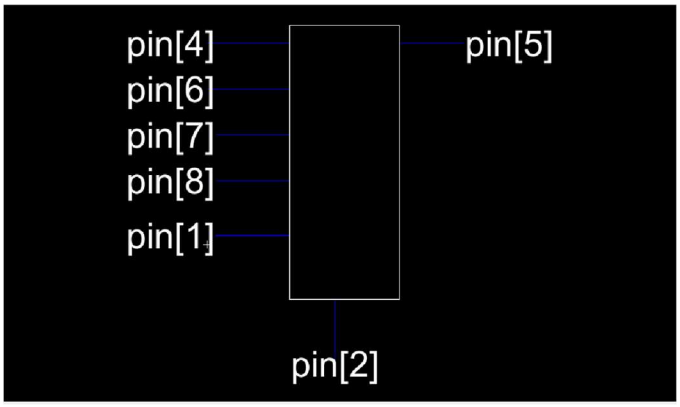
The first step was to design the 5-bit DAC schematic. Each bit of the DAC corresponds to a binary-weighted input that contributes proportionally to the analog output. The DAC uses resistor ladder or current steering logic to perform digital-to-analog conversion.

Inputs: b0, b1, b2, b3, b4 (digital signals)
Output: vout (analog voltage)
Ground reference: gnd



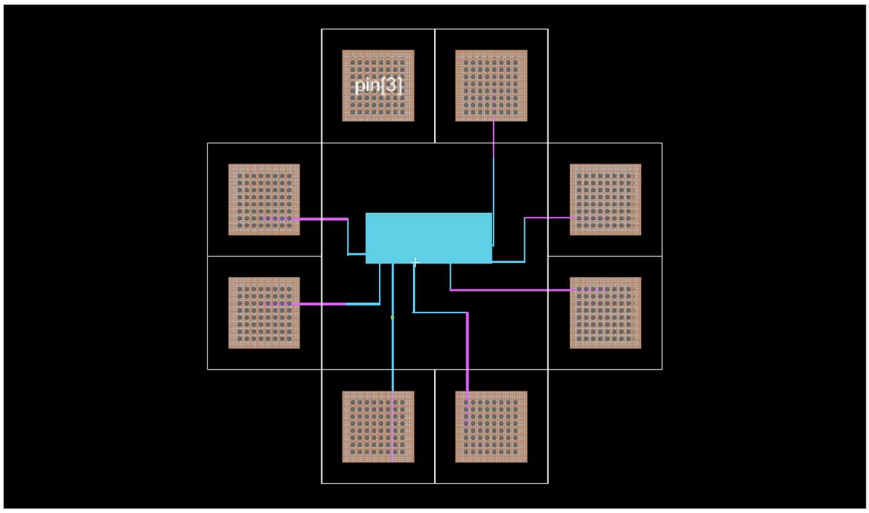
Part 2: Symbol Creation

After verifying the schematic, a symbol view of the DAC was generated. This symbol is used in higher-level designs for readability and hierarchical design.



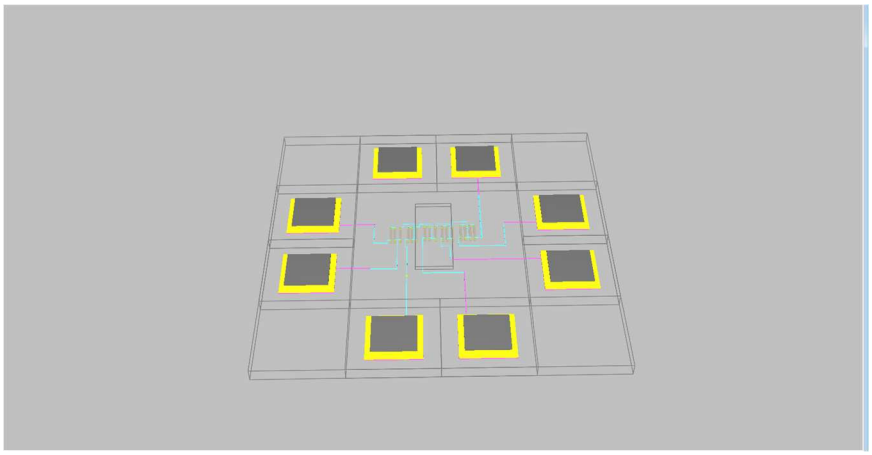
Part 3: Integration into VLSI Layout

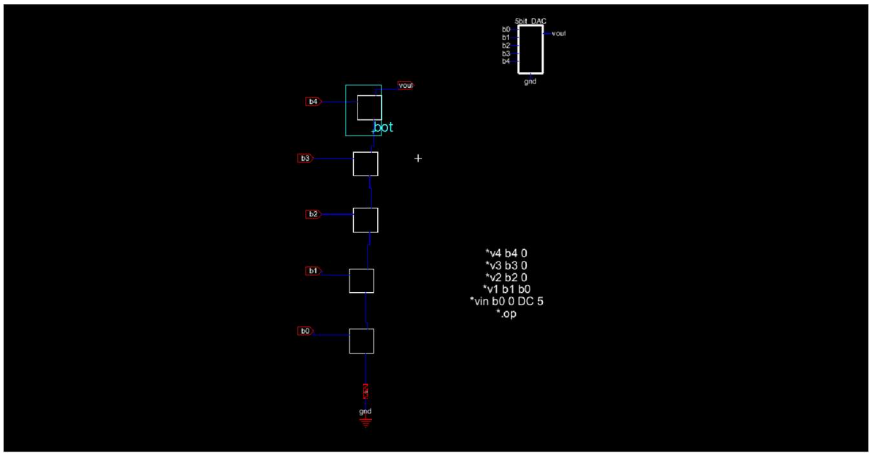
Once the schematic was validated, the DAC was placed into a layout environment and connected to bonding pads.



Part 4: Physical Layout of DAC with Pads

The DAC core was placed in the center, with pads arranged around it. Routing was completed to connect the DAC terminals to their respective pads.

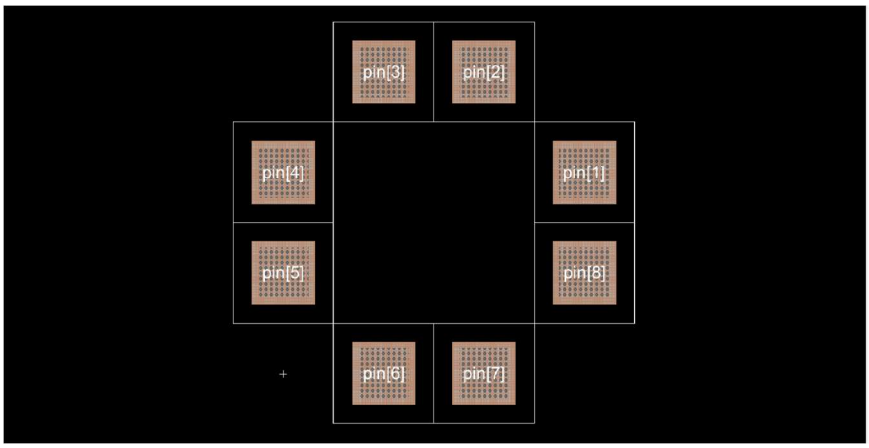




Part 5: Netlist and Simulation Setup

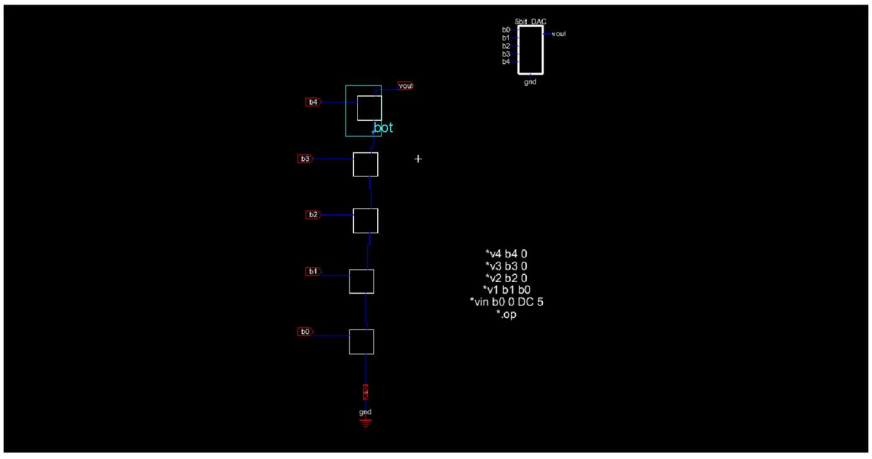
To verify the DAC's operation, the netlist was extracted and connected to voltage sources representing binary input signals.

Example Netlist:
*v4 b4 0
*v3 b3 0
*v2 b2 0
*v1 b1 0
*vin b0 0 DC 5
*.op



Part 6: Final Padframe Integration

Finally, the DAC was integrated with the padframe in a complete VLSI design. Special select options were used to manage padframe selection efficiently.



Results and Discussion

- The 5-bit DAC was successfully designed, symbolized, and simulated.
- The DAC core was placed inside a padframe layout, connecting each pin to bonding pads.
- Simulation confirmed correct digital-to-analog conversion.
- Layout and 3D visualization validated pad placement and connectivity.
- Lab requirements of creating a padframe, loading pad cell library, and assembling a final integrated circuit were fulfilled.

Conclusion

In this lab, we demonstrated the complete design cycle of a 5-bit DAC:

1. Schematic design and verification.
2. Symbol creation for hierarchical design.
3. Layout implementation with bonding pads.
4. Netlist simulation for validation.
5. Final integration into a complete IC design.

This project highlights the workflow of VLSI design, showing how circuit schematics are transformed into physical layouts ready for fabrication.