Lab Report – 5bit DAC

Course: VLSI
Instructor: Dr. Martins
Student: Ali Alalwia
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Abstract

This experiment investigates the design and simulation of digital-to-analog converters (DACs) using resistive networks. The work begins with the analysis of a basic resistor voltage divider, which is then extended into a 5-bit ladder DAC. Circuit schematics, layouts, and LTspice simulations were performed to evaluate performance. Results show that the voltage divider divides an input of 1 V into ~0.333 V output, and the 5-bit DAC provides correct binary-weighted outputs consistent with theory.

Introduction

A voltage divider is the simplest resistive circuit that scales down an input voltage by a fixed ratio. It forms the foundation of more complex circuits such as the R-2R ladder, which is a widely used architecture for digital-to-analog conversion due to its simplicity and scalability.

In the DAC, only two resistor values (R and 2R) are required regardless of bit resolution, ensuring uniformity and accuracy. The DAC converts binary digital signals into analog voltages by summing weighted contributions of each bit. Such DACs are used in microcontrollers, signal processing, and communication systems.

Materials and Methods

Software Tools:
- Electric VLSI for schematic/layout design
- LTspice for circuit simulation

Components:
- Resistors: 10 kΩ (used for both R and 2R equivalents)

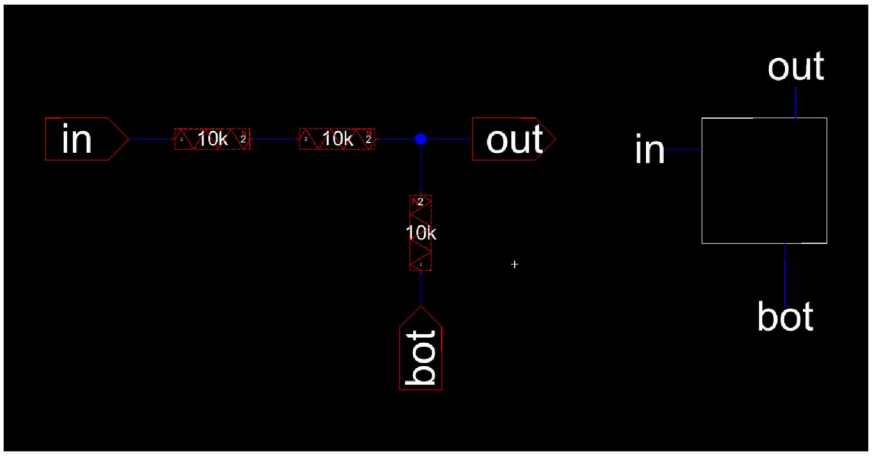
Procedure:
1. Designed a voltage divider circuit in Electric VLSI.
2. Exported netlist and simulated in LTspice to confirm voltage scaling.
3. Designed a 5-bit DAC using cascaded resistor ladders.
4. Implemented both schematic and layout, including 3D layout verification.
5. Ran DC operating point and transient simulations in LTspice.

Results

Voltage Divider

Input voltage: Vin = 1 V
Simulation output:
- Midpoint node: ~0.667 V
- Vout: ~0.333 V
- Current through resistors: ~33 µA

Voltage Divider Schematic:



Voltage Divider Layout:

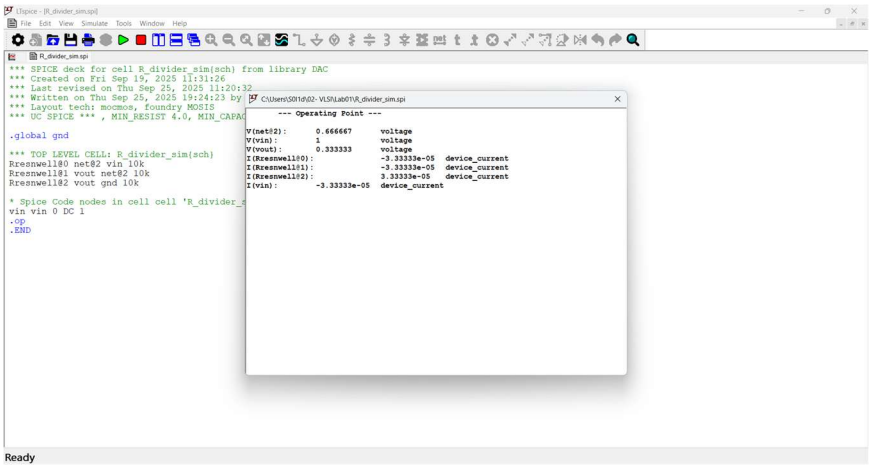
Resistance is determined by the material's **sheet resistance** RsR_sRs (Ω/square):

$$R = R_s \cdot \frac{L}{W}$$

To get exactly **R** and **2R**, the ratio L/W is adjusted. For example:

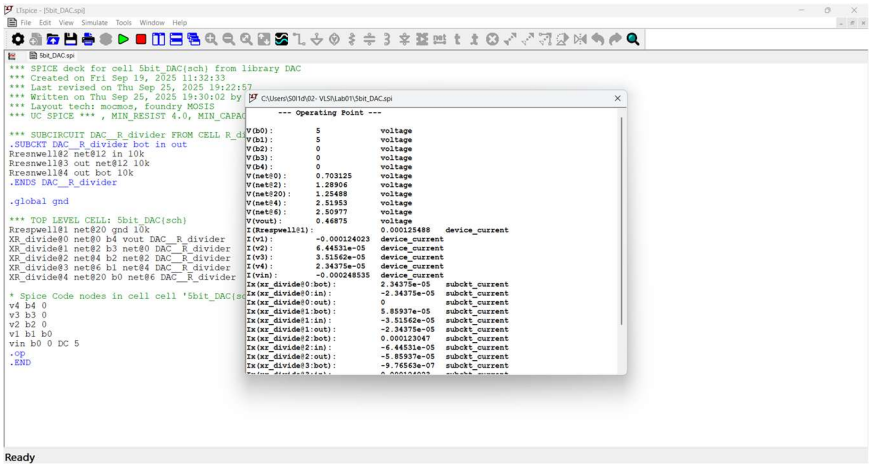
$$R = R_s \cdot \frac{L}{W}$$
$$2R = R_s \cdot \frac{2L}{W} \text{ (or same length, half width).}$$

LTspice Simulation Result:



5-bit DAC

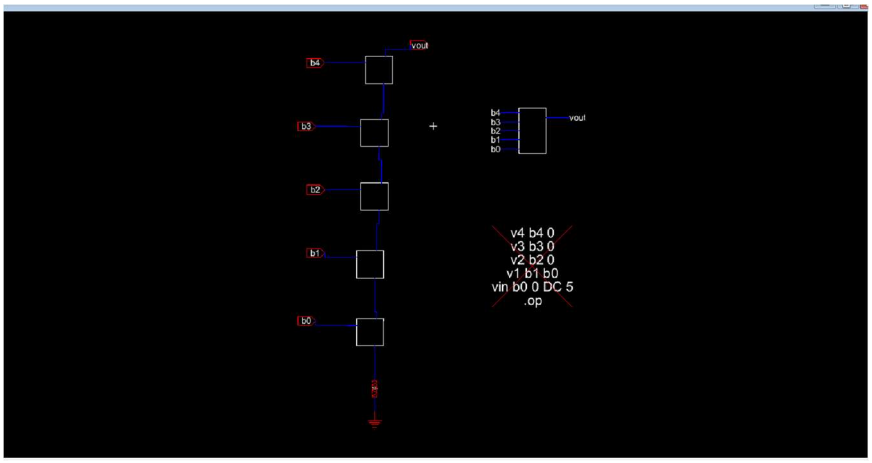
Binary inputs (b4…b0) connected to reference voltages.
LTspice simulations confirmed binary-weighted outputs.



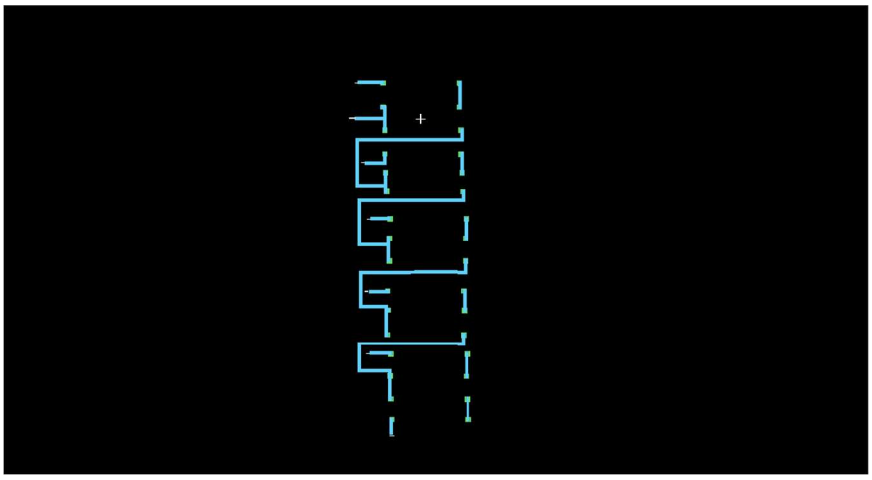
Sample LTspice results (Operating Point):
- b4=1, b3=0, b2=0, b1=0, b0=0 → Vout ≈ 0.703 V
- b4=1, b3=1, b2=0, b1=0, b0=0 → Vout ≈ 1.289 V
- b4=1, b3=1, b2=1, b1=0, b0=0 → Vout ≈ 2.519 V
- Full-scale (11111) → Vout ≈ 4.688 V

Transient Simulation:
- Vout increases smoothly as binary code increments.
- Maximum observed Vout ≈ 4.88 V (close to ideal 5 V).

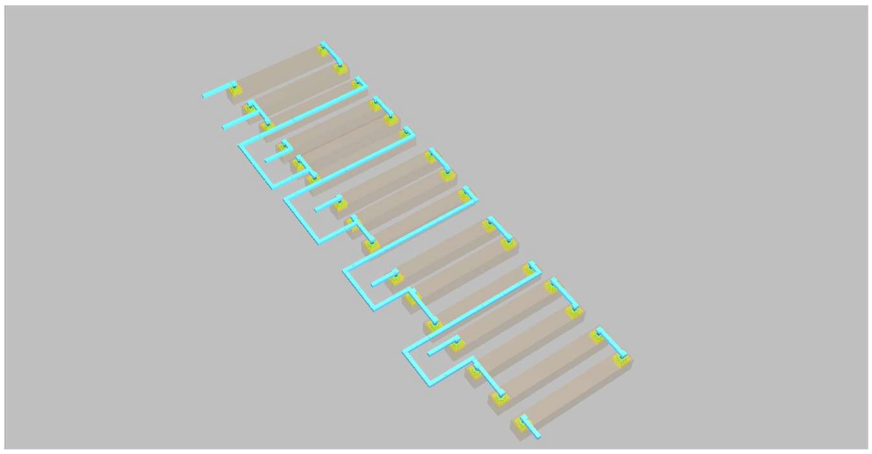
5-bit DAC Schematic:



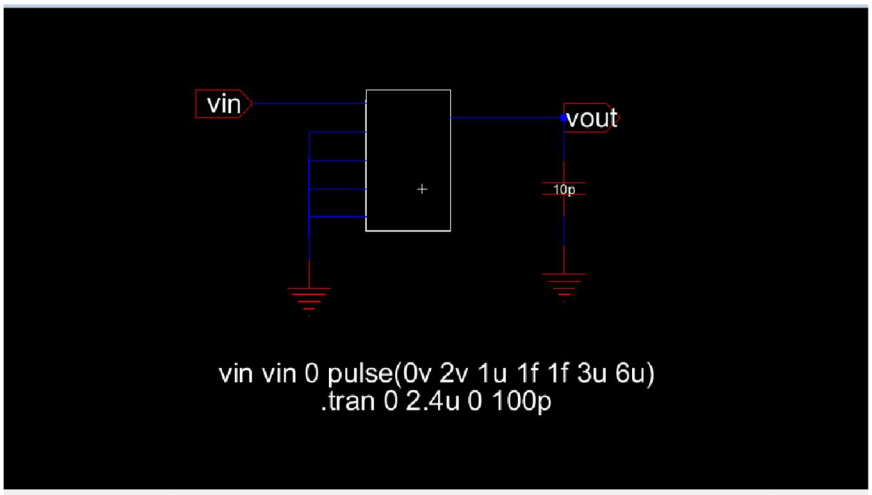
5-bit DAC Layout:



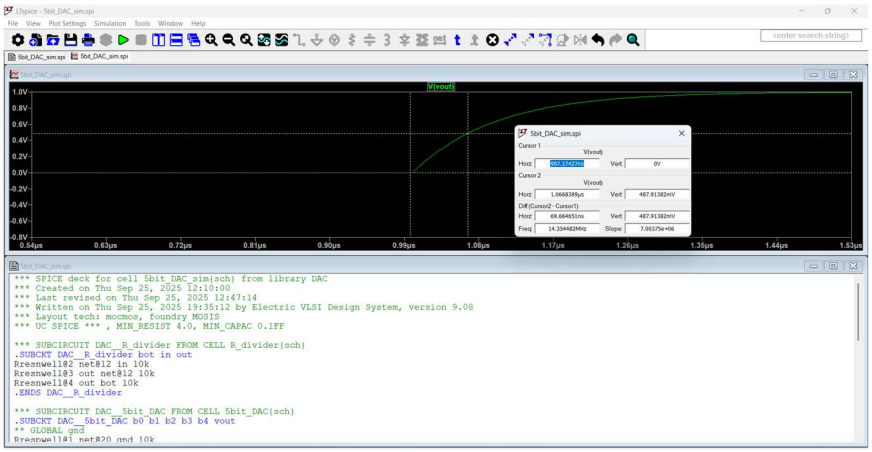
5-bit DAC 3D Layout:



LTspice Simulation - Transient Response:



LTspice Simulation - Final Result:



Discussion

The voltage divider results matched the expected theoretical values, validating the simulation setup. The 5-bit DAC produced correct binary-weighted outputs, confirming the accuracy of the R-2R ladder design. Small deviations (~10–20 mV) from ideal values can be attributed to simulation tolerances, resistor matching, and rounding errors in LTspice.

The R-2R DAC is efficient since it requires only two resistor values, making layout compact and scalable. However, real-world implementation depends heavily on resistor tolerance, which affects linearity and accuracy.

Conclusion

The lab successfully demonstrated the design and simulation of both a voltage divider and a 5-bit R-2R ladder DAC. The results confirm theoretical predictions, with accurate division and binary-weighted DAC outputs. This validates the use of the R-2R structure for efficient and scalable DAC design.

References

- Lab 1: R-2R Resistor Ladder DAC
- LTspice User Manual
- Electric VLSI Documentation