VLSI Design Laboratory Report

CMOS Logic Design and Full Adder Implementation

Course: EE421L – VLSI Design
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Software: Electric VLSI, LTSpice

1. Objective

The objective of this laboratory is to design, simulate, and verify CMOS logic circuits including NOT, NAND, and XOR gates, and integrate them into a complete full adder. Each circuit was implemented at the transistor level using 6 µm/2 µm CMOS technology in Electric VLSI, with functional verification performed using SPICE simulations. Layouts were constructed to comply with standard-cell design conventions, and DRC/NCC checks were used to validate correctness and manufacturability.

2. Background Theory

Complementary Metal-Oxide-Semiconductor (CMOS) logic employs pairs of NMOS and PMOS transistors to achieve low static power consumption and high noise margins. In CMOS gates, NMOS transistors pull outputs low when active, while PMOS pull outputs high when inactive. This lab focuses on transistor-level logic design, metal routing, and hierarchical gate integration using Electric VLSI.

3. S-Frame

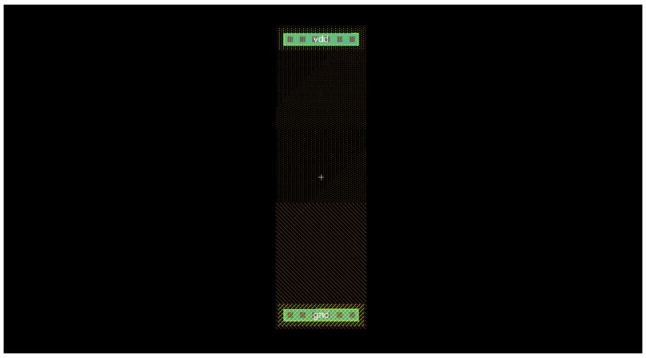

Figure 1. S-Frame Layout

To organize the layouts of the different components this design was used as a universal frame that contains vdd and gnd so all the gates can have a uniform size and make the design process easier

4. NOT Gate Design and Simulation

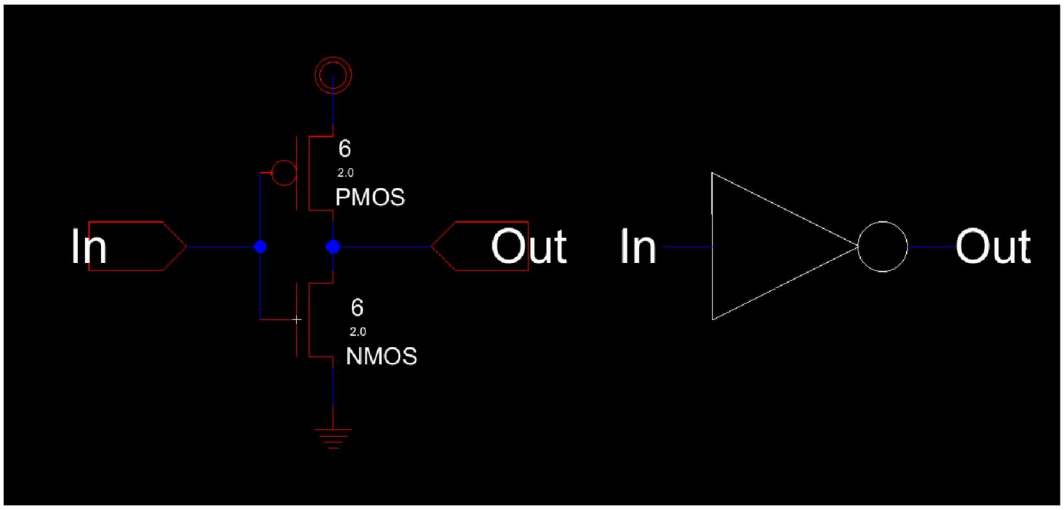

Figure 2. NOT Gate Schematic

The schematic shows one PMOS and one NMOS transistor sharing the same gate input. The output node connects at their drains, forming a complementary inverter. When the input is logic high, the NMOS conducts and the PMOS turns off, pulling the output low. When the input is low, the PMOS conducts and the NMOS turns off, pulling the output high.

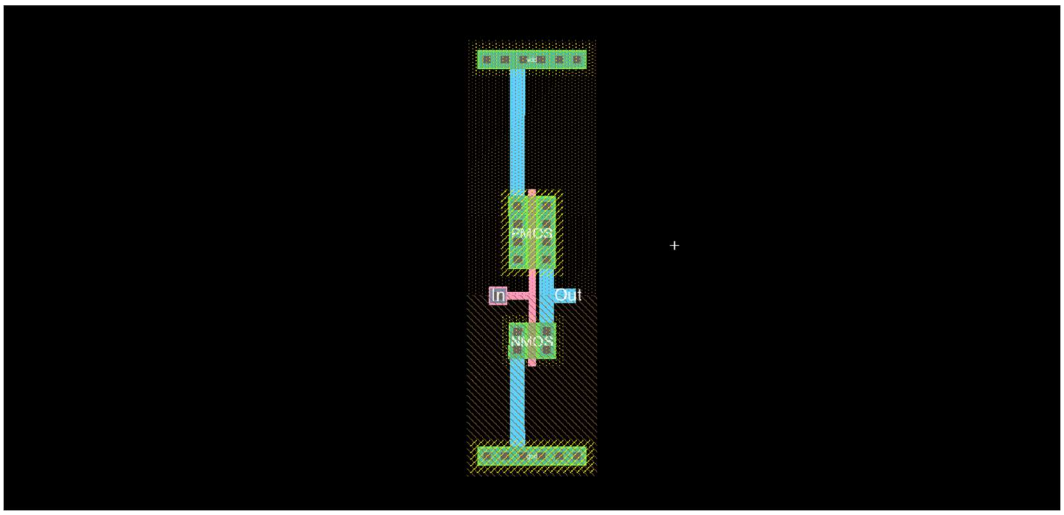

Figure 3. NOT Gate Layout

The inverter layout shows the PMOS transistor in the n-well and the NMOS in the p-substrate. The VDD and GND rails run horizontally using Metal1. The polysilicon gate line crosses both transistors to form the shared input. DRC confirmed rule compliance.

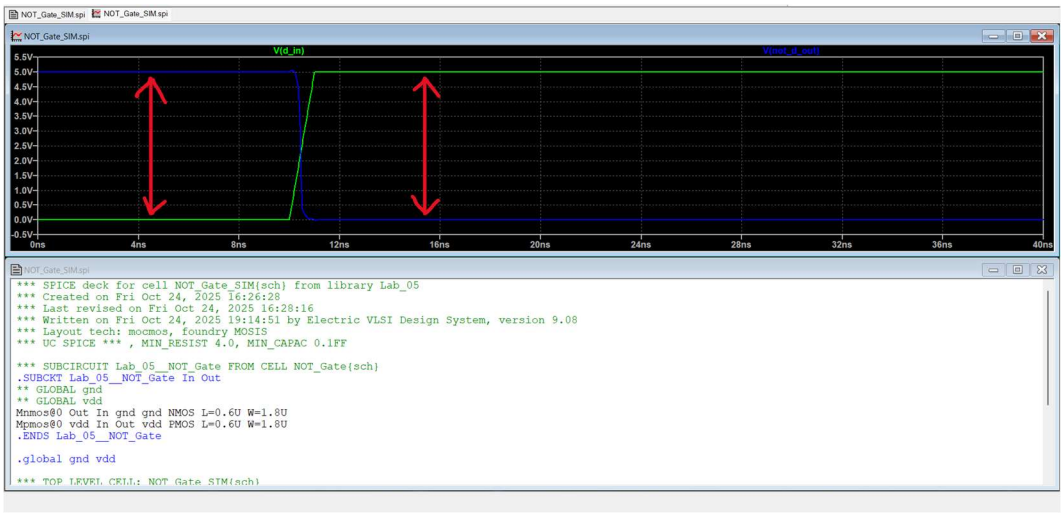

Figure 4. NOT Gate SPICE Netlist

The SPICE netlist defines the PMOS and NMOS transistors with W/L = 6µm/2µm and includes voltage sources for VDD and input pulses. Transient analysis verifies logic inversion across varying input frequencies.

From the Simulation it has been observed that when vd__in(input) is high = 5v

Vd_out (output) = 0 and when vd_in = 0 vd_out = 5 which confirms that the NOT gate is functioning as intended.

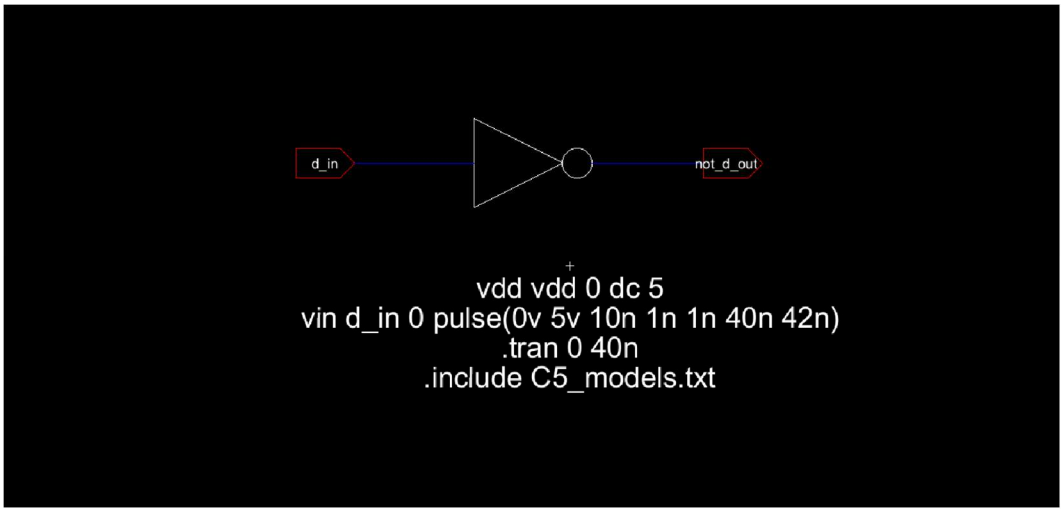

Figure 5. NOT Gate Simulation

The transient simulation shows correct inversion: the output goes high when the input goes low and vice versa. The propagation delay between transitions is minimal, confirming symmetrical switching.

4. NAND Gate Design and Simulation

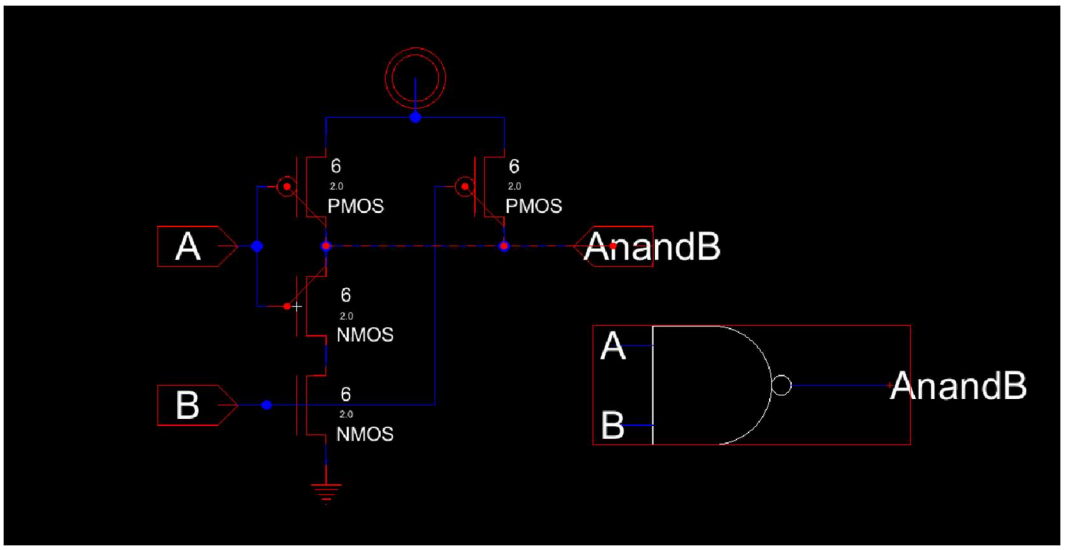

Figure 6. NAND Gate Schematic

The NAND gate schematic includes two PMOS transistors in parallel (pull-up network) and two NMOS transistors in series (pull-down network). The output logic follows Y = ¬(A·B).

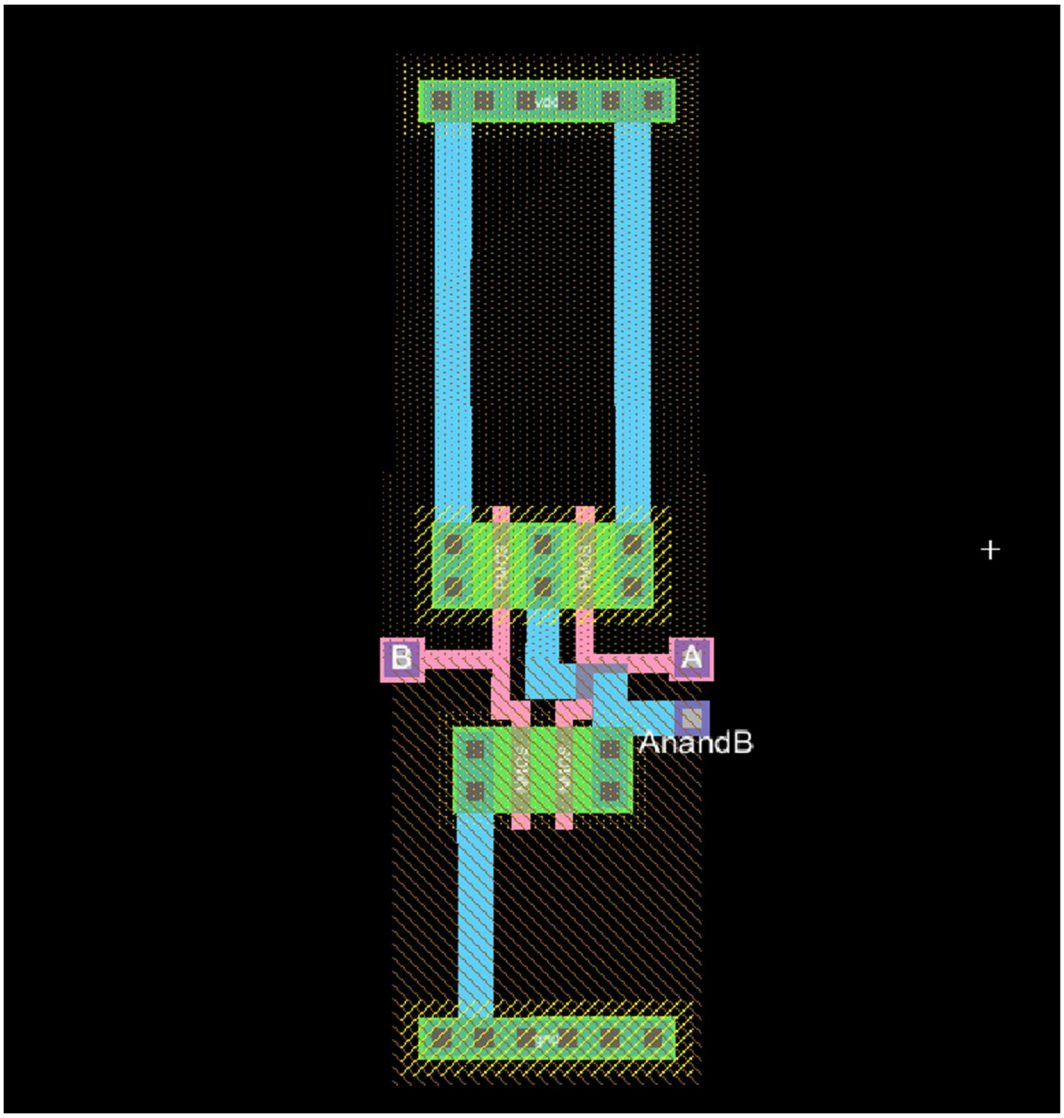

Figure 7. NAND Gate Layout

The layout shows PMOS transistors connected in parallel within the n-well and NMOS transistors connected in series in the p-substrate. Inputs A and B use polysilicon gates, and Metal1 is used for power routing.

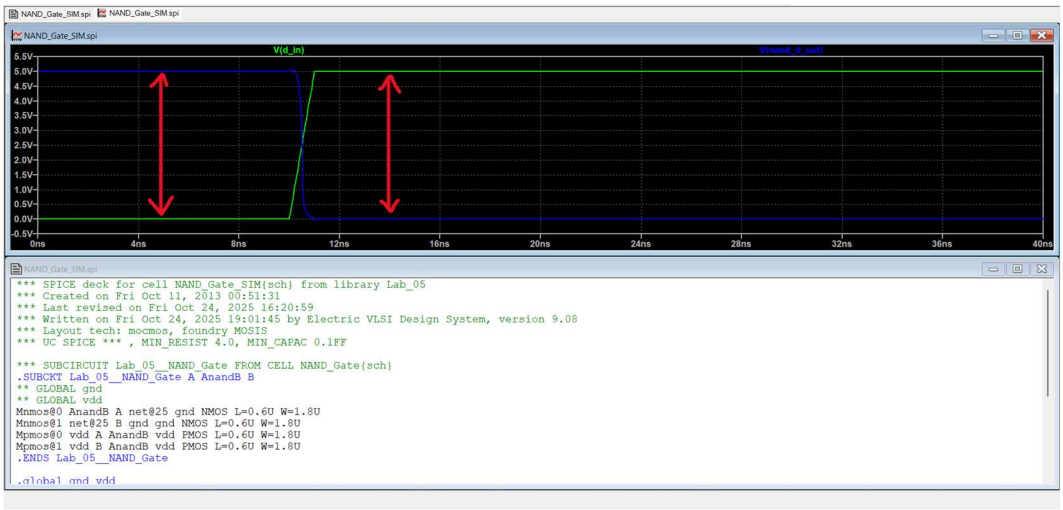

Figure 8. NAND SPICE Netlist 1

This netlist defines the NAND transistors and input signals. The simulation tests all four possible input states to validate correct logic operation.

From the spice simulation it was observed that when d_in is low nand with vdd (11)

The output nand_d_out is low but when d_in is low nand with vdd (01) nand_d_out

Becomes high which confirms that the gate is working properly as a nand gate

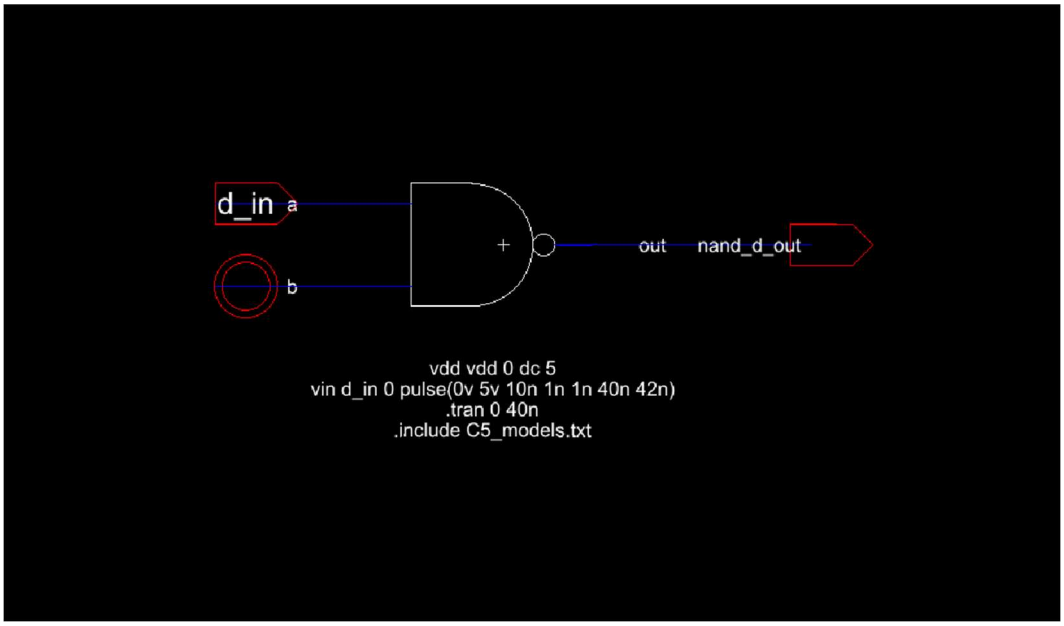

Figure 9. NAND Simulation 1

The waveform shows the NAND output remains high for all cases except when both inputs A and B are high. Propagation delay is under 1µs.

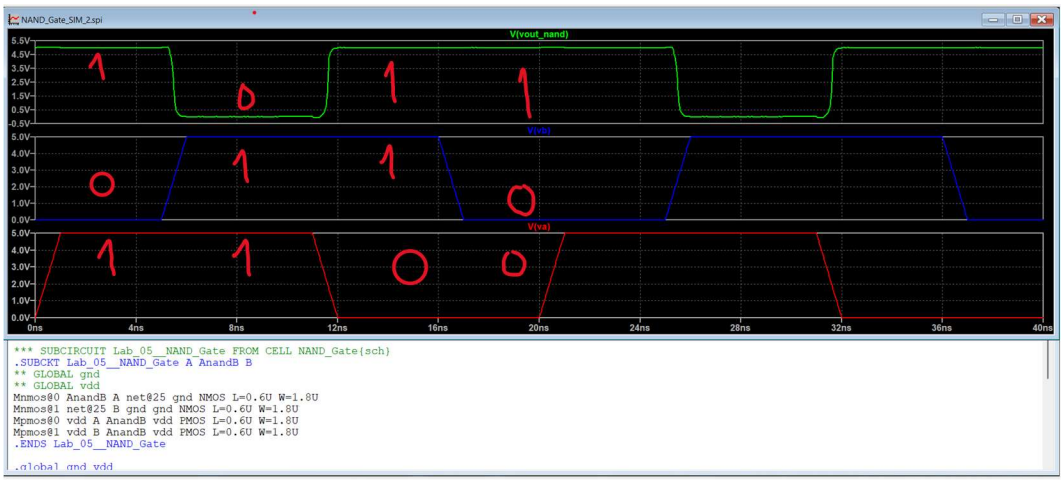

Figure 10. NAND SPICE Netlist 2

A modified SPICE configuration verifying consistent transistor connectivity.

It was observed that vout _nand becomes low only when both va and vb are high

(11) but if va and vb are both low(00) or low and high (01)or high and low(10) vout becomes high which confirms that the gate is functioning as a nand gate.

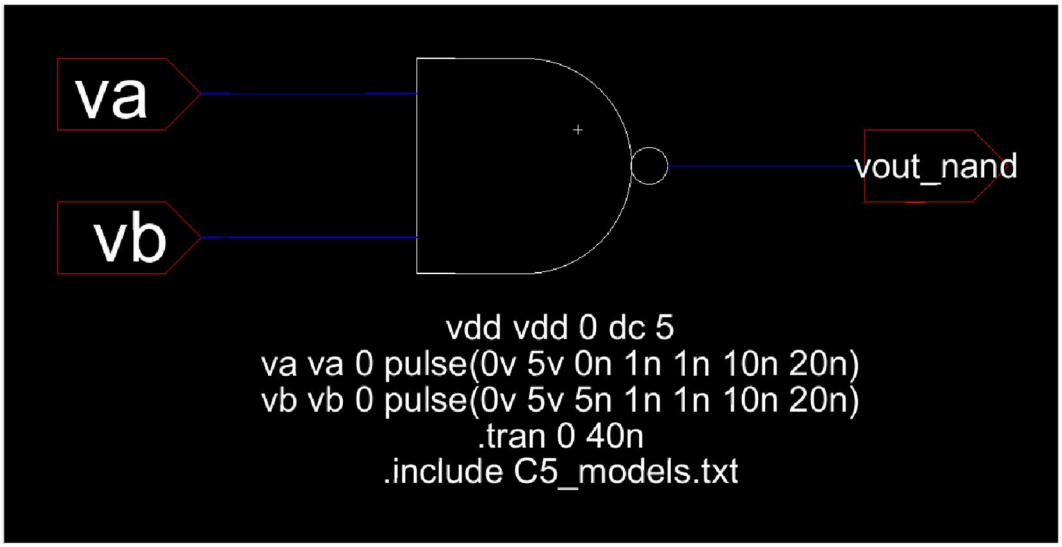

Figure 11. NAND Simulation 2

The second simulation confirms identical NAND gate behavior across alternate test conditions, validating reproducibility.

5. XOR Gate Design and Simulation

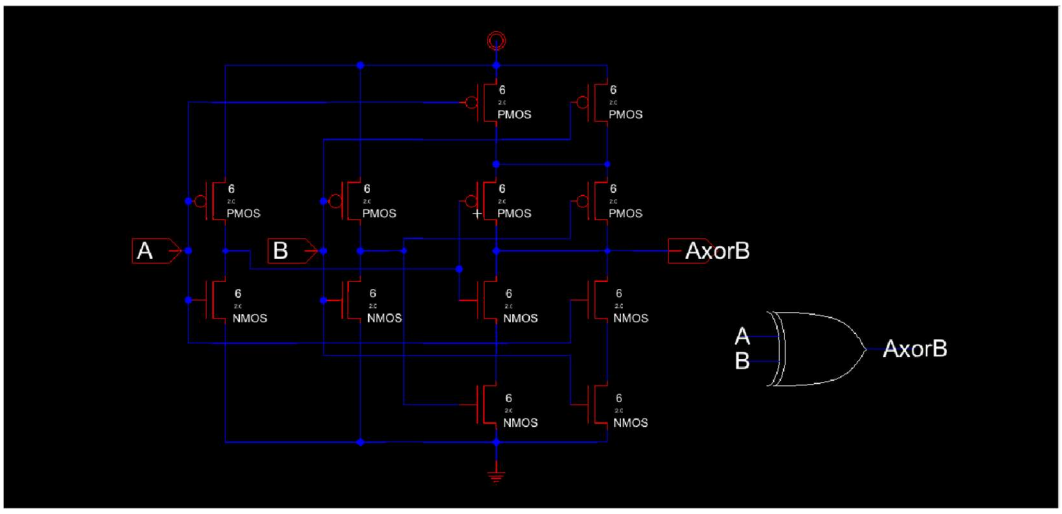

Figure 12. XOR Gate Schematic

The XOR schematic uses NAND and inverter structures to achieve Y = A⊕B. The output is high only when inputs differ.

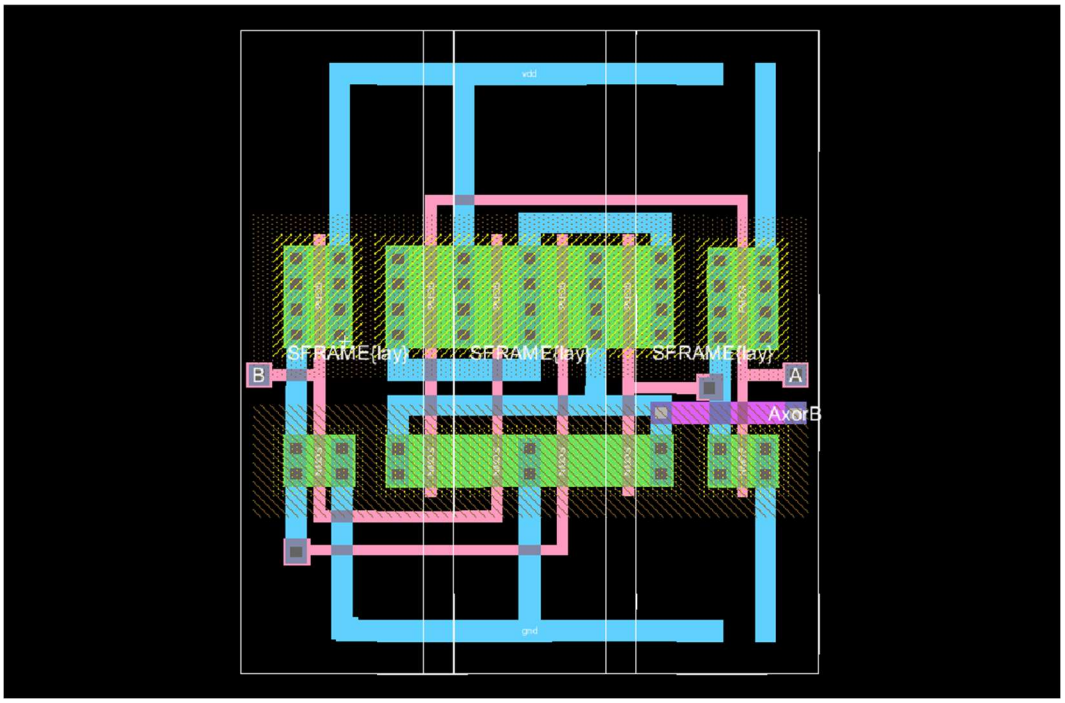

Figure 13. XOR Gate Layout

The layout integrates multiple subcells within a standard-cell frame, ensuring consistent VDD/GND alignment. DRC/NCC checks confirmed logical equivalence.

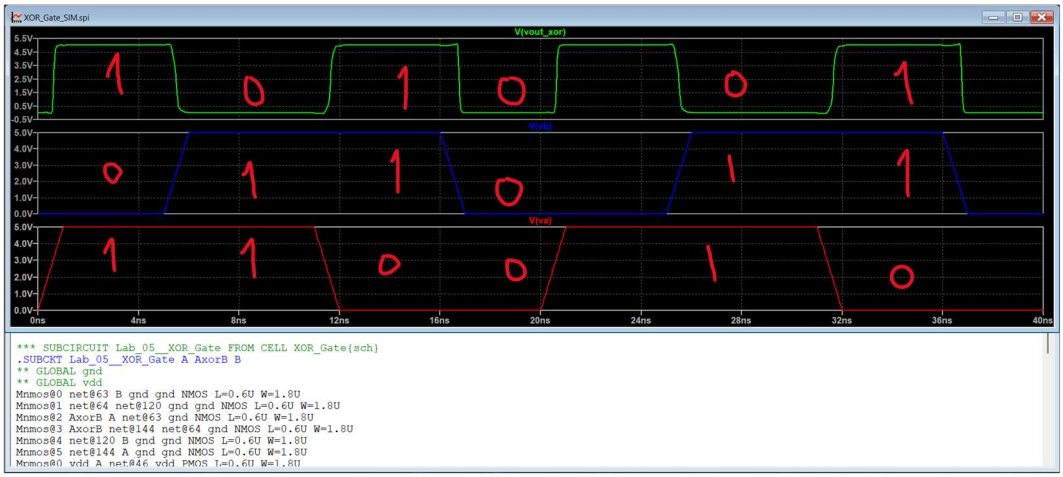

Figure 14. XOR SPICE Netlist 1

This netlist lists all XOR connections with transient analysis commands. Input pulses toggle alternately to verify exclusive-OR behavior.

From the simulation it was observed that vout becomes high only when va and vb are

Low and high(01) or high and low (10) but vout becomes low when va and vb are both low (00) or both high (11) which confirms that the gate is behaving as an XOR gate

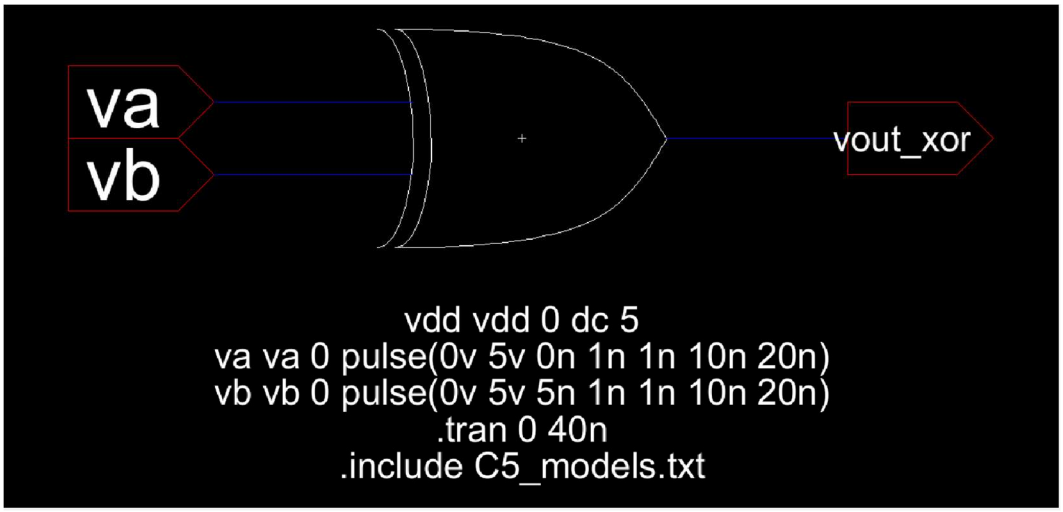

Figure 15. XOR Simulation 1

The waveform shows output high when inputs differ and low when they match. The transitions are sharp and glitch-free.

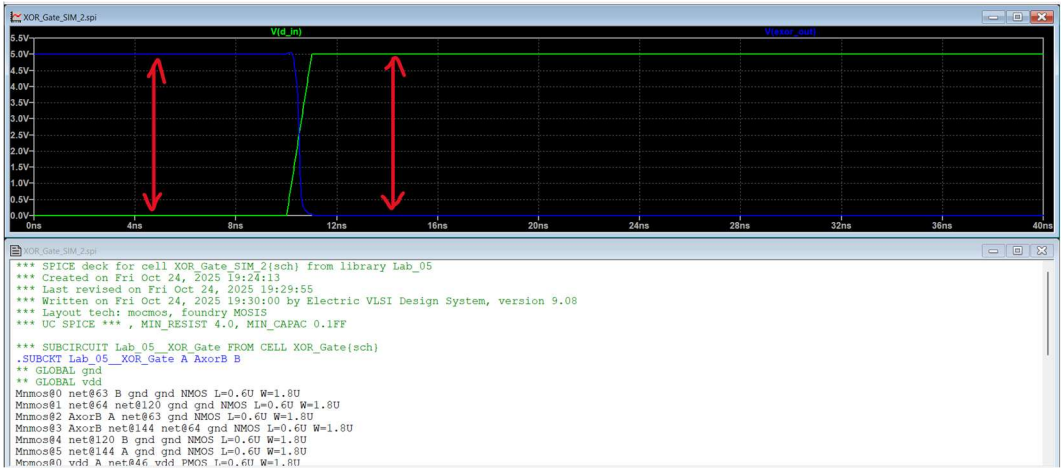

Figure 16. XOR SPICE Netlist 2

An alternative XOR configuration emphasizing transistor symmetry.It was observed that when d_in is low with vdd (01) exor_out becomes high but when vd__in is high and vdd (11) the exor out becomes low which indicates that the gate is behaving as intended

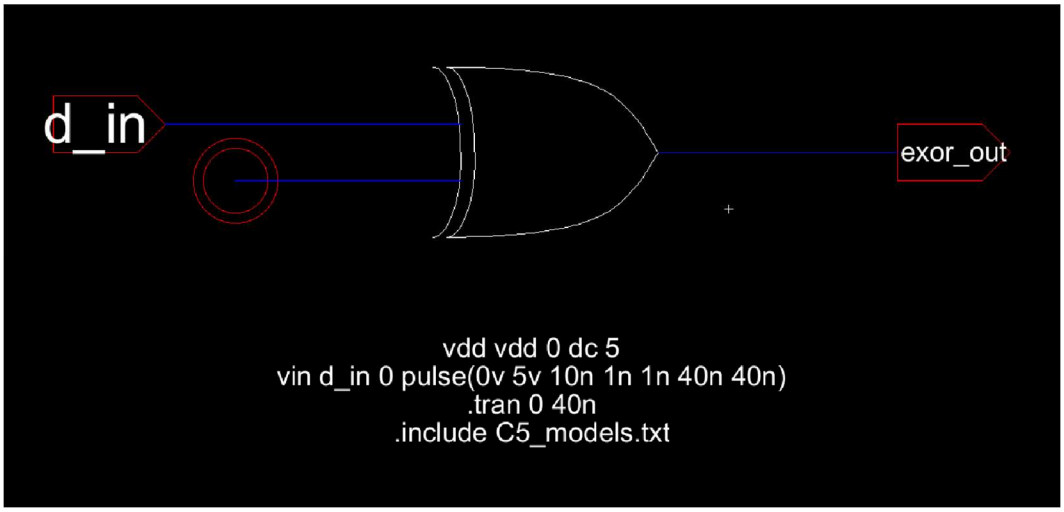

Figure 17. XOR Simulation 2

The second simulation validates consistent XOR output, confirming stable logic levels across all transitions.

6. Full Adder Design and Simulation

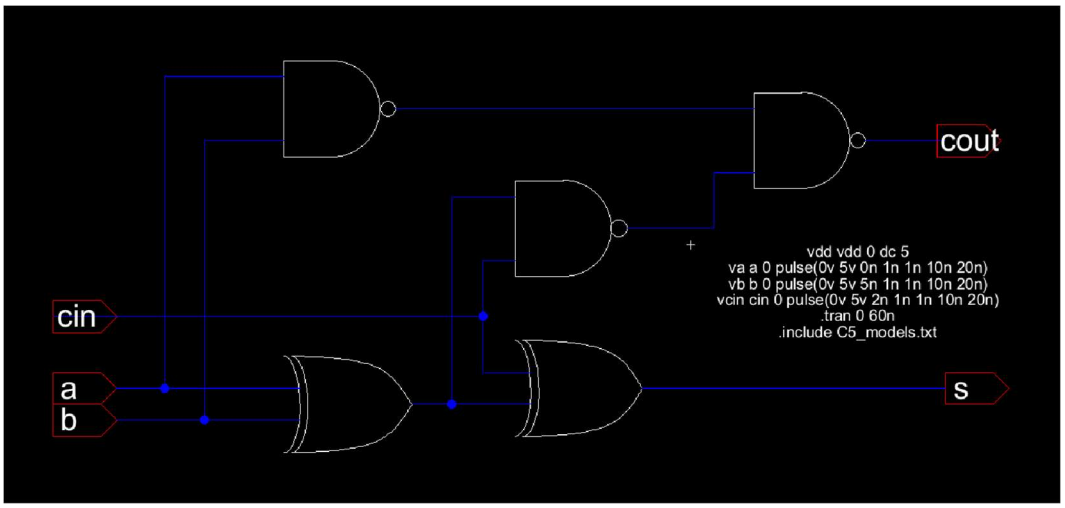

Figure 18. Full Adder Schematic

The full adder schematic integrates two XOR and three NAND gates. The first XOR computes partial sum A⊕B, the second XOR adds C_in to produce SUM. NAND gates form the carry-out logic according to C_out = AB + BC_in + AC_in.

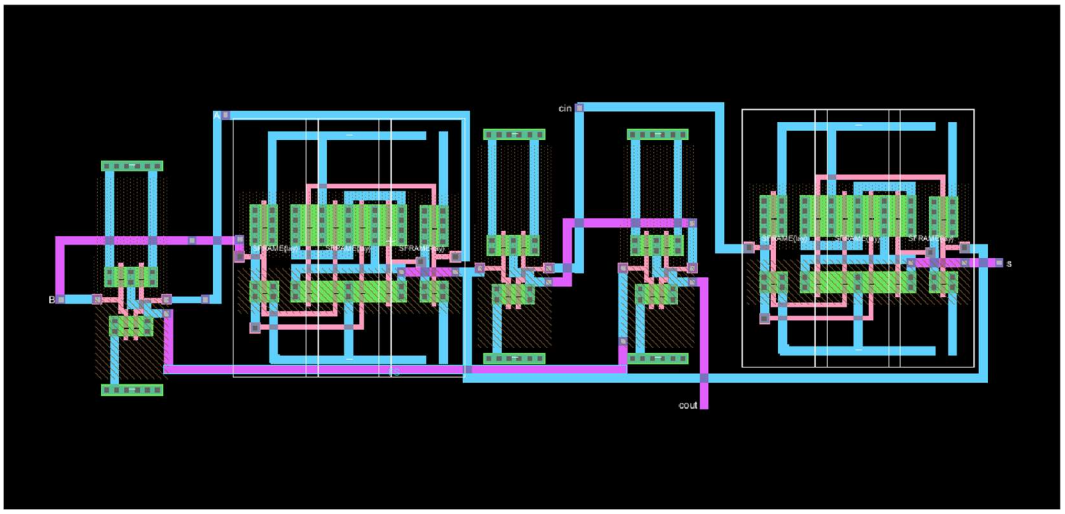

Figure 19. Full Adder Layout

The full adder layout arranges five gates horizontally within standard-cell frames, ensuring shared VDD/GND rails. Inputs and outputs are routed using Metal2 for cross-connections. DRC and NCC both passed.

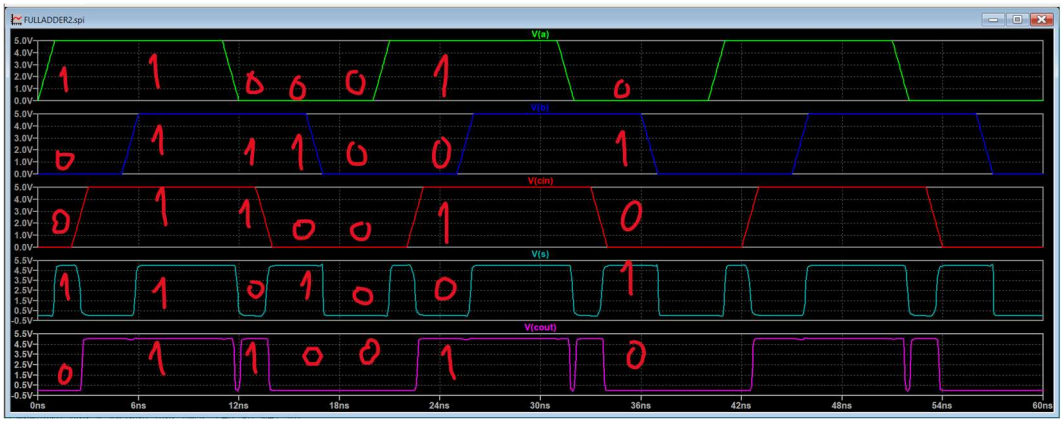

Figure 20. Full Adder SPICE Netlist

The SPICE file defines hierarchical connections and applies transient analysis to test all eight input combinations. The measured waveforms show correct SUM and CARRY outputs.

From the simulation it was observed that the circuit behavior matches the truth table of the full adder.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

7. Discussion

Each circuit was verified through schematic, layout, and simulation. The inverter achieved symmetrical rise and fall times, while the NAND and XOR gates demonstrated correct logical functionality. The full adder successfully produced accurate SUM and CARRY outputs for all input combinations. Minor transient glitches observed were attributed to propagation delays, typical in cascaded logic structures.

8. Conclusion

This laboratory demonstrated the complete CMOS VLSI design flow from transistor-level schematic design to physical layout and SPICE simulation. The results verified the theoretical operation of NOT, NAND, and XOR gates, and their integration into a full adder. All designs passed DRC and NCC verification, confirming manufacturability and functional correctness.