# DAT 103
# Datamaskiner og operativsystemer (Computers and Operating Systems)

## Supplementary exercises (Set 4)

### Problem 1

Which one of the following is correct?

(a) Program counter contains the instruction that is currently being executed.
(b) Instruction register contains the instruction that is currently being executed.
(c) Program counter contains the next instruction to be executed.
(d) Instruction register contains the next instruction to be executed.
(e) None of the above.

**Solution.**
Instruction register contains the instruction that is being executed by the CPU

### Problem 2

Which one of the following is not an element of a machine instruction?

(a) Operation code
(b) Source operand reference
(c) Result operand reference
(d) Next instruction reference
(e) None of the above

**Solution.**
None of the above

### Problem 3

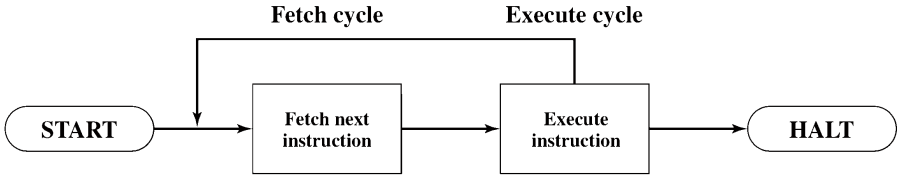
Which one of the following is not true?

(a) For programming in *software*, each new program requires rewiring the hardware
(b) For programming in *software*, each new program requires a new sequence of instructions
(c) For programming in *hardware*, each new program requires rewiring the hardware
(d) All of the above
(e) None of the above

**Solution.**
For programming in *software*, each new program requires rewiring the hardware

## Problem 4

Consider the basic instruction cycle in the following figure. Revise the instruction cycle such that it also includes the *interrupt cycle*.




**Solution.**

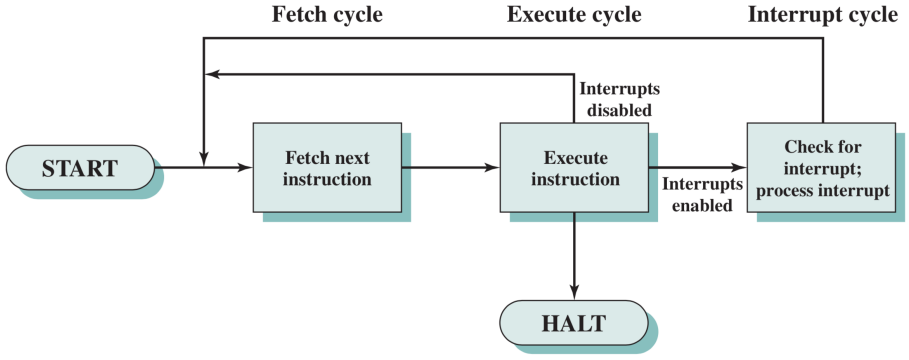



**Figure 3.9** Instruction Cycle with Interrupts

## Problem 5

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?
b. Discuss the impact on the system speed if the microprocessor bus has:
    1. 32-bit local address bus and a 16-bit local data bus, or
    2. 16-bit local address bus and a 16-bit local data bus.
c. How many bits are needed for the program counter and the instruction register?

**Solution.**

a. $2^{24} = 16$ MBytes
b. 1. If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.
    2. Since the address bus is too small to fetch the whole address, a more complex memory interface control is needed to latch the first part of the address and then the second part (because the microprocessor will end in two steps). For a 32-bit address, one may assume the first half will decode to access a "row" in memory, while the second half is sent later to access a "column" in memory. In addition to the two-step address operation, the microprocessor will need 2 cycles to fetch the 32-bit instruction/operand.

## Problem 6

Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator?

- Address 3 contains 15.
- Address 12 contains 18.
- Address 15 contains 24.
- Address 18 contains 36.

(a) LOAD IMMEDIATE 3
(b) LOAD DIRECT 3
(c) LOAD INDIRECT 3
(d) LOAD IMMEDIATE 15
(e) LOAD INDIRECT 12
(f) LOAD DIRECT 18

**Solution.**

(a) 3
(b) 15
(c) 24
(d) 15
(e) 36
(f) 36

## Problem 7

An address field in an instruction contains decimal value 96. Where is the corresponding operand located for

(a) immediate addressing?
(b) direct addressing?
(c) indirect addressing?
(d) register addressing?
(e) register indirect addressing?

**Solution.**

(a) the address field
(b) the memory location 96
(c) the memory location whose address is in memory location 96
(d) register 96
(e) the memory location whose address is in register 96

## Problem 8

Consider an instruction with two operands $O_1$, $O_2$. If $O_1$ uses *PC-relative* addressing mode, $O_2$ uses *indirect* addressing mode. How many memory accesses are required in total to fetch $O_1$ and $O_2$?

**Solution.**
1+2=3

## Problem 9

Consider an instruction with two operands $O_1$, $O_2$ that respectively use addressing modes $M_1$ and $M_2$. Specify the *total number* of memory accesses that are required to fetch the two operands by completing the following table.

| $M_1$ | $M_2$ | Total memory accesses |
|---|---|---|
| Register | PC-relative | |
| Base-register | register | |
| Register | 2-level indirect | |

**Solution.**

| $M_1$ | $M_2$ | Total memory accesses |
|---|---|---|
| Register | PC-relative | 0+1=1 |
| Base-register | register | 1+0=1 |
| Register | 2-level indirect | 0+3=3 |

## Problem 10

Which one of the following is **incorrect** about pipelining?

(a) Pipelining allows executing multiple instructions at the same time on one core

(b) The stages of an instruction cycle in the pipeline require different processing times

(c) Sometimes the prefetched instruction is not the instruction that is executed next

(d) All of the above

(e) None of the above

**Solution.**
Pipelining allows *executing* multiple instructions at the same time on one core

**NOTE:**The following type of questions will ***not*** be asked in the exam; however, through working on these questions, you will have a better understanding of how instructions execute on a computer.

## Problem 11

Consider the hypothetical machine in the following figure:

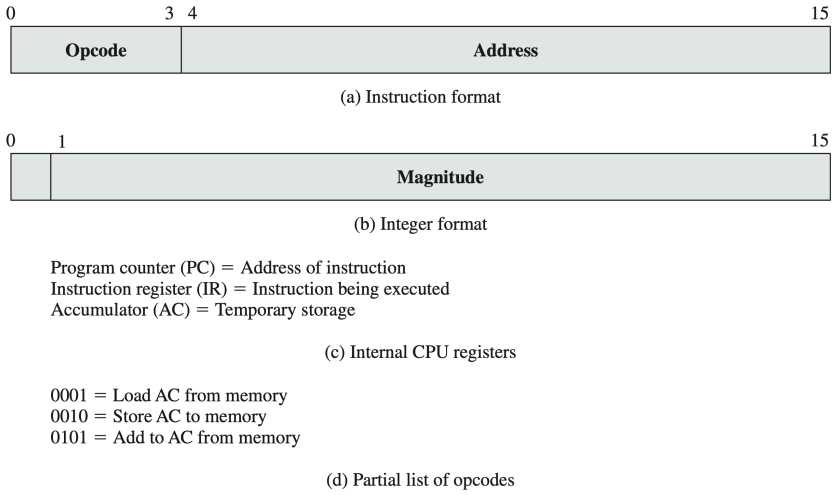



**Figure 3.4** Characteristics of a Hypothetical Machine

Assum the machine also has two I/O instructions:

0011 = Load AC from I/O
0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from I/O Device 5.
2. Add contents of memory location 940.
3. Store AC to I/O Device 6.

Assume that the values stored in Device 5 and memory location 940 are 3 and 2, respectively. You can further assume that Device 5 and Device 6 have address 005 and 006, respectively.

**Solution.**
Memory (contents represented in in hex): 300:3005; 301:5940; 302:7006

**Step 1:** 3005 → IR
**Step 2:** 3 → AC
**Step 3:** 5940 → IR
**Step 4:** 3+2=5 → AC
**Step 5:** 7006 → IR
**Step 6:** AC → 006