DAT 103
Datamaskiner og operativsystemer (Computers and Operating Systems)

Supplementary exercises (Set 1)

Problem 1

Which one of the following is a component inside a CPU?

(a) Program counter

(b) Memory address register

(c) L1 cache

(d) All of the above

(e) None of the above

Solution.
All of the above

Problem 2

Sort the following memory components in descending order according to the access time, that is, the component with the lowest access time should be the first, while the one with the highest access time should be the last.

(1) Main memory; (2) Level 1 cache; (3) Magnetic tape;
(4) Solid-state drive (SSD); (5) Level 2 cache; (6) Magnetic disk;
(7) Register

Solution.
7, 2, 5, 1, 4, 6, 3

Problem 3

Which **one** of the following is the major reason for the implementation of cache memory?

(a) To increase the amount of the system's internal memory

(b) The difference in speeds of operation of the processor and memory

(c) To reduce the memory access and cycle time

(d) None of the above

Solution.
The difference in speeds of operation of the processor and memory

Problem 4

Based on the following table which maps memory blocks B_i to cache lines L_j, e.g., B_{72} is mapped to L_8.

Memory block number (i)	Cache line number (j)
72	8
100	36
128	0
136	8
256	0

Assume memory blocks B_{100} and B_{128} are **in the cache** and all other blocks are **not**. What is the number of *cache misses* if a process accesses the blocks in each of the following sequences? Justify your answer by identifying which accesses lead to cache misses.

m refers to **m**iss, and h refers to **h**it

1. B_{100} ; B_{256} ; B_{100} ; B_{128}

   Solution.

   2 misses:

B_{100}	B_{256}	B_{100}	B_{128}
h	m	h	m

2. B_{128} ; B_{100} ; B_{72} ; B_{256} ; B_{128} ; B_{136} ; B_{128}

   Solution.

   4 misses:

B_{128}	B_{100}	B_{72}	B_{256}	B_{128}	B_{136}	B_{128}
h	h	m	m	m	m	h

Problem 5

Consider a computer system with main memory that is word-addressable, and a processor that supports at most 8 GB of memory. How many bits should the address bus of the processor at least have? ***Note**: assume a word is two bytes.*

Solution.

32

Maximum Memory = 8GB = 2^{33} bytes
Size of a word = 2 bytes
Number of words = 2^{33} / 2 = 2^{32}

Problem 6

If a main memory consists of `65535` addressable words, how many bits does the address of each of these words have?

Solution.

16

Problem 7

A cache line usually contains more than one word to ...

(a) Speed up the processor

(b) Exploit the locality of reference

(c) Free space in the main memory

(d) All of the above

(e) None of the above

Solution.
Exploit the locality of reference

Problem 8

Which one of the following is typically used to reduce memory access time?

(a) Stacks

(b) Faster processors

(c) Main memory with larger capacity

(d) Cache memory

(e) Pointers

Solution.
Cache memory

Problem 9

Which one of the following is **correct** if "Programmed I/O" is used to handle I/O operations?

(a) The processor is occupied in handling an I/O transfer

(b) The processor periodically checks the status of the I/O module

(c) Data transfer from I/O module to memory goes through the processor

(d) All of the above

(e) None of the above

Solution.
All of the above

Problem 10

Which **one** of the following improves the speed of I/O transfers?

(a) Interrupts

(b) Direct Memory Access (DMA)

(c) Program-controlled I/O

(d) All of the above

(e) None of the above

Solution.
DMA