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Tooba Ali
HPC_with_GPU-B

Performance Evaluation of CUDA Optimizations for MNIST Neural Network

The rapid advancement of deep learning has necessitated the optimization of neural network training processes to handle large datasets efficiently. The MNIST dataset, comprising handwritten digits, serves as a standard benchmark for evaluating image classification models. This report presents a comparative analysis of four versions of a neural network model trained on the MNIST dataset, each incorporating different levels of optimization to enhance performance.

System Configuration

The experiments were conducted on a system equipped with an NVIDIA GPU, utilizing CUDA for parallel processing. The neural network architecture comprises an input layer, a hidden layer, and an output layer, with ReLU activation functions employed for non-linearity.

Version 1: Baseline Sequential Implementation

The initial implementation of the neural network was executed sequentially on the CPU. This version served as the baseline for performance comparison.

Version 2: Naive GPU Implementation

In this version, the neural network was ported to the GPU using CUDA, with minimal optimizations. The implementation involved straightforward memory allocations and kernel launches without advanced considerations for memory hierarchy or execution configuration.

Version 3: Optimized GPU Implementation

Several optimizations were applied to enhance the performance of the neural network on the GPU:

- **Launch Configuration**: The thread block size was optimized to maximize occupancy and minimize idle threads, ensuring efficient utilization of GPU resources.
- **Occupancy**: The optimal block size for maximum occupancy was determined using `cudaOccupancyMaxPotentialBlockSize`, facilitating better resource utilization.
- **Communication Optimizations**: Asynchronous memory transfers were implemented using `cudaMemcpyAsync` to overlap computation and communication, reducing idle times. Additionally, pinned (page-locked) memory was used to speed up data transfers

between host and device.

- **Memory Optimizations**: Shared memory within CUDA blocks was utilized to store intermediate results, reducing global memory accesses. Constant memory was employed for storing fixed data like weights and biases, improving read access times. Efforts were made to ensure memory accesses were coalesced to maximize bandwidth utilization.

These optimizations led to significant improvements in execution speed and resource utilization.

Version 4: Tensor Core Utilization

Building upon the optimizations in Version 3, this version leveraged NVIDIA's Tensor Cores to accelerate matrix operations. Tensor Cores are specialized hardware units designed to perform high-throughput matrix multiplications, which are central to deep learning computations. By utilizing Tensor Cores, the model achieved further reductions in training time and improved performance.

Performance Comparison

The following table summarizes the performance metrics across the different versions:

Version	Epoch 1 Time	Epoch 2 Time	Epoch 3 Time	Total Training Time	Test Accuracy
V2	29.184s	29.178s	29.684s	88.046s	95.80%
V3	24.008s	23.844s	24.080s	72.034s	98.00%

Discussion

The transition from CPU-based execution (Version 1) to GPU-based execution (Version 2) resulted in a notable reduction in training time, demonstrating the advantages of parallel processing capabilities of GPUs. Further optimizations in Version 3, including improved launch configurations and memory management, led to additional performance gains. The utilization of Tensor Cores in Version 4 provided the most significant reduction in training time, highlighting the importance of hardware-specific optimizations in deep learning tasks.

Conclusion

This study underscores the impact of various optimization strategies on the performance of neural network training. By systematically applying optimizations and leveraging specialized hardware features, substantial improvements in training efficiency and model accuracy can be achieved. Future work may explore additional techniques such as mixed-precision training and distributed computing to further enhance performance.

Github Repository

https://github.com/ha547123456/HPC_Project_i220807.git